Analysis, Design, and Investigation of a Soft-Switched Buck Converter With High Efficiency

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***Abstract*—In this article, a new simple buck converter with zero voltage switching (ZVS) performance and almost zero output current ripple is proposed. The proposed structure's auxiliary circuit contains a capacitor and an inductor without any switches, which makes it possible to minimize the switching losses and eliminate other additional losses. The main power diode also turns OFF under zero current switching condition and the reverse recovery losses of the power diode is minimized. Eliminating the switching losses and the reverse recovery losses allows the converter to operate with high power efficiency, which makes it a good option for high power efficiency-required applications. In this article, five operational modes are explained. The design section includes the designing criteria of the components. Also, the efficiency analysis, control system for stabilizing the output voltage, and applying a variable inductor to ensure the soft-switching operation are analyzed. The comparison results are also discussed. Moreover, an experimental prototype of the proposed structure at 200 W output power and 75 kHz frequency is built to prove the above-mentioned advantages. Finally, the soft-switching waveforms are obtained for different output powers with various duty cycles and equal switching frequency to verify the ZVS performance of the converter at different loads and changes in input voltage and duty cycle.**

***Index Terms*—Buck converter, dc–dc converter, high power efficiency, soft-switching.**

I. Introduction

In THIS modern era, providing reliable energy sources for various uses is essential for the world industries, as fossil fuels are going to be more expensive and inefficient due to the world's sharply-increasing energy demand.

Considering the necessity of a reliable uninterrupted power supply to inject to the grid, storage systems are required to store renewable energies' power production and provide dependable sources. In this case, dc–dc converters are required to convert the dc voltage to a higher or lower level, depending on the output demand [1]–[7].

The ZVS condition can be achieved by the switch's parallel diode conduction. The parallel diode will conduct just before the switch's turn-ON moment so that the switch's voltage will be fixed at zero and the switch will turn ON with soft-switching condition [8]. In [9], an auxiliary circuit is added to the conventional synchronous buck converter. This converter is capable of providing ZVS turn-ON and ZCS turn-OFF of the switches. In [10], ZVS condition is obtained based on the DCM operation of the added LC resonant circuit to the bidirectional converter. However, this structure suffers from high input current ripple in boost mode and high output current ripple in buck mode. In [11], the ZVS condition is obtained by the leakage current of the coupled inductor. Also, in [12]–[17], there are several approaches to obtain ZVS condition. Another soft-switching technique to achieve ZCS condition can be obtained by using resonant circuits, which stabilizes the switch's current before it turns ON [18]. In [19], adding a resonant circuit, ZCS turn-ON and ZVS turn-OFF of the conventional buck converter can be achieved. In [20], an isolated buck converter is presented. In this structure, the leakage inductance of the utilized transformer is used as resonant element and ZCS condition is obtained for the switch. In [21], a resonant network is utilized to provide ZVZCS condition for the bidirectional converter. Moreover, in [22], another active resonant circuit is added to the synchronous buck converter to obtain ZVZCS condition. In these structures, soft-switching condition is provided for the auxiliary elements too.

In this article, a novel topology based on the conventional buck converter is proposed. In fact, the purpose of this article is proposing, analyzing, and testing a modified structure for buck converters, which has noticeable superiorities in the following listed features:

1) simplicity of the auxiliary circuit and topology;
2) full soft-switching capability;
3) volume, cost, and power density;
4) power efficiency.

The above-mentioned claims are proved by a comprehensive comparison between the proposed converter and several similar structures.

In this article, the operation of the converter is analyzed and auxiliary components are designed to achieve the ZVS condition. Furthermore, the power efficiency and closed-loop

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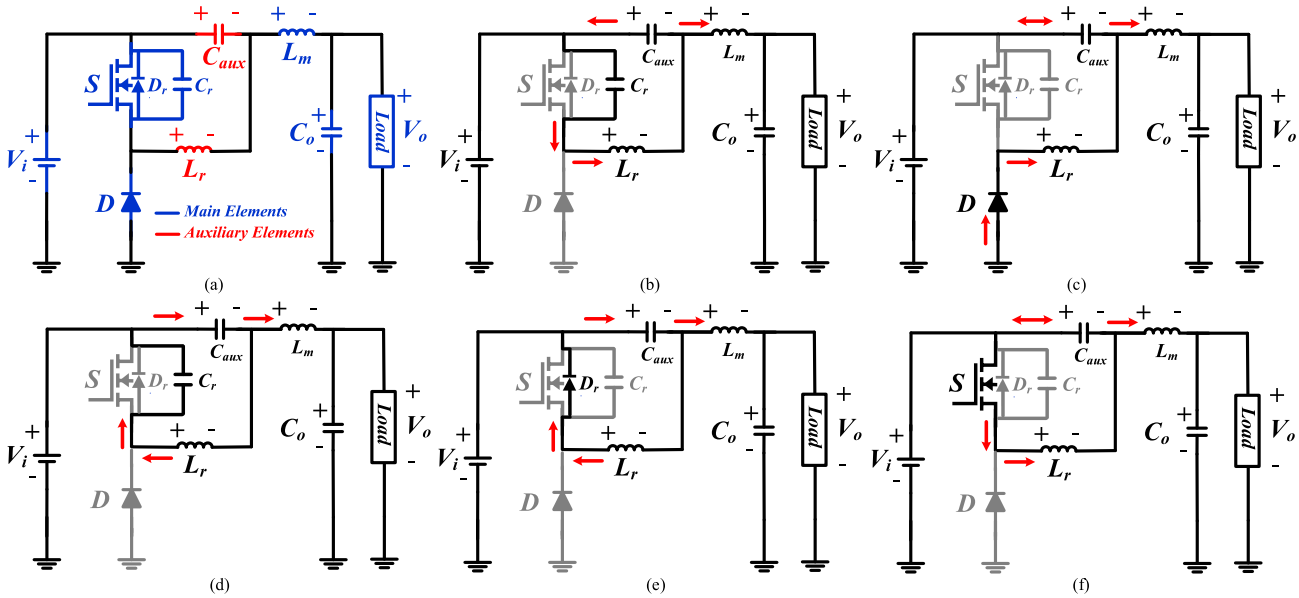


Fig. 1. Proposed auxiliary circuit with conventional buck converter and its operational modes. (a) Proposed auxiliary circuit with conventional buck converter. (b) Mode I $[t_0, t_1]$. (c) Mode II $[t_1, t_2]$. (d) Mode III $[t_2, t_3]$. (e) Mode IV $[t_3, t_4]$. (f) Mode V $[t_4, t_5]$.

modeling are described. After comparison section, the experimental soft-switching waveforms are obtained for 100- and 200-W output powers with various duty cycles and equal switching frequency to verify ZVS performance of the converter at different loads and changes in input voltage and duty cycle.

II. Proposed Converter and Operational Modes

The analyzed auxiliary circuit with the conventional buck converter is illustrated in Fig. 1(a). In this figure, L_r and $C_{\rm aux}$ are the auxiliary inductor and capacitor, respectively. Also, L_m, *S,* and *D* are the main inductor, the power switch, and the power diode, respectively. Moreover, D_r and C_r are the antiparallel diode and parallel capacitor, respectively. This structure has five operational modes. The equivalent circuits of these modes are mentioned in Fig. 1(b)–(f). It is assumed that the second and fifth operational modes have a longer duration compared to other modes.

A. Mode I [t_0, t_1]: Fig. 1(b) shows the first mode. Before mode 1, the switch was in ON-mode. At t_0, the parallel capacitor gets charged and the switch's voltage increases slowly. Therefore, the switch turns OFF with soft-switching condition. Also, the main and the auxiliary inductor conduct positive currents and the auxiliary capacitor gets discharged

$$V_{\rm Cr} + V_D = V_{\rm in} \tag{1}$$

$$V_{\rm Lm} = V_i - V_o - V_{\rm Caux} \tag{2}$$

$$V_{\rm Lr} = V_{\rm Caux} - V_{\rm Cr} \tag{3}$$

where $V_{\rm Cr}$, $V_{\rm Caux}$, $V_{\rm Lm}$, $V_{\rm Lr}$, and $V_{\rm D}$ are the parallel and auxiliary capacitor, main and auxiliary inductor, and diode voltage.

The switch voltage is zero at t_0. By the end of this mode, the parallel capacitor (C_r) gets charged and the switch voltage equals to the input voltage slowly. At t_1, the main diode voltage equals to zero, as C_r gets charged to the input voltage. Consequently, at t_1, the following equations are obtained:

$$V_S(t_1) = V_{\rm Cr}(t_1) = V_{\rm in} \tag{4}$$

$$V_D(t_1) = 0. \tag{5}$$

B. Mode II [t_1, t_2]: Fig. 1(c) shows the equivalent circuit of second mode. At t_1, V_D reaches zero. Therefore, the main diode starts conducting. Moreover, the switch is in OFF-mode, the main and auxiliary inductors conduct a positive current, the auxiliary capacitor gets discharged and then starts getting charged. By applying KVL, the following equation is achieved:

$$V_{\rm Lr} = V_{\rm Caux} - V_i. \tag{6}$$

The main inductor voltage can be obtained from [2]. The switch voltage equals to input voltage and the switch is in OFF mode. Considering [6], the auxiliary inductor current will be

$$i_{\rm Lr}(t) = ((V_{\rm Caux} - V_i)/L_r)t + i_{\rm Lr}(t_1). \tag{7}$$

Since the auxiliary inductor current changes from its maximum value ($i_{r\rm MAX}$) to zero during the modes 1 and 2, considering [7] as the current equation for these modes, the duration of these modes can be obtained as follows:

$$t_2 - t_0 = L_r i_{r\rm MAX}/(V_i - V_{\rm Caux}). \tag{8}$$

At the end of the second mode, the main diode current reaches zero and it turns OFF under ZCS condition.

C. Mode III [t_2, t_3]: The equivalent circuit of third mode is mentioned in Fig. 1(d). In this mode, the auxiliary capacitor $C_{\rm aux}$ gets charged. The main inductor conducts a positive current. However, the auxiliary inductor conducts a negative current. This negative current makes the parallel capacitor discharge and the switch voltage fall. In this mode

$$V_{\rm Lr} = V_{\rm Caux} - V_{\rm Cr} \tag{9}$$

$$i_{\mathrm{Cr}} = i_{\mathrm{Lr}}. \tag{10}$$

Also, since the duration of third mode is much less than the second mode, the auxiliary inductor current of third mode can be estimated with [7]. Therefore, since the auxiliary inductor current changes from zero to its minimum value ($i_{r\mathrm{MIN}}$) during the third mode, this equation can be written as follows:

$$t_3 - t_2 = L_r i_{r\mathrm{MIN}}/(V_{\mathrm{Caux}} - V_i). \tag{11}$$

At t_3, the parallel capacitor has completely been discharged. As a result, the switch's voltage reaches zero and the main diode's voltage reaches the input voltage.

D. Mode IV [t_3, t_4]: As clarified in Fig. 1(e), the switch voltage reaches zero because of the complete discharging of the parallel capacitor in third mode. Also, the main and auxiliary inductor conduct positive and negative currents, respectively. Therefore, the switch's parallel diode starts conducting and the switch voltage is fixed at zero while the antiparallel diode starts conducting. Also, the auxiliary capacitor C_{aux} gets charged.

At t_4, the current direction changes and the parallel diode turns OFF. This mode lasts too short and consequently

$$V_{\mathrm{Lr}} = V_{\mathrm{Caux}} \tag{12}$$

$$i_{\mathrm{Dr}} = i_{\mathrm{Lr}}. \tag{13}$$

E. Mode V [t_4, t_5]: The equivalent circuit of this mode is shown in Fig 1(f). In the previous modes, the switch voltage reached zero and was fixed at zero by the antiparallel diode conduction.

In this mode, the current direction is changing from negative to positive. Therefore, the switch turns ON under ZVS condition. Also, the auxiliary capacitor gets charged and then starts getting discharged. In addition, the main and auxiliary inductors conduct a positive current.

$$i_S = i_{\mathrm{Lr}}. \tag{14}$$

In this mode, similar to the prior mode, the auxiliary inductor voltage is equal to the auxiliary capacitor voltage. Therefore, the auxiliary inductor current can be calculated as follows:

$$i_{\mathrm{Lr}}(t) = \frac{V_{\mathrm{Caux}}}{L_r} t + i_{\mathrm{Lr}}(t_3). \tag{15}$$

During the fourth mode, the inductor current changes from its minimum value to zero. Therefore, considering [15], the duration of fourth mode can be achieved as follows:

$$t_4 - t_3 = \frac{-L_r i_{r\mathrm{MIN}}}{V_{\mathrm{Caux}}}. \tag{16}$$

In the fifth mode, the auxiliary inductor current changes from zero to its maximum value. Also, the duration of fifth mode is equal to the ON-mode duration of the switch (dT). The maximum value of the auxiliary inductor current can be achieved as follows:

$$i_{r\mathrm{MAX}} = \frac{dTV_{\mathrm{Caux}}}{L_r}. \tag{17}$$

At the end of mode 5, the power switch turns OFF and the switching period is completed.

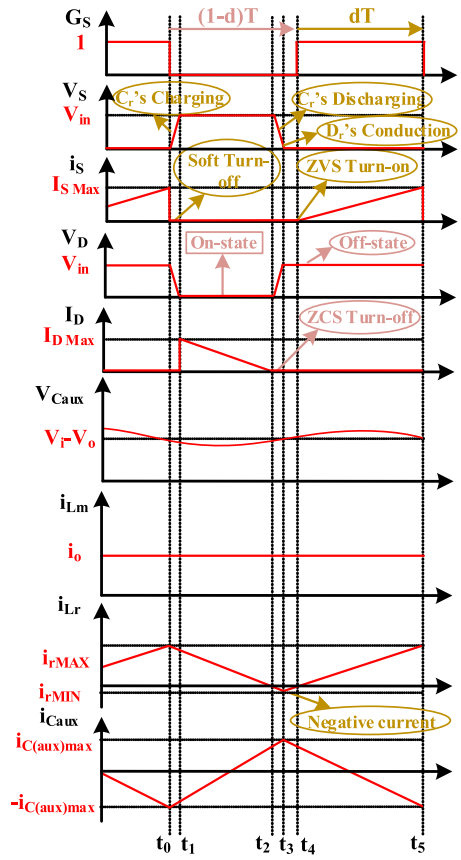


Fig. 2. Key theoretical waveforms.

III. Theoretical Waveforms, Voltage Stress, and Voltage Gain

A. Theoretical Waveforms

The theoretical waveforms of the proposed structure are illustrated in Fig. 2.

Modes 2 and 5 are the main operational modes due to their long durations. Regarding the mentioned modes, it is supposed that the mentioned structure performs in two main modes.

B. Voltage Stress

In this structure, the voltage stress across the switch equals to the input voltage

$$V_{S\,\mathrm{MAX}} = V_i. \tag{18}$$

The voltage stress across the power diode also equals to the input voltage

$$V_{D\,\mathrm{MAX}} = V_i. \tag{19}$$

C. Voltage Gain

Considering that the current ripple of the main inductor can be neglected, it can be assumed that the main inductor average voltage is about zero. Therefore, by applying KVL, the following equation can be obtained:

$$V_{\mathrm{Caux}} = V_i - V_o. \tag{20}$$

TABLE I
AVERAGE AND RMS VALUES

PARAMETER	AVERAGE VOLTAGE	AVERAGE CURRENT	RMS CURRENT
SWITCH	$((1-d)/d)V_o$	di_o	$i_o\sqrt{d}$
DIODE	V_o	$(1-d)^2 i_o$	$(1-d)^{\frac{3}{2}} i_o$
MAIN INDUCTOR	0	i_o	i_o
AUXILIARY INDUCTOR	0	i_o	i_o
AUXILIARY CAPACITOR	$(1-d)V_o$	0	di_o

TABLE II
VALUES OF VARIOUS TYPES OF LOSSES

Type	$P_{Core-tot}$	P_{L-cond}	$P_{Switch-cond}$	$P_{Caux-cond}$	$P_{Forward}$	Sum
$P_{Loss}(W)$	3.04	1.2	0.13	0.08	0.98	5.43
$\frac{P_{Loss}}{P_{Loss(total)}}(\%)$	55.9	22.0	2.40	1.47	18.05	*Eff.%* 97.35
Input voltage=48V, output voltage=24V, output power=200W, switching frequency=75*kHz*, d=50%, Magnetic cores: EE30, P_{Core} <2.03W(at f=100*kHz*, B_{MAX}=200*mT*, and T=100°*C*), R_{Li}=10*m*Ω, R_{Lm}=8*m*Ω, R_{Caux}=5*m*Ω Power switch: IRFP3306PBF, $R_{S\text{-}on(S)}$=3.9*m*Ω, t_{off}=25*ns* Diode: SBR10U60CT, V_F=0.48V						

Considering [8], [20], and the fact that the main modes are the second and fifth modes, the following equation can be written:

$$i_{r\mathrm{MAX}} = \frac{(1-d)T(V_i - V_{\mathrm{Caux}})}{L_r}. \tag{21}$$

Now, based on [17], [20], and [21], the voltage gain of the proposed converter is obtained as follows:

$$G = \frac{V_o}{V_i} = d. \tag{22}$$

Therefore, the voltage gain of the proposed converter will be equal to the conventional buck converter.

IV. DESIGN INVESTIGATION

In this part, the soft-switching condition is analyzed in order to design the auxiliary components. Also, considering the needed values from Table IV, the suitable ranges for the required components' values in the assembled 200-W laboratory prototype are calculated.

The time length of the second mode is greater than that of the first and third modes. The auxiliary inductor current has the same equation for these modes. Therefore, based on [7] and [20], we have the following:

$$i_{\mathrm{rr}} = \frac{V_o}{L_r f_s}(1-d) \tag{23}$$

where i_{rr} is the current ripple of the auxiliary inductor.

Furthermore, in order to have a bidirectional auxiliary inductor current and using the auxiliary inductor negative current to achieve soft-switching condition for the switch's turn-ON, the auxiliary inductor current ripple should be more than twice than that of the main inductor current.

$$i_{\mathrm{rr}} > 2i_{\mathrm{Lm}}. \tag{24}$$

The main inductor current equals with the output current. Consequently

$$i_{\mathrm{Lm}} = i_o = \frac{V_o}{R_o}. \tag{25}$$

Considering [23]–[25], the auxiliary inductor should have the following condition:

$$L_r < \frac{R_o(1-d)}{2f_s} \rightarrow L_r < 9.6\,\mu\mathrm{H}. \tag{26}$$

Therefore, a 9 μH auxiliary inductor is selected for the laboratory prototype at nominal power and 48-V input voltage.

Also, in order to have a small increase in the switch voltage waveform during the switch's turn-OFF, the charging time of the parallel capacitor should be longer than the implemented switch's turn-OFF time ($t_{\mathrm{off-switch}}$). Therefore, since the auxiliary inductor current charges the parallel capacitor during the turn-OFF time, the following equations can be achieved:

$$i_{\mathrm{Cr}} \approx C_r \frac{\Delta V_{\mathrm{Cr}}}{\Delta t} \tag{27}$$

$$\Delta t_{\mathrm{Discharge}} > t_{\mathrm{off-switch}} \tag{28}$$

$$C_r > \frac{t_{\mathrm{off-switch}}}{V_i} i_{r\mathrm{MAX}}. \tag{29}$$

Moreover, the auxiliary inductor current should be large enough to make C_r get charged and discharged.

$$C_r {V_i}^2 < L_r (i_{r\mathrm{MAX}})^2 \tag{30}$$

$$C_r {V_i}^2 < L_r (i_{r\mathrm{MIN}})^2. \tag{31}$$

Considering (29)–(31), the following range can be achieved:

$$\frac{t_{\mathrm{off-switch}}}{V_i} i_{r\mathrm{MAX}} < C_r < \frac{L_r (i_{r\mathrm{MIN}})^2}{{V_i}^2} \rightarrow 9.37\,\mathrm{nF} < C_r < 15.62\,\mathrm{nF}. \tag{32}$$

In order to fulfil (32), 12 nF will be selected as the parallel capacitor value.

The auxiliary capacitor's maximum current value and the current equation of this capacitor will be as follows:

$$i_{\mathrm{CauxMAX}} = i_{r\mathrm{MAX}} - i_o \tag{33}$$

$$i_{\mathrm{Caux}} = C_{\mathrm{aux}} \frac{\Delta V_{\mathrm{Caux}}}{\Delta t}. \tag{34}$$

The auxiliary capacitor (C_{aux}) should have the same characteristics of a voltage source. Therefore, it is assumed that its voltage ripple is lower than 0.05 of its voltage rates. The auxiliary capacitor's current while it is being charged, is equal to the half of its maximum value. As a result, based on [20], (33), and (34), the auxiliary capacitor should match the following range:

$$C_{\mathrm{aux}} > \frac{i_{r\mathrm{MAX}} - i_o}{0.1 \times f_s V_i} \rightarrow C_{\mathrm{aux}} > 25.9\,\mu\mathrm{F}. \tag{35}$$

As a result, a 33 μF capacitor is utilized as the auxiliary capacitor.

TABLE III
COMPARISON RESULTS

Ref.	Number of auxiliary circuit elements					Switch		Diode	f_s (kHz)	Rated Power (W)	Total Volume (mm^3)	Total Cost ($)	Power Density (w/mm^3)	Maximum Efficiency
	S^*	I^*	D^*	C^*	T^*	on	off	off						
[8]	1	2	1	3	7	ZVS	ZVS	ZCS	37	200	19587	6.65	10×10^{-3}	96.1%
[9]	3	2	1	2	8	ZVS	ZCS	-	195	60	21648	5.38	2.7×10^{-3}	93.1%
[11]	2	1	2	1	6	ZVS	-	-	125	300	40304	5.82	7.5×10^{-3}	95.4%
[13]	2	1	1	2	6	ZVS	-	-	50	200	13530	6.1	5.2×10^{-3}	95.7%
[18]	1	2	2	2	7	ZCS	ZVS	-	50	600	48926	7.21	12.3×10^{-3}	96.9%
[24]	2	2	2	2	8	ZCS	ZCS	-	100	200	44047	8.3	4.6×10^{-3}	90.0%
[25]	2	2	2	2	8	ZVS	ZVS	-	40	1200	110701	16.28	11×10^{-3}	97.12%
[26]	4	2	2	2	9	ZVS	ZVS	-	50	1000	76052	10.6	13.2×10^{-3}	97%
Proposed	1	2	1	2	6	ZVS	ZVS	ZCS	75	200	13530	4.66	14.8×10^{-3}	97.17%

S^*: Switch, I^*: Inductor, D^*: Diode, C^*: Capacitor, T^*: Total.

TABLE IV
HARDWARE PROTOTYPE VALUES

Parameters	Values	Parameters	Values
V_i	(34-80)V	f	75kHz
V_o	24V	C_r	12nF
P_o	(100-200)W	C_o	100μF
D	(30-70)%	C_{aux}	33μF
L_m	80μH	L_r	(5-15)μH

V. LOSS ANALYSIS AND EFFICIENCY CALCULATION

The average and RMS current and voltage values are mentioned in Table I for analyzing the efficiency. This structure does not have the switching and the reverse recovery losses. Therefore, total losses consist of the semiconductors' conduction losses, core losses, and forward-voltage losses. The conduction losses of the utilized components, based on the parameter values from laboratory prototype and RMS current values from Table I, can be achieved as follows:

$$P_{\text{Switch-cond}} = R_{\text{S-on}} I^2_{\text{Switch-RMS}} = 0.13\,\text{W} \quad (36)$$

$$P_{\text{Lm-cond}} = R_{\text{Lm}} I^2_{\text{Lm-RMS}} = 0.67\,\text{W} \quad (37)$$

$$P_{\text{Lr-cond}} = R_{\text{Lr}} I^2_{\text{Lr-RMS}} = 0.53\,\text{W} \quad (38)$$

$$P_{\text{Caux-cond}} = R_{\text{Caux}} I^2_{\text{Caux-RMS}} = 0.08\,\text{W} \quad (39)$$

where $R_{S\text{-on}}$, R_{Lm}, R_{Lr}, and $R_{C\text{aux}}$ are the switch's ON resistance, the main and auxiliary inductors' internal resistances, and the auxiliary capacitor's internal resistance, respectively.

The overall conduction losses can be obtained based on the prior calculations

$$P_{\text{Cond-Overall}} = P_{\text{Switch-Cond}} + P_{\text{Lm-cond}} + P_{\text{Lr-cond}} + P_{\text{Caux-cond}} = 1.41\,\text{W}. \quad (40)$$

The utilized magnetic cores are EE30 ferrite cores. Therefore, based on the manufacturer datasheet, the maximum core losses at standard condition ($f = 100$ kHz, $B_{\text{MAX}} = 200$ mT, and $T = 100$ °C) is 2.03 W per each implemented ferrite core.

Considering the above-mentioned value and the fact that the constant core loss has an approximately direct relation with the switching frequency, the maximum constant core losses of the implemented magnetic cores in the laboratory prototype with $f = 75$ kHz switching frequency can be calculated as follows:

$$P_{\text{Core-tot}} = [P_{\text{Lm-core}} + P_{\text{Lr-core}}]_{f_s=75\,\text{kHz}} = \frac{75}{100}[P_{\text{Lm-core}} + P_{\text{Lr-core}}]_{f_s=100\,\text{kHz}} = 3.04\,\text{W}. \quad (41)$$

Moreover, considering the forward-voltage drop of the implemented power diode, the forward-voltage losses can be achieved as follows:

$$P_{\text{D-Forward}} = V_{\text{D-Forward}} I_{\text{D-Avg}} = 0.98\,\text{W}. \quad (42)$$

Eventually, the total losses and the efficiency of the proposed converter will be as follows:

$$P_{\text{Loss-tot}} = P_{\text{Cond-total}} + P_{\text{Core-tot}} + P_{\text{D-Forward}} = 5.43\,\text{W} \quad (43)$$

$$\text{Efficiency}\% = \frac{P_o}{P_i} = \frac{P_o}{P_o + P_{\text{Loss-tot}}} \times 100 = 97.35\%. \quad (44)$$

The proportion of losses at full-load are mentioned in Table II. About 74% of the total losses include the core losses and forward voltage losses of the power diode. In addition, due to eliminating the switching and reverse recovery losses, the switch and diode do not have a significant share in the total losses. The theoretical efficiency of the proposed converter is calculated 97.35% at full load.

The loss distribution of the proposed converter is shown in Fig. 3(a). Based on Fig. 3(a), 1.55% of total losses are related to the switch. Also, 18.17% of the losses are the diode's forward-voltage losses, 78.73% of total losses contribute to the main and auxiliary inductors, and the remained 1.55% relates to the

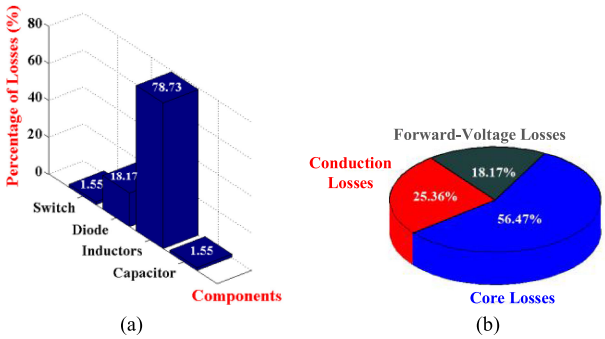


Fig. 3. Loss distribution. (a) Bar graph of the percentage of the components' losses. (b) Pie chart of losses.

auxiliary capacitor's losses. The pie chart of losses has also been shown in Fig. 3(b). Considering this figure, 56.47% of losses are the core losses, 18.17% of losses are the forward-voltage losses of the power diode, and finally, 25.36% of the overall losses refer to the conduction losses.

VI. Control Scheme to Stabilize Output Voltage

In order to stabilize the output voltage in different conditions, the closed-loop model of the proposed converter is analyzed in this part. Two parameters (i_{Lr} and V_{Co}) are assumed as state space variables. Therefore, the state space model of the proposed converter can be composed as follows:

$$\dot{x} = A_1 x + A_2 u, \quad y = A_3 x + A_4 u \tag{45}$$

$$x^T = \left[v_{Co}\ i_{Lr} \right], \ u = [v_i], \ y = [v_o] \tag{46}$$

where x, u, and y are the state variable vectors, input vector, and output vector, respectively. Based on the steady state analysis, $A_{1\text{-}4}$ can be achieved as follows:

$$A_1 = \begin{bmatrix} \frac{-(1-d)}{R_o C_o} & \frac{1-d}{C_o} \\ -\frac{1}{L_r} & 0 \end{bmatrix}, A_2 = \begin{bmatrix} 0 \\ \frac{d}{L_r} \end{bmatrix}, A_3 = \begin{bmatrix} 1\ 0 \end{bmatrix}, A_4 = [0]. \tag{47}$$

The above-mentioned state variables consist of a dc part ($\bar{X}$, $\bar{Y}$, $\bar{U}$, ...) and an ac part ($\tilde{x}$, $\tilde{y}$, $\tilde{u}$, ...), which is constant and can be neglected compared to the dc part [7]. Taking into account the above-mentioned ac and dc parts, the new dynamic model will be reached as following:

$$\begin{cases} \dot{\tilde{x}} = A'_1 \tilde{x} + A'_2 \tilde{u} + B' \tilde{d} \\ \tilde{y} = A'_3 \tilde{x} + A'_4 \tilde{u} \end{cases} \tag{48}$$

$$\tilde{x}^T = \left[\tilde{v}_{Co}\ \tilde{i}_{Lr} \right], \ \tilde{d} = \left[\tilde{d} \right], \ \tilde{u} = [\tilde{v}_i], \ \tilde{y} = [\tilde{v}_o] \ . \tag{49}$$

Short-circuiting the input vector ($u = 0$) in the previous model, the small signal model can be achieved [7]. Therefore, $A'_1(n\times n)$, $B'(n\times r)$, and $A'_3(m\times n)$ matrixes of the small signal model are achieved as follows:

$$A'_1 = \begin{bmatrix} -\frac{(1-\bar{D})}{R_o C_o} & \frac{(1-\bar{D})}{C_o} \\ \frac{-1}{L_r} & 0 \end{bmatrix}, B' = \begin{bmatrix} \frac{\bar{V}_{\mathrm{Co}}}{RC_o} - \frac{\bar{i}_{\mathrm{Lr}}}{C_o} \\ \frac{\bar{V}_i}{L_r} \end{bmatrix}, A'_3 = \begin{bmatrix} 1\ 0 \end{bmatrix}. \tag{50}$$

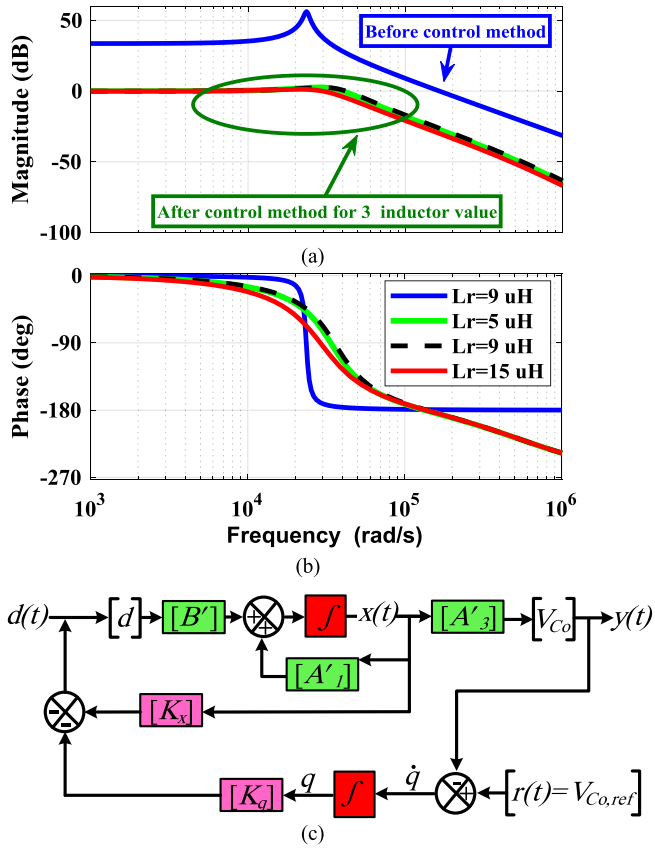


Fig. 4. Bode plots and block diagram of the control system. (a) Magnitude versus frequency diagrams before and after applying control approach with different values of auxiliary inductors in different conditions. (b) Phase versus frequency diagrams before and after applying control approach with different values of auxiliary inductors in different conditions. (c) Block diagram of the control system.

In this article, pole placement approach is utilized by integral state feedback. Fig. 4(c) visualizes the utilized control approach. Based on this figure we have the following:

$$\tilde{d} = -K_x \tilde{x} - K_q q \tag{51}$$

$$\dot{q} = r - A'_3 \tilde{x} \tag{52}$$

where q is the integrator output, and r is the reference signal, which equals to

$$r = V_{\mathrm{Co,\,ref}}. \tag{53}$$

In this approach, the controllability of the system makes it possible for the closed-loop poles to posit in desirable points. As a result, the controllability matrix of the system will be derived as follows:

$$\varphi_c = \left[B' \middle| A'_1 B' \middle| {A'_1}^2 B' \middle| \ldots {A'_1}^{(n-1)} B' \right] = [B' | A'_1 B'] \tag{54}$$

$$Rank\,(\varphi_c) = n = 2. \tag{55}$$

Considering the small signal model matrices (50), the closed-loop matrices will be derived from the open-loop matrices

$$\begin{cases} \begin{bmatrix} \dot{\tilde{x}}(t) \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A'_1 & 0 \\ -A'_3 & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} + \begin{bmatrix} B' \\ 0 \end{bmatrix} \tilde{d}(t) + \begin{bmatrix} 0 \\ 1 \end{bmatrix} r(t) \\ \tilde{y} = \begin{bmatrix} A'_3 & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} \end{cases} \tag{56}$$

$$\tilde{A}'_1 = \begin{bmatrix} A'_1 & 0 \\ -A'_3 & 0 \end{bmatrix}, \quad \tilde{B}' = \begin{bmatrix} B' \\ 0 \end{bmatrix}. \tag{57}$$

The new system ($\bar{\varphi}_c$) controllability matrix will be achieved as follows:

$$\varphi_c = \left[\tilde{B}' \middle| \tilde{A}'_1 \tilde{B}' \middle| \tilde{A}'^{2}_{1} \tilde{B}' \middle| \ldots \tilde{A}'^{(n-1)}_{1} \tilde{B}' \right] = \left[\tilde{B}' \middle| \tilde{A}'_1 \tilde{B}' \right] \tag{58}$$

$$\bar{\varphi}_c = \underbrace{\begin{bmatrix} B' & A'_1 \\ 0 & -A'_3 \end{bmatrix}}_{Q} \begin{bmatrix} I & 0 \\ 0 & \varphi_c \end{bmatrix}. \tag{59}$$

The system will be fully controllable if the rank of matrix Q equals to $n+m$ as follows:

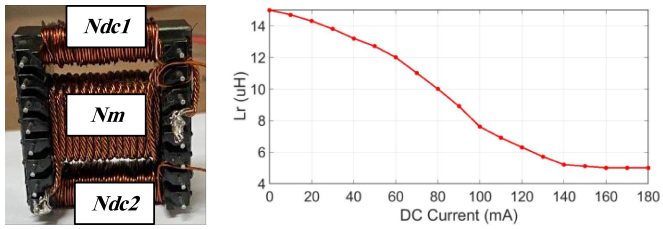
$$Rank\,(M) = n + m = 3. \tag{60}$$

The state equations of the system will be achieved by substituting (51) and (52) in (56) as follows:

$$\begin{cases} \begin{bmatrix} \dot{\tilde{x}}(t) \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A'_1 - B'K_x & -B'K_q \\ -A'_3 & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} + \begin{bmatrix} B' \\ 0 \end{bmatrix} \tilde{d}(t) \\ \qquad + \begin{bmatrix} 0 \\ 1 \end{bmatrix} r(t) \\ \tilde{y} = \begin{bmatrix} A'_3 & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix}. \end{cases} \tag{61}$$

Now, all three eigenvalues of the system should be shifted to the left side of the *jw* axis for various values of the auxiliary inductor.

The control coefficients K_x and K_q will be designed by using the placing equations in MATLAB software, in order to place the poles in required positions. The output voltage bode plots are achieved before and after implementing the control approach. Fig. 4(a) and (b) shows the output voltage magnitude and phase versus frequency bode plots with various values of the variable auxiliary inductor. These figures clearly prove that applying the control approach for the output voltage leads to placing the gain margin and phase margin in desirable ranges (60<PM<90, GM>10) with various values of the auxiliary inductor. Therefore, the closed-loop model performs well, and the output voltage is well-fixed at the desired value.



(a) (b)

Fig. 5. (a) Photograph of the utilized variable auxiliary inductor. (b) Variable inductance versus various dc control current values.

VII. Applying Variable Auxiliary Inductor for Guaranteeing the Soft-Switching Operation in Wide Ranges of Input Voltages and Loads

In order to guarantee the soft-switching operation of the proposed topology in wide input voltages and load ranges, a variable inductor is designed and applied in this section, instead of the regular auxiliary inductor. Considering the design limitations and reaching the favorable soft-switching condition, the auxiliary inductor and parallel capacitor should be adjustable and align with [26] and (32). Furthermore, given that the parallel capacitor's limitation is related to the auxiliary inductor value, adjusting the auxiliary inductor can satisfy both [26] and (32).

The applied auxiliary inductor consists of a gaped EE core with one main and two control windings [23]. Fig. 5(a) shows the photograph of the applied variable inductor, which clarifies the main winding's turn ratio (N_m) and the turn ratios of the control windings ($N_{\rm dc1}$ and $N_{\rm dc2}$). The variable inductor operates by applying a controllable dc current ($i_{\rm dc}$)(mA). Various inductance values of the auxiliary inductor are achieved only by changing the dc current. As a result, based on this characteristic, the variable inductor will be built and utilized.

Fig. 5(b) shows the relation between the dc current and auxiliary inductor value. Based on this figure, the maximum inductance value is achieved when the dc current equals to zero ($L_{r\text{-Max}} = 15\ \mu$H). Also, the auxiliary inductor's values will be reduced when the dc current is increasing up to the magnetic core saturation (150 mA), where the minimum inductance value will be attained ($L_{r\text{-Min}} = 4.5\ \mu$H).

The proposed converter operates between 100<P_o<200 W output powers and 30% and 70% duty cycles.

Moreover, the output voltage is fixed at 24 V, thanks to the closed-loop control approach. It is clear that the auxiliary inductor value directly relates to the duty cycle and output current.

$$L_r < \frac{R_o(1-d)}{2\,f_s} \overset{R_o=\frac{V_o}{i_o},\ V_o=\text{Const}}{\rightarrow} L_r = f(i_o,\ d). \tag{62}$$

The parallel capacitor's value is also fixed to provide a longer charging time than the switch's turn-OFF delay. The selected parallel capacitor is 12 nF. Finally, the auxiliary inductor will be supposed to have 80% of its maximum value, so that its negative current will be enough for full charge and discharge of the parallel capacitor in the designed ranges. Therefore

$$L_r = \frac{80}{100} \frac{R_o(1-d)}{2\,f_s}. \tag{63}$$

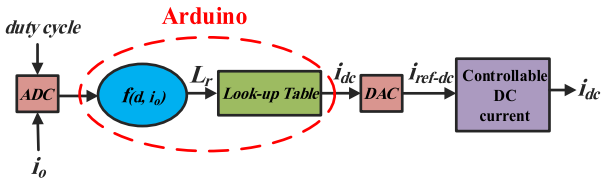


Fig. 6. Control loop of the auxiliary inductor.

By replacing the actual values in (63), the minimum and maximum values of the auxiliary inductor to provide soft-switching condition in $100<P_o<200$ W and $30\%<d<70\%$ ranges are as follows:

$$5\,\mu\text{H} < L_r < 15\,\mu\text{H}. \tag{64}$$

Based on (64) and Fig. 5(b), the variable auxiliary inductor will be able to provide the expected inductor values for soft-switching operation of the proposed converter in the above-mentioned design ranges. Fig. 6 shows the control block diagram of updating the inductor values for various duty cycles and loads. The output currents and duty cycles will be achieved from the current sensor and control section, respectively. Finally, the expected dc control current and in turn, the related inductor value for each dc current will readily be available.

VIII. Comparison Results

In Table III, the important features of the proposed converter and several similar structures are investigated. In the presented calculations, several assumptions are considered, which are listed as follows.

1) The volume of the switches and diodes is neglected.
2) In order to have a fair comparison, all the selected capacitors are chosen from mouser.com website. Also, the values of the selected capacitors are obtained based on the reported values in the compared articles.
3) All the implemented capacitors in the calculations are from the same brand (Panasonic) to have a fair price comparison.
4) Since the type of the implemented magnetic cores is not mentioned in some of the compared articles, similar to the implemented magnetic core of the proposed converter, E30/15/7 and E42/21/20 are chosen for these structures.

In fact, in Table III, all the features that play a role in the converter's worthiness are investigated. The first important factor is the simplicity of the topology. Considering Table III, the number of the required elements to assemble the proposed converter is six, which is equal to or less than all the other compared structures. The second important feature for this type of high-efficient and high-frequency converters is soft-switching capability. Considering the presented comparison, the proposed converter is capable of providing full soft-switching condition for both the power switch and power diode. The other important characteristics are volume, cost, and power density.

Considering the presented analysis, the total volume, assembling cost, and power density of the proposed converter is the least among all compared similar structures. Consequently, the proposed converter is well optimized in terms of volume, cost, and power density. The maximum obtainable power efficiency of the proposed converter and other similar structures are reported in Table III. Also, in order to have a clearer view regarding the power efficiency characteristic of the proposed converter and other compared structures, the measured power efficiency of the proposed converter and the reported experimental efficiencies of the other compared structures are illustrated in Fig. 7. In fact, all the above-mentioned priorities of the proposed converter, such as simplicity, full soft-switching capability, cost, and volume efficient, lead to a better power efficiency characteristic of the proposed converter in comparison to the similar structures.

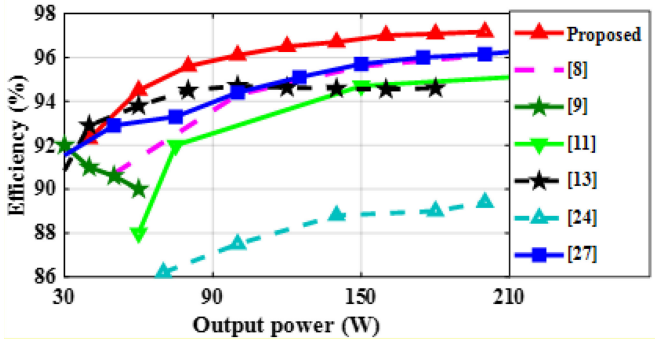


Fig. 7. Experimental efficiency comparison.

TABLE V
Hard Switching-Caused Losses of the Conventional Converter and Auxiliary Circuit-Caused Losses of the Proposed Converter at Different Output Powers ($f_s = 75$ kHz)

P_o	P_S+P_R	P_{Aux}	P_o	P_S+P_R	P_{Aux}
20W	0.69W	1.51W	120W	3.17W	1.75W
40W	1.19W	1.53W	140W	3.67W	1.84W
60W	**1.68W**	**1.56W**	160W	4.16W	1.95W
80W	2.18W	1.61W	180W	4.65W	2.07W
100W	2.67W	1.68W	200W	5.15W	2.20W

P_S: Summation of the turn-on and turn-off losses of the switch in the conventional converter.
P_R: Reverse recovery losses of the power diode in the conventional converter.
P_{Aux}: Additional losses caused by the auxiliary circuit in the proposed converter.

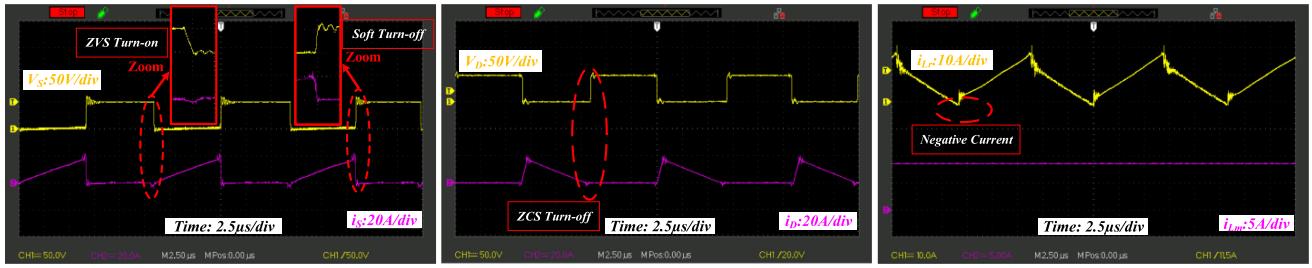
$$P_S = \frac{1}{2} f_S (t_r + t_f) V_S I_S + \frac{1}{2} f_S C_{oss} V_S{}^2 \;,\; P_R = \frac{1}{2} f_S (t_{re}) V_D I_D$$

$$P_{Aux} = P_{Core-Lr} + P_{Conduction-Lr} + P_{Conduction-Caux}$$

IX. Experimental Results

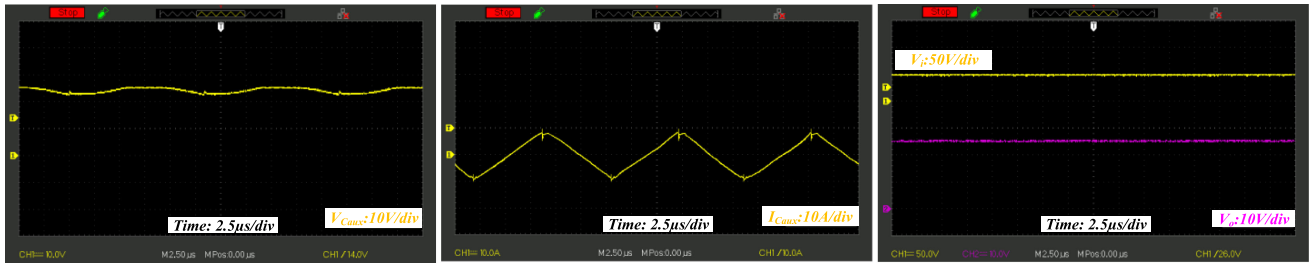
In this part, a 200-W experimental sample of the proposed soft-switched buck converter is built on the basis of the designed parameter values reported in Table IV.

The experimental results are illustrated in Figs. 8 –12. Figs. 8 and 9 show the experimental results of the proposed structure with the aforementioned designed values. Fig. 8(a) shows the switch voltage and current waveforms with its soft-switching operation. Considering this figure, the power switch turns ON under ZVS condition and also turns OFF under ZVS condition.



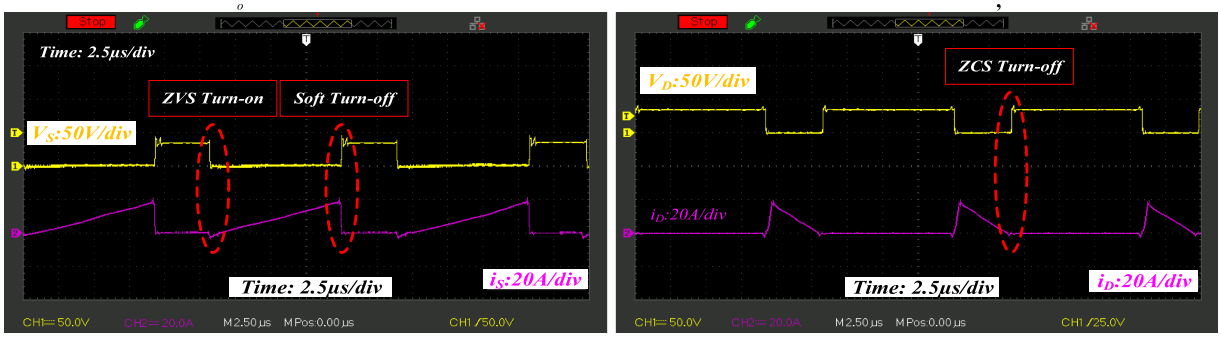
(a) (b) (c)

Fig. 8. Experimental waveforms ($P_o = 200$ W and $d = 50\%$). (a) Switch voltage and current waveforms. (b) Diode voltage and current waveforms. (c) Main and auxiliary inductors current waveforms.



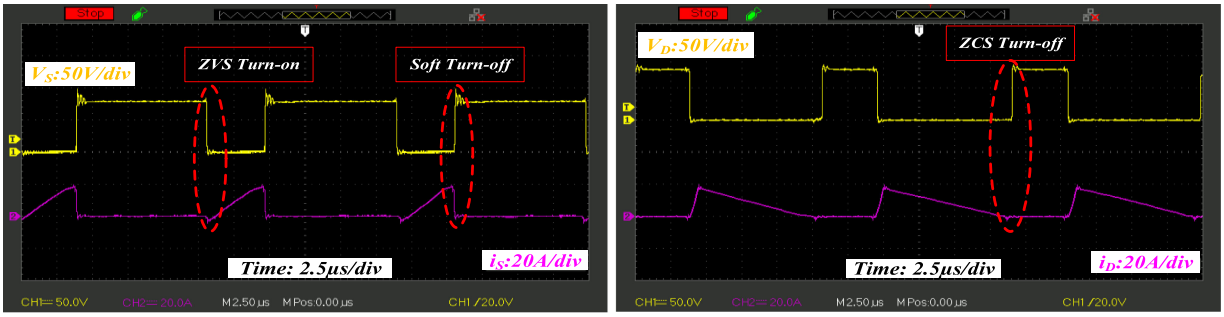
(a) (b) (c)

Fig. 9. Experimental waveforms ($P_o = 200$ W and $d = 50\%$). (a) Auxiliary capacitor voltage figure. (b) Auxiliary capacitor current figure. (c) Input and output voltages.



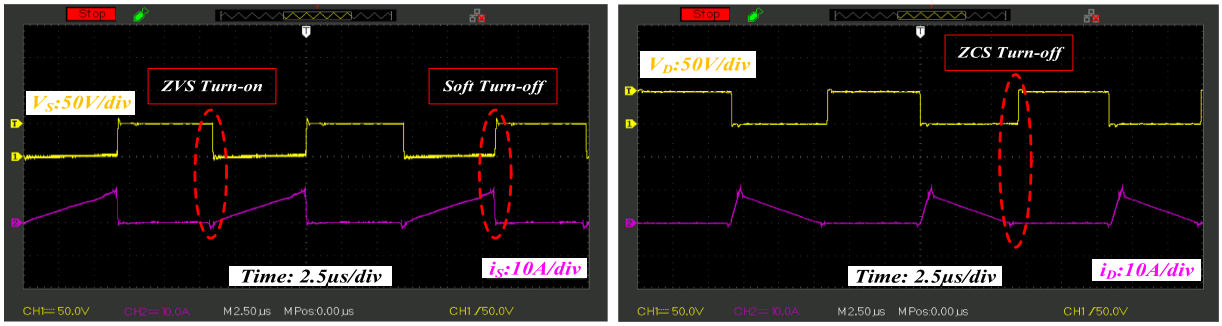
(a) (b)

Fig. 10. ($P_o = 200$ W and $d = 70\%$). (a) Switch voltage and current waveforms. (b) Diode voltage and current waveforms.



(a) (b)

Fig. 11. ($P_o = 200$ W and $d = 30\%$). (a) Switch voltage and current waveforms. (b) Diode voltage and current waveforms.



(a) (b)

Fig. 12. ($P_o = 100$ W and $d = 50\%$). (a) Switch voltage and current waveforms. (b) Diode voltage and current waveforms.

TABLE VI
HARD SWITCHING-CAUSED LOSSES OF THE CONVENTIONAL CONVERTER AND AUXILIARY CIRCUIT-CAUSED LOSSES OF THE PROPOSED CONVERTER AT DIFFERENT OUTPUT POWERS ($f_s = 150$ kHz)

P_o	P_S+P_R	P_{Aux}	P_o	P_S+P_R	P_{Aux}
20W	1.34W	2.28W	120W	6.29W	2.56W
40W	**2.33W**	**2.31W**	140W	7.28W	2.66W
60W	3.32W	2.35W	160W	8.27W	2.78W
80W	4.31W	2.40W	180W	9.26W	2.91W
100W	5.3W	2.47W	200W	10.25W	3.06W

TABLE VII
HARD SWITCHING-CAUSED LOSSES OF THE CONVENTIONAL CONVERTER AND AUXILIARY CIRCUIT-CAUSED LOSSES OF THE PROPOSED CONVERTER AT DIFFERENT OUTPUT POWERS ($f_s = 225$ kHz)

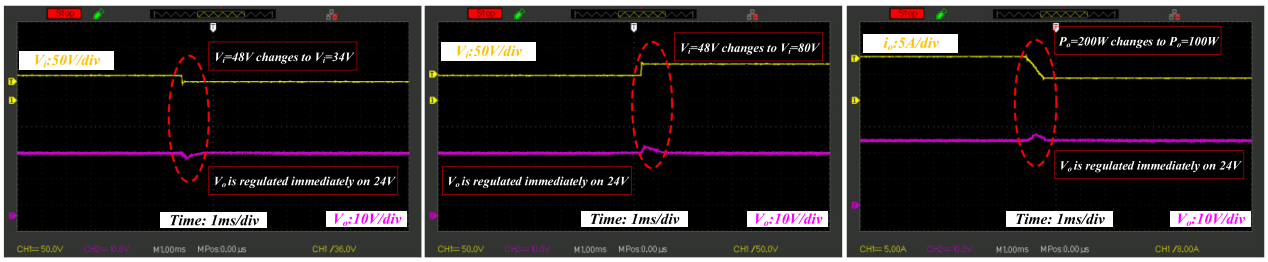
P_o	P_S+P_R	P_{Aux}	P_o	P_S+P_R	P_{Aux}
20W	2.01W	2.44W	120W	9.43W	2.72W
30W	**2.75W**	**2.45W**	140W	10.91W	2.82W
60W	4.97W	2.51W	160W	12.40W	2.94W
80W	6.46W	2.56W	180W	13.88W	3.07W
100W	7.94W	2.63W	200W	15.37W	3.22W

In addition, this figure indicates that the switch voltage-stress is equal to the input voltage. The power diode voltage and current waveforms are shown in Fig. 8(b). Based on this figure, the power diode current reaches zero before its turn-OFF moment and it turns OFF under ZCS condition. Moreover, the diode voltage stress is equal to the input voltage. Fig. 8(c) visualizes the main and auxiliary inductors current waveforms. Considering this figure, the main inductor current, which is equal to the output current, is practically constant. Therefore, the output current ripple is negligible. In addition, the auxiliary inductor current is bidirectional and has negative values just before the switch's turn-ON instant.

Fig. 9(a) and (b) shows the auxiliary capacitor voltage and current waveforms, respectively. Considering Fig. 9(a), the auxiliary capacitor voltage is approximately constant and its average value is $V_i - V_o$. Fig. 9(c) shows the input and output voltages of the proposed converter. Based on this figure, the voltage gain of the proposed structure equals to the conventional buck converter, which indicates that the voltage gain of this structure has not been affected by the auxiliary circuit.

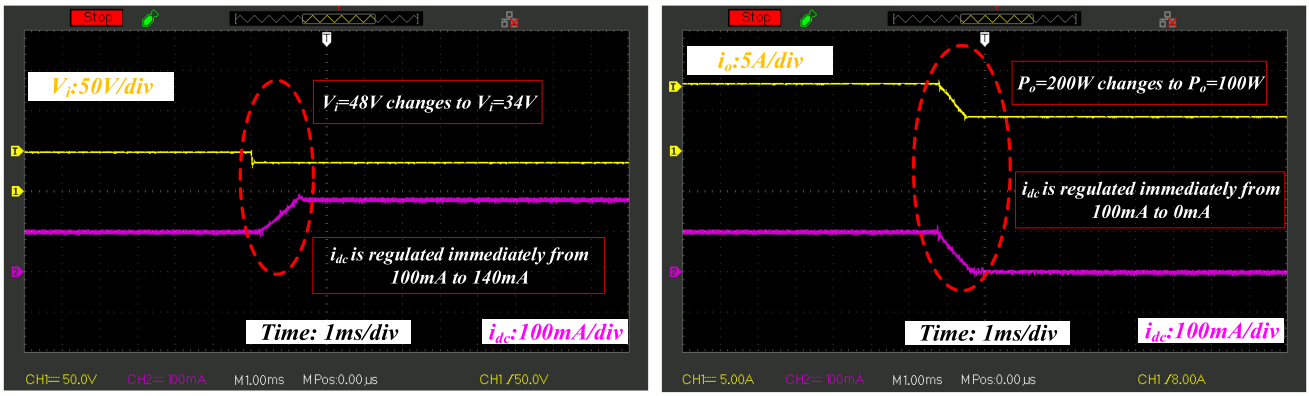
Taking into account the fact that in order to optimize the operation of the required buck converters in industrial applications, it is essential not only to provide soft-switching condition for a specific working point, but also it is necessary to guarantee the soft-switching performance for acceptable input voltage and load ranges in case of their step changes. In order to evaluate the capability of the proposed converter in providing the expected soft-switching condition with different values of input voltages and loads, the performance of the assembled prototype is tested in three different conditions ($P_o = 200$ W, $d = 70\%$, $V_i = 34.3$ V, $V_o = 24$ V, and $L_r = 5$ μH), ($P_o = 200$ W, $d = 30\%$, $V_i = 80$ V, $V_o = 24$ V, and $L_r = 13$ μH), and ($P_o = 100$ W, $d = 50\%$, $V_i = 48$ V, $V_o = 24$ V, and $L_r = 15$ μH). The obtained waveforms are illustrated in Figs. 10–12. When the input voltage falls to 34.3 from 48 V, in order to obtain the desired 24 V output voltage, the control system regulates the duty cycle to 70%. Moreover, the regulation loop of the auxiliary inductor tunes the dc control current of the variable inductor to provide 5 μH auxiliary inductor. Therefore, the soft-switching condition is ensured, as well as providing the desired output voltage. Considering Fig. 10, the power switch operates with soft-switching condition and the power diode turns OFF with ZCS condition as well. When the input voltage raises from 48 (nominal value) to 80 V, in order to achieve the desired output voltage, the control system regulates the duty cycle to 30%. In addition, the control loop of the variable inductor tunes the dc current and provides 14 μH auxiliary inductor. Consequently, based on Fig. 11, not only the soft-switching is attained, but also the output voltage is fixed on the desired value of 24 V. Now, it is assumed that the output load undergoes a step-change and the output power drops to the half of the nominal power value. In this case, since the input voltage is still 48 V, the duty cycle remains 50%. However, the control loop of the variable inductor regulates the dc current to provide 15 μH auxiliary inductor. Again, based on Fig. 12, it can be seen that the expected soft-switching condition and output voltage are achieved in the new condition. Therefore, based on Figs. 10–12, providing the expected soft-switching condition and desired output voltage of the assembled buck converter are guaranteed for $V_i = (34.3–80)$ V and $P_o = (100–200)$ W.

The dynamic responses of the output voltage and variable inductor control loops for step changes in the input voltages



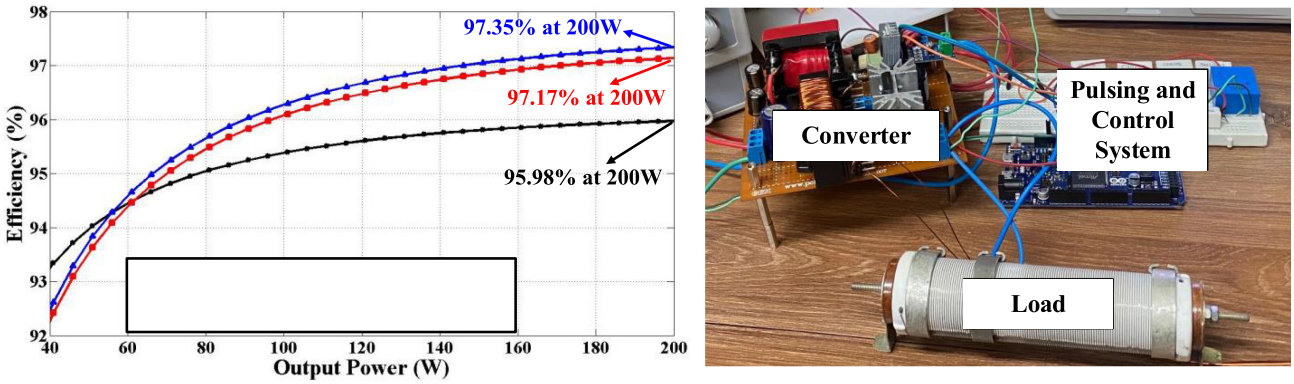
(a) (b) (c)

Fig. 13. Dynamic responses of the voltage control loop. (a) Dynamic response of the voltage control loop for step change of the input voltage from 48 to 34 V. (b) Dynamic response of the voltage control loop for step change of the input voltage from 48 V to 80 V. (c) Dynamic response of the voltage control loop for step change of the output power from 200 to 100 W.



(a) (b)

Fig. 14. Dynamic responses of the variable inductor control loop. (a) Dynamic response of the variable inductor control loop for step change of the input voltage from 48 to 34 V. (b) Dynamic response of the variable inductor control loop for step change of the output power from 200 to 100 W.



(a) (b)

Fig. 15. (a) Theoretical and experimental efficiency versus output power. (b) Experimental setup.

and output power have been illustrated in Figs. 13 and 14, respectively. As can be seen from Figs. 1(b) and 13(a), when the input voltage changes suddenly from 48 to 34 and 80 V, the output voltage control loop regulates the output voltage on the desired value immediately with very small overshoot. In addition, based on Fig. 13(c), the dynamic response of the output voltage control loop to the sudden load changes is fast with very small overshoot. In addition, considering Fig. 14(a) and (b), the variable-inductor control loop is capable of adjusting the desired dc current of the auxiliary inductor under sudden changes of the input voltage and load. As can be seen, the dc current reaches its desired value very fast to ensure the desired soft-switching performance of the converter in updated condition.

The theoretical and experimental efficiency waveforms of the proposed converter with the efficiency of the conventional buck converter (with similar components to the the proposed converter's prototype) versus output power are shown in Fig. 15(a). The experimental efficiency at full load condition is 97.17%, which proves the theoretical efficiency value (97.37%). Based on Fig. 15(a), the power efficiency modification of the proposed

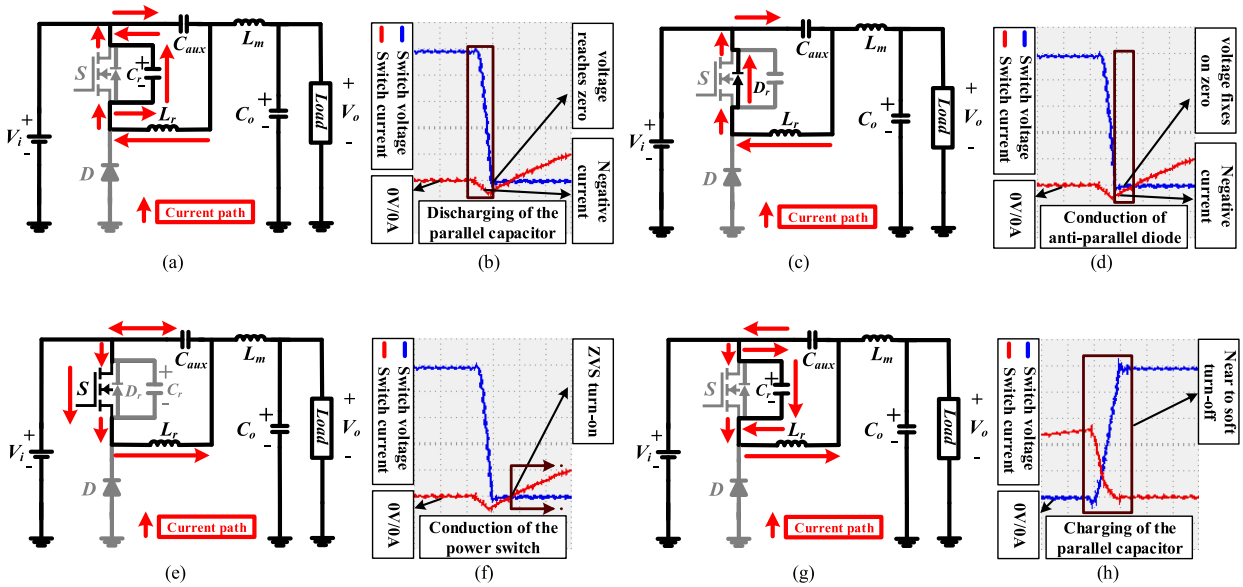


Fig. 16. Clarification of ZVS turn-ON and turn-OFF. (a) Equivalent circuit of the third operational mode. (b) Zoomed area of the third operational mode. (c) Equivalent circuit of the fourth operational mode. (d) Zoomed area of the fourth operational mode. (e) Equivalent circuit of the fifth operational mode. (f) Zoomed area of the fifth operational mode. (g) Equivalent circuit of the first operational mode. (h) Zoomed area of the first operational mode.

auxiliary circuit starts from around 60 W and its improvement starts to be significant from 100 W output power. Therefore, this significant improvement from 100 W output power makes using the proposed auxiliary circuit reasonable and it is the reason of choosing the above-mentioned soft-switching range for the proposed adjustable auxiliary circuit ($100<P_o<200$ W, $30\%<d<70\%$).

A photograph of the assembled laboratory prototype and the experimental setup are shown in Fig. 15(b), including the control and pulsing system and the proposed converter for 200-W output power.

The zoomed figures of the power switch's experimental voltage and current waveforms with the related equivalent circuits have been illustrated in Fig. 16. Based on Fig. 16(a), the generated negative current of the adjusted auxiliary inductor discharges the parallel capacitor of the power switch during the third operational mode. This claim can be proved by Fig. 16(b), which is the zoomed image of the experimental waveforms. Considering Fig. 16(b), the negative current, which flows through the power switch, discharges the parallel capacitor and the switch voltage decreases to zero. After complete discharging of the parallel capacitor, the switch voltage reaches zero and the only available path for the auxiliary inductor's negative current is the switch's antiparallel diode. Therefore, as it is illustrated in Fig. 16(c) and (d), during the fourth mode, the auxiliary inductor's negative current flows through the antiparallel diode and the power switch's voltage is stabilized at zero (it should be noted that the time duration of the third and fourth operational modes are too short in comparison to the switching period T_s). As it can be seen from Fig. 16(d), during the fourth operational mode, the switch voltage is sufficiently fixed at zero voltage and at the end of this mode, the auxiliary inductor's current reaches zero and the antiparallel diode turns OFF. Based on Fig. 16(e) and (f), at the beginning of the fifth operational mode, the auxiliary inductor's current increases from zero to positive

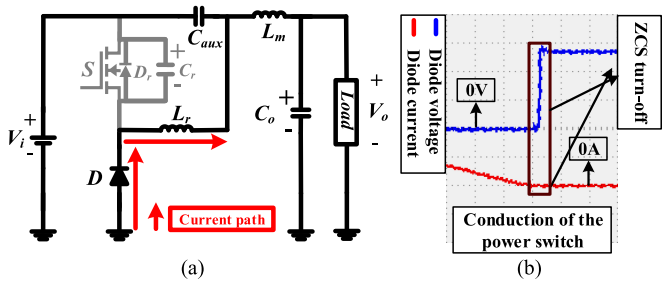


Fig. 17. Clarification of ZCS turn-OFF of the power diode. (a) Equivalent circuit of the second operational mode. (b) Zoomed area of the second operational mode.

values and the power switch turns ON under ZVS condition. The zoomed figures of the power switch's experimental voltage and current waveforms with the related equivalent circuit during the power switch's turn-OFF are illustrated in Fig. 16(g) and (h). Fig. 16(g) illustrates the equivalent circuit of the proposed converter at the moment that the power switch starts to be turned OFF. As it can be seen from Fig. 16(h), the positive current of the auxiliary inductor flows through the parallel capacitor and the switch voltage increases gradually. Therefore, based on Fig. 16(h) since the charging time of the parallel capacitor is designed to be more than the turn-OFF delay of the power switch, the junction point of the switch's voltage and current waveforms is almost zero and an approximate ZVS condition is provided for the power switch's turn-OFF.

The zoomed figures of the power diode's experimental voltage and current waveforms with the related equivalent circuit during the power diode's turn-OFF are illustrated in Fig. 17. As mentioned in the article, the auxiliary inductor should be adjusted to generate a bidirectional current. As mentioned above, by implementing the defined control system and variable inductor, the ZVS turn-ON of the power switch is ensured. Consequently,

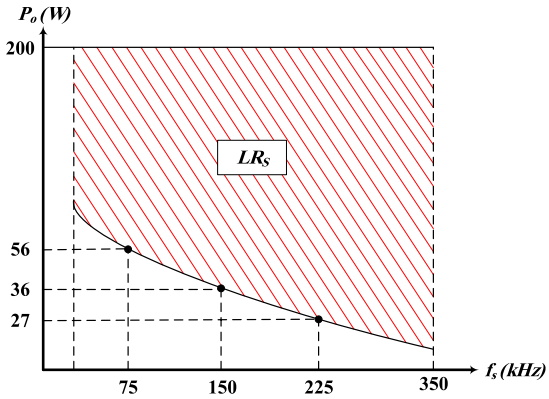


Fig. 18. Reasonable load range for soft-switching versus switching frequency.

during the power diode's turn-OFF, the auxiliary inductor's current should reach zero and be negative to discharge the switch's parallel capacitor. Therefore, as it can be seen from Fig. 17(b), the power diode turns OFF with ZCS condition.

X. Clarifying the Reasonable Load Range for Soft-Switching

In general, it is the nature of the auxiliary circuit-based soft-switching approaches to have low power efficiency at very light loads and low switching frequencies. In fact, at these situations, the eliminated switching losses of the soft-switching approach is not significant to cover the additional losses caused by the additional auxiliary circuit elements. Therefore, it is obvious that there should be an estimation of the reasonable load range at different switching frequencies for enabling the soft-switching block. The reasonable load range for soft-switching at a given switching frequency is the load range that using the soft-switching approach can modify the general performance of the system and importantly its power efficiency that is the main purpose of implementing the soft-switching circuits. In addition, the soft-switched converters are usually implemented with high switching frequencies ($f_s > 150 - 200\,\text{kHz}$) to reduce the cost and volume of the circuit and intensify the advantages of the soft-switching capability. Therefore, the reasonable load range of the proposed approach for soft-switching is investigated from very low frequencies ($f_s = 25\,\text{kHz}$) to the practical frequencies ($f_s = 350\,\text{kHz}$). Among all the frequencies in the investigated range, the detailed analysis and calculations for $f_s = 75\,\text{kHz}$ which is the switching frequency of the simplified laboratory prototype, $f_s = 150\,\text{kHz}$, and $f_s = 225\,\text{kHz}$ are presented in Tables V–VII, respectively.

Considering Tables V–VII, it can be seen that the reasonable load range for soft-switching is 60–200 W at $f_s = 75\,\text{kHz}$, 40–200 W at $f_s = 150\,\text{kHz}$, and 30–200 W at $f_s = 225\,\text{kHz}$. Fig. 18 illustrates the reasonable load range for soft-switching of the proposed converter at different switching frequencies. Based on this figure, as it is expected from an auxiliary circuit-based soft-switching circuit, increasing the switching frequency extends the reasonable load range for soft switching, and at practical high switching frequencies, it covers around 90% of the whole load range. In this article, all the required design and information are presented. Therefore, by implementing these design equations and control approach, it is possible to design a suitable high-efficient converter for any specific application.

XI. Conclusion

In this article, a simple auxiliary circuit was proposed and designed in order to achieve soft-switching condition for the conventional buck converter. Some advantages of this auxiliary circuit are as follows:

1) full ZVS condition for the power switch3
2) ZCS condition for the diode's turn-OFF and solving the reverse recovery problem of the power diode;
3) simple auxiliary circuit with two auxiliary components (a single auxiliary inductor and capacitor);
4) low volume;
5) low cost;
6) high power density;
7) adjustable auxiliary circuit, flexible control method, and complete design investigation which makes it practical to design and implement the proposed converter for different applications;
8) zero output current ripple by transferring the main inductor's current ripple to the auxiliary inductor.

In order to stabilize the output voltage, the closed-loop modeling of the proposed converter was presented. Also, the soft-switching operation of this structure for different input voltages and duty cycles was guaranteed, using a variable inductor. In order to verify the mentioned advantages, this structure has been compared with other structures. Moreover, a laboratory setup of this structure was designed and tested in order to show the soft-switching capability. In addition, the power losses and efficiency analysis were described at full load in details. Finally, the proposed structure had a 97.17% experimental power efficiency at full load.

References

[1] E. Amiri, R. Rahimzadeh, E. Adib, and A. Khoshkbar-Sadigh, "Multi-input high step-up DC–DC converter with independent control of voltage and power for hybrid renewable energy systems," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12079–12087, Dec. 2021.

[2] P. Alavi, V. Marzang, E. Nazari, M. Dezhbord, and E. Babaei, "New interleaved structure with high voltage-gain and low voltage-stress on semiconductors," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf.,* 2019, pp. 498–503.

[3] V. Marzang, P. Alavi, A. Khoshkbar-Sadigh, P. Mohseni, S. M. Hashemzadeh, and I. Talebian, "An interleaved high step-up DC-DC converter with low voltage-stress on semiconductors," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc.*, 2020, pp. 1223–1228.

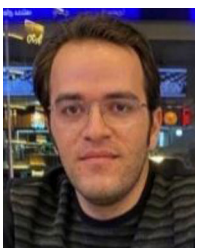
[4] I. Talebian and E. Babaei, "A simple DC-DC boost converter with soft-switching performance," in *Proc. 11th Power Electron., Drive Syst., Technol. Conf.*, 2020, pp. 1–5.

[5] V. Marzang, P. Alavi, M. Dezhbord, S. H. Hosseini, and N. Rostami, "Symmetric extendable ultra high step-up non-isolated DC-DC converter," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf.*, 2019, pp. 683–688.

[6] V. Marzang, S. H. Hosseini, N. Rostami, P. Alavi, P. Mohseni, and S. M. Hashemzadeh, "A high step-up non-isolated DC-DC converter with flexible voltage gain," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10489–10500, Oct. 2020.

[7] P. Alavi, P. Mohseni, E. Babaei, and V. Marzang, "An ultra-high step-up DC–DC converter with extendable voltage gain and soft-switching capability," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9238–9250,

[8] P. Alavi, E. Babaei, P. Mohseni, and V. Marzang, "Study and analysis of a DC–DC soft-switched buck converter," *IET Power Electron.*, vol. 13, pp. 1456–1465, 2020.
[9] K. I. Hwu and Y. T. Yau, "Simple design of a soft-switching buck converter," in *Proc. IEEE Int. Conf. Sustain. Energy Technol.*, 2008, pp. 410–414.
[10] D. Y. Jung, S. H. Hwang, Y. H. Ji, J. H. Lee, Y. C. Jung, and C. Y. Won, "Soft-switching bidirectional DC/DC converter with a LC series resonant circuit," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1680–1690, Apr. 2012.
[11] S. S. Lee, "Step-down converter with efficient ZVS operation with load variation," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 591–597, Jan. 2013.
[12] M. Kumar, M. Pattnaik, and J. Mishra, "An improved ZVS-PWM buck converter with ZCS auxiliary circuit," in *Proc. Int. Conf. TENCON*, 2017, pp. 1279–1284.
[13] G. Chen, Y. Deng, X. He, Y. Wang, and J. Zhang, "Zero-voltage-switching buck converter with low-voltage stress using coupled inductor," *IET Power Electron.*, vol. 9, no. 4, pp. 719–727, 2016.
[14] D. Cheshmdehmam, E. Adib, and H. Farzanehfard, "Soft-switched non-isolated high step-down converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 183–190, Jan. 2019.
[15] F. Cheng, Y. Zhang, and C. Yin, "A family of coupled-inductor-based soft-switching DC–DC converter with double synchronous rectification," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 6936–6946, Sep. 2018.
[16] N. S. Ting, I. Aksoy, and Y. Sahin, "ZVT-PWM DC–DC boost converter with active snubber cell," *IET Power Electron.*, vol. 10, no. 2, pp. 251–260, 2017.
[17] A. K. Panda, S. Sarode, and R. Tejavathu, "A novel active auxiliary circuit for efficiency enhancement integrated with synchronous buck converter," *Int. J. Circuit Theory Appl.*, vol. 44, no. 12, pp. 2043–2057, 2016.
[18] L. Jiang, C. C. Mi, S. Li, C. Yin, and J. Li, "An improved soft-switching buck converter with coupled inductor," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4885–4891, Nov. 2013.
[19] M. Ilic and D. Maksimovic, "Interleaved zero-current-transition buck converter," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1619–1627, Jun. 2007.
[20] A. Emrani, E. Adib, and H. Farzanehfard, "Single-switch soft-switched isolated DC–DC converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1952–1957, Apr. 2012.
[21] R. H. Ashique and Z. Salam, "A family of true zero voltage zero current switching (ZVZCS) nonisolated bidirectional DC–DC converter with wide soft switching range," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5416–5427, Jul. 2017.
[22] W. Zhang, X. Zhang, Z. Chen, Y. Liu, and X. Zhao, "A novel soft switching technique for special buck converter with high power and high efficiency," in *Proc. IEEE Region 10 Conf.*, 2006. pp. 1–4.
[23] M. S. Perdigão, M. F. Menke, Á. R. Seidel, R. A. Pinto, and J. M. Alonso, "A review on variable inductors and variable transformers: Applications to lighting drivers," *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 531–547, Jan. 2016.
[24] E. Adib and H. Farzanehfard, "Analysis and design of a zero-current switching forward converter with simple auxiliary circuit," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 144–150, Jan. 2010.
[25] S. Fan, L. Sun, J. Duan., and K. Zhang, "Improved active clamped ZVS buck converter with freewheeling current transfer circuit," *IET Power Electron.,* vol. 12, no. 6, pp. 1341–1348, 2019.
[26] V. V. Subrahmanya Kumar Bhajana, P. Drabek, R. Thumma, and R. Makireddi, "Improved bidirectional DC/DC converter configuration with ZVS for energy storage system: Analysis and implementation," *IET Power Electron.,* vol. 13, no. 5, pp. 1103–1112, 2020.
[27] M. Kim, D. Yang, and S. Choi, "A fully soft-switched single switch isolated DC-DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1106–1111.



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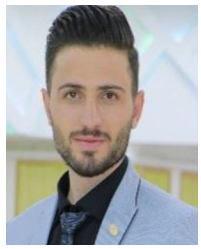

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