An AC–DC Coupled Droop Control Strategy for VSC-Based DC Microgrids

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***Abstract*—Droop control is a common strategy to facilitate appropriate load sharing among different sources in dc microgrids (MGs). To endow simple control structure and fast bus voltage transient response to dc MGs with multiple voltage source converters (VSCs), this article proposes an ac–dc coupled droop control strategy, which yields the ac current (active components i_d) reference of the VSCs inner loop directly in the *dq* frame. In this way, the ac current (i_d) of the VSCs inner loop is directly linked to the load sharing performance of the dc MG. In contrast with the existing droop approaches, the proposed method does not require any extra outer dc voltage/current proportional–integral (PI) loops, which avails fast bus voltage dynamics during transients. Systematic evaluation of its performance is conducted by small-signal modeling and subsequent analysis from a single-source operation to a multisource operation. The effects of inner current loop bandwidth and droop gain on system stability are studied while feeding constant power loads. The theoretical analysis has been validated by both simulation and experimental results.**

***Index Terms*—Constant power load (CPL), dc microgrid (MG), droop control, impedance model, stability, voltage source converter (VSC).**

I. Introduction

THE concept of a microgrid (MG) is gaining ever-increasing attention and momentum in both industry and academia, which is known as a relatively independent small-scale power system. With the fast development of dc sources and loads, e.g., photovoltaics, fuel cells, energy storage systems, and electric vehicles, dc MGs inherently have higher efficiency attributed to less power conversion stages [1], [2]. Also, reactive power, synchronization, and skin effect are not present in dc MGs. For these reasons, a dc MG has been recognized as an attractive choice to integrate distributed generators (DGs) and loads in terrestrial applications, as well as in marine/aircraft onboard electrical systems [3], [4].

Appropriate load sharing among different sources is of importance in a dc MG [5]. Strategies for load sharing can be mainly grouped into two categories, i.e., active load sharing (e.g., master–slave control, centralized control, and circular current chain control [1], [6], [7]) and passive load sharing (e.g., droop control [8], [9]). The main shortcoming of active load sharing is the dependence on the communication infrastructure, which is not always convenient to implement. Instead, droop control has been widely adopted as a passive load sharing technique in dc MGs to achieve autonomous load sharing with improved reliability.

The main concerns of a droop-controlled dc MG can be classified into two aspects, i.e., static performance and dynamic performance. The static performance mainly falls on the tradeoff between load sharing accuracy and desired voltage regulation at a steady state. The existing literature have improved the static performance of the dc MG [10]–[12]. It is found that nonlinear droop methods have demonstrated better performance than linear droop in achieving voltage regulation and load sharing [13], [14]. A polynomial function is used as the droop characteristic in [13], which combines droop curves with odd coefficients. An inverse parabolic function is used in [14] to improve the voltage regulation at light loads and current sharing at heavy loads. The drawback of nonlinear droop is that the parameters of nonlinear droop are difficult to design and they only focus on the droop characteristic with dc port variables, i.e., dc voltage and dc current/power.

The other main concern is the dc bus voltage's dynamic, which is influenced by converters at both source and load side. When the load converter tightly regulates its output power, it performs as a constant power load (CPL) with negative impedance [11], which may lead to voltage oscillation and even system instability [15]. The most critical scenario of dc bus stability happens when an instantaneous source and load power mismatch leads to a sudden voltage change in the bus capacitor. Fast dynamics of the source converter can mitigate the negative effect of CPL, which requires instantaneous current injection at the dc bus [16]. Thus, the bus voltage's dynamic can be improved by the source converter with a faster dynamic under CPL transients and the whole system will present a larger stability margin.

Several control techniques have been adopted on source converters in dc MGs to improve the dc bus voltage

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performance, containing both linear and nonlinear methods. With proportional–integral (PI) controller, a dual loop compensator is usually adopted, i.e., the outer loop (dc voltage/current PI loop) and inner loop (inductor PI current) [17]. The existence of the outer dc voltage/current PI loop provides explicit regulation to the voltage/current but imposes the overall bandwidth reduction due to the cascaded control structure [18]. Since simply increasing the control loop bandwidth of the source converter may lead to system instability [17], [18], linear approaches focus on stabilizing the closed-loop transfer function with active damping. In [19], a virtual resistor is proposed to connect in series with the source converter to reshape the source impedance as an active damping technique. Similarly, a frequency-dependent virtual impedance is proposed in [20] to reshape the source impedance in the selected frequency range. Passivity-based control is another method of designing a stabilizing controller [21], which can be derived from the energy function of the system. However, it is difficult to transform the high-order system into specific energy form when the number of converters is large. Under heavy load, linear control techniques may lead to poor bus voltage regulation performance [22], whereas nonlinear controllers are proposed based on large-signal models, which can achieve robust and fast dynamics in a wider range [23], [24]. In [25], a control design procedure is presented on a shipboard dc MG where a linearization via state feedback method is proposed to face the CPL destabilizing effect and to ensure the dc bus voltage stability. In [26], a composite nonlinear controller is proposed for stabilizing CPLs in dc MGs by integrating a nonlinear disturbance observer-based compensation with a backstepping design algorithm. The disadvantage of the aforementioned advanced controllers is the requirement of accurate and detailed parameters of the whole system, which is usually difficult in an MG. Meanwhile, they also only focus on the dc variables, i.e., dc voltage and dc current/power.

In general, previous dynamic performance enhancements of dc MGs rely on the droop characteristic of dc variables [18], and their derivatives [19]. To use a metaphor, the latest works further improve the performance of converters by packaging "new boxes" outside the "black box" (dual-PI-ruled converters) or introducing advanced controllers instead of PI controllers. Although the static and dynamic performance is improved, the controller is becoming more complex and computationally intensive. As opposed to the aforementioned methods, this article aims to open up the "black box" to look for a more concise way to implement the load sharing strategy in dc MGs. Since many DGs use vector-controlled voltage source converters (VSCs) as interfaces to the dc bus, the active power can be controlled via ac current (i_d) of the inner loop in the *dq* frame. As far as the authors know, no work has directly linked the ac current control to the load sharing of the dc MG before. This article proposes a droop characteristic between the dc output voltage and ac current, namely an ac–dc coupled droop controller. It directly yields the ac current reference for the inner current loop, to enable the load sharing among DGs. Faster dynamics are expected since the outer dc voltage/current controller is eliminated from the cascaded structure, compared with the traditional dual-PI-ruled converters.

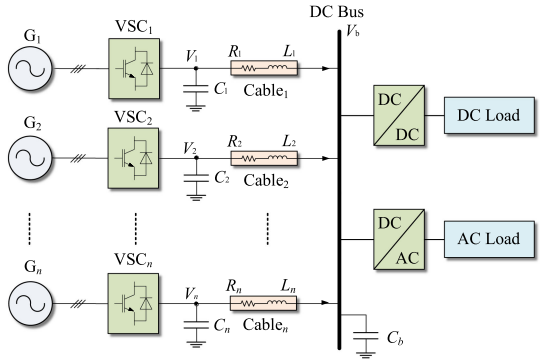

Fig. 1. DC MG architecture under study.

The main contributions of this article are highlighted as follows.

1) An ac–dc coupled droop characteristic of ac current with respect to dc voltage is proposed for VSCs in dc MGs. Small-signal modeling and subsequent stability analysis are conducted in detail in terms of inner current loop bandwidth and droop gain when supplying CPLs.
2) Impedance analysis with the ac–dc coupled droop control strategy has been generalized from a single-source single-load system to a multisource multiload dc MG. A global droop gain is proposed to facilitate the design of the dc MG. A detailed design procedure is given from the perspective of steady-state, dynamic, and stability of the system.

The rest of this article is organized as follows. Section II introduces the working principle and small-signal modeling of the proposed droop control strategy. Section III derives the source/load impedance and analyses the system stability. Section IV extends the analysis to a generalized multisource multiload dc MG. Validations of the analysis with experimental studies are presented in Section V. Finally, Section VI concludes this article.

II. AC–DC Coupled Droop Strategy

Fig. 1 illustrates the configuration of the dc MG studied in this article. Multiple VSCs powered by DGs are connected to the same dc bus, forming the bus voltage and feeding power to the load. C_i ($i = 1, 2, \ldots, n$) corresponds to a local capacitor, and C_b is the common capacitor installed on the dc bus. R_i and L_i ($i = 1, 2, \ldots, n$) represent the cable impedance from the source converter to the dc bus. Typical loads in a dc MG interfaced with dc–dc or dc–ac converters can be tightly regulated as CPLs. Fig. 2 shows the typical vector control strategy for the VSC.

A. Working Principle of the AC–DC Coupled Droop Characteristic

The traditional current-mode droop control scheme yields the dc current reference from the *I–V* droop characteristic as shown in Fig. 3, which is shown as

$$i_{\mathrm{dc}}^{*} = \frac{1}{k}\left(V_0 - v_{\mathrm{dc}}\right). \tag{1}$$

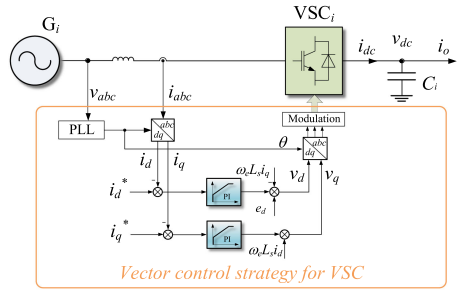

Fig. 2. Vector-controlled VSC.

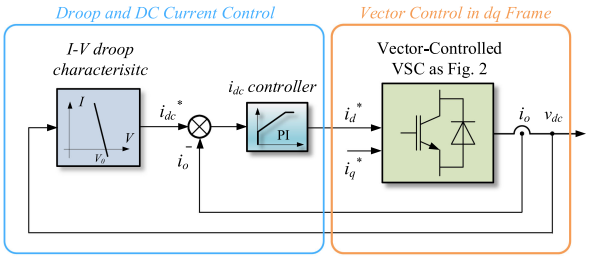

Fig. 3. Traditional current-mode droop control scheme.

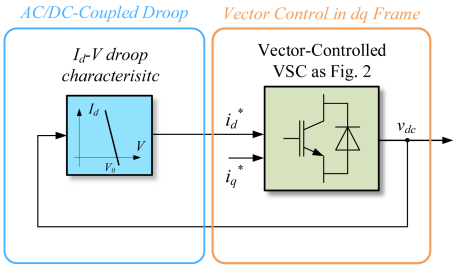

Fig. 4. Proposed $i_{\rm d}$–$v_{\rm dc}$ droop control scheme.

In the *dq* frame, a decoupled vector control strategy can be implemented, as shown in Fig. 2, where the *d*-axis and *q*-axis are used to control the active and reactive power, respectively. This property gives the theoretical basis to achieve the active power sharing among DGs by controlling the ac current (i_d) directly. Hence, a droop characteristic of dc voltage ($v_{\rm dc}$) and ac current (i_d), namely an ac–dc coupled droop controller, can be proposed, where the i_d reference is generated directly from the droop characteristic as shown in Fig. 4, based on the dc voltage measurement as follows:

$$i_d^* = \frac{1}{k}\left(V_0 - v_{\rm dc}\right) \tag{2}$$

where k is the droop gain, V_0 is the nominal bus voltage, $v_{\rm dc}$ is the measured dc voltage, and $i_d{}^*$ is the generated *d*-axis current reference. As compared in Figs. 3 and 4, the cascaded $i_{\rm dc}$ controller is eliminated, which could lead to a fast dynamic response of the system. Detailed modeling and evaluation of the proposed droop method will be conducted in the following part.

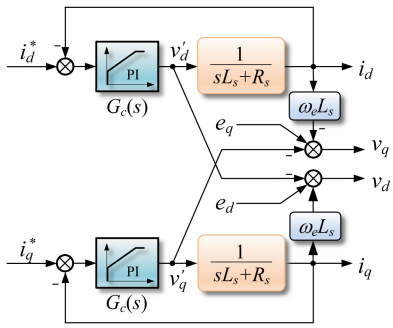

Fig. 5. Control block diagram of the inner current loop.

B. Small-Signal Modeling

1) Vector Control of Inner Loop Current: As shown in Fig. 5, using the classical vector control in the *dq* frame, the *d*/*q*-axis voltages of the VSC yield

$$\begin{cases} v_d = -(R_s + L_s s)i_d + \omega_e L_s i_q + e_d \\ v_q = -(R_s + L_s s)i_q - \omega_e L_s i_d + e_q \end{cases} \tag{3}$$

where e_d and e_q are the bus voltages at the point of common coupling, R_s and L_s are the ac-side resistance and inductance, and ω_e is the frequency of the ac source in rad/s. In this article, the *d*-axis is used to regulate the active power. Thus, e_q is controlled to be zero and e_d is the magnitude of the phase voltage vector.

According to (3), dynamics of the inner loop current can be expressed as

$$\begin{cases} \frac{di_d}{dt} = \frac{1}{L_s}(v'_d - R_s i_d) \\ \frac{di_q}{dt} = \frac{1}{L_s}(v'_q - R_s i_q) \end{cases} \tag{4}$$

where $v'_d = -v_d + \omega_e L_s i_q + e_d$ and $v'_q = -v_q - \omega_e L_s i_q + e_q$.

Hence, the plant of the decoupled inner loop can be obtained as

$$\frac{i_d(s)}{v'_d(s)} = \frac{1}{sL_s + R_s}. \tag{5}$$

Assuming the inner current loop is designed to be a first-order system with the corner frequency ω_c, and the zero of PI compensator $G_{\rm c}(s)$ is set to cancel the pole of the controlled plant. Hence, the proportional gain k_{pc} and integral gain k_{ic} are given as follows:

$$k_{pc} = \omega_c L_s,\ k_{ic} = \omega_c R_s \tag{6}$$

where ω_c is the bandwidth of the inner current loop, and $\tau = 1/\omega_c$.

Given the above, the inner current loop can be expressed as

$$T_{id}(s) = \frac{i_d(s)}{i_d^*(s)} = \frac{1}{1 + \frac{s}{\omega_c}} = \frac{1}{1 + \tau s} \tag{7}$$

where τ is the bandwidth of the inner current loop.

2) DC Current Control: The equivalent control block diagram of the ac–dc coupled droop control scheme is shown in Fig. 6.

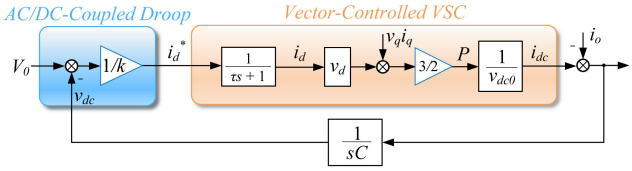

Fig. 6. Control block diagram for the ac–dc coupled droop method.

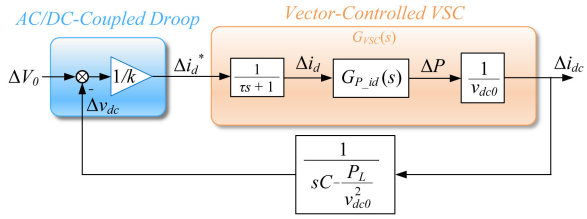

Fig. 7. Linearized control block diagram for the $i_{\rm d}$–$v_{\rm dc}$ droop-controlled system.

According to (3), assuming the reactive power equals zero ($i_q = 0$), the d-axis voltage v_d can be linearized as

$$\Delta v_d = -(R_s + L_s s)\Delta i_d + \omega_e L_s \Delta i_q \approx -(R_s + L_s s)\Delta i_d. \tag{8}$$

Likewise, the active power component can be linearized as

$$\Delta P = \frac{3}{2}(v_{d0}\Delta i_d + \Delta v_d i_{d0}) \tag{9}$$

where the parameter with subscript "0" represents the steady-state equilibrium point.

Substituting (8) into (9), the i_d-to-P transfer function can be derived as

$$G_{P\_i_d}(s) = \frac{\Delta P}{\Delta i_d} = \frac{3}{2}\left[(v_{d0} - R_s i_{d0}) - L_s i_{d0} s\right]. \tag{10}$$

Corresponding control to output (Δi_d^* to $\Delta i_{\rm dc}$) transfer function of the vector-controlled VSC in Fig. 6, i.e., $G_{\rm VSC}(s)$, can be expressed as

$$\begin{aligned} G_{\rm VSC}(s) = \frac{\Delta i_{\rm dc}}{\Delta i_d^*} &= \frac{3\left[(v_{d0} - R_s i_{d0}) - L_s i_{d0} s\right]}{2v_{\rm dc0}(\tau s + 1)} \\ &= K_{\rm VSC}\frac{(1 - \frac{s}{\omega_{z0}})}{(1 + \frac{s}{\omega_c})} \end{aligned} \tag{11}$$

where $K_{\rm VSC}$ is the dc gain of $G_{\rm VSC}(s)$, and ω_{z0} is the frequency corresponding to the right-half-plane zero (RHPZ). Their detailed expressions are shown in Appendix (38)–(39). The RHPZ of $G_{\rm VSC}(s)$ will pose some challenges to the system stability, as investigated in Section III.

3) DC Voltage Control: Considering the dc bus voltage dynamics, the relationship between dc output current and voltage under load P_L can be written as

$$\begin{cases} \Delta i_{\rm dc} - \Delta i_o = C\frac{d}{dt}\Delta v_{\rm dc} \\ i_o = \frac{P_L}{v_{\rm dc}} \Rightarrow \Delta i_o = -\frac{P_L}{v_{\rm dc0}^2}\Delta v_{\rm dc}. \end{cases} \tag{12}$$

Therefore, the transfer function from dc current to dc voltage can be obtained as

$$\frac{\Delta v_{\rm dc}}{\Delta i_{\rm dc}} = \frac{1}{sC - \frac{P_L}{v_{\rm dc0}^2}}. \tag{13}$$

Fig. 7 shows the linearized control block diagram of the proposed droop-controlled system. According to Fig. 7, the open-loop transfer function of the dc voltage can be written as

$$T_{\rm vdc}(s) = \frac{G_{\rm VSC}(s)}{k(sC - \frac{P_L}{v_{\rm dc0}^2})} = K_{\rm vdc}\frac{(1 - \frac{s}{\omega_{z1}})}{(1 - \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_c})}. \tag{14}$$

Correspondingly, the overall closed-loop transfer function of $v_{\rm dc}$ can be expressed as

$$\frac{\Delta v_{\rm dc}}{\Delta v_o} = \frac{G_{\rm VSC}(s)}{G_{\rm VSC}(s) + k(sC - \frac{P_L}{v_{\rm dc0}^2})}. \tag{15}$$

Detailed expressions of $K_{\rm vdc}$, ω_{z1}, and ω_{p1} in $T_{\rm vdc}(s)$ and the closed-loop transfer function are shown in Appendix (40)–(43). It can be inferred from (15) that the droop gain will influence the bandwidth of the voltage control loop under the ac–dc coupled droop control, which will affect the dynamic performance and stability.

III. Analysis of the Single-Source Single-Load System

Before the multisource operation of the ac–dc coupled droop control in a dc MG, this section will first investigates the characteristics of a basic single-source single-load system, including the steady-state performance and dynamic performance.

A. Steady-State Performance

Assuming the reactive power equals zero, the $I_{\rm d}-V_{\rm dc}$ characteristic at steady state can be expressed as

$$\begin{cases} I_d = \frac{V_0 - V_{\rm dc}}{k} \\ V_d = e_d - I_d R_s \\ V_{\rm dc} I_{\rm dc} = \frac{3}{2} V_d I_d. \end{cases} \tag{16}$$

By combining (16), the external V–I characteristic of the source converter under ac–dc coupled droop control can be expressed as

$$I_{\rm dc} = \left(\frac{3R_s V_0}{k^2} - \frac{3e_d}{2k}\right) + \left(\frac{3ke_d V_0 - 3R_s V_0^2}{2k^2}\right)\frac{1}{V_{\rm dc}} - \frac{3R_s}{2k^2}V_{\rm dc}. \tag{17}$$

For the load, a CPL can be expressed as a hyperbolic line when

$$I_{\rm dc} = \frac{P_L}{V_{\rm dc}} \tag{18}$$

where $V_{\rm dc}$ at steady state can be expressed as follows:

$$V_{\rm dc} = \frac{6R_s V_0 - 3ke_d + \sqrt{3}k\sqrt{3e_d^2 - 8P_L R_s}}{6R_s}. \tag{19}$$

Fig. 8 shows the V–I characteristic of the source and load subsystem expressed by (17) and (18), respectively. The dashed line represents the CPL and the solid lines represent the source characteristics under different droop gains ($k_1 < k_2 < k_3 < k_4$).

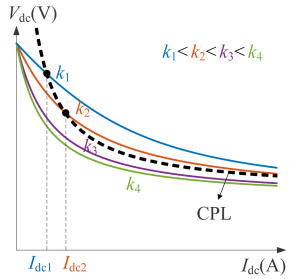

Fig. 8. Interaction between the droop-controlled source and CPL.

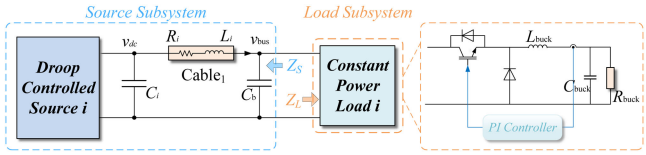

Fig. 9. Equivalent circuit of the single-source single-load system.

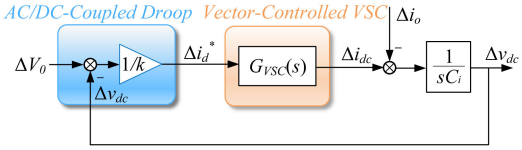

Fig. 10. Linearized block diagram for the v_{dc} dynamic character.

It is worth noting that two intersections exist between the CPL and droop curve. Only the left one with a higher dc voltage is stable, which can be selected as a steady-state operating point. The term "$3e_d{}^2$–$8P_LR_S$" should be always positive to ensure the existence of the steady-state operating point.

As one can see in Fig. 8, a larger droop gain will lead to a larger voltage deviation at dc bus. When the droop gain is selected as k_3 and k_4, there is no intersection point between the source and load curve, indicating that no equilibrium point exists. Thus, the droop gain should be designed to ensure that an equilibrium point (an intersection in Fig. 8) exists when feeding a CPL, which is derived as

$$k < \frac{6R_sV_0}{3e_d - \sqrt{3}\sqrt{3e_d^2 - 8P_LR_s}}. \tag{20}$$

B. Impedance Modeling of Source and Load Subsystem

In the dc MG, the state-space model will become more complicated with higher order. Thus, an impedance model is preferred for the port analysis of the subsystem and consequent system stability with easy expansibility.

Assuming that the source and load converters are individually stable, when the output impedance of the source converter Z_S is less than the input impedance of the load converter Z_L over the entire frequency range, the stability of the cascaded system can be guaranteed based on Middlebrook's criterion [28]. The equivalent circuit of the single-source single-load system is shown in Fig. 9. Dynamic characteristic of the linearized dc voltage v_{dc} is shown in Fig. 10.

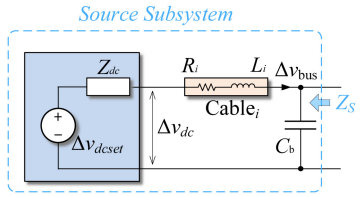

Fig. 11. Linearized equivalent circuit for a source subsystem.

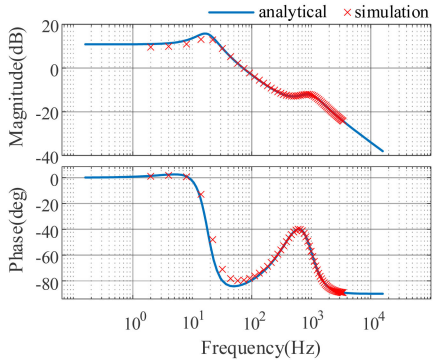

Fig. 12. Impedance verification of the source subsystem.

Then, the dc voltage can be obtained as

$$\begin{aligned}\Delta v_{\rm dc} &= \frac{G_{\rm VSC}(s)}{ksC + G_{\rm VSC}(s)}\Delta V_0 - \frac{k}{ksC + G_{\rm VSC}(s)}\Delta i_o \\ &\triangleq \Delta v_{\rm dcset} - Z_{\rm dc}\Delta i_o\end{aligned} \tag{21}$$

where $\Delta v_{\rm dcset}$ is defined as the equivalent voltage source, and $Z_{\rm dc}$ is defined as the equivalent output impedance related to inner current control and droop control.

Based on the Thevenin theorem, the equivalent circuit can be obtained from (21), as shown in Fig. 11, where the dc bus capacitor is represented by C_b, and the cable impedance is represented by R–L series (R_i, L_i).

Thus, the total source impedance can be expressed as

$$Z_S(s) = \frac{1}{sC_b} // \left(R_i + sL_i + \frac{k}{ksC_i + G_{\rm VSC}}\right). \tag{22}$$

The detailed expression of $Z_s(s)$ is shown in Appendix (44). Frequency responses are simulated in MATLAB/Simulink and plotted in the Bode diagram to verify the correctness of (22), as shown in Fig. 12. The circuit parameters including hardware and control parameters are listed in Table I. The dc MG is based on a 270-V dc bus, which is a typical application scenario in the more-electric aircraft. The ac source parameters are determined by the DGs in reality, and the R–L series is set to represent a 10-m cable connecting the DG to the bus, with 20 mΩ/m and 6.5 μH/m. The local capacitor is designed to ensure both a small voltage ripple rate and a fast dynamic response. Meanwhile, the design of controller parameters is studied in Sections III and IV with single-source and multisource operations, respectively.

As for the load converter, a tightly regulated buck converter is controlled as a CPL, whose input impedance Z_L can be derived

TABLE I
SYSTEM PARAMETERS

	Parameter	Symbol	Value
Hardware parameters	Cable resistance	R_i	0.2 Ω
	Cable inductance	L_i	65 μH
	Local capacitance	C	1.6 mF
	Bus capacitance	C_b	0.6 mF
	AC source	e_{d0}	100 V
	AC source resistance	R_s	0.05 Ω
	AC source inductance	L_s	3 mH
Controller parameters	Inner control bandwidth	ω_c	800 Hz
	Nominal voltage	V_o	270 V
	Droop gain	k_i	1

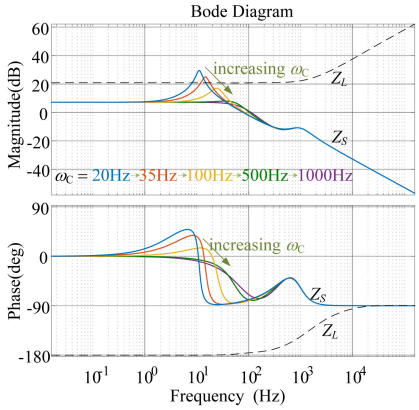

Fig. 13. Bode plot of source/load impedances with varying ω_c.

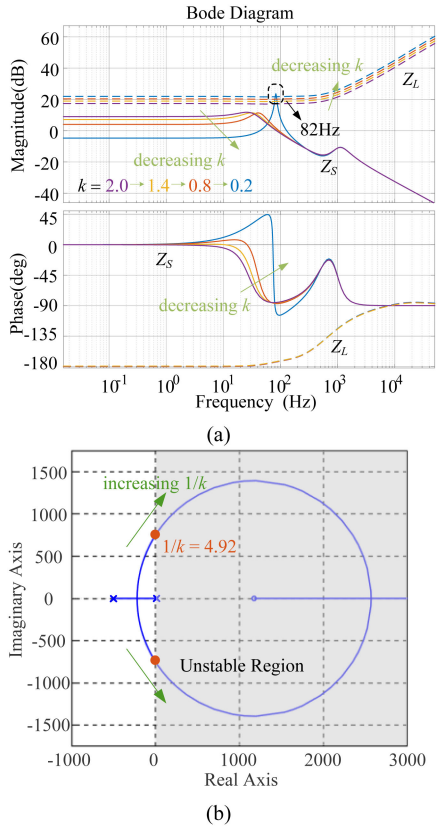

Fig. 14. Small-signal analysis of the single-source single-load system with different droop gains. (a) Bode plot of source/load impedances with different values of droop gains. (b) Eigenvalue contour with respect to the inverse of the droop gain.

according to [29] as

$$Z_L(s) = \frac{{V_{\rm dc}}^2 (s+\omega_L)\,\Delta}{P_L\left(R_{\rm buck}C_{\rm buck}s^2 + s - \omega_L\Delta\right)} \tag{23}$$

where ω_L is the control bandwidth of the CPL, $V_{\rm dc}$ is the dc bus voltage, and $\Delta = L_{\rm buck}C_{\rm buck}s^2 + \frac{L_{\rm buck}}{R_{\rm buck}}s + 1$.

C. Parametric Analysis

After deriving the equivalent source and load impedance, the stability assessment with regard to control parameters can be evaluated. As can be inferred from (11) and (22), control parameters have prominent effects on $G_{\rm VSC}(s)$, which will influence the system stability. To test the validity of the ac–dc coupled droop controller on a wider range of system conditions, a parametric analysis is performed. In this section, a detailed discussion on the ac–dc coupled droop controller is presented to assess the impact of both inner current loop bandwidth and droop gain on small-signal stability of the system.

1) Effect of the Inner Current Control: Stability analysis is conducted based on the impedance model built in Section III-B. The influence of inner current loop bandwidth on the source impedance is investigated in Fig. 13.

The source (solid lines, Z_S) and load (dashed lines, Z_L) impedance and interaction are shown with different inner current loop bandwidth, where a buck converter under constant power control is utilized as an example of CPL. As shown in Fig. 13, slow inner loop control bandwidth (less than 100 Hz) will challenge the stability since the magnitude of the source hits the load while the phase discrepancy exceeds 180°. Increasing the inner current bandwidth can attenuate the peak magnitude and enlarge the stability margin, while the magnitude in the low-frequency band is not influenced. Thus, there is no upper limit for inner current loop bandwidth ω_c in the ac–dc coupled droop-controlled system from the standpoint of linearized small-signal stability. However, this requires that the switching frequency is much higher than ω_c (typically set to one-tenth of the switching frequency) to prevent switching harmonics to be amplified by the controller.

2) Effect of Droop Gain: For the steady-state performance of the ac–dc coupled droop controller, decreasing droop gain will assure the existence of the equilibrium point and reduce the dc voltage deviation, as shown in Fig. 8. While for dynamic performance, from the perspective of linear control theory, the inverse of the droop gain can be regarded as the proportional gain of the dc voltage controller. Decreasing droop gain increases the open-loop gain $K_{\rm vdc}$ in the transfer function $T_{\rm vdc}$ of dc voltage in (14), which may reduce the settling time, reduce the system damping, and even lead to instability. This phenomenon will be verified with the experiment, as shown in Figs. 25 and 26.

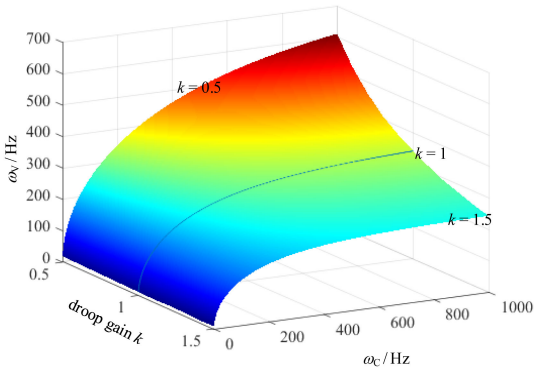

Fig. 15. Bandwidth of voltage loop with variable ω_c under different droop gains.

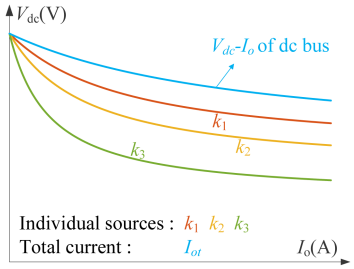

Fig. 16. Droop characteristic of paralleled sources.

The source and load impedance interactions are presented with different droop gains in Fig. 14(a), where the solid lines represent the source impedance (Z_S) and the dashed lines represent the load impedance (Z_L). The amplitude of source impedance in low-frequency range increases gradually as k increases. Meanwhile, the dc bus voltage decreases, and thus the input impedance amplitude of the CPL also decreases. On the other hand, when k becomes smaller, the resonance peak of the source impedance in middle-frequency range will rise obviously, and the stability margin of the system will decrease due to the intersection of the Z_L and Z_S at the resonance peak.

Following the discussion in Section II-B, due to the presence of the RHPZ in the voltage control loop, a high proportional gain (inverse of droop gain, 1/k) will push the non-minimum phase system to instability. The reason for this instability is that some eigenvalues of the system move to the RHP (toward the RHPZ) if the proportional gain of the open-loop transfer function keeps increasing. Fig. 14(b) shows the eigenvalue contour with respect to the proportional gain (1/k), demonstrating that the system is unstable when 1/k is larger than 4.92, correspondingly, k is smaller than 0.20. The corresponding oscillation frequency can be observed in both Fig. 14(a) and the experimental verification in Fig. 26.

3) Investigation Into the DC Voltage Loop Bandwidth: Although there is not an explicit dc voltage controller in the ac–dc coupled droop control, dynamic of the dc voltage can be linearized as (14), from which bandwidth of the voltage loop ω_v can be derived as

$$\left| K_{\mathrm{vdc}} \frac{(1 - j\frac{\omega_v}{\omega_{z0}})}{(1 - j\frac{\omega_v}{\omega_{p0}})(1 + j\frac{\omega_v}{\omega_c})} \right| = 1. \tag{24}$$

Here, the cutoff frequency of the open loop transfer function T_{vdc} is chosen as an indicator of the voltage loop bandwidth, namely ω_v. In Fig. 15, the relationship between ω_v and inner loop bandwidth ω_c is depicted with different droop gains. It can be inferred that there is an upper limit of ω_v for each droop gain, which can be derived as

$$\lim_{\omega_c \to \infty} \omega_v = \sqrt{\frac{{K_{\mathrm{vdc}}}^2 - 1}{\frac{1}{\omega_{p0}^2} - \frac{{K_{\mathrm{vdc}}}^2}{\omega_{z0}^2}}}. \tag{25}$$

That is to say, dc loop bandwidth will not increase likewise as ω_c increases although there is no explicit dc outer loop controller constraining the outer loop bandwidth. The upper limit of ω_v decreases as the droop gain increases. From the point of impedance modeling, the source impedance will keep unchanged when ω_v is approaching the limit, which is a typical feature of the proposed droop method as can be seen from Fig. 13, where the source impedance is almost unchanged when ω_c is higher than 500 Hz.

As a short summary for the parametric analysis, bandwidth of the inner current loop ω_c has a lower limit, due to the stability of the dc voltage shown in (15). Droop gain k is constrained by both an upper and a lower limit. The upper limit is mainly determined by the existence of the equilibrium point and specified voltage deviation, whereas the lower limit is associated with RHPZ of nonminimum phase property. There is an inherent theoretical upper limit of the dc voltage loop bandwidth, which is influenced by the droop gain.

IV. Generalized Multisource MG Operation

In the dc MG shown in Fig. 1, multiple VSCs provide electrical power to feed the common dc bus. This section will investigate the generalized multisource system in terms of steady-state and stability performance.

A. Global Droop Gain at DC Bus

Under the ac–dc coupled droop control, the dc bus voltage V_b can be expressed as

$$V_b = V_0 - k_i I_{di} - r_i I_{oi} = V_0 - (\mu_i k_i + r_i) I_{oi} \tag{26}$$

where r_i is the cable resistance of source i, μ_i is defined as the ratio between i_{di} and i_{oi} ($i = 1, 2, \ldots, n$), i.e., $\mu_i = i_{di}/i_{oi}$.

Assuming $e_d >> I_d R_s$ and e_d is the same for different sources, V_d can be regarded as the same for different sources according to (16). Thus, μ_i is approximately equal for different sources ($i = 1, 2, \ldots, n$), which is called μ in (28). Thus, a global droop gain k_t can be defined to describe the *V–I* characteristic of the dc bus under the ac–dc coupled droop control, as shown in the following equation:

$$I_o = \sum_{i=1}^{n} I_{oi} = \frac{1}{k_t} (V_0 - V_b) \tag{27}$$

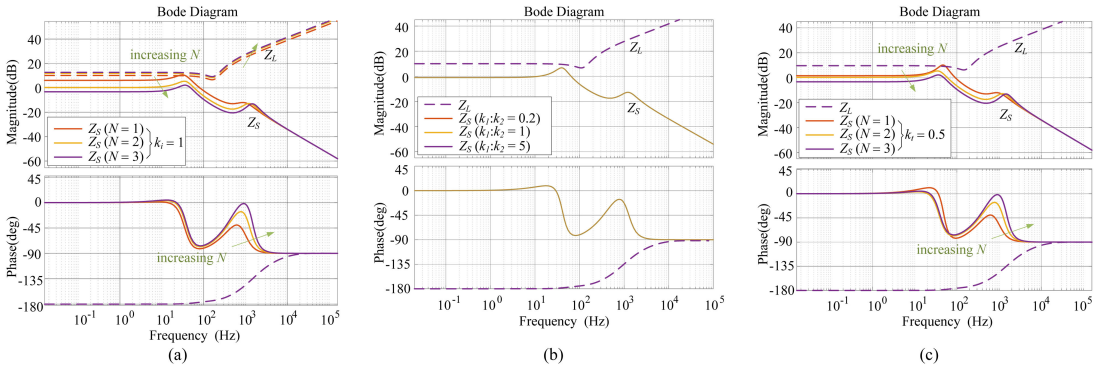

Fig. 17. Source impedance in multisource cases. (a) Effect of a number of parallel sources with same individual droop gain k_i. (b) Effect of load sharing ratio. (c) Effect of a number of parallel sources with same global droop gain k_t.

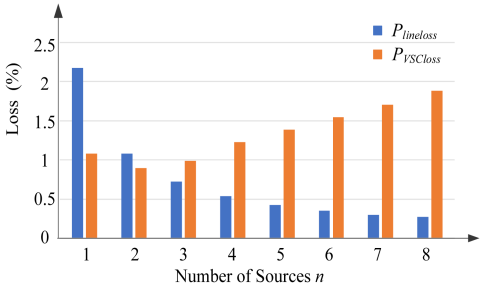

Fig. 18. Power losses versus the number of sources. .

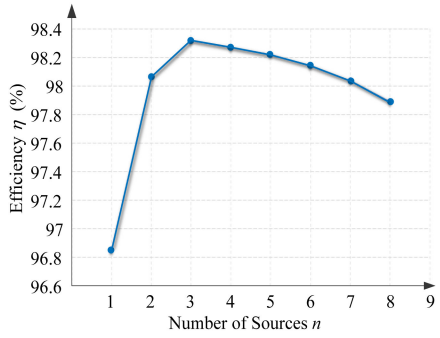

Fig. 19. Efficiency versus the number of sources.

where the global droop gain can be expressed as

$$\begin{cases} \mu_i = \frac{i_{di}}{i_{oi}} \\ k_t = \frac{1}{\sum_{i=1}^{n} \frac{1}{\mu_i k_i + r_i}} \approx \frac{\mu}{\sum_{i=1}^{n} \frac{1}{k_i}} \end{cases}. \tag{28}$$

Here, the droop gain is assumed to be much larger than the cable resistance ($k_i >> r_i$). At the same time, the current sharing ratio among sources can be obtained as

$$I_{o1} : I_{o2} : \cdots : I_{on} = \frac{V_{d1}}{k_1} : \frac{V_{d2}}{k_2} : \cdots : \frac{V_{dn}}{k_n} \approx \frac{1}{k_1} : \frac{1}{k_2} : \cdots : \frac{1}{k_n}. \tag{29}$$

It can be inferred from (27) that the dc bus voltage can be determined by the global droop gain k_t and total load current I_o.

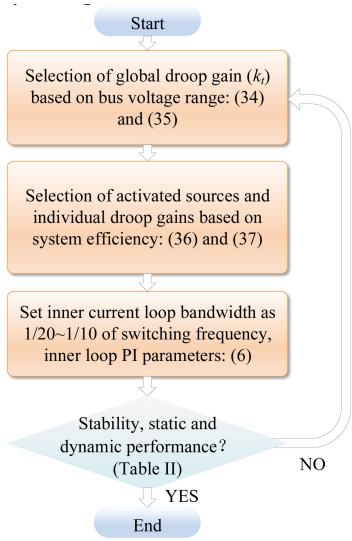

Fig. 20. Design a flowchart of the ac–dc coupled droop controller.

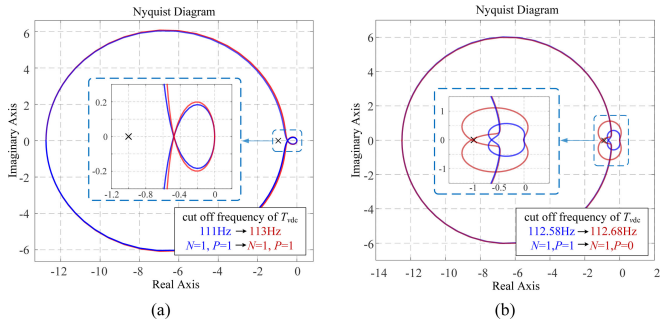

Fig. 21. Nyquist diagrams of a dc voltage transfer function with different T_{vdc} cutoff frequencies, where the system is stable when $P = N$. P stands for the number of poles of T_{vdc} in RHP of s plane, and N stands for the number of encirclements of the critical point $(-1+j0)$ in the counterclockwise direction. (a) AC–DC coupled droop in this article. (b) *I–V* droop.

The bus voltage can be invariant as long as the individual droop gains yield the same k_t, and different sources can be designed separately as shown in Fig. 16. The dc bus *V–I* characteristic is also a droop curve, which is stiffer than the individual droop

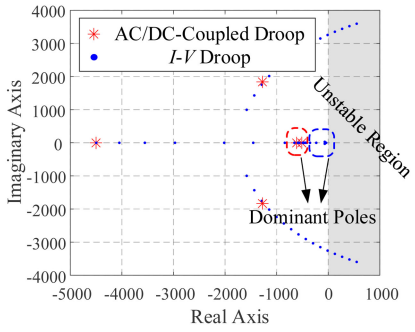

Fig. 22. Eigenvalue contours of a ac–dc coupled droop-controlled system and the traditional *I–V* droop-controlled system with the same steady-state performance. The bandwidth of $I_{\rm dc}$ loop in *I–V* droop-control increases from 10 to 100 Hz. Both used the same 1-kHz inner current loop.

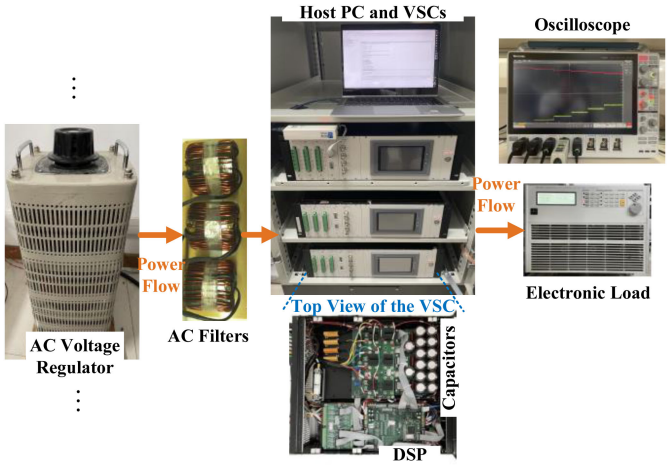

Fig. 23. Schematic diagram of the experimental setup.

curve of k_1, k_2, and k_3. With a larger number of paralleled sources, the dc bus voltage deviation will be reduced at the same load condition.

B. Impedance Modeling and Stability Analysis

Extending the derivation of Section III-B to a multisource system as shown in Fig. 1, the overall source impedance can be derived as

$$Z_{S\_t} = \frac{1}{\sum_{i=1}^{N} \frac{1}{(L_i s + R_i + \frac{1}{sC_i + \frac{G_{\rm VSC}}{k_i}})} + C_b s}. \tag{30}$$

There are different kinds of loads in a dc MG, such as CPLs and constant impedance loads. The total power is supplied by the dc bus, and the proposed droop control is applied for power distribution among the sources. Among various loads, CPL is the leading cause of dc voltage oscillations [20], [30]. Therefore, the stability of the system containing a CPL is mainly studied in the article. It is worth noticing that the proposed method can be also extended for non-CPLs.

Fig. 17(a) shows the Bode diagram of the source/load impedance with the different number of sources, adopting the

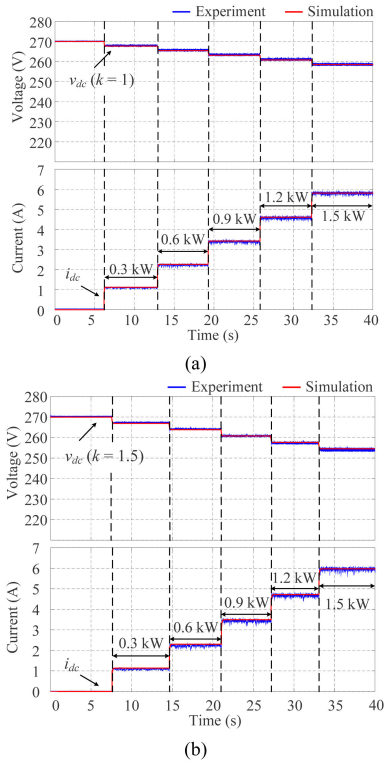

Fig. 24. Experimental and simulation results of steady-state performance with different droop gains. (a) Droop gain $k = 1$. (b) Droop gain $k = 1.5$.

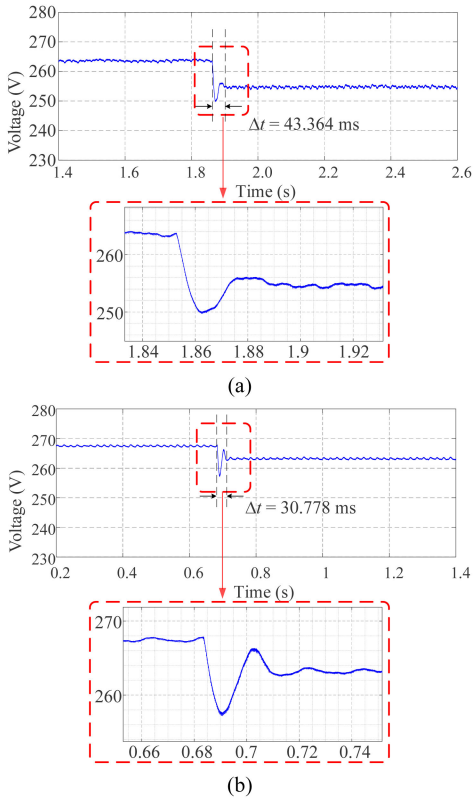

Fig. 25. Bus voltage dynamics in the ac–dc coupled droop-controlled system when subjected to a load power step from 0.5 to 1 kW. (a) $k = 2$. (b) $k = 1$.

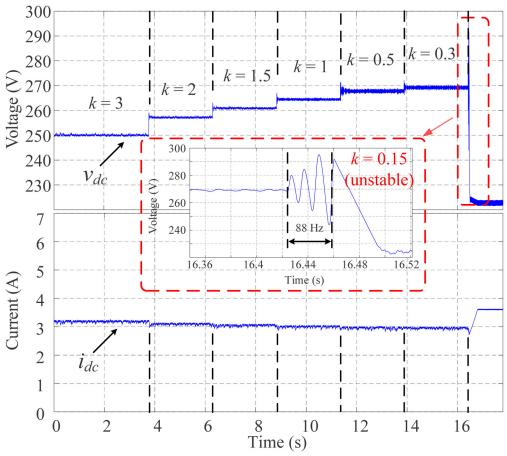

Fig. 26. Experimental results with decreased droop gain (0.8-kW CPL).

same individual droop gain (k_i) for each source. As one can see, the source impedance magnitude is reduced with an increasing number of sources. The load impedance magnitude increases because the global droop gain decreases with more sources (same k_i), yielding higher dc bus voltage, as indicated from (23).

The load current sharing ratio can be adjusted by tuning the individual droop gains as in (29). While two parallel sources operate in parallel and keep the same global droop gain (k_t), the output impedance is shown in Fig. 17(b) under different load sharing ratios. As one can see, the source impedance magnitude is almost unchanged with different current sharing ratios.

By setting the same global droop gain, the dc bus voltage in a multisource system will keep invariant with the increased number of sources. The output impedance of the multisource subsystem under same global droop gain (k_t) is shown in Fig. 17(c), where N stands for the number of sources. As can be seen in Fig. 17(c), the magnitude of the output impedance reduces, indicating that the stability margin is increased with the increased number of paralleled sources under same global droop gain. In summary, following conclusions can be drawn with the generalized multisource MG operation.

1) The dc bus *V–I* characteristic is a droop curve, which is stiffer than the individual droop curves of different sources. With a larger number of paralleled sources, the dc bus voltage deviation will be reduced at the same load condition, indicating a smaller global droop gain. Meanwhile, the system stability margin is increased.
2) With the identical global droop gain, the source impedance is almost unchanged with different load sharing ratios, with the same circuit parameters for the parallel sources.
3) With an increased number of paralleled sources while maintaining the identical global droop gain, the MG shows a higher stability margin than the single-source system under the proposed droop control method.

C. Design Procedure for the DC MG

With an increased number of sources, system stability can be improved from the above analysis, while power losses (including converter losses and line losses) might be increasing in a dc MG. Assuming a single source can provide enough power to feed the load, it is worthwhile investigating the optimization of the overall system efficiency. The design procedure of the multisource MG under ac–dc coupled droop control is illustrated in this section.

1) Selection of Droop Gains: The first step is to select the droop gains in the dc MG, based on the load situation (P_L) and the allowable voltage deviation at the dc bus (steady-state performance), e.g., [250 V, 280 V] in the standard MIL-STD-704F for the 270-V onboard aircraft dc system [31]. Therefore, $V_{\rm dc}$ can be expressed with an inequality relationship as $V_{\rm dc\_low} < V_{\rm dc} < V_{\rm dc\_high}$.

When a single source exists, substituting the inequality relationship with (19), the single droop gain can be derived as

$$\frac{6R_s\left(V_0-V_{\rm dc\_high}\right)}{3e_d-\sqrt{3}\sqrt{3e_d^2-8P_LR_s}}<k<\frac{6R_s\left(V_0-V_{\rm dc\_low}\right)}{3e_d-\sqrt{3}\sqrt{3e_d^2-8P_LR_s}}. \tag{31}$$

When multiple sources operate in parallel, according to (27), the global droop gain should satisfy

$$\frac{\left(V_0-V_{\rm dc\_high}\right)V_{\rm dc\_high}}{P_L}<k_t<\frac{\left(V_0-V_{\rm dc\_low}\right)V_{\rm dc\_low}}{P_L}. \tag{32}$$

The dc bus voltage depends on the global droop gain, whereas individual droop gains are defined by the MG designer or operator. Different individual droop gains can yield the same global droop gain according to (28). Assuming that n DGs work in parallel, and the load sharing ratio among DGs can be expressed as

$$\begin{cases} I_{o1}:I_{o2}:\cdots:I_{on}=\lambda_1:\lambda_2:\cdots:\lambda_n \\ \sum_i^n I_{oi}=I_{ot} \\ \sum_i^n \lambda_i=1. \end{cases} \tag{33}$$

Assuming different sources are distributed with similar distances from the dc bus, the dc MG can be designed as an optimization task to achieve high-efficiency operation at a steady state.

The optimization task to determine load sharing ratio (λ_i) and number of parallel sources (n) can be formulated as

$$\begin{cases} \max\left(\eta\right)=\max\left(\frac{P_L}{P_L+P_{\rm lineloss}+P_{\rm VSCloss}}\right) \\ P_{\rm VSCloss}=\sum_i^n\left[a(\lambda_iI_{ot})^2+b\left(\lambda_iI_{ot}\right)+c\right] \\ P_{\rm lineloss}=\sum_i^n\left(\lambda_iI_{ot}\right)^2R_i\approx {I_{ot}}^2R\sum_i^n{\lambda_i}^2 \end{cases} \tag{34}$$

where $P_{\rm VSCloss}$ represents the total losses of the source converters, based on a generalized converter loss estimation in [32], $P_{\rm lineloss}$ represents the total line losses connecting individual DGs and the dc bus, P_L is the total load power, and I_{ot} is the total source current at the dc bus.

By solving (34) together with (33), $P_{\rm lineloss}$ can be first minimized on the condition that each DG shares the equivalent load power with each other, i.e., $\lambda_1=\lambda_2=\cdots=\lambda_n=1/n$. Hence, the optimal droop gain for each DG is

$$k_{i\_\rm op}=\frac{nk_t}{\mu} \tag{35}$$

where n is the number of parallel sources, and μ_i is the ratio between i_d and i_o as defined in (28). Then, the optimization task

TABLE II
OPERATION CHARACTERISTICS ALLOWED FOR THE 270-V DC SYSTEM [31]

Specification	Limits
Steady state voltage	250 to 280 V
Ripple amplitude	6 V maximum
Voltage transient	330 V ~ , forbidden
	280 ~ 330V, 0.04 s ~ 0.02 s
	250 ~ 280 V, allowable
	200 ~ 250 V, 0.01 ~ 0.04 s
	~ 200 V, forbidden

can be simplified as

$$\begin{cases} \max(\eta) = \max\left(\frac{P_L}{P_L + P_{\text{lineloss}} + P_{\text{VSCloss}}}\right) \\ P_{\text{VSCloss}} = \sum_i^n \left[a\left(\frac{1}{n} I_{ot}\right)^2 + b\left(\frac{1}{n} I_{ot}\right) + c\right] \\ P_{\text{lineloss}} = {I_{ot}}^2 R \sum_i^n \left(\frac{1}{n}\right)^2. \end{cases} \tag{36}$$

It can be seen from Figs. 18 and 19 that, as the number of sources increases, the loss of VSCs increases generally (only decreases from 1 to 2), whereas the line loss decreases, and thus an optimal number of parallel sources can be selected considering the system efficiency at steady state ($n = 3$ in this case).

2) Selection of PI Parameters of Inner Current Loop: To achieve better dynamic response characteristics which can meet the requirements of the standard MIL-STD-704F in [31], bandwidth of the dc voltage loop ω_v can be increased by increasing the inner current loop bandwidth ω_c. Since higher ω_c will not lead to instability in the ac–dc coupled droop-controlled system as depicted in Section III-C, ω_c can be selected as 1/10–1/20 of the VSCs switching frequency to prevent switching harmonics. According to (6), corresponding PI parameters of the inner current loop are given as: $k_{pc} = \omega_c L_s$ and $k_{ic} = \omega_c R_s$. The design flowchart of the ac–dc coupled droop-controlled dc MG with multiple sources is shown in Fig. 20. The operation characteristics allowed in the 270-V dc system in [31] is summarized in Table II.

As a short summary, the above procedure provides a basic design example for the ac–dc coupled droop-controlled dc MG. With specific circuit parameters and system requirements, number of sources, global droop gain, and control parameters of individual sources can be designed properly with case-by-case optimization calculations.

D. Comparison With the Traditional Droop Method

Since there is an upper limit of ω_v as shown in Fig. 15, a comparative study is conducted to discuss the scope of ω_v. In [33], it turns out that the *I–V* droop dynamic is faster than the *V–I* droop controller, thus *I–V* droop is chosen as the opponent for comparison. Under the same circuit condition, increasing ω_v in both cases, T_{vdc} Nyquist diagrams change from the blue curve to the red curve, as shown in Fig. 21(a) and (b), respectively, for I_d–*V* droop and *I-V* droop. It can be inferred that the ac–dc coupled system can achieve a higher ω_v than the *I–V* system without losing system stability. Hence, the theoretical upper limit of ω_v is higher than that of traditional droop-controlled system, which should be high enough to meet the corresponding requirements of dynamic performance.

Eigenvalue contours of the ac–dc coupled droop-controlled system and traditional *I–V* droop-controlled system with the same steady state performance are shown in Fig. 22. It can be seen that dominant poles of the ac–dc coupled droop-controlled system are further from imaginary axis, than the *I–V* droop-controlled system, as bandwidth of the I_{dc} loop increases in the whole stable region.

The comparison between the two droop controls shows that the system with ac–dc coupled droop control will shorten the settling time compared with the traditional *I–V* droop system so that the dynamic response of the proposed control is faster. Collectively, a comparison of the proposed and traditional droop methods [17], [18] is listed in Table III.

V. EXPERIMENTAL VERIFICATION

To verify the feasibility of the proposed ac–dc coupled droop control strategy, an experimental prototype was built as shown in Fig. 23, and the corresponding parameters are listed in Table I.

A. Steady-State Performance

To verify the steady-state performance, a single-source single-load system is tested in the experiment. The bus voltage and current while increasing the power load from 0.3 to 1.5 kW are shown in Fig. 24(a) and (b) with droop gain of 1 and 1.5, respectively. It demonstrates that the measured dc voltage with respect to dc current agree with the simulation results and theoretical analysis (17)–(19) under varying load power. A larger droop gain will lead to a larger voltage deviation at dc bus under the same CPL as compared in Fig. 24(a) and (b).

Since the dc current loop is eliminated in the proposed droop method, the ac-side voltage disturbances will have an influence on the dc voltage. The steady-state value of v_{dc} is shown in (19), and the derivative of v_{dc} with respect to e_d can be derived as

$$\frac{\partial v_{\text{dc}}}{\partial e_d} = \frac{k}{2R_s}\left(\sqrt{\frac{3e_d^2}{3e_d^2 - 8P_L R_s}} - 1\right) > 0. \tag{37}$$

Therefore, an overvoltage at ac side will increase the dc voltage at the dc side. It is worth noting that the impact is relatively small since "${e_d}^2$" is much larger than "$P_L R_S$" in most cases (e.g., $100^2 >> 1000 \times 0.05$ in our case). The corresponding experimental results are summarized in Table IV. Under the ac voltage disturbance, the variation rate of dc voltage is 0.113% and 0.228% at 0.5 and 1 kW load power, respectively, which will also meet the design standards in Section IV-C.

As a comparison, the traditional droop methods have more complicated control loops and slower dynamic characteristics, whereas ours show a faster dynamic performance with a small voltage deviation when there are ac-side voltage disturbances. To address the voltage deviation problem, traditional secondary control methods can be used. The dynamic performance comparison is conducted in the next part.

TABLE III
COMPARISON OF THE PROPOSED AND TRADITIONAL DROOP METHODS

		Current Mode (*I–V* droop) [17][18]	**Voltage Mode (*V–I* droop)** [17][18]	**AC/DC-Coupled Droop**
Control Loops		Droop + dc current control + inner current control	Droop + dc voltage control + inner current control	Droop + inner current control
Droop Gain	Upper limit	Equilibrium point + source/load impedance interaction	Equilibrium point + source/load impedance interaction	Equilibrium point + source/load impedance interaction
	Lower limit	RHP zero (nonminimum phase property)	/	RHP zero (nonminimum phase property)
DC Control Loop Bandwidth	Upper limit	RHP zero (nonminimum phase property)	RHP zero (nonminimum phase property)	/
	Lower limit	Source/load impedance interaction	Source/load impedance interaction	/
Role of the Droop Controller		Essentially a proportional controller, influence both static and dynamic performance	a feedforward term in the control loop, only influence the static performance	Essentially a proportional controller, influence both static and dynamic performance
DC and AC Cascaded Control Loop		Yes	Yes	No
AC Inner Current Loop		Reduced to first order system, Not critical on dc voltage dynamic	Reduced to first order system, Not critical on dc voltage dynamic	Critical on dc voltage dynamic
Dominant factors of DC Voltage Dynamics		Droop gain, dc current loop bandwidth	DC voltage loop bandwidth	Droop gain, inner current loop bandwidth
DC Voltage Dynamic Performance		Medium (limited by the bandwidth of outer dc current loop)	Medium (limited by the bandwidth of outer dc voltage loop)	Fast
Stability	Droop gain	Upper and lower limit	Upper limit	Upper and lower limit
	DC control loop bandwidth	Upper and lower limit	Upper and lower limit	/

TABLE IV
IMPACT OF AC-SIDE DISTURBANCE ON THE DC VOLTAGE

Load power	AC side (line-to-line voltage)		
	Before disturbance	After disturbance	Rate of variation
0.5 kW	173 V	156 V	9.83 %
1 kW	173 V	156 V	9.83 %
Load power	DC bus voltage		
	Before disturbance	After disturbance	Rate of variation
0.5 kW	265.7 V	265.4 V	0.113 %
1 kW	263.0 V	262.4 V	0.228 %

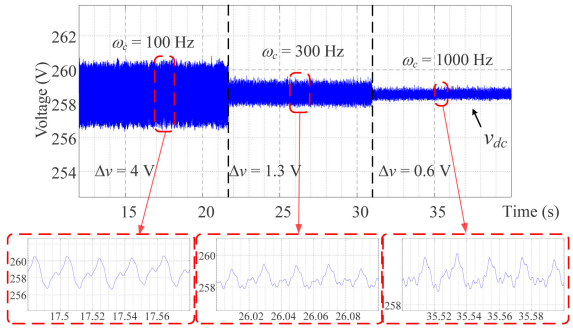

Fig. 27. Experimental results with increasing inner current control bandwidth (1-kW CPL).

B. Dynamic Performance

To verify the dynamic performance of the proposed ac–dc coupled droop control strategy, Fig. 25 shows the corresponding experimental result when the system is subjected to a load change from 0.5 to 1 kW. It can be seen that when the droop gain is set to 2 and 1, respectively, the corresponding transient time is 43.364 and 30.778 ms. It confirms the finding in Section III-C that the decreased droop gain will reduce the system settling time. The dc voltage control bandwidth is increased, as illustrated in Fig. 15.

C. Effect of Droop Gain and Inner Current Control Bandwidth on System Stability

Fig. 26 shows the effect of droop gain on system stability. Due to the nonminimum phase property of the system, oscillation and even instability can be observed when droop gain k is reduced to 0.15. The result matches the stability prediction in Fig. 14 (see Section III-C), where the RHP zero poses a challenge to the bus voltage stability under a small droop gain. The oscillation frequency (88 Hz) is basically consistent with the theoretical analysis (82 Hz) in Fig. 14(a).

Fig. 27 shows the experimental result under varying inner current loop bandwidth. It can be seen that increasing the inner current control bandwidth results in attenuation of the voltage ripples, which matches the discussion in Section III-C (as shown in Fig. 13).

D. Multisource Operation

The effect of the number of parallel sources on voltage stability is examined in Fig. 28. It can be seen in Fig. 26 that the single-source system becomes unstable when $k = 0.15$ under a CPL of 0.8 kW. However, with the same global droop gain and steady-state performance, stable operation of two-source and three-source system is achieved, as shown in Fig. 28(a) and (b), respectively. Again, the experimental results verify the discussion of multisource operation in Section IV-B and confirm that compared with single-source operation, multisource parallel

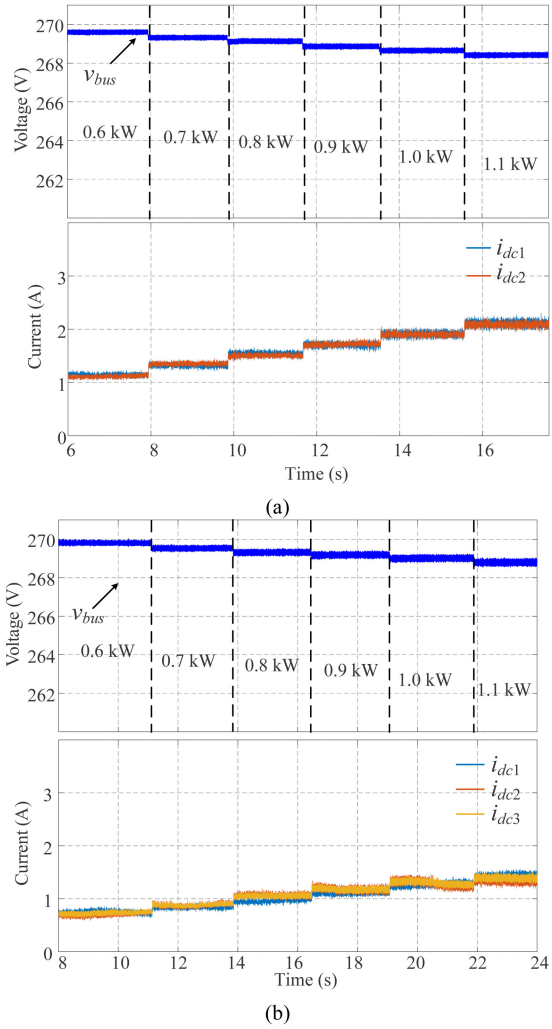

Fig. 28. Experimental results for parallel operation. (a) Two-source system with $k_1 = 0.3$ and $k_2 = 0.3$. (b) Three-source system with $k_1 = 0.45$, $k_2 = 0.45$, and $k_3 = 0.45$.

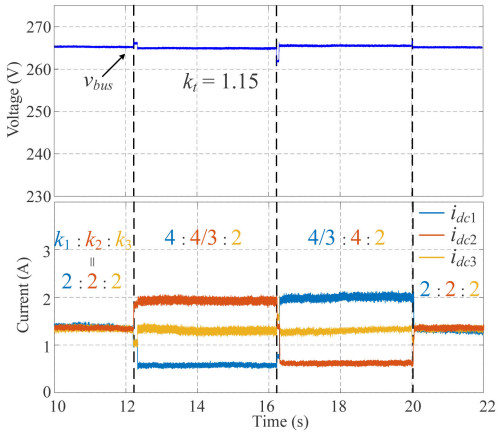

Fig. 29. Experimental results for parallel sources with identical global droop gain.

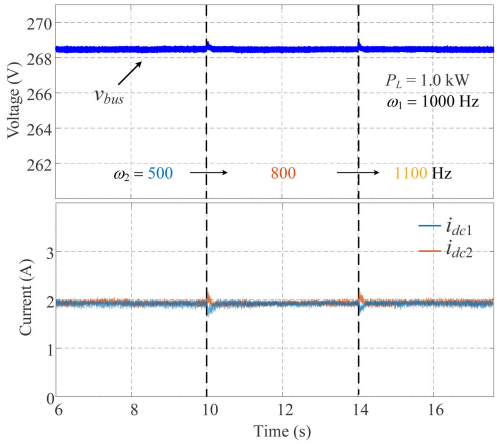

Fig. 30. Experimental results for parallel DGs with different inner current loop bandwidth.

operation can improve the system stability while keeping the same steady state performance.

Multisource operation with identical global droop gain has also been tested to validate the expected load sharing performance. In Fig. 29, the global droop gain k_t is fixed to 1.15 with a CPL of 1 kW, and the load sharing ratio among three sources are varied. The individual droop gains are set according to (35). As one can observe, the steady-state bus voltage is not affected by the step changes in the current sharing ratio, but the load currents provided by source 1, 2, and 3 vary according to the set ratio of individual droop gains (2:2:2, 4:1.33:2, 1.33:4:2, 2:2:2). As a short summary, here, the experimental results are consistent with the theoretical analysis in Section IV-A.

Experimental results of two parallel DGs with different inner current loop bandwidth are shown in Fig. 30, feeding a 1 kW CPL. One of the inner current loop bandwidths is 1 kHz, and the other varies from 500 and 800 Hz to 1100 Hz. Since the inner current loop bandwidth is set 1/10–1/20 of the switching frequency, it can be inferred from Fig. 13 that the output impedance

TABLE V
SPECIFIC PARAMETERS OF VSCS

Specification	Infineon IGBT FF225R12ME4	
Component	Switches	Diodes
Parameters	$V_{CES} = 1200$ V, $I_{Cnom} = 225$ A, $I_{CES} = 3$ mA, $t_{don} = 0.16$ µs, $t_{doff} = 0.38$ µs,	$V_{RRM} = 1200$ V, $I_F = 225$ A, $I^2t = 8100$ A^{2}s, $V_F = 2.1$ V

is almost unchanged when ω_c is higher than 500 Hz. It leads to the finding that the dc bus voltage was barely changed, which also verifies the effectiveness of the design process in Fig. 20.

The loss of the source subsystem is mainly divided into two parts: line losses P_{lineloss} and VSC losses P_{VSCloss}, where P_{lineloss} represents the total line losses connecting DGs and the dc bus; and the P_{VSCloss} represents the losses of source converters. Part parameters of VSCs used for the loss analysis are shown in Table V.

The loss analysis results of the dc MG under I_d–V droop control are shown in Fig. 31, whereas the load power is set as 1 kW. It can be seen that the line losses keep reducing with

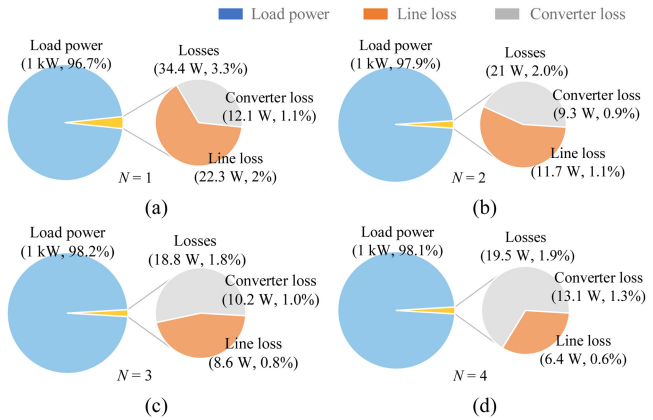

Fig. 31. Power losses analysis with different number (N) of source converters. (a) $N = 1$. (b) $N = 2$. (c) $N = 3$. (d) $N = 4$.

the increased number of DGs when the load power is invariant. Meanwhile, the VSC losses reduce to a certain threshold with increased number of parallel VSCs and then increase with the number of sources. Therefore, with the appropriately selected number of VSCs, parallel operation ($N = 3$ in the studied case) can effectively reduce the losses to some extent, which is consistent with the theoretical analysis in Section IV-C.

E. Comparison With Traditional Droop Method

The bus voltage dynamics of the I–V and $I_{\rm d}$–V droop-controlled systems are compared in Fig. 32. The experimental verification is performed under the same load conditions, same inner current loop bandwidth (1 kHz) and the droop gains are set to keep the dc bus voltage identical (from 263 to 261 V) in both cases, when the system is subjected to a load power step from 0.9 to 1.2 kW.

As shown in Fig. 32(a), as the bandwidth of the $I_{\rm dc}$ current loop increases from 50 to 80 Hz, the dynamic performance of the bus voltage under I–V droop control improves. The settling time is reduced from 0.89 to 0.6 s, but it remains inferior to the proposed I_d–V droop with 0.03 s. In Fig. 32(b), when the $I_{\rm dc}$ current loop increases to 110 Hz, the settling time of dc voltage under I–V droop control is reduced to 0.045 s, which is comparable to the I_d–V droop (0.03 s). However, the dc voltage is shifting toward an unstable state with large ripples (3.5 V in magnitude), as shown in the zoomed yellow curve in Fig. 32(b).

The second comparison is between V–I and I_d–V droop. Similar to the I–V droop-controlled system, there is also an RHPZ in V–I droop-controlled system, as illustrated in [17] and [18]. An overly large $V_{\rm dc}$ control bandwidth should be avoided. Otherwise, the eigenvalue of the closed-loop system will shift to the right half plane, leading to system instability.

The bus voltage dynamics are compared in Fig. 33. As shown in Fig. 33(a), as the bandwidth of the $V_{\rm dc}$ current loop increases from 40 to 60 Hz, the dynamic performance of the bus voltage under V–I droop control improves. The settling time is reduced

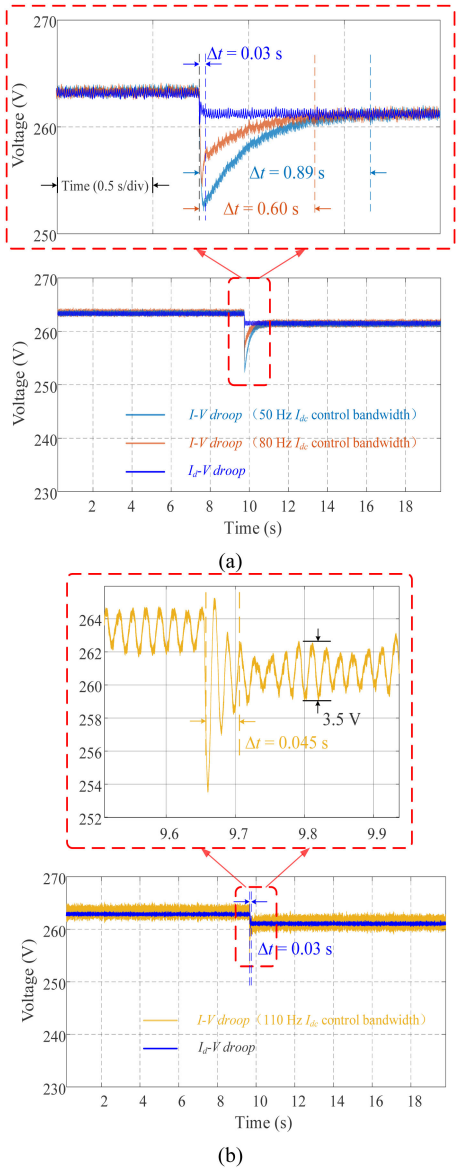

Fig. 32. Bus voltage dynamics comparison between I–V and I_d–V droop. (a) I_d–V droop and I–V droop with 50- and 80-Hz $I_{\rm dc}$ control bandwidth. (b) I_d–V droop and I–V droop with 110 Hz $I_{\rm dc}$ control bandwidth.

from 1.65 to 1.49 s, but it remains inferior to the proposed I_d–V droop with 0.03 s.

In Fig. 33(b), when the $V_{\rm dc}$ current loop increases to 80 Hz, the settling time of dc voltage under V–I droop control is reduced to 0.07 s. However, the dc voltage is shifting toward an unstable state with large ripples (4 V in magnitude), as shown in the zoomed yellow curve in Fig. 33(b).

In summary, the dynamic performance of the dc bus voltage can be improved by increasing the $I_{\rm dc}/V_{\rm dc}$ control bandwidth in I–V/V–I droop-controlled system. However, its dynamic performance is still not as fast as I_d–V droop-controlled system until the $I_{\rm dc}/V_{\rm dc}$ bandwidth increases to the critical point at which the system is becoming unstable, which is consistent with the theoretical analysis in Section IV-D.

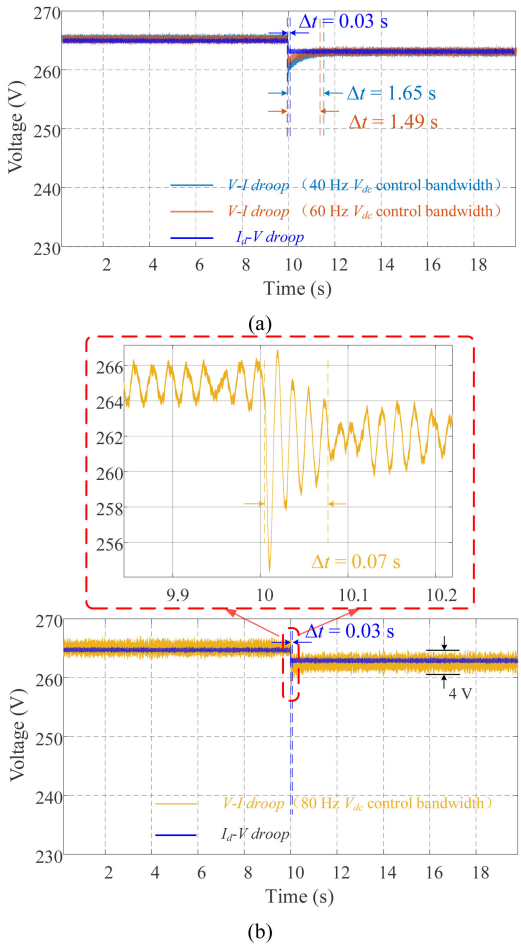

Fig. 33. Bus voltage dynamics comparison between V–I and I_d–V droop. (a) I_d–V droop and V–I droop with 40 and 60-Hz $V_{\rm dc}$ control bandwidth. (b) I_d–V droop and V–I droop with 80-Hz $V_{\rm dc}$ control bandwidth.

VI. Conclusion

This article has presented an ac–dc coupled droop control strategy, which could simplify the control structure and improve the control dynamics of the dc MG. A mathematical model of the proposed droop-controlled dc system has been developed. The equivalent source/load impedance has been derived when taking into account the converter dynamics in a single-source single-load system, and then extended to a generalized system consisting of multiple sources and loads. The main findings of this article can be highlighted as follows.

1) An ac–dc coupled droop controller is proposed with an improved transient performance of the dc MG. Based on the proposed method, the "black box" (dual-PI-ruled converter) is opened up and ac current control of VSC is directly linked to the load sharing performance among DGs, which provides a new way of primary control in dc MG.
2) Under the ac–dc coupled droop control, dc voltage dynamics are affected by the inner current control bandwidth and the droop gain. Increased inner current control bandwidth and decreased droop gain can improve the system dynamics.
3) To ensure the system stability, the lower limit of the inner current bandwidth is constrained due to the interaction of source/load impedance, and the upper limit of the inner current loop is constrained by the switching frequency. The upper limit of the droop gain is obtained from the existence of the equilibrium point, and the lower limit of the droop gain is constrained due to the RHP zero of the source impedance.
4) Parallel sources can improve the system stability while maintaining the identical global droop gain (identical bus V–I characteristic). Detailed design procedure of the multisource dc MG is presented taking into account the efficiency, control dynamics and stability. Given the voltage and power requirements, the selection of global and individual droop gains is presented to assure system stability, appropriate power sharing performance and dc bus voltage dynamics.

Appendix

A. DC Current Modeling

The detailed parameters of transfer function $G_{\rm VSC}(s)$ in Section II-B.2 is shown as

$$\begin{cases} \omega_{z0} = \frac{v_{d0}-R_s i_{d0}}{L_s i_{d0}} \\ K_{\rm VSC} = \frac{3(v_{d0}-R_s i_{d0})}{2v_{\rm dc0}}. \end{cases} \tag{38}$$

Substituting (38) with the equilibrium point, ω_{z0} and K_{in} can be rewritten as

$$\begin{cases} \omega_{z0} = \frac{2R_s\sqrt{3e_d^2-8P_LR_s}}{L_s\left(\sqrt{3}e_d-\sqrt{3e_d^2-8P_LR_s}\right)} \\ K_{VSC} = \frac{3\sqrt{3}R_s\sqrt{3e_d^2-8P_LR_s}}{-3ke_d+\sqrt{3}k\sqrt{3e_d^2-8P_LR_s}+6R_sv_0} \end{cases} \tag{39}$$

where $K_{\rm VSC}$ is the dc gain of $G_{\rm VSC}(s)$, and ω_{z0} is the frequency corresponding to the RHPZ.

B. DC Voltage Modeling

The detailed parameters of transfer function $T_{\rm vdc}(s)$ in Section II-B3 is shown as

$$\begin{cases} K_{\rm vdc} = \frac{-3v_{\rm dc0}(v_{d0}-R_s i_{d0})}{2kP_L} \\ \omega_{z1} = \frac{v_{d0}-R_s i_{d0}}{L_s i_{d0}} \\ \omega_{p1} = \frac{P_L}{Cv_{\rm dc0}^2}. \end{cases} \tag{40}$$

Substituting (40) with equilibrium point, $K_{\rm vdc}$, ω_{z0}, and ω_{p0} can be written as

$$\begin{cases} K_{\rm vdc} = \frac{-3ke_d^2+8kP_LR_s+\sqrt{3}ke_d\sqrt{3e_d^2-8P_LR_s}}{4kP_LR_s} \\ \quad -\frac{\sqrt{3}R_s\sqrt{3e_d^2-8P_LR_s}v_0}{2kP_LR_s} \\ \omega_{z1} = \frac{2R_s\sqrt{9e_d^2-24P_LR_s}}{L_s\left(3e_d-\sqrt{9e_d^2-24P_LR_s}\right)} \\ \omega_{p1} = \frac{36P_LR_s^2}{C\left(-3ke_d+k\sqrt{9e_d^2-24P_LR_s}+6R_sv_0\right)^2}. \end{cases} \tag{41}$$

The overall closed-loop transfer function of $v_{\rm dc}$ can be expressed as

$$\frac{\Delta v_{\rm dc}}{\Delta v_o} = \frac{G_{\rm VSC}(s)}{G_{\rm VSC}(s)+k(sC-\frac{P_L}{v_{\rm dc0}^2})} = \frac{(v_{d0}-R_s i_{d0})-sL_s i_{d0}}{\rm den} \tag{42}$$

where

$$\begin{aligned}{\rm den} = {} & \frac{2}{3}\frac{v_{\rm dc0}kCs^2}{\omega_c} + \left[\frac{2}{3}v_{\rm dc0}\left(kC-\frac{kP_L}{\omega_c v_{\rm dc0}^2}\right) - L_s i_{d0}\right]s \\ & + \left[(v_{d0}-R_s i_{d0}) - \frac{2kP_L}{3v_{\rm dc0}}\right]. \end{aligned} \tag{43}$$

C. Source Impedance Expression

The detailed source impedance (22) in Section III-B is expressed as

$$\begin{aligned} Z_S(s) &= \frac{1}{sC_b}//(R_i + sL_i + \frac{k}{ksC_i + G_{\rm VSC}}) \\ &= \frac{k(L_iC_is^2+R_iC_is+1)+G_{VSC}(L_is+R_i)}{ks(L_iC_iC_bs^2+R_iC_iC_bs+C_i+C_b)+G_{VSC}(L_iC_bs^2+R_iC_bs+1)}. \end{aligned} \tag{44}$$

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