A Novel Bidirectional Five-Level Multimode *CLLC* Resonant Converter

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***Abstract*—In order to widen voltage gain of bidirectional on-board charger to meet requirements of electric vehicle with different voltage levels, a novel bidirectional five-level multimode *CLLC* resonant converter is proposed by combining the *CLLC* resonant tank module (RTM) with the five-level cascaded neutral-point clamp active bridge which is composed of two three-level neutral-point clamp (3L-NPC) bridge arms. Furthermore, the converter can, respectively, establish three voltage gain modes of high, medium, and low to effectively widen voltage gain adjustment capabilities through the fixed-frequency plus phase-shift hybrid modulation independently adopted in each 3L-NPC bridge arm, while soft-switching is realized by phase control between resonant current and input voltage of RTM. Meanwhile, the key parameters of RTM would be symmetrically designed to make bidirectional power transmission characteristics, which become consistent based on soft-switching and monotonic voltage gain control. Finally, according to the simulation platform and experimental prototype, it can be shown that the practical voltage gain is close to the theoretical design gain and converter has good dynamic performances after realizing soft-switching in each mode.**

***Index Terms*—Bidirectional on-board charger (OBC), *CLLC* resonant tank module (RTM), five-level, voltage gain modes, widen voltage gain adjustment capabilities.**

NOMENCLATURE

3L-NPC	Three-level neutral-point clamp.
5L-CNPC	Five-level cascaded neutral-point clamp.
PFM	Pulse frequency modulation.
FF-PSHM	Fixed-frequency plus phase-shift hybrid modulation.
HFIT	High-frequency isolated transformer.
ZVS	Zero voltage switching-ON.
ZCS	Zero current switching-OFF.
λ	Inductance ratio.
f_s	Switching frequency.
f_{rp}	First resonant frequency.
U_{inp}	Input voltage.
U_{ins}	Output voltage.
i_{ins}	Output current.
RTM	Resonant tank module.
PMBA (SMBA)	Primary (secondary) main bridge arm.
PABA (SABA)	Primary (secondary) auxiliary bridge arm.
u_{mo}	PABA port ac voltage.
u_{ao}	PMBA port ac voltage.
u_{ab}	Input port ac voltage of RTM.
$u_{\text{ho}'}$	SABA port ac voltage.
$u_{\text{co}'}$	SMBA port ac voltage.
u_{cd}	Output port ac voltage of RTM.
k	Turns ratio.
L_m	Magnetizing inductance.
L_{rp} and L_{rs}	Resonant inductor.
C_{rp} and C_{rs}	Resonant capacitor.
R_L	Rated load resistance.
C_{oss}	Parasitic capacitances value.
HVGM	High-voltage gain mode.
MVGM	Medium-voltage gain mode.
LVGM	Low-voltage gain mode.
i_p	Resonant current.
i_m	*TX* exciting current.
i_s	RTM output current.
u_{Lm}	Exciting voltage of L_m.
α	Fixed minimum phase-shift angle.
β	Phase-shift angle variable in MVGM.
θ	Phase-shift angle variable in LVGM.
FHA	Fundamental harmonic analysis.
f_n	Normalized frequency.
R_{eq}	AC equivalent resistance.
Z_r	Characteristic impedance.
Q	Quality factor.
f_{n1}	Threshold normalized frequency of ZVS.
f_{rmp}	Second resonant frequency.

I. INTRODUCTION

With the development and popularization of the new energy industry represented by electric vehicles, higher performances are put forward to on-board charger (OBC) [1], [2]. In order to expand the function and application scenarios of OBC, the conventional one-way power transmission is changed to bidirectional power transmission [3]–[5]. In recent years, most of the bidirectional OBC use voltage source type dc–dc converters. The *LLC* resonant converter [6]–[8] is one of the popular topologies and gets more and more attention caused by realizing of ZVS of switches in wide load range and ZCS of

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rectifier diodes to make high operating efficiency, thus a variety of bidirectional converter topologies derived from *LLC* have been developed. Literature [9], [10] proposes a bidirectional *LLC* topology, but it is only a conventional full-bridge buck converter when working in backward which only can step-down regulation. Literature [11] proposes an asymmetrical bidirectional *CLLC* topology which achieved soft switching characteristics in two-way operation, but its forward and backward power control characteristics are different. Literature [12]–[14] proposes a symmetrical bidirectional full-bridge *CLLC* topology which not only has the same power control characteristics, but also maintains the soft switching characteristics in two-way operation.

Furthermore, the input and output voltage of OBC ports between various vehicles is extremely different due to the specific design standards [15]; therefore, OBC needs to have a wider voltage gain adjustment capabilities [16]. Generally, PFM is used to realize the voltage gain adjustment of *LLC* resonant converter [17], this variable frequency modulation requires the λ to be designed smaller which could keep a narrow f_s interval to extend the wider voltage gain adjustment capabilities, but it will make larger rms of resonant current increasing conduction and magnetic losses to reduce the converter operating efficiency. If λ to be designed larger which has to keep a wide f_s interval to extend the wider voltage gain adjustment capabilities, it will make the design difficulty to magnetic components and enhance the influence of EMI [18]. Especially in beyond-resonance mode (i.e., $f_s > f_{rp}$), the voltage gain adjustment performance of PFM will be greatly weakened [19]. In order to overcome the aforementioned drawback of PFM, literature [20], [21] proposes a fixed-frequency plus phase-shift hybrid modulation (FF-PSHM) which adjusts the voltage gain by phase shifting of the PWM duty cycle while f_s is fixed. Furthermore, based on the conventional three-level neutral-point clamp (3L-NPC) PWM converter, literature [22], [23] propose a type of three-level *LLC* resonant converter which not only retains soft-switching characteristics, but also make the voltage stress of switches reduced to be half of the input supply voltage. And, literature [24], [25] proposes the two-phase interleaved parallel *LLC*/*CLLC* resonant converter, the output ports of two *LLC* resonant modules is cascaded to improve the voltage gain through two HFITs. Literature [26], [27] proposes a unidirectional (bidirectional) three-level *LLC* resonant converter where the ac output ports of the 3L-NPC bridge arm and half bridge arm are cascaded, the dc input ports of these two bridge arms are paralleled, which can build a hybrid full bridge to generate three-level or five-level by a complicated pulsewidth and amplitude modulation control. Similarly, literature [28] makes ac output ports and dc input ports of two 3L-NPC bridge arms cascaded and paralleled, respectively, to generate five-level by modulation of five control degrees of freedom with hard switching. Literature [29] only has more flying capacitors than literature [28], and adopts different modulation methods, respectively, on two 3L-NPC bridge arms to generate three-level that makes parts of switches realize ZVS. Literature [30] introduces *CLLC* resonant network into literature [29] and adopts different combination of switching states of the active bridges to establish multimodes for improving wider voltage gain adjustment capabilities.

In conclusion, for development widen voltage gain of bidirectional OBC, a novel bidirectional five-level multimode *CLLC* resonant converter is proposed, which is composed of a *CLLC* resonant tank module (RTM) and two five-level cascaded neutral-point clamp (5L-CNPC) active bridges that are connected to input port and output port of the RTM. It cannot be more emphasized that the derivation of 5L-CNPC active bridge is inspired by the idea of the literature [24]–[30] which makes the dc input ports of two 3L-NPC bridge arms still paralleled but makes ac output ports cascaded by a coupling transformer to generate five-level that can flexibly adjust the input voltage of RTM to establish three voltage gain modes of high, medium, and low by different modulation combination of FF-PSHM independently adopted in each 3L-NPC bridge arm to effectively widen voltage gain adjustment capabilities, while soft-switching is realized by phase control between resonant current and input voltage of RTM. Meanwhile, the key parameters of RTM would be symmetrically designed to make bidirectional power transmission characteristics, which become consistent based on soft-switching and monotonic voltage gain control. As a result, compared to [26]–[30], the topology of proposed novel converter can avoid analysis and design of backward, optimize control to easily realize ZVS, and achieve self-sharing of current and voltage by special bridge arm cascade measure.

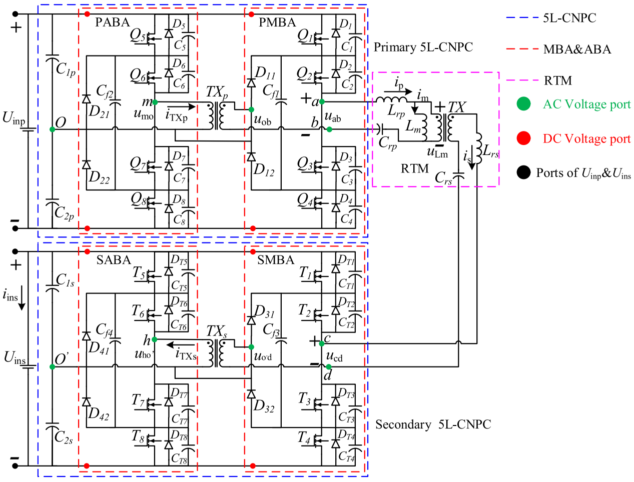


Fig. 1. Diagram of the topology structure.

The rest of this article is organized as follows. In Section II, topology of proposed novel converter and modulation strategies are described and analyzed. In Section III, an analysis and design about parameters of *CLLC* resonance tank under ZVS and monotonic voltage gain control is mainly presented. In Section IV, the simulation experiments are performed according to the given parameters. Section V gives the prototype experimental results. Finally, Section VI concludes this article.

II. ANALYSIS TO THE WORKING CHARACTERISTICS OF THE PROPOSED NOVEL CONVERTER

A. Topological Structure and Modulation Strategy of the Proposed Novel Converter

The proposed novel converter topology is shown in Fig. 1. It is composed of ports of U_{inp} and U_{ins} indicated by black points in Fig. 1, 5L-CNPC active bridges, and *CLLC* RTM. Particularly, the 5L-CNPC active bridge located on primary side

TABLE I
MODULATION METHODS TO EACH MODE

Working mode	PMBA	PABA
HVGM	PFM over $f_s<f_{rp}$	PFM over $f_s<f_{rp}$
MVGM	Fixed $f_s==f_{rp}$	FF-PSHM with $f_s==f_{rp}$
LVGM	FF-PSHM with $f_s==f_{rp}$	$u_{\mathrm{mo}}==0$

and secondary side of RTM has the same structure which is composed of two voltage-dividing capacitors C_{1p}, C_{2p} (C_{1s}, C_{2s}), two 3L-NPC bridge arms indicated as PMBA, PABA (SMBA and SABA) where the ac outputs indicated by green points, and dc inputs indicated by red points in Fig. 1 are cascaded by a coupling transformer TX_p (TX_s) with a fixed turns ratio 1 and paralleled, respectively. Q_1–Q_4 (T_1–T_4) are indicated as the switches of PMBA (SMBA), Q_5–Q_8 (T_5–T_8) are indicated as the switches of PABA (SABA), and D_1–D_8(D_{T1}–D_{T8}) are the body diodes with the parallel parasitic capacitances C_1–C_8 (C_{T1}–C_{T8}). Besides, D_{11}–D_{42} are the clamp diodes, C_{f1}–C_{f4} are the flying capacitors. And, the RTM is composed of an HFIT TX with k and L_m, L_{rp}, and L_{rs}, and C_{rp} and C_{rs}.

In primary 5L-CNPC, $u_{\mathrm{ab}} = u_{\mathrm{ao}} - u_{\mathrm{bo}} = u_{\mathrm{ao}} + u_{\mathrm{ob}}$, and due to the TX_p, $u_{\mathrm{mo}} = u_{\mathrm{ob}}$, thus $u_{\mathrm{ab}} = u_{\mathrm{ao}} + u_{\mathrm{mo}}$. Similarly, it can be derived that $u_{\mathrm{cd}} = u_{\mathrm{co'}} + u_{\mathrm{ho'}}$ in secondary 5L-CNPC. The voltage output control to u_{ao} and u_{mo} are irrelevant because PMBA/PABA can independently adopt FF-PSHM. Through different modulation combinations of PABA and PMBA, three voltage gain modes of high, medium, and low are established. The specific modulation methods to each mode are shown in Table I.

The following analysis is based on some principles as follows:

1) Power is transmitted from the RTM primary to the RTM secondary that make U_{ins} and i_{ins} be output voltage and current of converter.
2) In each mode, all switches of secondary 5L-CNPC are always turned OFF.
3) Switches and diodes are ideal devices that ON-resistance is 0, and the parasitic capacitances are all equal to C_{oss}.
4) TX_p and TX_s are regarded as ideal transformers, strictly guarding the law of turns ratio with the ignorance of excitation current.
5) U_{inp} and U_{ins} can be ideally shared by C_{1p}–C_{2s}.
6) There is no practical difference among C_{f1}–C_{f4}.

B. Operation Principles of MVGM

According to Table I, the specific driving and key waveforms of MVGM are shown in Fig. 2. Under $f_s == f_{rp}$, PMBA adopt a parameter α for realizing the ZVS of switches, and Q_1 and Q_4 are leading switches, and Q_2 and Q_3 are lagging switches. PABA performs FF-PSHM by adopting parameter β, and Q_5 and Q_8 are leading switches, and Q_6 and Q_7 are lagging switches. Each state of transient process in half-period based on Fig. 2 is analyzed as follows based on the whole key states of equivalent circuits that are plotted as shown in Fig. 3.

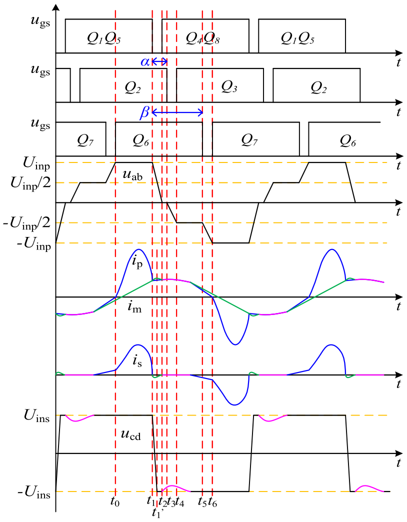


Fig. 2. Key waveforms of MVGM.

State I [t_0, t_1]: In Fig. 3(a), the i_p loop and the TX_p primary current i_{TXp} loop are identified by red mark of path in RTM and primary 5L-CNPC active bridge. These loops show that $i_{\mathrm{p}} = i_{\mathrm{TXp}}$ caused by TX_p and u_{ao} and u_{mo} are both clamped to $U_{\mathrm{inp}}/2$ by C_{1p} to make $u_{\mathrm{ab}} = U_{\mathrm{inp}}$. i_p will be sinusoidal changed and bigger than i_m caused by LC resonance generated from L_{rp} and C_{rp}. Thus, L_m will be clamped by reflection of u_{cd}. Meanwhile, $i_s = i_p - i_m$ that the loop is also identified by red mark of path in RTM and secondary 5L-CNPC active bridge as same as the TX_s primary current i_{TXs} loop. These loops also show that $i_s = i_{TXs}$ caused by TX_s, $i_{\mathrm{ins}} = i_s$, and u_{co} and u_{ho} are both clamped to $U_{\mathrm{ins}}/2$ by C_{1s} to make $u_{cd} = U_{\mathrm{ins}}$. Therefore, i_m will linearly rise. Besides, labels of current and voltage that exists in the loops are identified by green mark, and labels of ports and components that exist in the loops are identified by blue mark.

State II [t_1, t_1']: In Fig. 3(b), at t_1, Q_1 and Q_5 are turned OFF. i_p immediately charges C_1 and discharges C_4 through C_{f1} to form the commutation of ZVS. Similarly, i_{TXp} immediately charges C_5 and discharges C_8 through C_{f2} to form the commutation of ZVS. When $i_p = i_m$, $i_s = i_p - i_m = 0$ that enable LLC resonance, at the same time, $i_s = 0$ will also enable an LCR resonance involved winding inductance of TX_s, C_{T1}–C_{T8} and R_L in secondary 5L-CNPC that can form the commutation of ZCS to D_{T1}–D_{T8} which produces a short period of reverse i_s to make $i_m = i_p + i_s/k$. When C_{T3}, C_{T4}, C_{T7}, and C_{T8} are completely charge, C_{T1}, C_{T2}, C_{T5}, and C_{T6} at t_1', D_{T3}, D_{T4}, D_{T7}, and D_{T8} are turned ON, D_{T1}, D_{T2}, D_{T5}, and D_{T6} realized ZCS. Then, u_{cd} is dropped from U_{ins} to $-U_{\mathrm{ins}}$ because that u_{co} and u_{ho} are clamped to $-U_{\mathrm{ins}}/2$ by C_{2s}.

State II [t_1', t_2]: In Fig. 3(c), at t_2, commutations are finished, voltages of C_4 and C_8 are dropped to 0 to turn ON D_8 and D_4 that makes u_{ao} and u_{mo} dropped from $U_{\mathrm{inp}}/2$ to 0, then $u_{ab} = 0$. And, due to end of LCR, $i_s = 0$ again to decouple TX. At last, i_{ins} will not sustained by i_s, but by C_{1s}, C_{2s}.

State III [t_2, t_3]: In Fig. 3(d), Q_8 and Q_4 are turned on at t_2 to realize ZVS. i_p wheels through Q_4, D_4, i_{TXp} wheels through Q_8, D_8. u_{ab} maintains 0 level. And, in LLC resonance, u_{cd} is affected by a sinusoidal fluctuation caused by reflection of u_{Lm}.

State IV [t_3, t_4]: In Fig. 3(e), at t_3, Q_2 is turned OFF. i_p charges C_2 through C_{f1} and discharges C_3 to form the commutation of ZVS. At t_4, commutation is finished, voltage of C_3 is dropped

(a) (b) (c) (d) (e) (f) (g)

Fig. 3. Key states of equivalent circuits to MVGM. (a) State I $[t_0, t_1]$. (b) State II $[t_1, t_1{}']$. (c) State II $[t_1{}', t_2]$. (d) State III $[t_2, t_3]$. (e) State IV $[t_3, t_4]$. (f) State V $[t_4, t_5]$, and (g) State VI $[t_5, t_6]$.

to 0 to turn on D_3 that makes u_{ao} dropped from 0 to $-U_{\mathrm{inp}}/2$, thus $u_{ab} = -U_{\mathrm{inp}}/2$ caused by $u_{mo} = 0$.

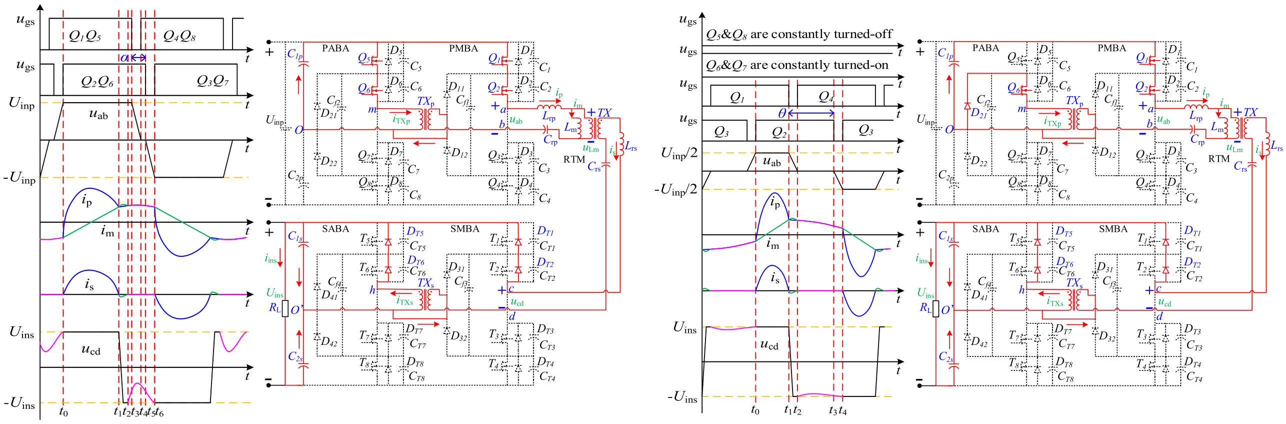
State V $[t_4, t_5]$: In Fig. 3(f), Q_3 is turned ON at t_4 to achieve ZVS. i_p wheels through Q_3, D_3, then, $i_p \neq i_m$ due to $u_{ab} = -U_{\mathrm{inp}}/2$, which disables *LLC* resonance and enables *LC* resonance. And i_s will be reversed to make an opposite transient process compared with $[t_0, t_1]$; therefore, it can be derived that $i_{\mathrm{ins}} = i_s$, but $u_{cd} = -U_{\mathrm{ins}}$.

State VI $[t_5, t_6]$: In Fig. 3(g), at t_5, Q_6 is turned OFF. i_{TXp} charges C_6 through C_{f2} and discharges C_7 to form the commutation of ZVS. At t_6, commutation is finished, voltage of C_7 is dropped to 0 to turn ON D_7 that makes u_{mo} dropped from 0 to $-U_{\mathrm{inp}}/2$, thus $u_{ab} = -U_{\mathrm{inp}}$ caused by $u_{ao} = -U_{\mathrm{inp}}/2$.

It is noted that state II is indicated as dead time t_{DTb} to PABA and PMBA leading switches, state IV is indicated as dead time t_{DTL1} to PMBA lagging switches, and state VI is indicated as dead time t_{DTL2} to PABA lagging switches. MVGM can generate five levels which are $U_{\mathrm{inp}}/2$, U_{inp}, 0, $-U_{\mathrm{inp}}/2$, and $-U_{\mathrm{inp}}$. The voltage stresses of switches in PABA and PMBA are all reduced to be half of the U_{inp}.

C. Operation Principles of HVGM and LVGM

According to Table I, in HVGM, the specific driving of PABA is the same as PMBAs to make $t_{\mathrm{DTL1}} = t_{\mathrm{DTL2}}$. In LVGM, Q_5 and Q_8 are constantly turned OFF, Q_6 and Q_7 are constantly



(a) (b)

Fig. 4. Key waveforms and state I [t_0, t_1] of equivalent circuits: (a) HVGM and (b) LVGM.

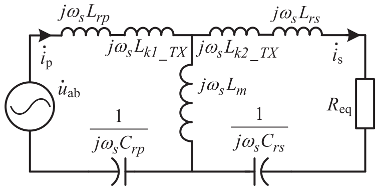


Fig. 5. AC equivalent operation circuit.

turned ON, that can short primary side of TX_p to make $u_{mo} = 0$, and PMBA performs FF-PSHM by adopting parameter θ. Then, the key waveforms and state I[t_0, t_1] of equivalent circuits to HVGM and LVGM are shown in Fig. 4.

State I [t_0, t_1] of Fig. 4 shows main current loop that is used for power transmission in HVGM and LVGM, and details in the rest of states could refer to states of MVGM. The key waveforms of Fig. 4 shows that the sinusoidal fluctuation of HVGM is significantly larger than MVGMs and LVGMs in *LLC* resonance because $|u_{ab}| = U_{\mathrm{inp}}$ in HVGM, while $|u_{ab}| = U_{\mathrm{inp}}/2$ in MVGM, $|u_{ab}| = 0$ in LVGM to make u_{Lm} of HVGM is bigger than u_{Lm} of MVGM and LVGM. Furthermore, comparing the key waveforms of each mode, the *LCR* resonance existed in state II can be ignored due to complicated process with extremely short time and small current. Therefore, the secondary 5L-CNPC active bridge can be completely equivalent to a full-bridge rectifier circuit that makes parameter analysis and design of the proposed novel converter approximately refer to the conventional full-bridge *CLLC* resonant converter.

III. PARAMETER ANALYSIS AND DESIGN OF THE PROPOSED NOVEL CONVERTER

A. Analysis to Converter Voltage Gain Characteristics

According to Sections II-B and II-C, when α is ignored, the FHA could also be applied in the analysis of voltage gain characteristics of HVGM, in which the corresponding ac equivalent operation circuit is constructed as shown in Fig. 5.

Where L_{k1_TX}, L_{k2_TX} are indicated as stray inductances of primary side and secondary side of *TX* that is generally equal to each other. Besides, to ensure that the parameters of RTM are symmetrical after secondary conversion of *TX*, there are

$$L_{rp} = k^2 L_{rs}, C_{rp} = \frac{C_{rs}}{k^2}. \tag{1}$$

The dc voltage gain M_h of HVGM can be expressed as

$$\begin{aligned} M_h &= \frac{U_{\mathrm{ins}}}{U_{\mathrm{inp}}} = \frac{U_{\mathrm{o.p}}\pi/4k}{U_{\mathrm{ab.p}}\pi/4} = \frac{|\dot{u}_{\mathrm{o}}|\pi/4k}{|\dot{u}_{\mathrm{ab}}|\pi/4} \\ &= \frac{1}{k\sqrt{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda f_n^2}\right)^2+\frac{Q^2}{\lambda^2}\left[(2\lambda+1)f_n-\frac{2\lambda+2}{f_n}+\frac{1}{f_n^3}\right]^2}} \end{aligned} \tag{2}$$

where $U_{ab.p}$ is the amplitude of the fundamental vector $\dot{u}_{ab}$ in u_{ab} square wave, and $U_{o.p}$ is the amplitude of the fundamental vector $\dot{u}_o$ in u_{cd} square wave. Besides, the key parameters f_n, λ, and Q are specifically expressed as

$$\begin{cases} f_n = \frac{f_s}{f_{rp}}; f_{rp} = \frac{1}{2\pi\sqrt{(L_{rp}+L_{k1\_TX})C_{rp}}}; \lambda = \frac{L_m}{L_{rp}+L_{k1\_TX}} \\ R_{\mathrm{eq}} = \frac{8k^2 R_{\mathrm{L}}}{\pi^2}; Z_r = \sqrt{\frac{L_{rp}+L_{k1\_TX}}{C_{rp}}}; Q = \frac{Z_r}{R_{\mathrm{eq}}}. \end{cases} \tag{3}$$

However, when β is introduced to MVGM with neglect of α and dead time, $U_{ab.p}$ will be changed from $4U_{\mathrm{inp}}/\pi$ to (3+cos(β)) U_{inp}/π which is substituted to (2) with $f_n = 1$. Then, dc voltage gain M_m is expressed as

$$M_m = \frac{U_{\mathrm{ins}}}{U_{\mathrm{inp}}} = \frac{3+\cos(\beta)}{4k}, 0 \le \beta \le \pi. \tag{4}$$

Similarly, $U_{ab.p}$ will be changed from (3+cos(β)) U_{inp}/π to (1+cos(θ)) U_{inp}/π in LVGM which is substituted to (2) with $f_n = 1$. Then, dc voltage gain M_L is expressed as

$$M_L = \frac{U_{\mathrm{ins}}}{U_{\mathrm{inp}}} = \frac{1+\cos(\theta)}{4k}, 0 \le \theta \le \pi. \tag{5}$$

According to (2), (4), and (5), the characteristic curve of voltage gain for each mode is plotted with $k = 1$, $\lambda = 4$, and different Q values, as shown in Fig. 6.

In Fig. 6, the left side to chain line $f_n = 1$ is HVGM area, a black solid line from point A to point B is MVGM area, and a cyan solid line from point B to point C is LVGM area. As Q value increased, adjustment range of M_h in HVGM area will be decreased. According to (4) and (5) and Fig. 6, under fixed $f_n = 1$, adjustment ranges of M_m and M_L are not affected by Q and λ but by β and θ. As β increased from 0 to π, M_m moves smoothly from point A ($M_m = 1$) to point B ($M_m = 0.5$). As θ increased

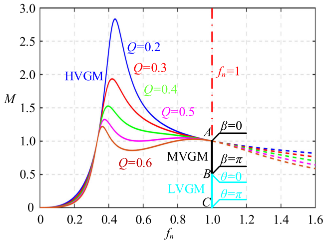


Fig. 6. Characteristic curve of voltage gain for each mode.

from 0 to π, M_L moves smoothly from point B ($M_L = 0.5$) to point C ($M_L = 0$). It means that the lower limit to adjustment range of voltage gain in the proposed novel converter can be zero.

As we know that full-bridge *CLLC* resonant converter has to work in beyond-resonance mode to make $M < 1$ as shown by colored dotted line where right side to chain line $f_n = 1$ and adopt PFM to control voltage gain so that, i_s is continuous to fail ZCS of rectifier diodes, and variation range of f_n has to be enlarged in order to satisfy wide voltage gain adjustment which leads to increased switching loss. However, compared with PFM, the FF-PSHM adopted in MVGM and LVGM adjust wide voltage gain with fixed $f_n = 1$ avoiding the extremely variation of f_n to reduce the design difficulty of magnetic components and the influence of EMI. Besides, body diodes of secondary 5L-CNPC active bridge can all realize ZCS by *LCR* resonance in each mode, even if HVGM adopt PFM, which is different from full-bridge *CLLC* resonant converter that realize ZCS of rectifier diodes by *LLC* resonance.

B. Parameter Design of RTM to Each Mode

In HVGM, it has to make body diodes turned ON to wheel current before turning ON the switches to realize ZVS, which means that the phase of vector $\dot{i}_p$ to i_p must lag behind the phase of $\dot{u}_{ab}$. And, input impedance Z_{in} of the RTM can be calculated to determine the phase relationship between $\dot{i}_p$ and $\dot{u}_{ab}$. According to FHA, Z_{in} can be derived as

$$Z_{\text{in}} = j\omega_s \left(L_{rp} + L_{k1\_TX}\right) + \frac{1}{j\omega_s C_{rp}} + j\omega_s L_m // \left(j\omega_s \left(L_{rs} + L_{k2\_TX}\right) + \frac{1}{j\omega_s C_{rs}}\right) = |Z_{\text{in}}| \angle\varphi \tag{6}$$

where ω_s is the switching angular frequency equaled to $2\pi f_s$, and φ can be simplified by substituting (1) and (3) to (6)

$$\varphi = \arctan\left(\frac{Q\left(1 - f_n^2\right)\left[\left(2\lambda + 1\right) f_n^2 - 1\right]}{f_n\left[\left(\lambda + 1\right) f_n^2 - 1\right]}\right) + \arctan\left(\frac{f_n}{Q\left[\left(\lambda + 1\right) f_n^2 - 1\right]}\right). \tag{7}$$

Assuming that the initial phase of $\dot{u}_{ab}$ is 0, since $\dot{i}_p = \dot{u}_{ab} / Z_{\text{in}}$, the initial phase of $\dot{i}_p$ is $-\varphi$ which could be less than 0 to make phase of $\dot{i}_p$ lag behind phase of $\dot{u}_{ab}$, then, it can be derived as

$$\frac{Q^2\left(1 - f_n^2\right)\left[\left(2\lambda + 1\right) f_n^2 - 1\right] + f_n^2}{f_n Q\left[\left(\lambda + 1\right) f_n^2 - 1\right]} > 0. \tag{8}$$

Assign

$$Q_{\min} = \frac{f_n}{\sqrt{\left(1 - f_n^2\right)\left[\left(2\lambda + 1\right) f_n^2 - 1\right]}}. \tag{9}$$

When $Q > Q_{\min}$, it can be derived as

$$\frac{Q^2\left(1 - f_n^2\right)\left[\left(2\lambda + 1\right) f_n^2 - 1\right] + f_n^2}{f_n Q\left[\left(\lambda + 1\right) f_n^2 - 1\right]} > \frac{2 f_n}{Q_{\min}\left[\left(\lambda + 1\right) f_n^2 - 1\right]}. \tag{10}$$

Assign

$$f\left(f_n, \lambda, Q_{\min}\right) = \frac{2 f_n}{Q_{\min}\left[\left(\lambda + 1\right) f_n^2 - 1\right]}. \tag{11}$$

Assign

$$f_{n1} = \frac{1}{\sqrt{\lambda + 1}} = \frac{f_{rmp}}{f_{rp}}; f_{rmp} = \frac{1/2\pi}{\sqrt{\left(L_{rp} + L_{k1\_TX} + L_m\right) C_{rp}}}. \tag{12}$$

According to (10), when $f_n > f_{n1}$, the $Q_{\min}$ and $f(f_n, \lambda, Q_{\min})$ are both always greater than 0 to make (8) always established. Furthermore, in order to avoid wider f_n interval to adjust voltage gain and be convenient for PFM, a requirement to parameters design proposed in the article is $M_h > M_{h\_\max} = 1.3$ over $f_n \in [0.6, 1]$ with continuous monotone decreasing under $k = 1$. Then, it can be inferred that $f_n \geq f_{n\_\min} = 0.6 > f_{n1}$ which makes $\lambda > 1.78$ based on (12), and the influence law of Q and λ to make continuous monotone decreasing of M_h can be found by M_h' which is derivative to M_h and can be derived as (13) based on (2)

$$M_h' = \frac{\mathrm{d} M_h}{\mathrm{d} f_n} = -\frac{\text{NUM}}{\text{DEN}} \tag{13}$$

where

$$\text{NUM} = \frac{4}{\lambda f_n^3}\left(\frac{1}{\lambda} - \frac{1}{\lambda f_n^2} + 1\right) + \frac{2Q^2}{\lambda^2} \left[\frac{1}{f_n^3} - \frac{2\left(\lambda + 1\right)}{f_n} + f_n\left(2\lambda + 1\right)\right]\left[2\lambda + \frac{2\left(\lambda + 1\right)}{f_n^2} - \frac{3}{f_n^4} + 1\right] \tag{14}$$

$$\text{DEN} = 2k\left[\left(\frac{1}{\lambda} - \frac{1}{\lambda f_n^2} + 1\right)^2 + \frac{Q^2}{\lambda^2}\left[\frac{1}{f_n^3} - \frac{2(\lambda+1)}{f_n} + f_n\left(2\lambda + 1\right)\right]^2\right]^{\frac{3}{2}}. \tag{15}$$

Due to DEN always greater than 0 from (15), whether M_h' always less than 0 which makes continuous monotone decreasing of M_h is entirely determined by NUM > 0.

We can directly plot that the function curves included NUM = 0 based on (14) to distinguish NUM > 0 region and NUM < 0 region, included $M_{h\_\max} = 1.3$ based on (2) to distinguish $M_h > M_{h\_\max} = 1.3$ region and $M_h < M_{h\_\max} = 1.3$ region, and included $f_n = f_{n1}$ based on (12) to distinguish $f_n > f_{n1}$ region and $f_n < f_{n1}$ region in a plane over $f_n \in [0, 1]$, $\lambda \in [1.78, 20]$ under different Q as shown in Fig. 7.

According to Fig. 7, the $f_n > f_{n1}$ and NUM > 0 region located between NUM = 0 and $f_n = f_{n1}$ will be reduced as Q increased, which is the same as the $M_h > M_{h\_\max} = 1.3$ region surrounded by $M_{h\_\max} = 1.3$. Particularly, the shadow part of $M_h > M_{h\_\max}$

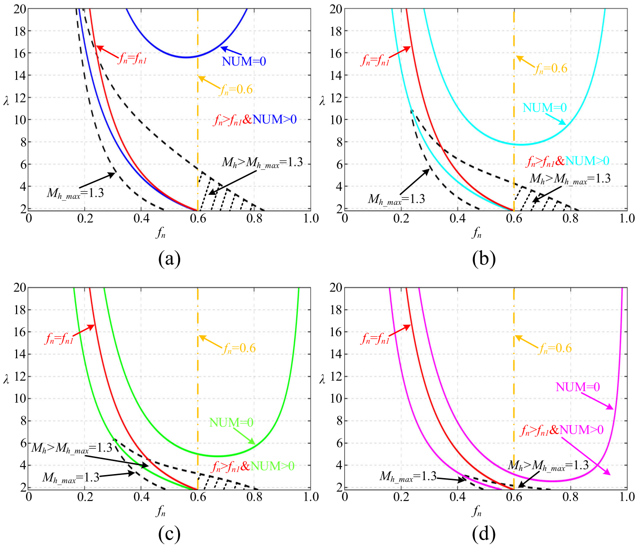


Fig. 7. Function curves of NUM $= 0$, $M_{h\_\max} = 1.3$, and $f_n = f_{n1}$ with (a) $Q = 0.2$, (b) $Q = 0.3$, (c) $Q = 0.4$, and (d) $Q = 0.6$.

$= 1.3$ region located at the right side of $f_n = 0.6$ is always included in $f_n > f_{n1}$ and NUM > 0 region which can make value ranges of f_n and λ to satisfy $f_n > f_{n1}$, NUM > 0, and $M_h > M_{h\_\max} = 1.3$ at the same time. That is, the M_h will be continuously monotone decreasing from beyond 1.3 to 1 with realization of ZVS when f_n increased from 0.6 to 1.0 in this shadow part. But, λ has to be smaller to keep $M_h > M_{h\_\max} = 1.3$ over $f_n \in [0.6, 1]$ because the shadow part will also be reduced as Q increased. Therefore, Q should be decreased to enhance λ that can reduce conduction losses of power devices caused by lower rms of i_p. As usual, λ had better to be greater than 4. At last, a particular design flowchart of calculation of passive components can be established as shown in Fig. 8.

MVGM and LVGM have a longer *LLC* resonance time which makes the polarity of i_p for wheeling current unchanged regardless of the loop loss before changing polarity of u_{ab}, compared with HVGM. Thus, $\dot{i}_p$ will naturally lag behind phase of $\dot{u}_{ab}$. In addition, in Section III-A, it has been analyzed that MVGM and LVGM have the ability to adjust the voltage gain monotonically by FF-PSHM.

C. Design of Dead Time

The charge–discharge process between i_p in the dead time and the parasitic capacitance of the switches builds the ZVS commutation process. Therefore, the dead time to realize ZVS can be designed through the principle of charging conservation. i_p is regarded as constant in dead time which is generally very short, and can be directly represented by the i_{p_OFF} which is indicated as turned-OFF current of switches in each mode.

However, because the current loop losses in *LLC* resonance is so small that the *LLC* resonant current can be regarded as unchanged. According to Sections II-B and II-C, i_{p_OFF} within t_{DTb} to each mode is approximately equal to the *LLC* resonant current that is also equal to the i_{m_OFF} indicated as the *TX* exciting current i_m at the end of the *LC* resonance, then, $i_{p\_\mathrm{OFF}} = i_{m\_\mathrm{OFF}}$. Because in the *LC* resonance process, L_m is always clamped by the u_{cd} with the amplitude U_{ins} calculated by the (2), (4), and (5), time-domain expression of i_m can be derived. Then, an inequality is established to obtain the value range of t_{DTb} based on the principle of charge conservation, and t_{DTL1} and t_{DTL2} will be taken larger than t_{DTb} due to the loop loss of i_p in *LLC* resonance. At last, the design progress of the dead time to each mode is listed as shown in Table II.

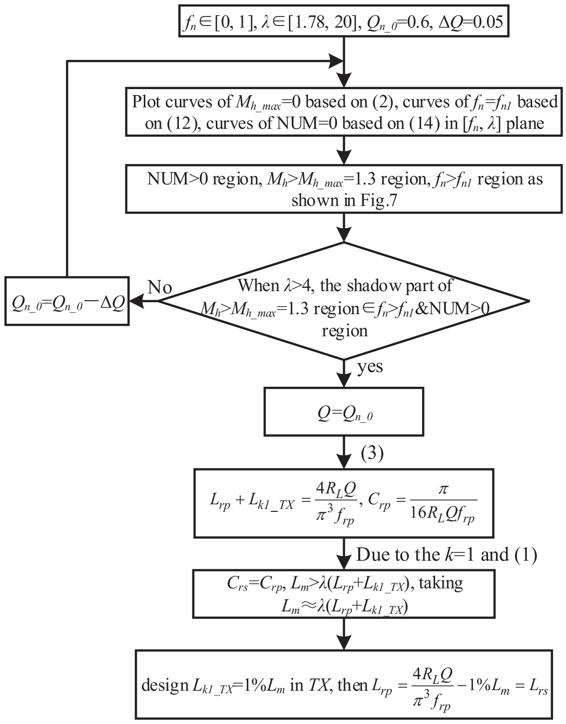


Fig. 8. Flowchart of calculation of passive components.

IV. SIMULATION VERIFICATION AND ANALYSIS TO THE PROPOSED NOVEL CONVERTER

A. Simulation Parameters Design

The simulation experiment is based on SABER platform and the relevant parameters are shown in Table III.

When the parameters of Table III are substituted into Fig. 8, it can be derived that $Q = 0.25$, $L_{rp}+L_{k1\_TX} = 32$ μH, $C_{rp} = C_{rs} = 80$ nF, and taking $\lambda = 4.09$ in practical, then $L_m \approx \lambda\ (L_{rp}+L_{k1\_TX}) = 131$ μH, $L_{k1\_TX} = 1\%L_m = 1.3$ μH, and $L_{rp} = L_{rs} = 30.7$ μH.

B. Simulation Verification and Analysis to Each Mode

In HVGM, according to Section IV-A, $M_h = 1.1$ with Q, λ which are substituted into (2) to figure out $f_n = 0.83$ and $f_{sh} = 83$ kHz. And, $t_{\mathrm{DTb}} > 0.046$ μs based on (19) and (20). Besides, taking $t_{\mathrm{DTb}} = 0.2$ μs $= (\alpha_h/2\pi)/f_{sh}$, $t_{\mathrm{DTL1}} = t_{\mathrm{DTL2}} = 0.3$ μs to make t_3 coincide with t_4. The simulation results are shown in Fig. 9.

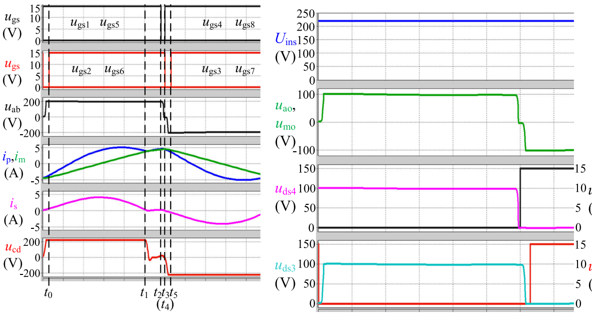
From Fig. 9(a), a bit of different from Fig. 4(a), when $i_p = i_m$, $i_s \approx 0$ at t_1, u_{cd} would not be quickly dropped from U_{ins} to $-U_{\mathrm{ins}}$ by *LCR* resonance due to a wheeling current of i_s which can release the residual energy storage of L_{rs} and C_{rs} delaying *LCR* resonance. At the same time, u_{cd} is also affected by sinusoidal fluctuation. In $[t_2, t_5]$, the phase of $\dot{i}_p$ obviously

TABLE II
DESIGN TABLE OF THE DEAD TIME TO EACH MODE

Design process	HVGM	MVGM	LVGM
1)Time domain expression of i_{m}	$i_{\mathrm{m}}(t)=\frac{kU_{\mathrm{ins}}}{L_m}t-\frac{kU_{\mathrm{ins}}}{L_m}\frac{1}{4f_{rp}}$ (16)		
2)$i_{\mathrm{p\_off}}$	$i_{\mathrm{p\_off\_h}}=i_{\mathrm{m\_off\_h}}=i_{\mathrm{m\_h}}\left(\frac{1}{2f_{rp}}\right)=\frac{kM_hU_{\mathrm{inp}}}{4f_{rp}L_m}$ (17)	$i_{\mathrm{p\_off\_m}}=\frac{kM_mU_{\mathrm{inp}}}{4f_{rp}L_m}$ (21)	$i_{\mathrm{p\_off\_L}}=\frac{kM_LU_{\mathrm{inp}}}{4f_{rp}L_m}$ (25)
3)inequality	$i_{\mathrm{p\_off\_h}}\cdot t_{\mathrm{DTb}}\geq 4\cdot C_{oss}\cdot\frac{U_{\mathrm{inp}}}{2}$ (18)	$i_{\mathrm{p\_off\_m}}\cdot t_{\mathrm{DTb}}\geq 4\cdot C_{oss}\cdot\frac{U_{\mathrm{inp}}}{2}$ (22)	$i_{\mathrm{p\_off\_L}}\cdot t_{\mathrm{DTb}}\geq 2\cdot C_{oss}\cdot\frac{U_{\mathrm{inp}}}{2}$ (26)
4)t_{DTb}	$t_{\mathrm{DTb}}\geq\frac{2C_{oss}U_{\mathrm{inp}}}{i_{\mathrm{p\_off\_h}}}=\frac{8C_{oss}f_{rp}L_m}{kM_h}$ (19)	$t_{\mathrm{DTb}}\geq\frac{8C_{oss}f_{rp}L_m}{kM_m}$ (23)	$t_{\mathrm{DTb}}\geq\frac{4C_{oss}f_{rp}L_m}{kM_L}$ (27)
5)t_{DT1}&t_{DTL2}	$t_{\mathrm{DTL1}}=t_{\mathrm{DTL2}}\geq t_{\mathrm{DTb}}$ (20)	$t_{\mathrm{DTL2}}\geq t_{\mathrm{DTL1}}\geq\frac{4C_{oss}f_{rp}L_m}{kM_m}$ (24)	$t_{\mathrm{DTL1}}\geq t_{\mathrm{DTb}}$ (28)

TABLE III
PARAMETERS OF SIMULATION EXPERIMENT

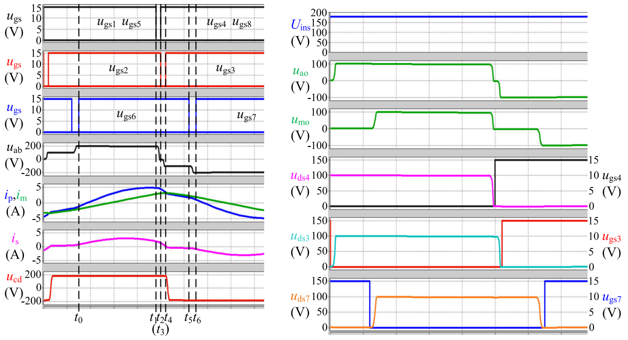
Simulation parameters	Values
U_{inp}	200V
U_{ins}	220V in HVGM, M_h=1.1 180V in MVGM, M_m=0.9 50V in LVGM, M_L=0.25
C_{1p}~C_{2s}	940μF
TX_p&TX_s	1.5mH∶1.5mH
k of TX	1∶1
R_L	100Ω
f_{rp}	100kHz
Q_1~Q_8、T_1~T_8	IRF460
C_{oss}	480pF
D_{11}~D_{42}	Power diode
C_{f1}~C_{f4}	0.2μF



(a) (b)

Fig. 9. (a) Key simulation waveforms of HVGM. (b) Waveforms of U_{ins} and ZVS realized in Q_4 and Q_3.

lags behind phase of $\dot{u}_{ab}$. Q_1 and Q_5 are turned OFF at t_2 to make commutation of ZVS completed before $t_3(t_4)$, then, Q_2 and Q_6 are turned OFF at $t_3(t_4)$ to make commutation of ZVS completed before t_5 and disable *LLC* resonance. From Fig. 9(b), Q_4 and Q_3 have achieved ZVS, voltage stress u_{ds4} and u_{ds3} of Q_4 and Q_3 are both successfully reduced to half of U_{inp} equaled to 100 V. Finally, u_{ao} and u_{mo} outputs three levels with same PWM duty cycle which are combined to form three-level u_{ab}. At last, $U_{\mathrm{ins}}\approx 220$ V, and the rated full-load outputs power $P_{\mathrm{rate\_}h}=484$ W.



(a) (b)

Fig. 10. (a) Key simulation waveforms of MVGM. (b) Waveforms of U_{ins} and ZVS realized in Q_4, Q_3, and Q_7.

In MVGM, $M_m=0.9, f_{sm}=f_{rp}=100$ kHz are substituted into (4) to figure out $\beta=0.93$ rad, then $t_\beta=(\beta/2\pi)/f_{sm}=1.5$ μs. And, $t_{\mathrm{DTb}}>0.056$ μs, $t_{\mathrm{DTL2}}>t_{\mathrm{DTL1}}>0.028$ μs based on (23) and (24). Besides, taking $t_{\mathrm{DTb}}=0.2$ $\mu\mathrm{s}=(\alpha_m/2\pi)/f_{sm}$, $t_{\mathrm{DTL1}}=0.2$ μs, and $t_{\mathrm{DTL2}}=0.3$ μs to make t_2 coincide with t_3. The simulation results are shown in Fig. 10.

From Fig. 10(a), $[t_1,\ t_6]$ shows that the phase of $\dot{i}_p$ lags behind phase of $\dot{u}_{ab}$, Q_1 and Q_5 are turned OFF at t_1 to make commutation of ZVS completed before $t_2(t_3)$, Q_2 is turned OFF at $t_2(t_3)$ to make commutation of ZVS completed before t_4. And, when $i_p=i_m$, $i_s\approx 0$ at t_4 by influence of the dead time, u_{cd} is quickly dropped from U_{ins} to $-U_{\mathrm{ins}}$ by *LCR* resonance with little sinusoidal fluctuation as same as Fig. 2. When an appropriate β is taken, it can be ensured that Q_6 is turned OFF at t_5 to make commutation of ZVS completed before t_6. From Fig. 10(b), Q_4 and Q_3 and Q_7 have achieved ZVS, voltage stress u_{ds4} and u_{ds3} and u_{ds7} of Q_4 and Q_3 and Q_7 are successfully reduced to half of U_{inp} equaled to 100 V. Finally, u_{ao} and u_{mo} output three levels with different PWM duty cycle which are combined to form five-level u_{ab}. At last, $U_{\mathrm{ins}}\approx 180$ V, and the rated medium-load outputs power $P_{\mathrm{rate\_m}}=324$ W$\approx 67\%P_{\mathrm{rate_h}}$.

In LVGM, $M_L=0.25, f_{sL}=f_{rp}=100$ kHz are substituted into (5) to figure out $\theta=\pi/2$rad, then $t_\theta=(\theta/2\pi)/f_{sL}=2.5$ μs, but will be changed to 3.4 μs in practical. And, $t_{\mathrm{DTb}}>0.100$ μs based on (27) and (28). Besides, taking $t_{\mathrm{DTb}}=0.3$ μs, $t_{\mathrm{DTL1}}=0.6$ μs. The simulation results are shown in Fig. 11.

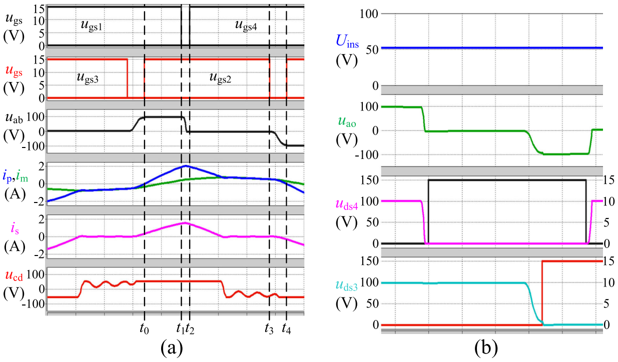


Fig. 11. (a) Key simulation waveforms of LVGM. (b) Waveforms of U_{ins} and ZVS realized in Q_4 and Q_3.

From Fig. 11(a), θ design error is getting worse when LVGM operates at light load caused by the influence of dead time. In [t_1, t_4], the phase of $\dot{i}_p$ barely lags behind phase of $\dot{u}_{ab}$, and Q_1 is turned OFF at t_1 to make commutation of ZVS completed before t_2. When $i_p = i_m$, i_s≈0 between t_2 and t_3, u_{cd} is quickly dropped from U_{ins} to $-U_{\text{ins}}$ by *LCR* resonance, then affected by a small amplitude and long holding time sinusoidal fluctuation as same as Fig. 4(b). In addition, in [t_3, t_4], due to the loop loss of i_p, when an appropriate θ and larger t_{DTL1} is taken, it can be ensured that Q_2 is turned OFF at t_3 to make commutation of ZVS completed before t_4 with enough current charge. From Fig. 11(b), Q_4 and Q_3 have achieved ZVS, and voltage stress u_{ds4} and u_{ds3} of Q_4 and Q_3 are successfully reduced to half of U_{inp} equaled to 100 V. Finally, u_{ao} outputs three levels with $u_{mo} = 0$ and forms three-level u_{ab}. At last, U_{ins}≈50 V, and the rated light-load outputs power $P_{\text{rate\_}L} = 25$ W≈5%$P_{\text{rate\_}h}$.

V. EXPERIMENTAL VERIFICATION AND ANALYSIS OF THE PROPOSED NOVEL CONVERTER

A. *Experimental Parameters Design*

The experimental parameters of the prototype are the same as the simulation parameters. Moreover, voltage and current stress of power devices is an important index to guide selection of MOSFETs. Sections II-B and II-C have explained that the voltage stress of switches of primary 5L-CNPC could be reduced to half of the input sources (i.e., max $u_{\text{ds}} = U_{\text{inp}}/2$), while the voltage stress of switches of secondary 5L-CNPC could be reduced to half of the output voltage (i.e., max $u_{\text{ds}} = U_{\text{ins}}/2$). And, in MVGM and LVGM, due to the voltage gain M_m and $M_L < 1$, $U_{\text{ins}}/2 < U_{\text{inp}}/2$. In HVGM, due to the voltage gain $M_h > 1$, $U_{\text{ins}}/2 > U_{\text{inp}}/2$, so the upper limit of voltage stress to MOSFETs and diodes is $U_{\text{ins}}/2 = 110$ V. Furthermore, the max current stress is obviously depended by HVGM because the i_p is largest and $i_p = i_m + i_s$. According to *LC* resonance, it can be derived that the max peak and rms of i_p could be $i_{p\_\text{peak}} = U_{\text{inp}}/Z_r = 10$ A, $i_{p\_\text{peak\_rms}} = i_{p\_\text{peak}}/\sqrt{2} = 7.07$ A which is the upper limit of current stress to MOSFETs and diodes. And, SiC MOSFETs are selected to easily realize ZVS of switches. The specific models of components are shown in Table IV.

And, the prototype is shown in Fig. 12.

TABLE IV
SPECIFIC MODEL OF COMPONENTS

Components		Models
Q_1~Q_8、T_1~T_8		IMW65R107M1H(650V/20A), $R_{DS(on),typ}$=107mΩ, $V_{\text{F\_body\_diodes}}$=1V
D_{11}~D_{42}		APT30DQ60BG(600V/30A), $V_{\text{F\_clamp\_diodes}}$=1.7V
gate driver		2EDF7175FXUMA1
DSP		TMS320F28379D
sampling		Hall Sensor
TX_p/TX_s	magnetic core	Ferrite EE55(PC40)
	number of turns	15:15
	wire	Litz with 0.1mm×180, d=1.8mm, S=1.412mm^2, $i_{\text{max\_rms}}$=7.1A
TX	magnetic core	Ferrite EE55(PC40)
	number of turns	20:20
	wire	Litz with 0.1mm×180, d=1.8mm, S=1.412mm^2, $i_{\text{max\_rms}}$=7.1A
L_{rp}/L_{rs}	magnetic core	Ferrite PQ40(PC40)
	number of turns	15
	wire	Litz with 0.1mm×180, d=1.8mm, S=1.412mm^2, $i_{\text{max\_rms}}$=7.1A
C_{rp}/C_{rs}		CBB/2000V
C_{f1}~C_{f4}		CBB/630V
C_{1p}~C_{2s}		ECAP/500V

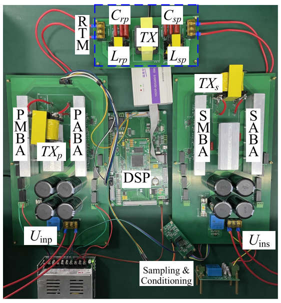


Fig. 12. Prototype in practical.

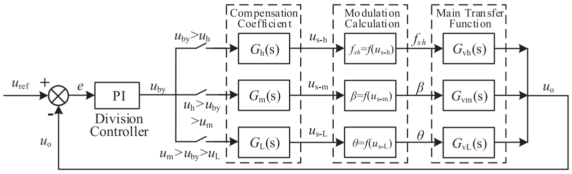


Fig. 13. Control block diagram.

B. *Closed-Loop Control Design*

A digital control method is adopted in order to realize the mode switching, and the control block diagram is shown in Fig. 13.

According to Fig. 13, the compensation controller of each mode is composed of two parts: a unified division controller and the compensation coefficient corresponding to each mode. The control flow is that first reference u_{ref} minus actual value u_o, i.e., U_{ins} to equal error e, then e passes through the division controller to generate a signal u_{by}. Second, u_{by} enters certain mode to multiply compensation coefficient by comparing with the threshold values u_{h}, u_m, and u_L of each mode. Third, the control signals $u_{s\text{-}h}$, $u_{s\text{-}m}$, and $u_{s\text{-}L}$ are generated to be independent variable of modulation calculation which is used for deriving modulation variables, i.e., f_{sh}, β, and θ. Finally, modulation variables are

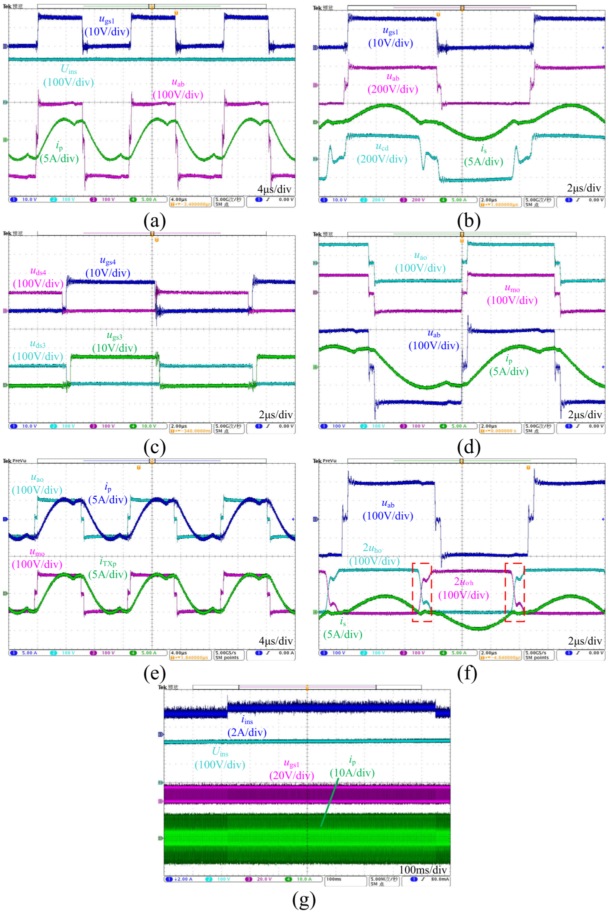


Fig. 14. (a) u_{gs1}, U_{ins}, i_{p}, u_{ab}, (b) u_{gs1}, u_{ab}, i_{s}, u_{cd}, (c) u_{ds4}, u_{gs4}, u_{ds3}, u_{gs3}, (d) u_{ao}, u_{mo}, u_{ab}, i_{p}, (e) u_{ao}, i_{p}, u_{mo}, i_{TXp}, (f) u_{ab}, $2u_{\mathrm{ho'}}$, $2u_{\mathrm{o'h}}$, i_{s}, and (g) i_{ins}, U_{ins}, u_{gs1}, i_{p}.

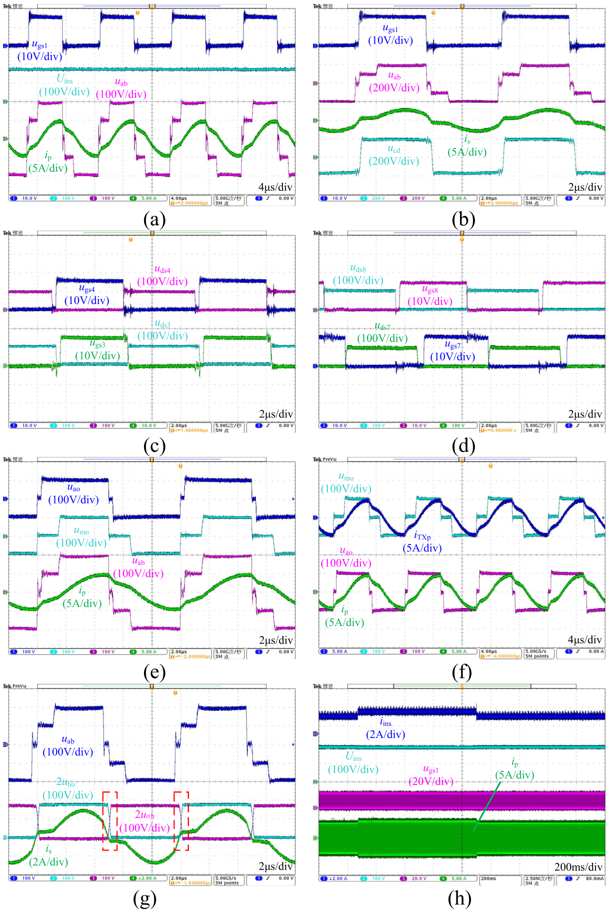


Fig. 15. (a) u_{gs1}, U_{ins}, i_{p}, u_{ab}, (b) u_{gs1}, u_{ab}, i_{s}, u_{cd}, (c) u_{ds4}, u_{gs4}, u_{ds3}, u_{gs3}, (d) u_{gs8}, u_{ds8}, u_{gs7}, u_{ds7}, (e) u_{ao}, u_{mo}, i_{p}, u_{ab}, (f) u_{mo}, i_{TXp}, u_{ao}, i_{p}, (g) u_{ab}, $2u_{\mathrm{ho'}}$, $2u_{\mathrm{o'h}}$, i_{s}, and (h) i_{ins}, U_{ins}, u_{gs1}, i_{p}.

applied to the main circuit by modulation methods of each mode. After sampling, a negative feedback closed-loop control is built.

C. Prototype Experimental Verification and Analysis to Each Mode

In HVGM, based on the simulation experiment, f_{sh} is changed to 80 kHz, $t_{\mathrm{DTb}} = 0.3$ μs $= (\alpha_h/2\pi)/f_{sh}$, $t_{\mathrm{DTL1}} = t_{\mathrm{DTL2}} = 0.3$ μs to make the 0 level more clear. The experimental results of HVGM are shown in Fig. 14.

Fig. 14(a) shows $U_{\mathrm{ins}} = 220$ V, u_{ab} outputs U_{inp}, 0, and $-U_{\mathrm{inp}}$ levels, phase of $\dot{i}_p$ lag behind phase of $\dot{u}_{ab}$. Fig. 14(b) shows when $i_s = 0$, u_{cd} will drop from U_{ins} by the *LCR* resonance, but then affected by a severe sinusoidal fluctuation as same as Fig. 9(a). Fig. 14(c) shows Q_4 and Q_3 realize ZVS, and voltage stress u_{ds4} and u_{ds3} of Q_4 and Q_3 are successfully reduced to half of U_{inp} equaled to 100 V. Fig. 14(d) shows since PMBA and PABA use the same modulation method, $u_{ao} = u_{mo}$ and $u_{ao}+u_{mo}$ form three-level u_{ab} by coupling effect of TX_p as same as Fig. 9(b). Particularly, from Fig. 14(e), it can find that TX_p has self-sharing current to make the $i_p = i_{\mathrm{TXp}}$ with same phase and amplitude which can, respectively, lag behind phases of u_{ao} and u_{mo}. Therefore, according to Fig. 14(c), Q_8 and Q_7 can realize ZVS too. Fig. 14(f) shows body diodes of MOSFETs realize ZCS indicated in red dotted box where peaks of $2u_{\mathrm{ho'}}$, $2u_{\mathrm{o'h}}$ are both equal to $U_{\mathrm{ins}} = 220$ V. Fig. 14(g) shows good dynamic response with steady 220 V output in the dynamic process of 28% onloading and unloading based on P_h.

In MVGM, as same as the simulation experiment, $t_\beta = 1.5$ μs, $f_{sm} = 100$ kHz. Then, taking $t_{\mathrm{DTb}} = 0.3$ μs $= (\alpha_m/2\pi)/f_{sm}$, $t_{\mathrm{DTL1}} = 0.3$ μs, $t_{\mathrm{DTL2}} = 0.5$ μs in practical. The experimental results of MVGM are shown in Fig. 15.

Fig. 15(a) shows $U_{\mathrm{ins}} = 180$ V, u_{ab} outputs $U_{\mathrm{inp}}/2$, U_{inp}, 0, $-U_{\mathrm{inp}}/2$, and $-U_{\mathrm{inp}}$ levels, phase of $\dot{i}_p$ lag behind phase of $\dot{u}_{ab}$. Fig. 15(b) shows when $i_s = 0$, u_{cd} quickly drops from U_{ins} to $-U_{\mathrm{ins}}$ by the *LCR* resonance, then u_{cd} maintains $-U_{\mathrm{ins}}$ with little sinusoidal fluctuation as same as Fig. 10(a). Fig. 15(c) shows Q_4 and Q_3 realize ZVS, voltage stress u_{ds4} and u_{ds3} of Q_4 and Q_3 are successfully reduced to half of U_{inp} equaled to 100 V. Fig. 15(d) shows Q_8 and Q_7 realize ZVS, voltage stress u_{ds8} and u_{ds7} of Q_8 and Q_7 are successfully reduced to half of U_{inp} equaled to 100 V. Fig. 15(e) shows since PMBA and PABA use the different modulation method, $u_{ao} \neq u_{mo}$ and $u_{ao}+u_{mo}$ forms five-level u_{ab} by coupling effect of TX_p as same as Fig. 10(b). Fig. 15(f) still shows $i_p = i_{TXp}$, but angle of i_p lagged behind u_{ao} is more than angle of i_{TXp} lagged behind u_{mo} which means PABA adopted FF-PSHM is more difficult to realize ZVS compared to PMBA. Fig. 14(g) shows body diodes of MOSFETs realize ZCS indicated in red dotted box where peaks

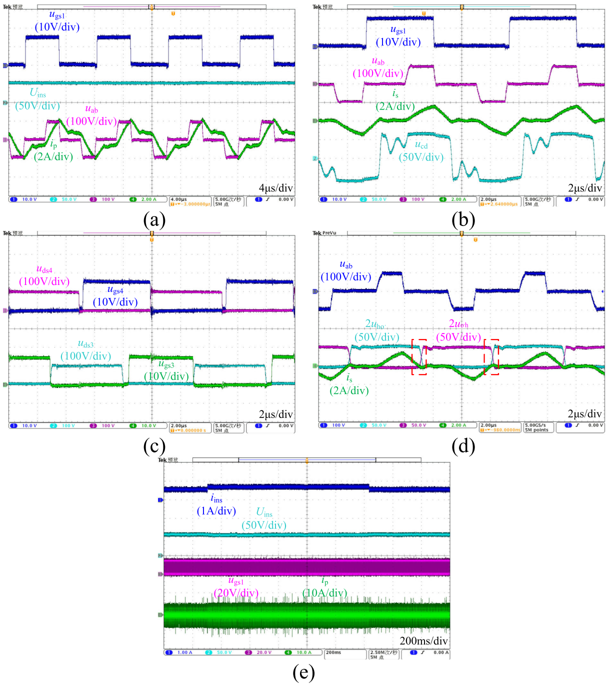


Fig. 16. (a) u_{gs1}, U_{ins}, i_p, u_{ab}, (b) u_{gs1}, u_{ab}, i_s, u_{cd}, (c) u_{ds4}, u_{gs4}, u_{gs3}, u_{ds3}, (d) u_{ab}, $2u_{ho'}$, $2u_{o'h}$, i_s, and (e) i_{ins}, U_{ins}, u_{gs1}, i_p.

of $2u_{ho'}$, $2u_{o'h}$ are both equal to $U_{ins} = 180$ V. Fig. 15(h) shows a good dynamic response with steady 180 V output in the dynamic process of 28% onloading and unloading based on P_m.

In LVGM, as same as the simulation experiment, $f_{sL} = 100$ kHz, but taking $t_\theta = 3.0$ μs, $t_{\mathrm{DTb}} = 0.3$ μs, and $t_{\mathrm{DTL1}} = 0.5$ μs in practical. The experimental results of LVGM are shown in Fig. 16.

Fig. 16(a) shows $U_{ins} = 50$ V, u_{ab} outputs $U_{inp}/2$, 0, and $-U_{inp}/2$ levels, phase of $\dot{i}_p$ lag behind phase of $\dot{u}_{ab}$. Fig. 16(b) shows when $i_s = 0$, u_{cd} drops from U_{ins} to $-U_{ins}$ by the *LCR* resonance, then affected by a sinusoidal fluctuation with small amplitude and long holding time as same as Fig. 11(a). Fig. 16(c) shows Q_4 and Q_3 realize ZVS, voltage stress u_{ds4} and u_{ds3} of Q_4 and Q_3 are successfully reduced to half of U_{inp} equaled to 100 V as same as Fig. 11(b). Fig. 14(d) shows body diodes of MOSFETs realize ZCS indicated in red dotted box where peaks of $2u_{ho'}$, $2u_{o'h}$ are both equal to $U_{ins} = 50$ V. Fig. 16(e) shows a good dynamic response with steady 50 V output in the dynamic process of 28% onloading and unloading based on P_L.

D. Prototype Voltage Gain Curves

Compared to MVGM and LVGM which both adopt FF-PSHM, the voltage gain adjustment of HVGM is seriously affected by PFM. Thus, the prototype voltage gain M curves under designed $Q = 0.25$, $\lambda = 4.09$ is mainly about HVGM that includes an experimental voltage gain and several theoretical voltage gain based on simulated dc sweep, FHA, and time-domain analysis. It can be shown in Fig. 17.

Fig. 17(a) shows that M is increased as f_n far away from 1. In $f_n \in [0.60, 0.75]$, the difference between the M of FHA and the M of dc sweep, time domain, experiment is bigger and bigger,

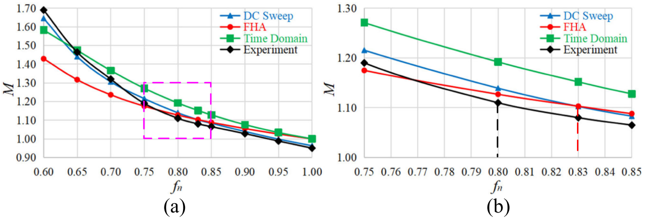


Fig. 17. Prototype voltage gain M curves of HVGM: (a) $f_n \in [0.60, 1.00]$ and (b) $f_n \in [0.75, 0.85]$.

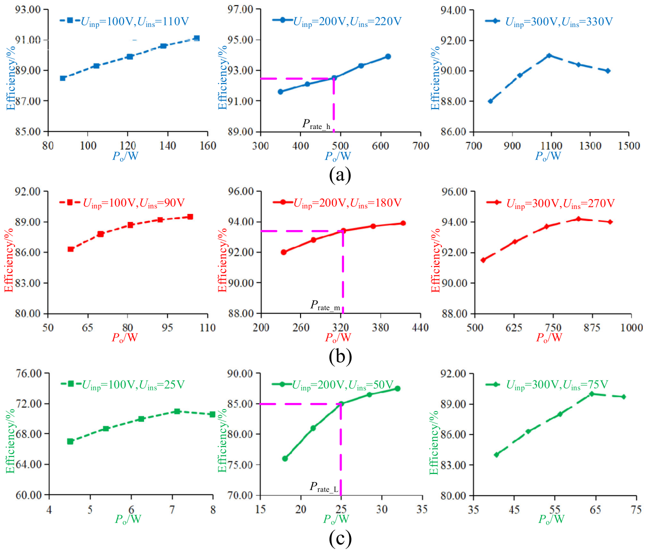


Fig. 18. Prototype experimental efficiency curves with three different voltage values to each mode: (a) HVGM, (b) MVGM, and (c) LVGM.

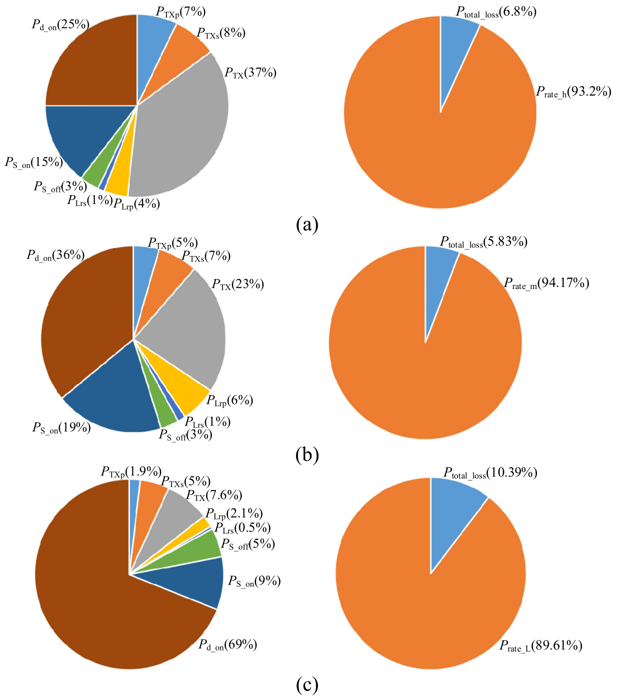
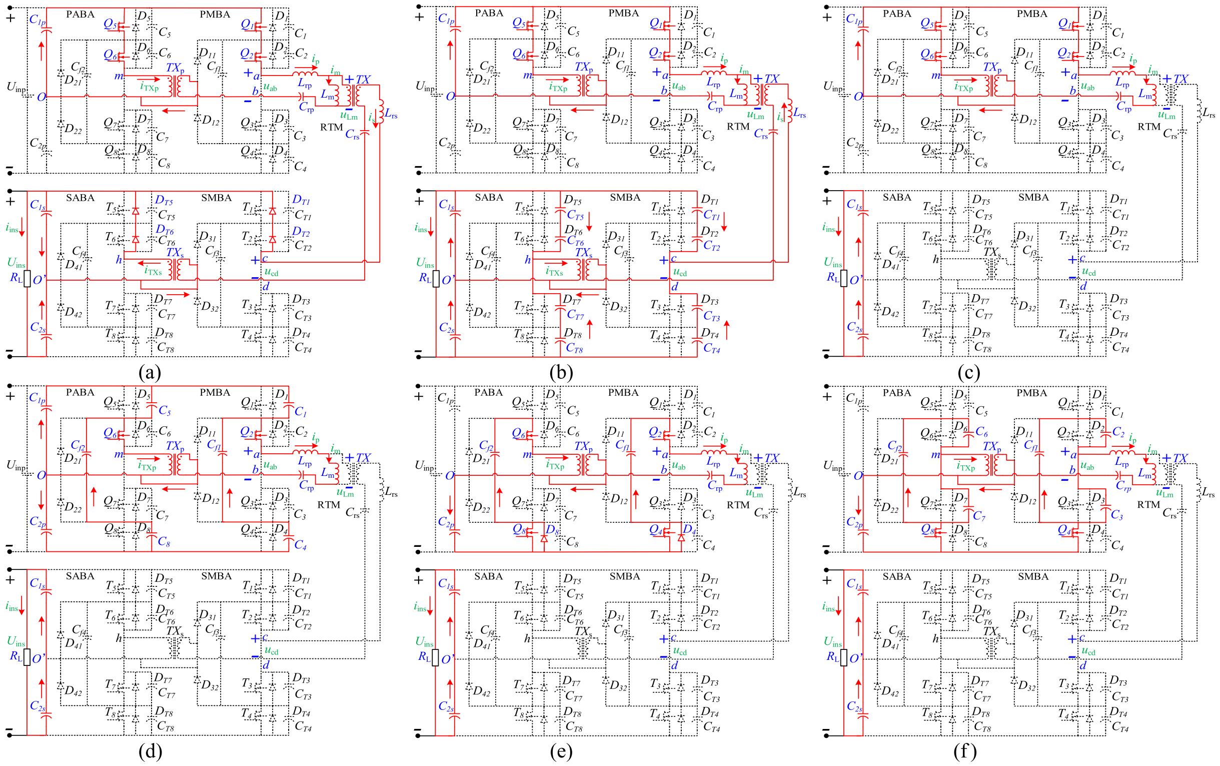


Fig. 19. Theoretical power losses distribution and efficiency of the prototype: (a) HVGM, (b) MVGM, and (c) LVGM.



(a) (b) (c) (d) (e) (f)

Fig. 20. Key states of equivalent circuits to HVGM. (a) State I [t_0, t_1]. (b) State II [t_1, t_2]. (c) State III [t_2, t_3]. (d) State IV [t_3, t_4]. (e) State V [t_4, t_5]. (f) State VI [t_5, t_6].

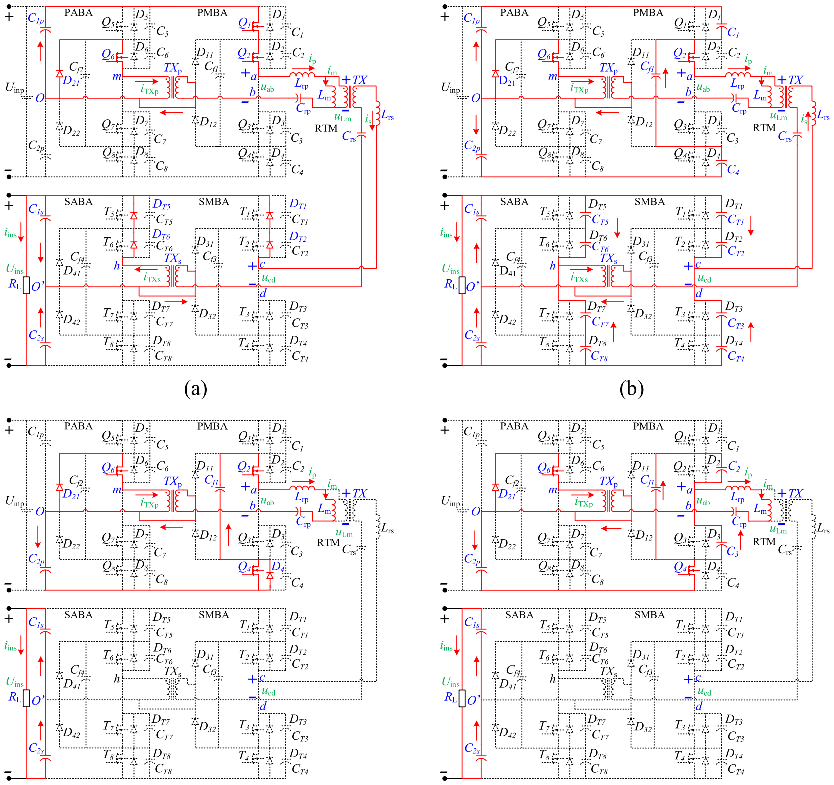
and this is because the third and fifth harmonic components of resonant current i_p are big enough in lower f_n compared with the fundamental harmonic component which is not a negligible effect of power transmission. In addition, the M of Experiment and dc sweep are almost the same and both less than 1 at $f_n = 1$ caused by the influence of dead time that can shorten *LC* resonance which is the main process for power transmission. Meanwhile, the M of time domain is almost highest in $f_n \in [0.65, 1.00]$ caused by bigger resonant current in theory. Then, $f_n \in [0.75, 0.85]$ of Fig. 17(a) is enlarged to Fig. 17(b) that shows the M of experiment at $f_n = 0.80$ is equal to 1.1 which is the designed rated voltage gain to HVGM, while the M of FHA at $f_n = 0.83$ is equal to 1.1. Therefore, it can be demonstrated that FHA can be adopted in PFM with higher f_n to close to the experiment.

E. Prototype Experimental Efficiency Curves

The prototype experimental efficiency curves with three different input voltages to each mode is shown in Fig. 18.

In Fig. 18, three different input voltages are divided into $V_{\text{in-max}} = U_{\text{inp}} = 300$ V, $V_{\text{in-rate}} = U_{\text{inp}} = 200$ V, $V_{\text{in-min}} = U_{\text{inp}} = 100$ V, while all are kept unified output voltage gain $M_h = 1.1$ to HVGM, $M_m = 0.9$ to MVGM, and $M_L = 0.25$ to LVGM. And, around $P_{\text{rate\_h}}$ (92.5%), the proposed novel converter has the same high operating efficiency as the conventional bidirectional full-bridge *CLLC* resonant converter. Around P_{rate_m} (93.4%), due to the FF-PSHM, the switching frequency is greatly lower than PFM worked in the beyond-resonant mode, which can maintain high operating efficiency by ZVS and ZCS. Around P_{rate_L} (85%), FF-PSHM is easier to realize ZVS than PFM worked in the beyond-resonant mode, and reduce the influence of high-frequency parasitic parameters of the circuit by fixed $f_s = = f_{rp}$. In addition, comparing Figs. 14(e) with 15(f), the i_p disturbance generated by FF-PSHM is much smaller than the i_p disturbance generated by PFM which can reduce magnetic loss. Actually, the converter will generate: 1) transformer losses P_{TXp}, P_{TXs}, P_{TX}; 2) resonant inductor losses P_{Lrp}, P_{Lrs}; 3) switching losses of MOSFETs that mainly refer to turn-OFF losses $P_{\text{S\_OFF}}$ of switches of primary 5L-CNPC since ZVS; 4) conduction losses $P_{\text{S\_ON}}$ of switches of primary 5L-CNPC; 5) conduction losses $P_{\text{d\_ON}}$ of body diodes of MOSFETs in secondary 5L-CNPC, while reverse recovery losses can be ignored due to ZCS. Then, the pie charts are plotted to show the theoretical power losses distribution and efficiency of the prototype on rated output power of each mode as Fig. 19.

Compared Fig. 19 with 18, the experimental efficiency is closed to theoretical efficiency on P_{rate_h} and P_{rate_m} of HVGM and MVGM, but is a bit far from theoretical efficiency on P_{rate_L} of LVGM which means that there may have some equivalent impedance caused by layout of PCB or components difference existed in practice. Furthermore, it is noted that Fig. 19(c) shows the P_{TXp} and P_{S_ON} are much smaller than P_{TXs} and P_{d_ON} on the power losses distribution of LVGM which is not same as HVGMs and MVGMs because the modulation method adopted in LVGM will be short primary side of TX_p by constant turn-OFF of Q_5 and Q_8 and constant turn-ON of Q_6 and Q_7 that can make $u_{mo} = 0$ to eliminate magnetic hysteresis losses of TX_p and conduction losses of two switches, but to add additional conduction losses of two clamp diodes according to current loop as shown in Fig. 4(b). And, as the P_{rate} decreased, percentage of P_{d_ON} is bigger and bigger caused by complexity of 5L-CNPC active bridge which is a sacrifice to achieve the same forward and backward power transmission characteristics.



(a) (b)

(c) (d)

Fig. 21. Key states of equivalent circuits to LVGM. (a) State I [t_0, t_1]. (b) State II [t_1, t_2]. (c) State III [t_2, t_3]. (d) State IV [t_3, t_4].

VI. CONCLUSION

A novel bidirectional five-level multimode *CLLC* resonant converter is proposed and successfully widen the voltage gain with realizing of ZVS in primary 5L-CNPC, maximum gain $M_{h\_\max}$ designed in HVGM, minimum gain existed in LVGM which can be zero, related analysis about operation principles of each mode, converter power losses distribution, and current/voltage stress for component design. At last, the simulation and experimental results are close to voltage gain and the key waveforms of theoretical design. Therefore, the feasibility of the proposed converter has been verified. In addition, some novel characteristics can be summarized as 1) voltage stress of the switches in 5L-CNPC can be reduced to half of input voltage of converter; 2) through the coupling transformer TX_p, PMBA and PABA have own current loop caused by electrical isolation which can automatically achieve self-sharing of current; and 3) when all switches in 5L-CNPC are constantly turned OFF, the 5L-CNPC can be regarded as full bridge rectifier circuit to easier to build ac equivalent operation circuit by FHA.

APPENDIX

The complete states of equivalent circuits are all plotted in the appendix Figs. 20 and 21 to help for understand of operation principles of HVGM and LVGM.

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