A Comprehensive Comparison of Two Fast-Dynamic Control Structures for the DAB DC–DC Converter

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***Abstract*—Benefitting from some significant advantages, the dual active bridge (DAB) dc–dc converter has become one of the most promising candidates for dc–dc power conversion. In recent years, some strategies have been proposed to boost the dynamic performance of DAB dc–dc converter under the disturbance of input voltage and load condition. According to the relationship between the compensation part and the model-based part, these existing schemes can be divided into two structures including the parallel structure and series structure. In the parallel control structure, the compensation part is added to the model-based part. In contrast, the compensation part is multiplied with the model-based part in the series control structure. By adopting proper feedback control, both control structures can provide excellent dynamic performance for DAB dc–dc converter easily. Hence, the modified parallel-structure fast-dynamic control scheme and the modified series-structure fast-dynamic control scheme are both proposed in this article. Then, using these two proposed schemes as examples, the merits and the demerits of both structures are analyzed, and the corresponding compensation methods are also presented. Moreover, a general PI design principle of the model-based control scheme for the DAB dc–dc converter is provided, which is different from the traditional concept for designing the PI parameters. In addition, the control delay of these two proposed schemes is analyzed, and a compensation method is also proposed. Finally, simulation results and experimental results are obtained to verify the analysis in this article and the excellent performance of the proposed methods.**

***Index Terms*—Comparison, control structures, dual active bridge (DAB) dc–dc converter, dynamic response.**

I. Introduction

With some merits such as high-power density, high efficiency, and excellent controllability, the dual active bridge (DAB) dc–dc converter has become a promising solution to the dc–dc power conversion [1], [2]. The DAB dc–dc converter has been widely studied in the distributed generating systems [3], [4], the automotive applications [5], the energy storage systems [6], [7], and the middle-frequency railway traction applications [8]. Obviously, in these above applications, the DAB dc–dc converter should be employed to deal with the change of input voltage, load condition, and so on [9], [10]. Sometimes, the pulsed power loads such as the radar, the sonar, and the electro-magnetic may connect with the DAB-based system, which expects more of the dynamic response performance [11]. Therefore, the robust and fast dynamic response is an essential requirement for the DAB dc–dc converter in industry applications. In the past decade, there are lots of strategies focusing on the improvement of the dynamic performance of the DAB dc–dc converter [12]–[15].

In the beginning, some mature dynamic optimizing concepts from the buck converters and boost converters are simulated for boosting the dynamic performance of the DAB dc–dc converter such as the current sensorless control concept [12], [13], [15], the load-current feedforward control concept [16], and the direct inductance-current concept [17], [18]. Generally, it is easy to obtain the fast-dynamic response for the buck converters and boost converters with the feedback of the input voltage. Nevertheless, the dynamic performance under the change of input voltage is usually neglectful. Based on these concepts, the existing control methods for the DAB dc–dc converter are more focusing on the change of load condition. Based on the current sensorless control concept, the dynamic performance of the DAB dc–dc converter can be boosted to some degree [12], [13], [15], but the limited loop gain and the inaccurate converter model will restrict the performance of these control methods because of some undesirable factors such as measurement noises. With the feedforward value of the load current, an energy feedforward scheme is proposed to boost the dynamic response of DAB dc–dc converter by considering the relationship between the phase-shift ratio and the load current [19]. However, this relationship is simplified in the controller system to reduce the complexity of control, which makes the feedforward value inaccurate. Moreover, the improvement of the dynamic response is restricted. Similarly, a feedforward compensation strategy is presented for boosting the dynamic response of the DAB converter under the load disturbance [20]. Although the dynamic response of the DAB converter can be improved significantly, this method lacks transportability. Moreover, it is not suitable for the online continuous control in digital controller since the lookup table is unavoidable. Besides, based on the control of the peak value or valley value of the inductance current, some dynamic optimization schemes are

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proposed for the DAB dc–dc converter [21]–[23]. In these existing peak/valley value controls of inductance current, the variant phase-shift method is usually adopted for eliminating the dc offset during the transient process. However, the improvement of the dynamic performance sometimes fails without the feedback of load current [22]. Therefore, by combining the knowledge of load current, a direct inductance-current control scheme is proposed for improving the dynamic response of the DAB dc–dc converter [23], which can improve the dynamic response of this converter significantly with the cost of two current sensors. The adopted simplified converter model will also influence the dynamic performance.

Without consideration of power losses, the power transferred characteristic of the DAB dc–dc converter during the transient process is verified to be the same as that at steady-state condition for the first time in [24]. Based on this characteristic, a virtual direct power control strategy is proposed in this article for the DAB dc–dc converter, and the excellent dynamic performance can be obtained under the change of input voltage and load condition. However, the design principle of PI parameters is not discussed. Then, based on this transferred characteristic of the DAB dc–dc converter, some power-based control schemes are extensively proposed for the DAB dc–dc converter with excellent dynamic response [25]–[27]. Meanwhile, by adding the control of inductance current, the dc offset of the inductance current can also be achieved [27]. Moreover, some model predictive control schemes are proposed to boost the dynamic response of the DAB dc–dc converter [28]–[30]. By establishing the cost function of the output voltage, the model predictive control method is proposed to improve the dynamic response of the DAB dc–dc converter under the change of load condition. Since the relationship between the phase-shift ratio and the transferred power of the DAB dc–dc converter is a one-to-one correspondence, these existing model predictive controls may bring a complicated control procedure. Moreover, the adopted criteria equation is sensitive to the measurement noise, which may make the predicative operation inaccurate.

Generally, according to the existing control methods for boosting the dynamic response of the DAB dc–dc converter, there are always two main aspects in the control diagrams including the compensation part and the model-based part [19]–[27]. Then, based on the relationship between these two parts, the existing schemes can be divided into two types of structures including the parallel structure and the series structure. According to these two structures, the further classification of the existing dynamic optimizing strategies will be shown in Section II. The modified parallel-structure fast-dynamic control (MPSFDC) scheme and the modified series-structure fast-dynamic control (MSSFDC) scheme are proposed for further ensuring the excellent dynamic performance for the DAB dc–dc converter. Then, based on these two modified schemes, the advantage and the disadvantage of these two structures will be presented. The corresponding compensation methods for omitting the disadvantages of these two structures will be proposed in Section III. Besides, the design principles of PI parameters for these two modified fast-dynamic control methods are provided in Section IV, which can be extended to another feedforward control method for DAB dc–dc converter. Then, since there is always a delay in the control system after the load resistor is changed, the delay compensation methods are also presented for these two structures in Section IV. Further, in Section V, the simulation results and experimental results are employed to verify these presented methods. Finally, Section VI concludes this article.

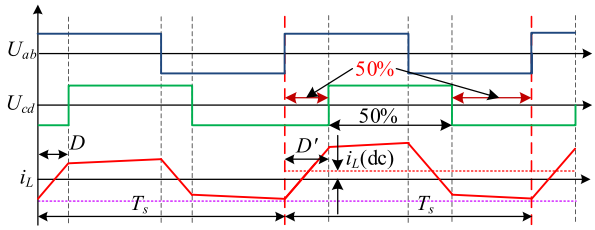

Fig. 1. Waveforms of the SPS modulation method during the transient process.

II. Parallel-Structure and Series-Structure Fast-Dynamic Control Schemes

In this section, a general modulation and control structure for the DAB dc–dc converter is analyzed, which can be employed to combine the phase-shift modulation method and the closed-loop control method. Then, based on the relationship between the compensation part and the model-based part, the existing model-based control methods are divided into two groups including the parallel-structure control scheme and the series-structure control scheme. Moreover, the MPSFDC scheme and the MSSFDC scheme are proposed for further boosting the dynamic response when the input voltage and the load condition are changed.

A. General Modulation and Control Structure for the DAB Converter

Without consideration of power losses, the relationship between the phase-shift ratio and transferred power or inductance current of the DAB dc–dc converter during the transient process is the same as that under steady-state condition, which is first presented in [24]. The waveforms of the single phase shift (SPS) modulation method during the transient process can be described as shown in Fig. 1, and then the transferred power P_T can be calculated as

$$\begin{aligned} P_T &= \frac{1}{T_s}\int_0^{T_s}\frac{U_{\rm cd}}{n}(i_L+\Delta i_L)dt = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} U_{\rm in} i_L dt \\ &\quad + \frac{\Delta i_L}{T_s}\int_0^{T_s} U_{ab}\,dt \\ &= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} U_{\rm in} i_L dt = \frac{U_{\rm in}U_o D(1-D)T_s}{2nL} \end{aligned} \tag{1}$$

where n is the transformer turn ratio, L is the middle ac inductance, D is the phases-shift ratio, T_s is the switching period, $U_{\rm in}$ is the input voltage, and U_o is the output voltage. As shown in (1), since the dc offset of inductance current cannot transfer the power from the input side to the output side with ac voltage, the transferred power or inductance current of the DAB

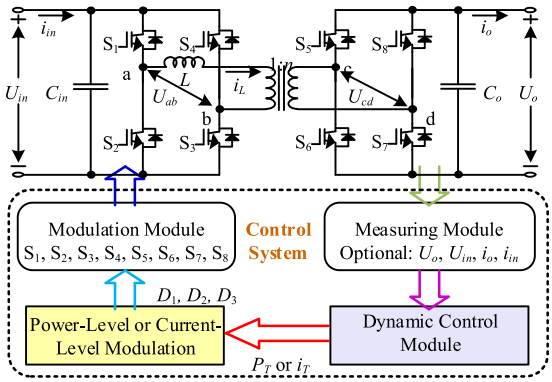

Fig. 2. Diagram of the general modulation and control structure for the DAB dc–dc converter.

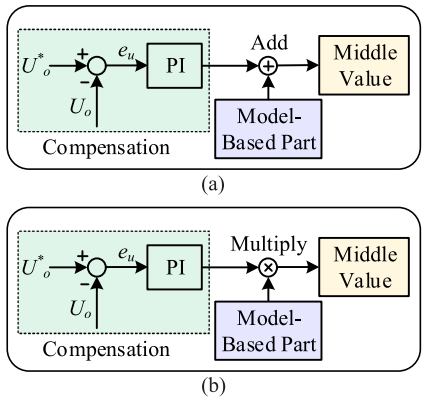

Fig. 3. Diagrams of the parallel-structure and series-structure dynamic controls for DAB dc–dc converter. (a) Parallel-structure control. (b) Series -structure control.

dc–dc converter is directly determined by the phase-shift ratio. Moreover, when the phase-shift ratio is not changed again at the new steady-state condition, the output voltages of two-side H bridges cannot generate the dc current; so the dc offset of inductance current will be consumed by the conduction resistor in the flowing loop.

Therefore, the phase-shift ratio can be calculated as the transferred power or inductance current of the DAB dc–dc converter and vice versa

$$D = \begin{cases} \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2nLP_T}{U_{\text{in}}U_o T_s}} & (P_T \geq 0) \\ -\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{2nLP_T}{U_{\text{in}}U_o T_s}} & (P_T < 0). \end{cases} \tag{2}$$

Similarly, this transient characteristic can also be obtained under other phase-shift modulations such as the dual phase shift (DPS) modulation and triple phase shift (TPS) modulation. Then, the power-level or current-level modulations can be realized, and the middle inductance will not influence the dynamic performance, which can be employed for obtaining a fast-dynamic response. So, a general structure including phase-shift based modulation and control for the DAB dc–dc converter can be presented as shown in Fig. 2 [2]. Then, based on some dynamic control methods, the desired transferred power or the desired transferred current can be obtained. Besides, based on the power-level or current-level modulation operation, these desired values can be directly realized by the DAB dc–dc converter, which is also suitable for other phase-shift modulation methods such as DPS modulation and TPS modulation.

In addition, the transferred current i_T of the DAB dc–dc converter can be calculated as

$$i_T = \frac{P_T}{U_o}. \tag{3}$$

Then, based on the SPS modulation method, the phase-shift ratio of the DAB dc–dc converter can also be calculated by the transferred current as

$$D = \begin{cases} \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2nLi_T}{U_{\text{in}}T_s}} & (i_T \geq 0) \\ -\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{2nLi_T}{U_{\text{in}}T_s}} & (i_T < 0). \end{cases} \tag{4}$$

TABLE I
CLASSIFICATIONS OF THE EXISTING DYNAMIC CONTROL SCHEMES FOR DAB CONVERTER

Categories	Existing Dynamic Control Methods
Parallel-Structure Control	1. The energy feedforward scheme [19]; 2. The feedforward control method [20]; 3. The inductance current control [22]; 4. The simplified feedforward control [23]; 5. The fast-dynamic control method with dc-offset current elimination [27];
Series-Structure Control	1. The virtual direct power control [24]; 2. The dynamic and static performance optimization method [25][26];

B. Parallel-Structure and Series-Structure Dynamic Control Schemes

To boost the dynamic response of the DAB dc–dc converter, there are some existing strategies such as load-current feedforward control method, inductance-current control method, and power-based control method [19]–[27]. According to the relationship between the compensation part and the model-based part, these existing methods can be divided into the parallel-structure group and the series-structure group. The parallel-structure control diagram and the series-structure control diagram can be presented as shown in Fig. 3.

As shown in Fig. 3, in the parallel-structure control, the compensation part is added with the model-based part for getting the outer-loop control value. By contrast, the compensation is multiplied with the model-based part for getting the outer-loop control value in the series-structure control. Generally, the model-based part is composed of measured input voltage and load current for dealing with the disturbances on input voltage and load condition. Besides, the compensation part is employed to compensate for the error caused by power losses and other uncertain factors between the model part and the actual converter system. Then, according to Fig. 3, the classification of the existing dynamic control schemes for boosting the dynamic performance of the DAB dc–dc converter can be shown in Table I.

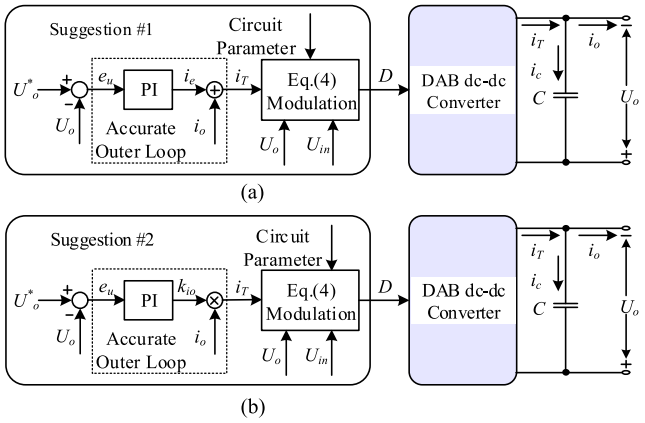

Fig. 4. Diagrams of the basic PSFDC and SSFDC methods. (a) PSFDC scheme. (b) SSFDC scheme.

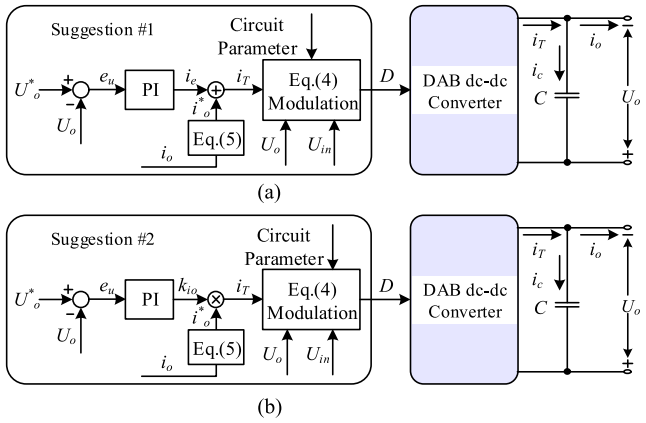

Fig. 5. Diagrams of the MPSFDC scheme and the MSSFDC scheme. (a) MPSFDC scheme. (b) MSSFDC scheme.

As shown in Fig. 2, when the required transferred current or transferred power is obtained, the DAB dc–dc converter can realize these values based on the inner current-level modulation or power-level modulation [2]. To boost the dynamic response when the load resistor is changed, the load current can be measured as the feedforward value for calculating the transferred current. Then, the excellent dynamic response can be got when the load condition changes. In addition, since the input voltage is used in the power-level or current-level modulation for calculating the phase-shift ratio as shown in (2) and (4), the disturbance of input voltage is contained, which can achieve fast dynamic performance under the change of input voltage. So, the existing virtual direct power control strategy [24] can provide an excellent dynamic response when the input voltage or load condition of the DAB dc–dc converter is changed, compared with other existing dynamic control methods [19]–[23]. Selecting the transferred current i_T as the middle value and combining (4) and Figs. 2 and 3, the parallel-structure fast-dynamic control (PSFDC) method and the series-structure fast-dynamic control (SSFDC) method can be shown in Fig. 4.

In Fig. 4, it is obvious that the load current i_o will bring positive feedback. Then, if the output voltage deviates from the desired value, the adopted load current will make the required transferred current i_T deviate its required value. Then, if the load current is switched to the actual steady-state load current $i^*{}_o$, the control system will be more stable, and the actual steady-state load current $i^*{}_o$ can be calculated as

$$i_o^* = \frac{U_o^*}{R} = \frac{U_o^* i_o}{U_o}. \tag{5}$$

Furthermore, by adding (5), the MPSFDC scheme and the MSSFDC scheme can be elaborated as shown in Fig. 5.

Then, based on the proposed MPSFDC method and the MSSFDC method in Fig. 5, the positive feedback impact caused by the load current is shown in Fig. 4, where the load current is adopted as the feedforward value directly, which can be eliminated. Moreover, the excellent dynamic control performance can be provided for the DAB dc–dc converter when the input voltage and the load condition are changed.

III. Disadvantages and Advantages of These Two Structures With Corresponding Compensation Methods

In this section, a comprehensive comparison between the MPSFDC scheme and the MSSFDC scheme is made, and the disadvantages of these two methods will be highlighted. Then, the corresponding compensation methods will be presented for omitting these disadvantages, which will ensure the excellent dynamic response of these proposed schemes.

A. Comparison of the Modified Parallel-Structure and Series-Structure Fast-Dynamic Strategies

According to (4) and Fig. 5, in the parallel-structure or series-structure methods, the circuit parameters including the transformer turn ratio n and the middle inductance L are employed to calculate the required phase-shift ratio. Therefore, the circuit-parameter dependence should be analyzed in case of the inaccurate circuit parameters, especially the inductance value. The inaccurate circuit parameters will influence the dynamic performance of these two schemes. Then, combining (4), (5), and Fig. 5, a middle variable $\mathrm{CP_{Test}}$ containing the circuit parameters and outer-loop control values are used as

$$\mathrm{CP_{Test}} = \begin{cases} 2nL(i_e + \frac{U_o^* i_o}{U_o}) & \text{(Parallel Structure)} \\ 2nL\frac{k_{io}U_o^* i_o}{U_o} & \text{(Series Structure).} \end{cases} \tag{6}$$

Assuming the adopted middle inductance is not accurate as L', L' can be expressed by the accurate middle inductance L as

$$L' = k_L L. \tag{7}$$

Then, when the steady-state condition is achieved, (6) can be expressed as

$$\mathrm{CP_{Test}} = \begin{cases} 2nL'(i'_e + \frac{U_o^* i_o}{U_o}) & \text{(Parallel Structure)} \\ 2nL'\frac{k'_{io}U_o^* i_o}{U_o} & \text{(Series Structure)} \end{cases} \tag{8}$$

where i'_e and k'_{io} are the corresponding compensation values under steady-state conditions. Combining (6), (7), and (8), the

compensation value in the MPSFDC method can be expressed as

$$i'_e = \frac{i_e + \frac{U_o^* i_o}{U_o}}{k_L} - \frac{U_o^* i_o}{U_o}. \tag{9}$$

Since i_e is close to zero with accurate circuit parameters, i'_e can be further expressed as

$$i'_e \approx \left(\frac{1}{k_L} - 1\right)\frac{U_o^* i_o}{U_o}. \tag{10}$$

When the load resistor is suddenly changed, the load current will be switched to $i_{o\mathrm{new}}$. Then, combining (7), (8), and (10), the middle variable $\mathrm{CP}_{\mathrm{TestP}}$ of the parallel-structure method with inaccurate middle inductance can be further expressed as

$$\mathrm{CP}_{\mathrm{TestP}} = 2nL[(1-k_L)\frac{U_o^* i_o}{U_o} + \frac{k_L U_o^* i_{o\mathrm{new}}}{U_o}]\,. \tag{11}$$

Moreover, since i_e is close to zero with accurate circuit parameters, the middle variable $\mathrm{CP}_{\mathrm{TestP}}$ of the parallel-structure method with accurate middle inductance can be further expressed as

$$\mathrm{CP}_{\mathrm{TestP}} = 2nL\frac{U_o^* i_{o\mathrm{new}}}{U_o}. \tag{12}$$

Combining (11) and (12), the error E_{CPTestP} of the middle variable of the parallel-structure method with changed load resistor can be calculated as

$$E_{\mathrm{CPTestP}} = 2nL(1-k_L)\frac{U_o^*(i_{o\mathrm{new}} - i_o)}{U_o}. \tag{13}$$

According to (13), when the middle inductance value is not accurate, there is always an error of the middle variable E_{CPTestP} with the MPSFDC method when the load resistor is changed, and the accurate required middle variable cannot be obtained immediately. Then, the PI controller must compensate for this error, and the dynamic performance of the MPSFDC scheme will be affected. Thus, the dynamic performance of the MPSFDC strategy is sensitive to the circuit parameter including the middle inductance and the transformer turn ratio.

Similarly, combining (6), (7), and (8), the compensation value in the MSSFDC method can be expressed as

$$k'_{io} = \frac{k_{io}}{k_L}. \tag{14}$$

When the load resistor is suddenly changed, the load current will be switched to $i_{o\mathrm{new}}$. Then, combining (7), (8), and (14), the middle variable $\mathrm{CP}_{\mathrm{TestS}}$ of the series-structure method with inaccurate middle inductance can be further expressed as

$$\mathrm{CP}_{\mathrm{TestS}} = 2nL'\frac{k'_{io} U_o^* i_o}{U_o} = 2nL\frac{k_{io} U_o^* i_o}{U_o}\,. \tag{15}$$

Comparing (6) with (15), based on the MSSFDC scheme, the dynamic response is not sensitive to the circuit parameters including the transformer turn ratio and the middle inductance. The PI controller will provide a proportional compensation for eliminating the influence caused by the inaccurate circuit parameter as shown in (14). Moreover, even though there is a slow variation of inductance value caused by varying temperatures, the corresponding compensation can also be provided by the PI control timely.

TABLE II
ADVANTAGES AND DISADVANTAGES OF THE MODIFIED PARALLEL-STRUCTURE AND THE MODIFIED SERIES-STRUCTURE FAST-DYNAMIC STRATEGIES

Strategy	Advantage	Disadvantage
Modified parallel-structure fast-dynamic control method	The loop gain of PI controller independent with load conditions.	Sensitive to the circuit parameters.
Modified series-structure fast-dynamic control method	Immune to the circuit parameters.	The loop gain of PI controller dependent with load conditions.

In addition, in the MSSFDC scheme, the load-current value will affect the gain of the PI controller since the output value k_i of the PI controller is multiplied with the feedforward value of load current i_o, and the required transferred current i_T can be calculated by the voltage error e_u as

$$i_T = (k_i i_o e_u + k_p i_o(e_u - e_{\mathrm{ulast}}) + k_{\mathrm{iolast}} i_o)\frac{U_o^*}{U_o} \tag{16}$$

where e_{ulast} is the voltage error in the last switching period and k_{iolast} is the compensation value in the last switching period. According to (16), when the DAB dc–dc converter is at light-load condition, the load current will be very small, which will affect the loop gain. Then, with a small loop gain at light-load condition, the amplification of the output error of the PI controller will be affected, which may influence the dynamic performance of the modified fast-dynamic control scheme at light-load condition. Moreover, under the MPSFDC scheme, the required transferred current i_T can be calculated by the voltage error e_u as

$$i_T = k_i e_u + k_p(e_u - e_{\mathrm{ulast}}) + i_{\mathrm{elast}} + \frac{i_o U_o^*}{U_o} \tag{17}$$

where i_{elast} is the last compensation value in the last switching period under the MPSFDC scheme. According to (17), the load condition will not influence the gain of the PI controller for reflecting the voltage error.

Based on the former analysis, the advantages and disadvantages of these two control structures can be concluded in Table II.

B. Corresponding Compensating Methods for Omitting the Disadvantages

According to the analysis in the former part, the MPSFDC scheme is sensitive to the circuit parameters, and the loop gain of the MSSFDC strategy is influenced by the load condition. Thus, the corresponding compensating methods will be presented for eliminating these drawbacks.

For the DAB dc–dc converter, the circuit parameter can be easily obtained since the relationship among input voltage, output voltage, load current, and phase-shift ratio is strictly determined

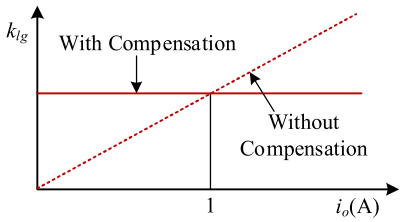

Fig. 6. Diagram of the control loop gains of the MSSFDC method with or without compensation.

by (1). Then, when the steady-state condition is obtained, the approximate inductance L_E of DAB dc–dc converter can be obtained as [31]

$$L_E = \frac{U_{\rm in}D'(1-D')T_s}{2ni_o}. \tag{18}$$

According to (18), the middle inductance L_E of the DAB dc–dc converter can be estimated, which can ensure the dynamic performance of the MPSFDC scheme. Moreover, in order to improve the stable loop gain for the modified series-structure fast-dynamic method, the PI parameters of the controller should be expressed as

$$\begin{cases} k_{\rm im} = \frac{k_i}{i_o} \\ k_{\rm pm} = \frac{k_p}{i_o} \end{cases} \tag{19}$$

where $k_{\rm im}$ and $k_{\rm pm}$ are the modified PI parameters. Then, combining (16) and (19), the transferred current based on the modified series-structure fast-dynamic method can be further expressed as

$$i_T = (k_i e_u + k_p i_o(e_u - e_{\rm ulast}) + k_{\rm ilast} i_o)\frac{U_o^*}{U_o}. \tag{20}$$

According to (20), the control loop gain $k_{\rm lg}$ for the voltage error of the MSSFDC scheme can be shown in Fig. 6.

In Fig. 6, $k_{\rm lg}$ can be expressed as

$$k_{\rm lg} = \begin{cases} k_i\frac{U_o^*}{U_o} \text{ or } k_p\frac{U_o^*}{U_o} & (\text{with compensation}) \\ k_i\frac{i_o U_o^*}{U_o} \text{ or } k_p\frac{i_o U_o^*}{U_o} & (\text{without compensation}). \end{cases} \tag{21}$$

Therefore, with compensation, the control loop gain of the MSSFDC method can be stable, which may ensure the dynamic performance at the light-load condition.

IV. Design Principle of the PI Parameters and the Control-Delay Compensation Method

In this section, based on the SPS modulation method, the design principle of the PI controller in the MPSFDC scheme and the MSSFDC scheme is presented, which can also be employed in another fast-dynamic control method with the feedforward operation. Then, the control delay compensation is discussed, which can be employed to reduce the potential output-voltage disturbance.

A. Design Principles of the PI Parameters for the Proposed Fast-Dynamic Control Schemes

Since the DAB dc–dc converter can be treated as the first-order model with capacitive characteristics, the phase margin is always bigger than 45°. So, the DAB dc–dc converter with the PI-based control system will be always convergent, and then it is not easy to design the PI parameter directly [32]. In the MPSFDC method and the MSSFDC method, the PI controller is employed to compensate the error between the adopted model and the actual converter system, and the dynamic response is mainly dependent on the feedforward operation. Moreover, since the phase-shift ratio and the transferred power or current of the DAB dc–dc converter is a one-to-one correspondence, the output voltage can be easily maintained at its desired value when the input voltage and the load condition are changed. So, even with higher PI parameters, the output voltage can keep at its desired value with the output capacitor [28]. However, although the oscillation of the output voltage can be easily avoided with the output capacitor, there may be obvious disturbances in the phase-shift ratio with measurement noise. Thus, the disturbances ΔD_α of the phase-shift ratio caused by the measurement noises should be treated as a criterion to evaluate the stability of the DAB dc–dc converter. Assuming the rated transferred current is $i_{\rm TR}$, and according to (4) and Fig. 5(a), the phase-shift ratio disturbance ΔD_p of the MPSFDC scheme can be expressed as

$$\begin{aligned} \Delta D_p \approx & \sqrt{\tfrac{1}{4} - \tfrac{2nLi_{\rm TR}}{U_{\rm in}T_s}} \\ & - \sqrt{\tfrac{1}{4} - \tfrac{2nL[i_{\rm TR}+(k_i+k_p)U_{\rm omn}]}{U_{\rm in}T_s}} \end{aligned} \tag{22}$$

where $U_{\rm omn}$ is the measurement noise of output voltage. Ignoring the higher minimum term in (22), k_i and k_p can be expressed by the limitation of phase-shift ratio disturbance $\Delta D_{p\min}$ as

$$(k_i + k_p) \le \frac{\Delta D_{p\min}U_{\rm in}T_s}{nLU_{\rm omn}}\sqrt{\frac{1}{4} - \frac{2nLi_{\rm TR}}{U_{\rm in}T_s}}. \tag{23}$$

Then, based on the proposed MPSFDC method, the requirement of the integral parameter k_i is limited, and the relatively large proportional parameter k_p can be employed to compensate the control delay. So, k_i can be designed as the tenth of k_p, and (23) can be further expressed as

$$\begin{cases} k_p \le \left|\frac{\Delta D_{p\min}U_{\rm in}T_s}{nLU_{\rm omn}}\sqrt{\frac{1}{4} - \frac{2nLi_{\rm TR}}{U_{\rm in}T_s}}\right| \\ k_i \le \left|\frac{\Delta D_{p\min}U_{\rm in}T_s}{10nLU_{\rm omn}}\sqrt{\frac{1}{4} - \frac{2nLi_{\rm TR}}{U_{\rm in}T_s}}\right| \end{cases}. \tag{24}$$

Similarly, according to (4) and Fig. 5(b), the phase-shift ratio disturbance ΔD_s of the MSSFDC scheme can be expressed as

$$\begin{aligned} \Delta D_s \approx & \sqrt{\tfrac{1}{4} - \tfrac{2nLi_{\rm TR}}{U_{\rm in}T_s}} \\ & - \sqrt{\tfrac{1}{4} - \tfrac{2nL[i_{\rm TR}+(k_i+k_p)i_{\rm TR}U_{\rm omn}]}{U_{\rm in}T_s}}. \end{aligned} \tag{25}$$

Ignoring the higher minimum term in (25), k_i and k_p can be expressed by the limitation of phase-shift ratio disturbance $\Delta D_{p\min}$ as

$$(k_i + k_p) \le \frac{\Delta D_{s\min}U_{\rm in}T_s}{nLi_{\rm TR}U_{\rm omn}}\sqrt{\frac{1}{4} - \frac{2nLi_{\rm TR}}{U_{\rm in}T_s}}. \tag{26}$$

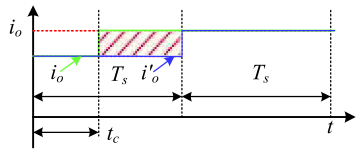

Fig. 7. Control delay when the load resistor is changed.

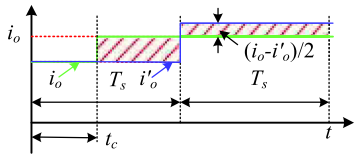

Fig. 8. Compensation method when the load resistor is changed.

Then, based on the proposed MSSFDC method, the requirement of the integral parameter k_i is limited, and the relatively large proportional parameter k_p can be employed to compensate the control delay. So, k_i can be designed as tenth of k_p, and (26) can be further expressed as

$$\begin{cases} k_p \le \left| \frac{\Delta D_{p\min} U_{\text{in}} T_s}{n L i_{\text{TR}} U_{\text{omn}}} \sqrt{\frac{1}{4} - \frac{2nLi_{\text{TR}}}{U_{\text{in}} T_s}} \right| \\ k_i \le \left| \frac{\Delta D_{p\min} U_{\text{in}} T_s}{10 n L i_{\text{TR}} U_{\text{omn}}} \sqrt{\frac{1}{4} - \frac{2nLi_{\text{TR}}}{U_{\text{in}} T_s}} \right| \end{cases}. \tag{27}$$

B. Compensation Method for the Control Delay of These Two Modified Fast-Dynamic Strategies

Based on the proposed two modified fast-dynamic strategies, when the load resistor is changed, the corresponding required transferred current of the DAB dc–dc converter can be obtained immediately. However, there will always be an uncertain delay in the controller because the changing point of the load resistor in the switching period cannot be determined, as shown in Fig. 7.

As shown in Fig. 7, i_o is the actual load current, and i'_o is the transferred current of the DAB dc–dc converter under these two modified fast-dynamic strategies. Obviously, from t_c to T_s, the transferred current cannot meet the requirement of the load current, and the additional current will be provided by the output-side capacitor. Then, the change of the output-side voltage ΔU_o can be expressed as

$$\Delta U_o = \frac{(i_o - i'_o)(T_s - t_c)}{C_o} \Delta U_o \in [0, \frac{(i_o - i'_o) T_s}{C_o}]. \tag{28}$$

According to (28), when the load resistor is changed, the maximum disturbance of output voltage with control delay is $(i_o - i'_o)T_s/C_o$. Then, this disturbance of output voltage should be compensated by the PI controller in the control system. In some existing model predictive control schemes, the charging model of the output-side capacitor is adopted to correct the output voltage directly, which always results in instability with measurement noise. In addition, although this output-voltage disturbance caused by the control delay is uncertain, a compensation as $(i_o - i'_o)T_s/(2C_o)$ in the next switching period can reduce the burden of the PI controller, which can reduce the settling time to some degree. Then, with the compensation operation, the actual transferred current in the next switching period can be shown in Fig. 8.

Then, as shown in Fig. 8, the disturbance of output voltage compensated by the PI controller can be expressed as

TABLE III
CIRCUIT PARAMETERS OF THE DAB DC–DC CONVERTER SYSTEM

Switches (Experiment platform)	ROHM SCT3080KL
L	40 μH
n	1
f_s	40 kHz
R	20 Ω ~ 1000 Ω
U_{in}	60 V ~ 80 V
U^*_o	60V
k_p	0.05
k_i	0.005
C_o	550μF
Max Counter Number in Simulation	500
Max Counter Number in Experiment	2500
U_{omn} in Simulation	0.5 V (White Noise)
R_{on} of Switches in Simulation	50 mΩ

$$\Delta U_o = \frac{(i_o - i'_o)(\frac{T_s}{2} - t_c)}{C_o} \Delta U_o \in \left[-\frac{(i_o - i'_o) T_s}{2C_o}, \frac{(i_o - i'_o) T_s}{2C_o} \right]. \tag{29}$$

Comparing (28) with (29), the maximum value of the potential output-voltage disturbance can be reduced by half.

V. VERIFICATION

In this section, based on the simulation results and the experiment results, the MPSFDC scheme and the MSSFDC scheme are verified. The simulation model is obtained based on MATLAB/Simulink, and a small-scale experiment platform is constructed based on dSPACE controller and the DAB prototype. The circuit parameters in both the simulation model and the experimental platform are listed in Table III.

A. Simulation Result

Different from the traditional dc–dc converters such as buck converters and boost converters, the phase-shift ratio, and the transferred power, is a one-to-one correspondence. As shown in the proposed modified fast-dynamic control scheme, the output voltage is not much sensitive to the PI parameters with suitable feedback control. To further verify this, the simulation is operated with $k_p = 5$ and $k_i = 0.5$, which are 100 times the adopted PI parameters under normal conditions. When the load resistor is changed between 50 and 1000 Ω, the simulation result under the MSSFDC scheme can be shown in Fig. 9. Based on Fig. 9(c), the output voltage with some disturbances can keep at its desired value when the R is switched between 50 and

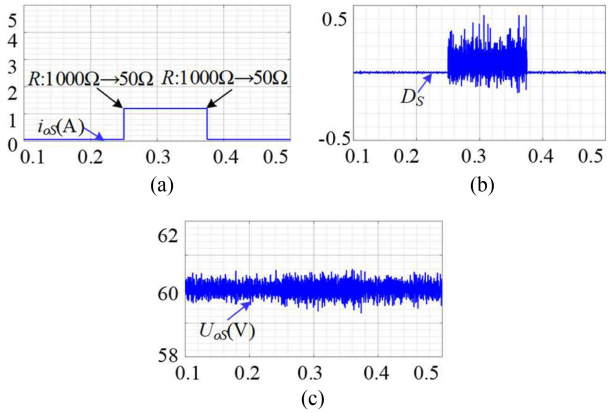

Fig. 9. Simulation result under the MSSFDC scheme with high PI parameters. (a) Load current. (b) Phase-shift ratio. (c) Output voltage.

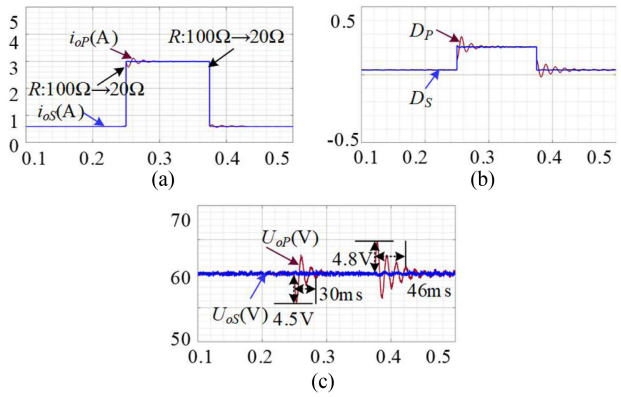

Fig. 10. Simulation result when the load resistor is changed under the proposed fast-dynamic control schemes with inaccurate inductance value. (a) Load current. (b) Phase-shift ratio. (c) Output voltage.

1000 Ω. But the disturbances of the phase-shift ratio are obvious as shown in Fig. 9(b). Therefore, it is better to design the PI parameters in the modified fast-dynamic control schemes based on the disturbance of the phase-shift ratio.

Then, when the adopted inductance L is 20 μH in the controller under the MPSFDC scheme and the MSSFDC scheme, the simulation results with variable load resistor and input voltage can be shown in Figs. 10 and 11, respectively. According to Fig. 10(c), the output voltage U_{oP} under the MPSFDC scheme has some disturbances up to 4.8 V with inaccurate inductance value, while the output voltage U_{oS} under the MSSFDC scheme can keep at its desired value. Therefore, the MSSFDC scheme is not sensitive to the inductance value, and the excellent dynamic performance can be maintained even with the wrong inductance value in the controller. Moreover, when the input voltages are changed, the output voltage under the MPSFDC scheme and the MSSFDC scheme can both keep at their desired values. Thus, even with an inaccurate inductance value, the MSSFDC method can provide excellent dynamic performance.

According to (18), the inductance can be estimated. The corresponding simulation result can be shown in Fig. 12, in which the estimated inductance is about 41 μH. Then, the dynamic

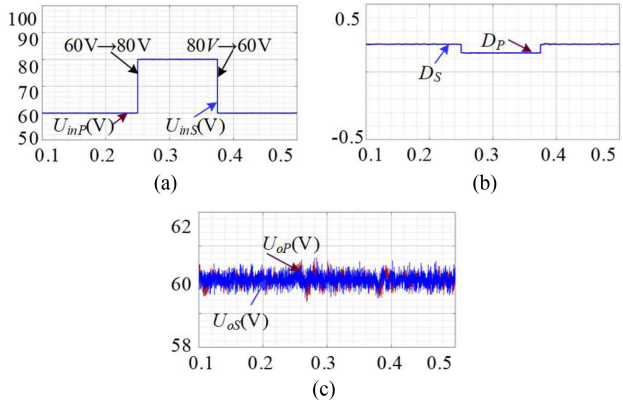

Fig. 11. Simulation result when the input voltage is changed under the proposed fast-dynamic control schemes with inaccurate inductance value. (a) Input voltage. (b) Phase-shift ratio. (c) Output voltage.

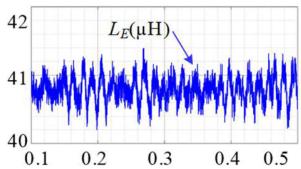

Fig. 12. Simulation result of the estimated middle inductance L_E.

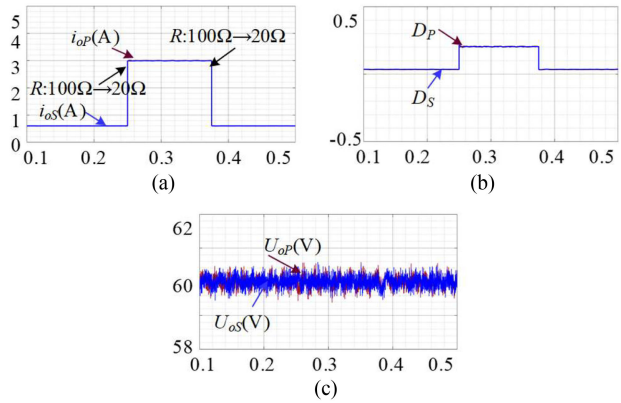

Fig. 13. Simulation result when the load resistor‘ is changed under the proposed fast-dynamic control schemes with accurate inductance value. (a) Load current. (b) Phase-shift ratio. (c) Output voltage.

performance of the MPSFDC scheme can be ensured. Usually, the inductance should be estimated at high-power conditions since the efficiency can be relatively high. Then, the estimated inductance value will be more accurate.

Moreover, under the MPSFDC scheme and the MSSFDC scheme with an accurate inductance value of 40 μH, the simulation results with a changed load resistor and input voltage can be shown in Figs. 13 and 14, respectively. According to Figs. 13(c) and 14(c), when the load resistor and input voltage are changed, the output voltages of these two modified fast-dynamic control schemes with different structures can both keep at their desired value, and the excellent dynamic performances can be obtained.

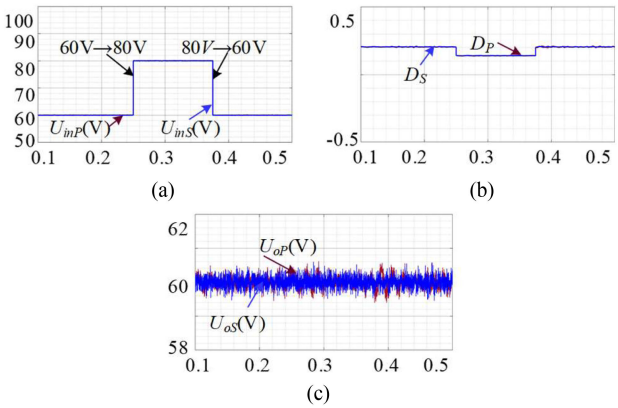

Fig. 14. Simulation result when the input voltage is changed under the proposed fast-dynamic control schemes with accurate inductance value. (a) Input voltage. (b) Phase-shift ratio. (c) Output voltage.

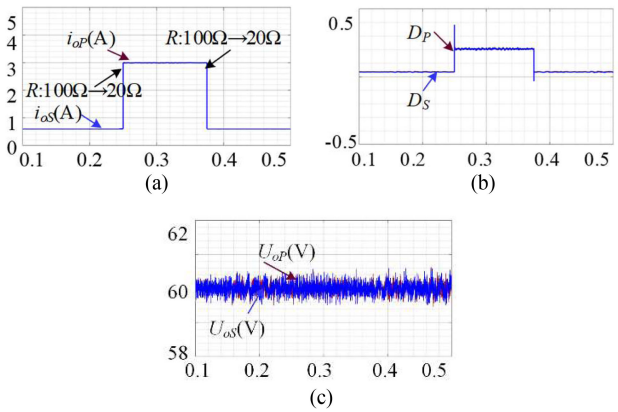

Fig. 15. Simulation result when the load resistor is changed under the proposed fast-dynamic control schemes with delay compensation. (a) Load current. (b) Phase-shift ratio. (c) Output voltage.

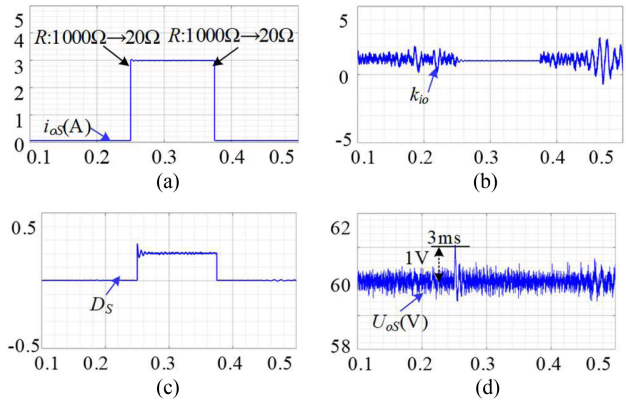

Fig. 16. Simulation result when the load resistor is changed under the proposed series-structure fast-dynamic control scheme with constant loop gain. (a) Load current. (b) Compensation value. (c) Phase-shift ratio. (d) Output voltage.

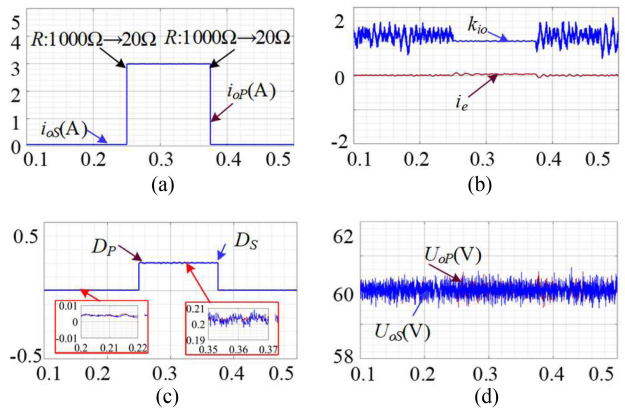

Fig. 17. Simulation result when the load resistor is changed under the proposed series-structure fast-dynamic control scheme with constant loop gain. (a) Load current. (b) Compensation value. (c) Phase-shift ratio. (d) Output voltage.

With the delay compensation operation elaborated in Section IV-B, the simulation results under the MPSFDC scheme and the MSSFDC scheme with changed load resistor can be shown in Fig. 15. According to Fig. 15(c), when the load resistor is changed, the output voltages of these two modified fast-dynamic control schemes with different structures can both keep at their desired value. In addition, excellent dynamic performances can be obtained, which is like the simulation result under these two proposed fast-dynamic control schemes without compensation operation as shown in Fig. 13(c).

In addition, since the compensation value is multiplied by the load current, the loop gain of the MSSFDC scheme will be affected. The loop gain will be very small especially at light-load conditions, which may influence the dynamic performance of the DAB dc–dc converter. So, a compensation method is proposed in Section III-B. Then, the simulation result under the MSSFDC scheme with constant loop gain can be shown in Fig. 16. According to Fig. 16(d), the output-voltage disturbance when the resistor is changed from 1000 to 20 Ω is about 1 V, the settling time is about 3 ms, and the dynamic performance is damaged. As shown in Fig. 16(a), when the load resistor is 1000 Ω, the disturbance of the compensation value k_{io} is obvious with higher PI parameters. Then, when the load resistor is changed, the calculated phase-shift ratio as shown in Fig. 16(b) will be random at the first switching period, which will deviate from its new steady-state value. So, the obvious output-voltage disturbance is created.

Furthermore, after the multiplication of k_{io} and $i_{\rm set}$ at extremely light load, the required transferred current i_T is very small; so the influence on the output voltage is limited with the output capacitor. Therefore, the compensation value k_{io} at relatively high power and high efficiency can be stored for resetting this compensation value when the load resistor is changed. Based on this operation, the output-voltage disturbance under the MSSFDC scheme with constant loop gain can be eliminated when the load condition is changed from extremely light load to high load, and the influence on the output-voltage disturbance when the load is changed from high load to extremely light load can be omitted with the output capacitor. Then, the simulation result under the MSSFDC scheme with constant loop gain and the MPSFDC strategy with estimated inductance can be shown in Fig. 17. As shown in Fig. 17(d), the output voltage under these

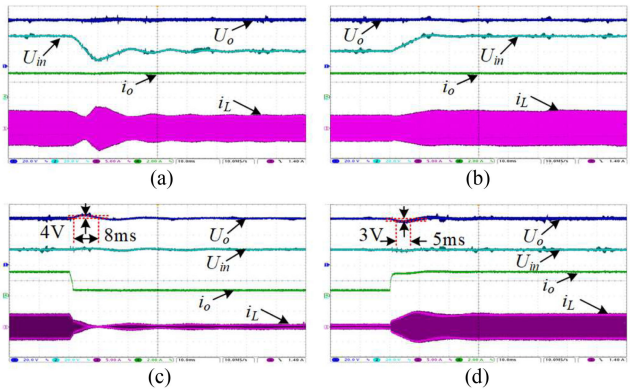

Fig. 18. Experimental result under the MPSFDC scheme with inaccurate inductance value ($U_{\rm in}$ and U_o: 20 V/div; i_o: 2 A/div; i_L: 5 A/div; t: 10 ms/div). (a) $U_{\rm in}$: 80–60 V. (b) $U_{\rm in}$: 60–80 V. (c) R: 20–100 Ω. (d) R: 100–20 Ω.

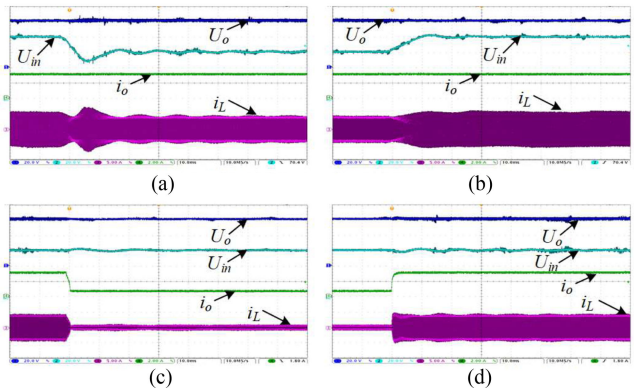

Fig. 19. Experimental result under the MSSFDC scheme with inaccurate inductance value ($U_{\rm in}$ and U_o: 20 V/div; i_o: 2 A/div; i_L: 5 A/div; t: 10 ms /div). (a) $U_{\rm in}$: 80–60 V. (b) $U_{\rm in}$: 60–80 V. (c) R: 20–100 Ω. (d) R: 100–20 Ω.

two schemes can both keep at its desired value when the load resistor is changed between 20 and 1000 Ω.

B. Experimental Result

When the adopted inductance L is 20 μH in the controller under both proposed fast-dynamic control schemes, the experiment results when the load resistor and the input voltage are changed can be shown in Figs. 18 and 19, respectively. As shown in Figs. 18(a) and (b) and 19(a) and (b), when the input voltage is changed between 60 and 80 V, the disturbances of the output voltage under the MPSFDC scheme and the MSSFDC scheme can be omitted. Benefitting from this phenomenon, the excellent dynamic performance under these two fast-dynamic control schemes can both be obtained. Moreover, when the load resistor is switched between 20 and 100 Ω, the output voltage under the MSSFDC scheme can keep at its desired value as shown in Fig. 19(c) and (d) even with inaccurate inductance value in the controller. In contrast, the output voltage disturbances under the PSFDC scheme are obvious up to 4 V. The experimental results are consistent with the simulation results as shown in Fig. 10. Therefore, the inductance estimation operation is required for ensuring the dynamic response of the MPSFDC scheme.

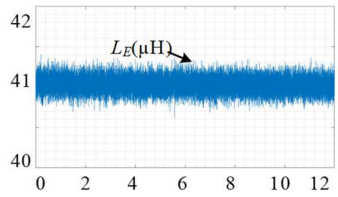

Fig. 20. Experimental result of the estimated inductance value.

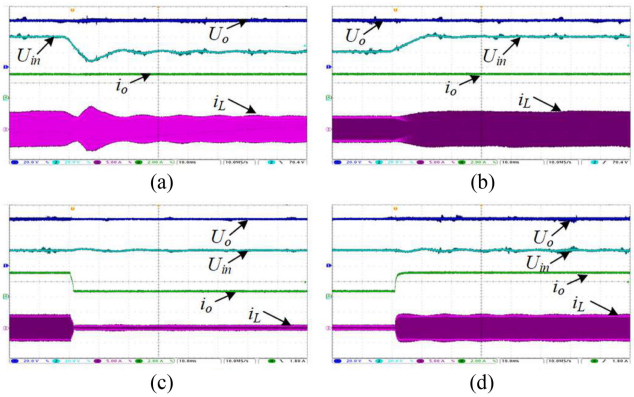

Fig. 21. Experimental result under the MPSFDC scheme with estimated inductance value ($U_{\rm in}$ and U_o: 20 V/div; i_o: 2 A/div; i_L: 5 A/div; t: 10 ms/div). (a) $U_{\rm in}$: 80–60 V. (b) $U_{\rm in}$: 60–80 V. (c) R: 20–100 Ω. (d) R: 100–20 Ω.

According to (18), the inductance can be estimated. The corresponding experimental result can be shown in Fig. 20, where the estimated inductance is about 41 μH. Usually, the inductance should be estimated at high-power conditions since the efficiency can be relatively high, and the estimated inductance value will be more accurate. Then, based on the estimated inductance, the corresponding experimental result of the MPSFDC scheme can be shown in Fig. 21, where the output voltage can keep at its desired value when the input voltage and the load resistor are changed.

Moreover, with the MPSFDC scheme and the MSSFDC scheme based on the accurate inductance value of 40 μH, the experiment results with a changed load resistor and input voltage can be shown in Figs. 22 and 23, respectively. So, when the load resistor and input voltage are changed, the output voltage of these two modified fast-dynamic control schemes with different structures can both keep at their desired value with accurate inductance value, and excellent dynamic performances can be obtained.

With the delay compensation operation in Section IV-B, the experiment results under the MPSFDC scheme and the MSSFDC scheme with changed load resistor can be shown in Figs. 24 and 25. Therefore, when the load is changed, the output voltage with both control schemes with delay compensation operation can keep at their desired value. Hence, the excellent dynamic performances can be obtained, which is similar to the dynamic performance as shown in Figs. 22 and 23.

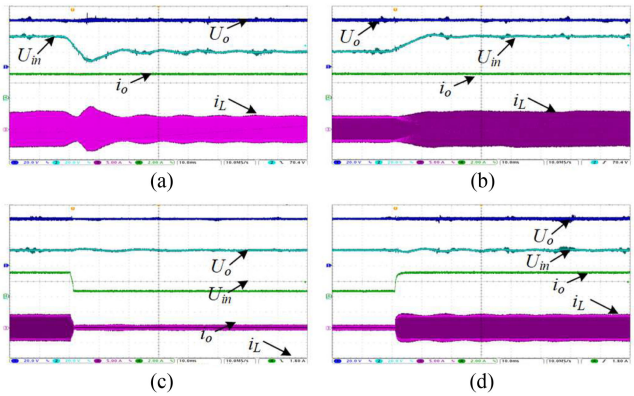

Fig. 22. Experimental result under the MPSFDC scheme with accurate inductance value ($U_{\rm in}$ and U_o: 20 V/div; i_o: 2 A/div; i_L: 5 A/div; t: 10 ms/div). (a) $U_{\rm in}$: 80–60 V. (b) $U_{\rm in}$: 60–80 V. (c) R: 20–100 Ω. (d) R: 100–20 Ω.

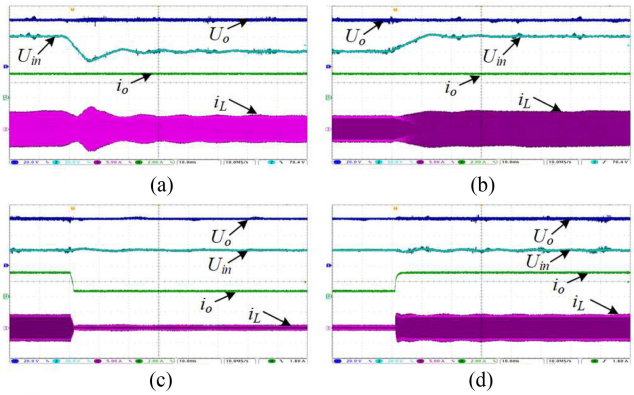

Fig. 23. Experimental result under the MSSFDC scheme with accurate inductance value ($U_{\rm in}$ and U_o: 20 V/div; i_o: 2 A/div; i_L: 5 A/div; t: 10 ms/div). (a) $U_{\rm in}$: 80–60 V. (b) $U_{\rm in}$: 60–80 V. (c) R: 20–100 Ω. (d) R: 100–20 Ω.

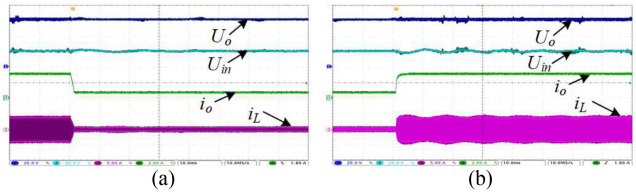

Fig. 24. Experimental result under the MPSFDC scheme with delay compensation ($U_{\rm in}$ and U_o: 20 V/div; i_o: 2 A/div; i_L: 5 A/div; t: 10 ms/div). (a) R: 20–100 Ω. (b) R: 100–20 Ω.

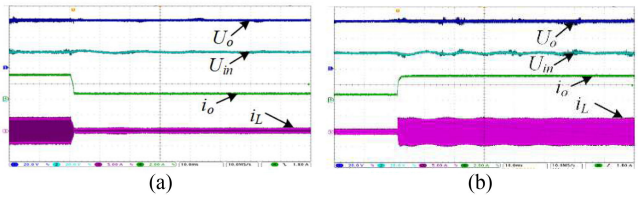

Fig. 25. Experimental result under the MSSFDC scheme with delay compensation ($U_{\rm in}$ and U_o: 20 V/div; i_o: 2 A/div; i_L: 5 A/div; t: 10 ms/div). (a) R: 20–100 Ω. (b) R: 100–20 Ω.

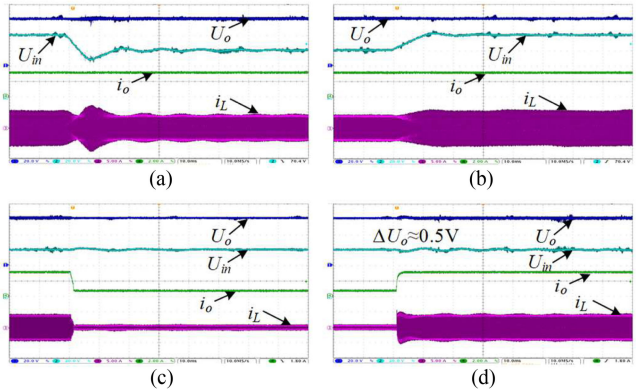

Fig. 26. Experimental result under the MSSFDC scheme with constant loop gain ($U_{\rm in}$ and U_o: 20 V/div; i_o: 2 A/div; i_L: 5 A/div; t: 10 ms/div). (a) $U_{\rm in}$: 80–60 V. (b) $U_{\rm in}$: 60–80 V. (c) R: 20–100 Ω. (d) R: 100–20 Ω.

In addition, based on (19) and (21), the loop gain of the MSSFDC scheme can be constant, and the corresponding experiment result can be shown in Fig. 26, where the output voltage can keep at its desired value with a changed load resistor and input voltage. It is worth mentioning that the dynamic performance is different from the simulation result as shown in Fig. 16, and the reason should be that 100 Ω is not the extreme light-load condition as 1000 Ω in the simulation part. Therefore, with the measurement noise, the PI parameter cannot influence the dynamic performance obviously.

VI. Conclusion

In this article, the existing model-based control schemes for boosting the dynamic performance of the DAB dc–dc converter are reviewed and classified. Based on the relationship between the compensation part and the model-based part, these existing model-based control methods can be divided into two groups including the parallel-structure control group and the series-structure control group. Then, the advantage and disadvantages of these two groups are analyzed, and the corresponding compensation methods are also presented. Moreover, based on these two basic control structures, the MPSFDC scheme and the MSSFDC scheme are proposed. Then, based on these two proposed schemes, the general PI design principle is presented, and a delay compensation method is also presented for reducing the control-delay impact to some degree. Based on simulation and experimental verifications of the proposed strategy, the conducted studies in this article can lead to the following conclusions.

1) In the model-based control schemes for DAB dc-dc converter, the design principle of the PI controller is different from the traditional concept, and the phase-shift ratio disturbance should be acted as the criterion for designing the PI parameters.
2) The MPSFDC scheme and the MSSFDC scheme can both provide excellent dynamic performance for DAB

dc-dc converter with changed input voltage and load current. However, the dynamic performance of the parallel-structure one is sensitive to the circuit-parameter error. So, it is better to adopt the series structure for ensuring the fast-dynamic performance of the DAB converter.

3) Since the compensation part is multiplied by the desired load current in the MSSFDC scheme, the control loop gain is changed along with the load current. Then, at light-load conditions, the regulation function of the PI controller will be weak, which cannot influence the dynamic response at light-load conditions. Moreover, the weak regulation function of the PI controller can reduce the influence caused by the measurement noise at the extreme light-load condition.
4) Although the presented control-delay compensation method can reduce the disturbance of output voltage theoretically, the optimizing performance is limited. The main factor that influences the further improvement of dynamic performance of the DAB dc-dc converter should be the power loss and other uncertain factors, such as the linearity of the measurement circuit and the dead time of modulation signals.

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