# Temperature-Dependent Reverse Recovery Characterization of SiC MOSFETs Body Diode for Switching Loss Estimation in a Half-Bridge

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***Abstract*—In a hard switched MOSFET based converter, turn-ON energy losses is predominant in the total switching loss. At higher junction temperature the turn-ON energy loss further increases due to the reverse recovery effect of the complementary MOSFETs body diode in a half-bridge configuration. Estimation of the switching loss under different operating conditions at an early design stage is essential for optimizing the thermal design. Analytical switching loss models available in literature are generally used for estimating the switching losses due to its accuracy and simplicity. In this article, the inaccuracy in the reported loss models due to non-inclusion of temperature-dependent reverse recovery characteristics of body diode, is investigated. A structured method to determine the temperature-dependent switching loss of a SiC MOSFET in a half-bridge is presented. A simple methodology has been proposed to analyze the carrier lifetime's temperature dependencies of a SiC MOSFETs body diode. Device parameters from a 1.2 kV/36 A SiC MOSFETs datasheet are used for developing the loss model and experimental validation of the model.**

***Index Terms*—Double pulse test (DPT), half-bridge, reverse recovery, SiC MOSFET, switching loss, temperature.**

## I. Introduction

SILICON carbide (SiC) MOSFETs have increasingly become popular as a replacement for silicon (Si) based insulated gate bipolar transistors due to its superior physical and electrical characteristics [1], [2]. Despite the improved performance, switching, and conduction losses are the major loss contributor in a power semiconductor device. The efficiency of power conversion further reduces at high ambient temperature, as the junction temperature ($T_j$) increases with the increment of heatsink temperature ($T_{\text{hs}}$), which is common in automotive and grid-connected converters. The maximum ambient temperature in such applications typically ranges from 40 to 50 °C for grid-connected converters and 85 to 100 °C for automotive-grade converters. Therefore, the accurate estimation of semiconductor losses in such high-temperature environment is essential for evaluating the efficiency and optimizing the cooling system for overall power density improvement. This article's primary focus is to model and accurately estimate the temperature-dependent switching losses of SiC MOSFETs in a half-bridge, which is the most commonly used building block for dc–dc/dc–ac converters.

In the overall loss of a converter, the conduction loss can be calculated using the temperature-dependent parameter ($R_{\text{DS}}$), available in the datasheet. To accurately estimate the switching losses, different approaches are described in the literature [3]. Among these, the most commonly used methods are physics-based models, numerical models, behavioral model, and analytical models. In physics-based models, physical device data for SPICE modeling and field expertise are necessary [4], [5]. Although physical models are accurate enough, it is hindered by the fact that many of its physical parameters are not present in the manufacturer datasheet. In numerical models, simulation tools like SILVACO and TCAD are being used. These simulation tools provide very accurate results, but these tools require material properties, device geometry, and are very computationally intensive [6]. Behavioral models are the simplest model, and its solution is dependent on a couple of nonlinear equations, which are based on curve fitting parameters [7], [8]. In analytical models, device characteristics are divided into different segments, and governing equations are being derived and parameterized based on datasheet parameters [9]–[11]. In this article, the model presented is a combination of both behavioral and analytical model.

The main problem in estimating the switching losses comes from modeling the nonlinear parasitic capacitances and the temperature-dependent reverse recovery loss ($E_{\text{rr}}$) of MOSFETs. Efforts have been made in [11] and [12] to consider the nonlinearity of the junction capacitance either by two-point or multipoint approximation through curve fitting approach. Furthermore, a voltage-dependent capacitor model is derived in [10] and [13], and a charge equivalent capacitance model is given in [9] to reduce the models' complexity. Switching performance analysis for different MOSFET technologies at different temperature has been given in [14]; however, an analytical model for estimating the MOSFET switching energy loss is not presented. The $E_{\text{rr}}$ has a substantial loss contribution in the turn-ON energy losses ($E_{\text{on}}$) from the total energy loss ($E_{\text{tot}}$) of an SiC MOSFET. As the $T_j$ increases, due to the temperature-dependent charge carrier lifetime of the body diode, $E_{\text{rr}}$ increases, which in turn increases

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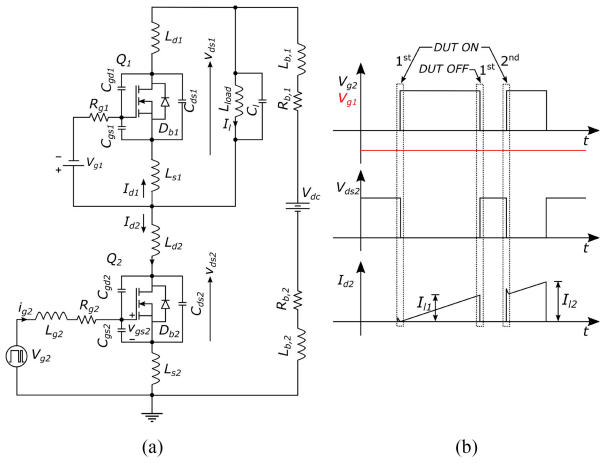


Fig. 1. (a) DPT circuit with circuit parasitics. (b) Switching waveforms in DPT.

$E_{\text{on}}$, whereas the turn-OFF energy loss ($E_{\text{off}}$) remains constant. Hence, in this article, estimation of $E_{\text{on}}$ has been emphasized more. Although many analytical models are present in the literature, the effect of $T_j$ on $E_{\text{rr}}$ is not taken into account for calculating $E_{\text{on}}$ of the MOSFETs. So, at higher $T_j$, the above-mentioned analytical techniques from the literature become erroneous. In this regard, this article makes the following contributions.

1) The temperature dependent time constants of the body diode has been considered for developing the analytical model for estimating $E_{\text{on}}$.
2) The parameter extraction routine for the body diode time constants has been described.
3) The impact of parasitic capacitance on the reverse recovery process of the body diode has been discussed.

The rest of this article is organized as follows. Section II describes the model parameters used, and Section III describes the switching segments during turn-ON with the effect of temperature on reverse recovery of the SiC MOSFETs body-diode. Section IV describes the experimental set-up and discusses experimental and analytical results. Finally, Section V concludes this article.

## II. Model Parameters

In the conventional MOSFETs loss estimation technique, a closed-form solution with a linear approximation of voltage and current is given for easy calculation [15]–[17]. However, this method does not consider the effect of circuit parasitics and temperature, which results in inaccurate estimation of losses. Given the high switching rate of the SiC MOSFETs, consideration of the effect of parasitics and temperature becomes crucial to remove these inaccuracies. This section introduces to the circuit parasitics and the data extraction process from device datasheet for describing the governing equations during the switching intervals of the DUT.

### A. Passive Parameters

The circuit diagram, with its parasitics, is shown in Fig. 1. The gate resistance $R_g$ and dc bus parasitic resistance $R_b$ ($R_b = R_{b,1}+R_{b,2}$) are included in this model. The parasitic inductances present in the circuit are $L_b$, $L_d$, and $L_s$. $L_b$ ($L_b = L_{b,1}+L_{b,2}$) is the dc bus inductance. $L_d$, $L_s$ are the drain and source lead inductances of the SiC MOSFETs, respectively. The parasitic capacitances considered in this model are the gate–source capacitance $C_{\text{gs}}$, drain–source capacitance $C_{\text{ds}}$, gate–drain capacitance $C_{\text{gd}}$ of the SiC MOSFETs and the load capacitance $C_L$.

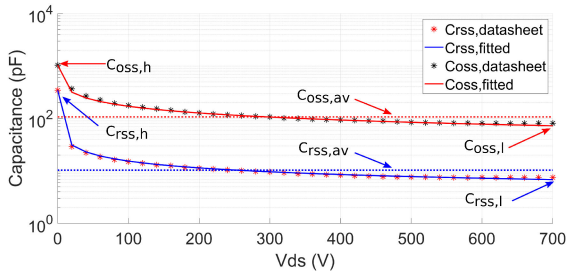


Fig. 2. $C_{\text{oss}}$ and $C_{\text{rss}}$ for CREE C2M0080120D SiC MOSFET and their fitted curves.

Typically, the capacitances values provided in the device datasheets are input, output, and reverse transfer capacitances ($C_{\text{iss}}$, $C_{\text{oss}}$, and $C_{\text{rss}}$), which are voltage dependent and can be modeled as per (1) [10], and the average charge equivalent capacitances can be determined as per (2)

$$C_x(V_{\text{ds}}) = \frac{C_{o,x}}{\sqrt{\left(1+\frac{V_{\text{ds}}}{a_x}\right)}+b_x} \tag{1}$$

$$C_{x,av} = \frac{1}{V_{\text{DC}}}\int_0^{V_{\text{DC}}} C_x(v_{\text{ds}})dv_{\text{ds}} \tag{2}$$

where $x = \text{iss}, \text{oss}, \text{rss}$, and $C_{o,x}$ is the capacitance value at $V_{\text{ds}}$ equals to zero. $a_x$ and $b_x$ can be found out by fitting the capacitance ($C_x$ versus $V_{\text{ds}}$) curves provided in datasheet [18]. $C_{\text{iss}}$ need not be fitted as its value remains almost constant with respect to $V_{\text{ds}}$ and can be directly taken from the datasheet. Fig. 2 shows the fitted curve of $C_{\text{oss}}$ and $C_{\text{rss}}$ of C2M0080120D SiC MOSFET [18]. From these capacitances, the MOSFETs terminal capacitances can be calculated as

$$\begin{aligned} C_{\text{gs}} &= C_{\text{iss}} - C_{\text{rss}} \\ C_{\text{ds}} &= C_{\text{oss}} - C_{\text{rss}} \\ C_{\text{gd}} &= C_{\text{rss}}. \end{aligned} \tag{3}$$

### B. Transfer Equation

During switching transition, the MOSFETs mainly operates in three regions: 1) cut-off region, 2) saturation region, and 3) ohmic region. For estimating the switching energy loss of the MOSFET, channel current $i_{\text{ch}}$ during saturation region is considered.

In the saturation region the transfer characteristics of a MOSFET is given in its datasheet for a given temperature and can be expressed per (4). The current transconductance factor $g_m$ depends on $i_{\text{ch}}$, and can be expressed as per (5) [19]. Due to the

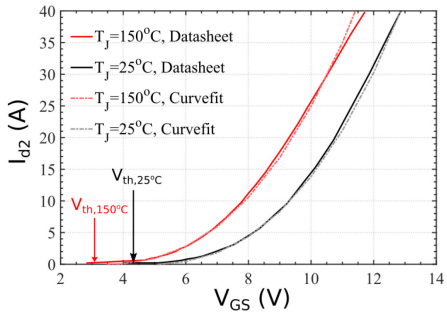


Fig. 3. Transconductance ($g_m$) characteristics of SiC MOSFET C2M0080120D.

dependency on temperature, $g_m$ changes as $T_j$ increases (see Fig. 3). The effect of $T_j$ on $V_{\text{th}}$ can be expressed as per (6)

$$i_{\text{ch}} = k_1[v_{\text{gs}} - V_{\text{th}}(T_j)]^x + k_2 \tag{4}$$

$$g_m(i_{\text{ch}}) = \sqrt[x]{\frac{k_1 i_{\text{ch}}^x}{i_{ch} - k_2}} \tag{5}$$

$$V_{\text{th}}(T_j) = aT_j^2 + bT_j + c. \tag{6}$$

Here $a$, $b$, $c$, $k_1$, $k_2$, and $x$ are the curve-fitting parameters. The values of these parameters are $29 \times 10^{-6}$, $-15 \times 10^{-3}$, 4.9, $195 \times 10^{-3}$, 0, and 2.5, respectively, for C2M0080120D.

## III. Switching Characterization and Discussion

This section introduces the switching process of the MOSFETs ($Q_1$ and $Q_2$) in a half-bridge configuration represented in Fig. 1(a). The lower MOSFET $Q_2$ is considered as the DUT.

The double-pulse test (DPT) has been divided into three parts as per Fig. 1(b). At the first turn-ON event, the voltages across $Q_1$, $Q_2$ are zero and $V_{\text{dc}}$, respectively. When the $Q_2$ is being turned ON the parasitic capacitance $C_{\text{oss},2}$ of $Q_2$ discharges and the $C_{\text{oss},1}$ of $Q_1$ charges. The current that flows through the MOSFETs in the first turn-ON event is due to the MOSFET's parasitic capacitances, which experiences a $dV_{\text{ds}}/dt$ across it. At the first turn-OFFevent of $Q_2$, $I_{d2}$ starts to fall and $V_{\text{ds2}}$ starts to rise while charging its $C_{\text{oss},2}$. The load current $I_{\text{load}}$ starts to transfer to the body-diode of $Q_1$ and $V_{\text{ds1}}$ starts to fall while discharging its $C_{\text{oss},1}$. In the second turn-ON event of $Q_2$, $I_{\text{load}}$ starts transferring from $Q_1$ to $Q_2$ and during this, in addition to the capacitive current, reverse recovery current of $Q_1$ increases the turn-ON loss of $Q_2$. This turn-ON loss increases significantly with the increase in $T_j$ due to reverse recovery current of the body diode of $Q_1$, which is explained in Section III-B.

### A. Turn-ON Transient

Under hard switching conditions, contribution of turn-ON loss $E_{\text{on}}$ in the total MOSFET switching loss $E_{\text{tot}}$ is significant. However, $E_{\text{on}}$ increases as $T_j$ increases, so the effect of temperature must be included in the loss estimation. A detailed interval wise turn-ON process can be seen from Fig. 4.

*1) Interval 0 (Delay Time):* This stage starts with increase in gate voltage $V_{\text{gs},2}$ from negative gate bias voltage $V_{\text{EE}}$ to threshold voltage $V_{\text{th}}$ with a time constant of $R_g(C_{\text{gs}} + C_{\text{gd},h})$.

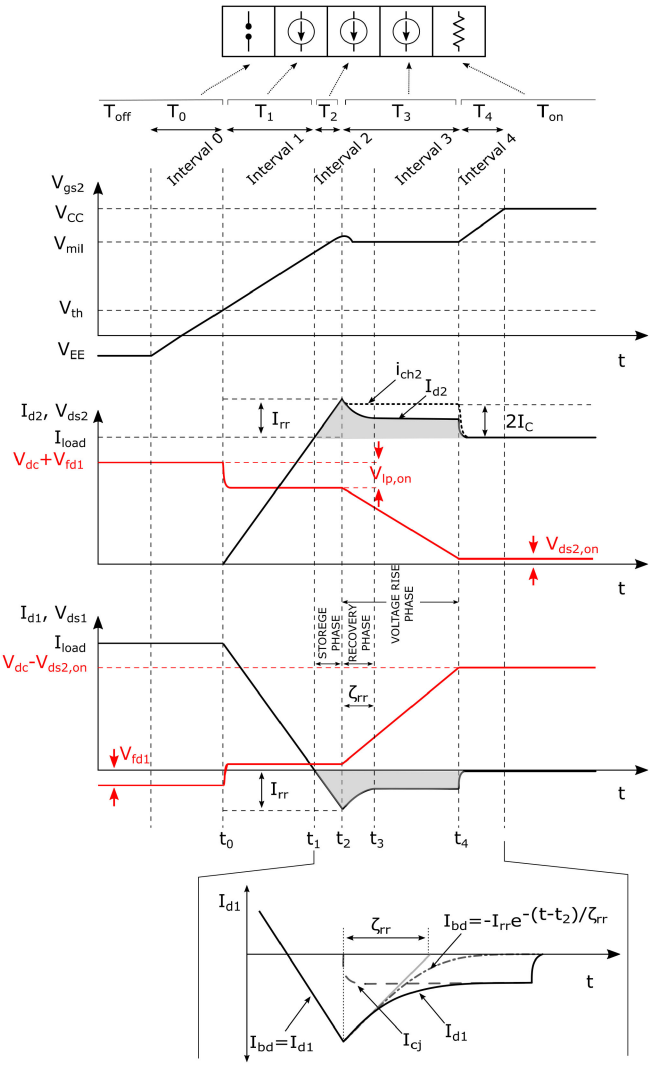


Fig. 4. Turn-ON process MOSFET $Q_1$ and $Q_2$ in a half bridge.

This interval is known as turn-ON delay time $t_{d,\text{on}}$. In this interval as $V_{\text{gs},2}(t) < V_{\text{th}}$, there is no drain current $I_{d2}$ in MOSFET $Q_2$ and all the $I_{\text{load}}$ flows through the body diode of MOSFET $Q_1$. The voltage across the $V_{ds,2}$ remains at $V_{\text{dc}} + V_{fd1}$.

$$v_{gs}(t) = V_{CC} + [V_{EE} - V_{CC}]e^{\frac{-t}{R_g(C_{gs} + C_{gd,h})}}$$

$$T_0 = R_g(C_{gs} + C_{gd,h})ln\frac{V_{CC} - V_{EE}}{V_{CC} - V_{\text{th}}(T_j)}. \tag{7}$$

*2) Interval 1 (Current Rise Time):* In this interval, as $v_{gs}(t)$ crosses the $V_{\text{th}}$, $Q_2$ channel current $I_{\text{ch2}}$ starts to rise to $I_{\text{load}}$. In this interval $I_{d2}$ remains equal to $I_{\text{ch2}}$ and the $V_{\text{ds2}}$ drops to $V_{\text{dc}} + V_{fd1} - V_{Lp,\text{on}}$. Voltage $V_{Lp,\text{on}} = (L_p * I_{\text{load}})/T_1$ is the addition of voltage drops across $L_b$, $L_d$, and $L_s$ (where $L_p = L_b + L_d + L_s$). The dynamics of the gate voltage, time duration, and the energy loss in this interval are expressed in (8). The $dV_{\text{gd}}/dt$ and $dV_{\text{ds}}/dt$ does not change significantly in this interval, so for

simplicity, these can be assumed to be zero.

$$v_{\rm gs}(t) = V_{CC} + [V_{\rm th}(T_j) - V_{CC}]e^{\frac{-t}{R_g C_{\rm gs} + L_s g_m(T_j)}}$$

$$T_1 = \left| -(R_g C_{\rm gs} + L_s g_m(T_j)) ln \left(1 - \frac{I_{\rm load}}{g_m(T_j)(V_{CC} - V_{\rm th}(T_j))}\right)\right|$$

$$E_{\rm on,1} = \frac{1}{2} T_1 (V_{\rm dc} + V_{fd1} - V_{Lp,\rm on}) I_{\rm load}. \quad (8)$$

*3) Interval 2 (Storage Time):* At this interval $I_{d2}$ continues to rise above $I_{\rm load}$ to $I_{\rm load} + I_{rr}$. Due to the reverse recovery of MOSFET $Q_1$, $V_{\rm ds2}$ stays at $V_{\rm dc} + V_{fd1} - V_{Lp,\rm on}$. The circuit condition does not change from interval 1, but the time duration $T_2$ changes with respect to the $I_{\rm load}$ and $T_j$. The detailed working process of MOSFETs body diode in this interval with $I_{\rm load}$ and $T_j$ dependencies is explained in Section III-B. The energy loss of $Q_2$ in this interval can be expressed as

$$E_{\rm on,2} = (V_{\rm dc} + V_{fd1} - V_{Lp,\rm on}) \left(I_{\rm load} + \frac{1}{2} I_{rr}\right) T_2. \quad (9)$$

*4) Interval 3 (Voltage Fall Time):* After the current $I_{d1}(t)$ in the body diode of MOSFET $Q_1$ reaches to $I_{rr}$, it starts to block the voltage $V_{ds1}$ across it and simultaneously the $V_{ds2}$ across $Q_2$ starts to fall. Here, as $V_{\rm ds1}$ starts to rise, the parasitic capacitance $C_{\rm oss1}$ starts to charge and the parasitic capacitance $C_{\rm oss2}$ starts to discharge. The charging current of $C_{\rm oss1}$ is termed as $I_{C1}$ and the discharging current of $C_{\rm oss2}$ is termed as $I_{C2}$. Due to $C_{\rm gd1}$ discharging, the voltage $V_{gs2}$ in this interval stays at miller plateau voltage $V_{\rm mil}$. The net current which flows through the channel of MOSFET $Q_2$ is $I_{\rm ch2} = I_{\rm load} + I_{C1} + I_{C2} + I_{rr} e^{-(t-t_2)/\tau_{rr}}$ (details about $\tau_{rr}$ is given in Section III-B). If both the MOSFET $Q_1$ and $Q_2$ are same then the parasitic capacitance across it can be considered to be same, so $I_{C1} = I_{C2} = I_C$. For calculating the energy loss in this interval, $i_{ch}$ has been divided in to two parts: first is due to $I_{\rm load} + 2I_C$ and the second is due to $I_{rr} e^{-(t-t_2)/\tau_{rr}}$. The capacitive current $I_C$ can be found from the quadratic equation given in [9] as

$$I_C = \left| \frac{-B_1 + \sqrt{B_1^2 - 4A_1 C_1}}{2A_1} \right| \quad (10)$$

where

$$A_1 = \frac{-2L_s}{Q_C R_g}$$

$$B_1 = \frac{C_{{\rm gd},av}}{C_{{\rm gd},av} + C_{{\rm ds},av}} + \frac{2}{g_m(T_j) R_g}$$

$$C_1 = \frac{V_{CC} - V_{\rm th}(T_j)}{R_g} - \frac{I_{\rm load}}{R_g g_m(T_j)}.$$

$I_C$ is being determined through numerical iterative method, as $g_m$ changes according to $i_{ch}$ and $T_j$. So, the iteration process will continue until the error in the calculation of $I_C$ becomes negligible. $Q_C$ is the net charge stored in the parasitic output capacitances of $Q_1$ or $Q_2$ (as the identical MOSFETs will have same charge storing capacity) and can be written as (11). The duration in which $V_{ds2}$ fall depends on the effective discharging time of the parasitic capacitance and is given as

$$Q_C = V_{\rm dc} C_{\rm oss2,av} \quad (11)$$

$$T_3 = \frac{Q_C}{I_C}. \quad (12)$$

The total energy loss in the MOSFET $Q_1$ in this interval can be written as

$$\begin{aligned} E_{\rm on,3} = {} & \frac{1}{2}(I_{\rm load} + 2I_C)(V_{\rm dc} + V_{fd1} - V_{Lp,\rm on} - V_{ds2,\rm on}) T_3 \\ & + (I_{\rm load} + 2I_C) V_{\rm ds2,on} T_3 \\ & + \tau_{rr} I_{rr} [(V_{\rm dc} + V_{fd1} - V_{Lp,\rm on})(1 - e^{(-T_3/\tau_{rr})})] \\ & + \tau_{rr} I_{rr} (V_{\rm ds2,on} - V_{\rm dc} - V_{fd1} + V_{Lp,\rm on}) \\ & [(\tau_{rr}/T_3)(1 - e^{(-T_3/\tau_{rr})}) - e^{(-T_3/\tau_{rr})}]. \end{aligned} \quad (13)$$

*5) Interval 4:* This interval starts when MOSFET $Q_2$ enters from saturation region to ohmic region. The gate voltage $V_{\rm gs2}$ starts rising from $V_{\rm mil}$ to $V_{\rm CC}$ and the $V_{\rm ds2}$ remains at $V_{\rm ds2,on}$, hence this interval can be neglected from the switching interval. The energy loss in this interval can approximated as $E_{\rm on,4} \approx V_{\rm ds2,on} I_{d2} T_4$, where $T_4 \approx 2R_g(C_{\rm gs} + C_{{\rm ds}2,l})$. From the five turn-ON switching intervals, interval 0, 4 remains in the cutoff and ohmic regions. In intervals 1, 2, and 3, the SiC MOSFET remains in saturation as in this interval $V_{\rm gs} > v_{\rm th}$ and $V_{\rm ds} > v_{\rm gs} - V_{\rm th}$. Therefore for calculating the total turn-ON energy loss, switching intervals 1, 2, and 3 are being considered and can be written as

$$E_{\rm on,tot} = E_{\rm on,1} + E_{\rm on,2} + E_{\rm on,3}. \quad (14)$$

### *B. Reverse Recovery Loss Model*

This section describes the reverse recovery process of the body diode of the SiC MOSFET. The time duration during this process increases with respect to $T_j$ and $I_{\rm load}$. Therefore, to estimate the time period during reverse recovery, the silicon power diode model from [20] and [21] has been improved by including temperature dependencies for higher accuracy under different $T_j$; further, the impact of capacitive displacement current $I_{cj}(t)$ due to the parasitic capacitance has been discussed. For developing a comprehensive MOSFETs body diode model, the behavior of the body-diode during turn-OFF needs to be analysed first. Fig. 5(a) shows the behavior of a 36 A/1.2 kV SiC MOSFETs body diode during turn-OFF at different $T_j$.

The reverse recovery process starts when the current through the diode starts to flow in the negative direction. The rate at which body-diode current $I_{d1}(t)$ falls below zero, $dI_{d1}/dt$ depends on the circuit stray inductance $L_p$ and the applied reverse bias voltage $V_{\rm ds1}$ across the MOSFET. As the diode current enters into the negative region, the excess charge carriers present in the junction starts to reduce while the $I_{d1}$ starts to fall toward the negative peak of the reverse recovery current $I_{rr}$. This region from $t_1$ to $t_2$ termed as storage phase. After the excess charge carriers become zero at $t_2$, depletion region starts to form and the reverse voltage across the diode starts to rise at the rate of

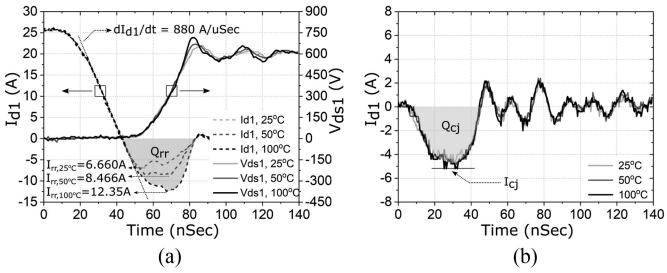


Fig. 5. (a) Reverse recovery of C2M0080120D at different $T_j$. (b) Capacitive displacement current $I_{cj}(t)$ of $Q_1$ (at no-load) under different $T_j$ at first DUT on instance.

$dV_{\rm ds1}/dt$. Time period from $t_2$ to $t_3$ is termed as recovery phase (see Fig. 4).

After $t_2$, as $V_{ds1}$ starts rising toward $V_{\rm dc} - V_{\rm ds2,on}$, parasitic capacitance across the body-diode $C_j = C_{\rm oss1} + C_l$ begins to charge and $I_{cj}(t)$ starts to flow. The magnitude of $I_{cj}(t)$ depends on the rate of $dV_{\rm ds1}/dt$. Time duration from $t_2$ to $t_4$ is termed as the voltage-rise phase. The reverse-recovery characteristics in the voltage-rise phase depends upon two currents: actual body-diode reverse recovery current due to the depletion region formation $I_{\rm bd}(t)$ and $I_{cj}(t)$. After $t_4$, $I_{d1}(t)$ reaches to its leakage current $I_{lk}$ level. The $I_{\rm bd}(t)$ during the entire reverse-recovery phase can be written as

$$I_{\rm bd}(t) = \begin{cases} I_{\rm load} - \frac{V_{\rm ds1}}{L_s}t, & t < t_2 \\ -I_{rr}e^{-\frac{(t-t_2)}{\tau_{rr}}} - I_{cj}(t), & t_2 \le t \le t_4 \\ I_{lk} \approx 0, & t \ge t_4. \end{cases} \tag{15}$$

To further describe the dynamics of the body diode and to find out $I_{rr}$ for any operating conditions, three time constants are introduced as [20]: drift region transit time $T_m$, charge carrier life time $\tau_c$, and time constant of decay fall $\tau_{rr}$. These are inter-related as per (16). From these time constants, $I_{rr}$ can be calculated by solving (17) numerically for $T_2$

$$\frac{1}{\tau_{rr}} = \frac{1}{\tau_c} + \frac{1}{T_m} \tag{16}$$

$$T_m\left[I_{\rm load} - \frac{I_{\rm load}}{T_1}(T_1+T_2)\right] = \frac{I_{\rm load}}{T_1}\tau_c\left[-T_2 + \tau_c - \tau_c e^{\frac{-(T_1+T_2)}{\tau_c}}\right]. \tag{17}$$

As the $T_j$ increases, these time constants tends to change. Hence, the proposed extraction method in [20] to find out $I_{rr}$ is not applicable for varying $T_j$. So, an equivalent reverse recovery charge model is presented to find out the time period $T_2$. The total reverse recovery charge $Q_{rr}$ is calculated as per (18). This $Q_{rr}$ combines both the reverse recovery charge $Q^*_{rr}$, which is due to $I_{\rm bd}(t)$ and the capacitive charge $Q_{cj}$ due to $I_{cj}(t)$ through parasitic capacitance $C_j$. As $T_j$ increases, the magnitude of $I_{rr}$ increases. Due to $I_{rr}$, $Q^*_{rr}$ also increases, but the $Q_{cj}$ remains constant, as $I_{cj}(t)$ does not change with respect to temperature [see Fig. 5(b)]

$$Q_{rr} = \int_{I_{d1}(t)<0} I_{\rm bd}(t)dt \tag{18}$$

$$Q_{rr} = Q^*_{rr} + Q_{cj} \tag{19}$$

$$I_{d1}(t) = I_{\rm bd}(t) + I_{cj}(t). \tag{20}$$

$I_{cj}(t)$ can be approximated as per (21) [22], which remains constant for period $T_3$ time period. The capacitive charge $Q_{cj}$ can be found out from the first turn-ON instant of DUT as per Fig. 5(b) by finding the area under the curve or from the datasheet parameters as per (21). At this instant the net $Q_{rr}$ is only due to $Q_{cj}$, as the $I_{d1}(t)$ prior to this instant is zero. From Fig. 5(b), $Q_{cj}$ can be experimentally calculated as per (18).

$$I_{cj}(t) = C_j\frac{dV_{\rm ds1}}{dt}$$

$$Q_{cj} = \int_{t_2}^{t_4} I_{cj}(t)dt. \tag{21}$$

To find out the temperature-dependencies of $Q_{rr}$, DPT at different $T_j$ needs to performed, from which $Q^*_{rr}$ can be calculated as per (19). In some manufacturer datasheet $Q_{rr}$ at two temperature are given which can be directly used to find out $Q^*_{rr}$. The time constant of decay fall $\tau_{rr}$ only depends on the $I_{rr}$, and the relationship between $\tau_{rr}$ and $Q^*_{rr}$ can be written as (22). Here, it is assumed that after $\tau_{rr}$ time, the contribution of $I_{\rm bd}(t)$ in $I_{\rm d1}(t)$ is negligible as per Fig. 4

$$Q^*_{rr} = 0.5 * I_{rr}\left(\frac{1}{dI_{d1}/dt}I_{rr} + \tau_{rr}\right). \tag{22}$$

To determine the $\tau_c$, $\tau_m$, and $\tau_{rr}$ for any arbitrary operating conditions (16), (23), and (24) need to be solved numerically

$$I_{rr} = \frac{1}{2\cdot dI_{d1}/dt}(\tau_c - \tau_{rr})\left(1 - e^{-T_1/\tau_c}\right) \tag{23}$$

$$\frac{I_{rr}}{dI_{d1}/dt}(\tau_c + T_m) = \tau^2_{rr}\left(1 - e^{-T_1/\tau_c}\right). \tag{24}$$

## IV. Results and Discussion

### A. Experimental Setup

To study the effect of reverse recovery and switching energy loss at high $T_j$, the DPT has been carried out at 600 V dc bus voltage and load current till 25 A. The experimental results are taken for the validation of the temperature-dependent loss model proposed in this article. An SiC MOSFET C2M0080120D rated at 1200 V and 36 A [18] is used for the half-bridge in the DPT setup.

For the gate-driver circuit, an isolated dc–dc converter with an output of $+20/-5$ V and an optoisolator ACPL $-$ 337 J are used. A total of 9.98 $\Omega$ resistance is used as gate resistance $R_g$ for the MOSFETs. Low ESL dc link capacitors are being used near the half-bridge to reduce the dc bus inductance. A single layer air core inductor with an inductance of 475 $\mu$H is used as a load inductor.

Measuring the switching transients of the SiC MOSFETs requires a high bandwidth measuring probes. As per [23] and

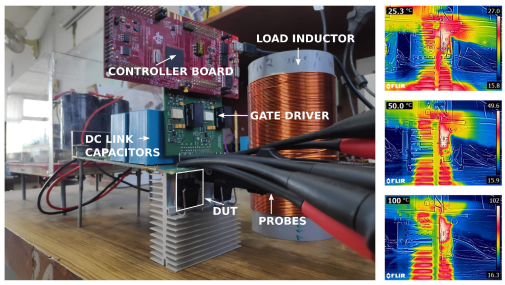


Fig. 6. Experimental test setup with thermal images ($T_{hs} = 25, 50,$ and 100 °C) of the DUT.

TABLE I
CAPACITANCE CURVE FITTING PARAMETERS

| $Capacitance$ | $C_{o,x}$ | $a_x$ | $b_x$ |
|---|---|---|---|
| $C_{oss}$ | 1040 pF | 3 | 1.25 |
| $C_{rss}$ | 344.2 pF | 0.19 | 1.25 |

[24], the effective bandwidth ($f_{\text{eff}}$) of a slope signal can be expressed as per (25). For the accurate measurement, the system band-width should be at least three times higher than the $f_{\text{eff}}$

$$f_{\text{eff}} = \frac{0.35}{\min(t_{\text{rise}}, t_{\text{fall}})}. \tag{25}$$

A passive differential voltage probe (P5200A) and a current probe (TCP0030A) from Tektronix are being used to measure the switching voltage and current transients. The heatsink was preheated before conducting the DPT at different temperatures until it reached a thermal equilibrium state to measure the switching performance. It is assumed that, under the thermal equilibrium state, the $T_j$ is equal to the $T_{hs}$. $T_{hs}$ is continuously monitored by a thermocouple temperature probe Fluke 80BK-A, and to further increase the accuracy of the reading, infrared thermal camera Flir E63900 is being used Fig. 6.

Switching energy loss estimation is very sensitive to voltage–current timing misalignment. The propagation delay between the two probes is known as skew. So, for accurate measurement, voltage, and current probes need to be properly de-skewed. A resistive DPT has been conducted with a low inductive 30 Ω resistor to verify the propagation delay time for each measuring probes.

### *B. Parameter Extraction*

The parameters used in the loss model are extracted from the SiC MOSFETs datasheet and from the experimental results.

For calculating the transconductance $g_m(i_{\text{ch}})$, curve fit values based on the transfer characteristics from the datasheet of C2M00801120D are being used as per (5). The datasheet and the fitted curves at two different $T_j$ are shown in Fig. 3. It can be seen that as the $T_j$ increases from 25 to 150 °C, $V_{\text{th}}$ decreases from 4.5 to 3.3 V.

For extracting the nonlinear capacitance values, (1) is used to find out the average capacitance values for saturation region. The maximum and minimum values of the capacitances are used for ohmic, cutoff regions, respectively. The curve fitting parameters and the extracted values are tabulated in Tables I and II.

TABLE II
NONLINEAR CAPACITANCES

| **Conditions** | $v_{gs} < V_{th}$ $V_{ds} \geq v_{gs} - V_{th}$ $Cutoff$ | $v_{gs} > V_{th}$ $V_{ds} > v_{gs} - V_{th}$ $Saturation$ | $v_{gs} > V_{th}$ $V_{ds} \leq v_{gs} - V_{th}$ $Ohmic$ |
|---|---|---|---|
| $C_{gd}$ | $C_{gd,l} = 8pF$ | $C_{gd,av} = 12pF$ | $C_{gd,h} = 500pF$ |
| $C_{ds}$ | $C_{ds,l} = 72pF$ | $C_{ds,av} = 111pF$ | $C_{ds,h} = 540pF$ |

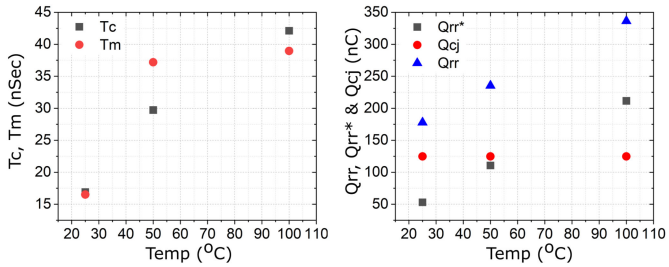


Fig. 7. (a) Variation of $T_m$ and $\tau_c$ with respect to $T_j$. (b) Variation of $Q_{rr}$, $Q^*_{rr}$ and $Q_{cj}$ with respect to $T_j$ ($V_{\text{dc}} = 600$ V and $R_g = 9.98\,\Omega$).

The dc bus inductance is calculated from the voltage drop $V_{Lp,\text{on}}$ in $V_{\text{ds2}}$ due to the parasitic inductances from the turn-ON switching waveform as shown in Fig. 9(d). The total path inductance is found out to be 66.21 nH ($L_p = (V_{Lp,\text{on}}{*}T_1)/I_{\text{load}}$)). The influence of $L_{s2}$ is more on the switching transients and hence needs to be subtracted from the total path inductance and considered separately. In this article, the value of $L_{s2}$ is considered to be 9 nH [25], [26].

The extraction of fitting parameters for $Q_{rr}$ and $Q^*_{rr}$ are done at $T_j = 25, 50$ and 100 °C. Further to see the effect of load current on $dI_{d1}/dt$ during the fall time, $I_{d1}$ is varied from 0 to 25 A as per Fig. 8(a)–(c). From all the test conditions, it is observed that $dI_{d1}/dt$ approximately remains constant at 880 A/$\mu$s. It can be observed from Fig. 8(a), at lower temperature ($T_j = 25$ °C), during the storage phase the change in $dI_{d1}/dt$ is not significant with respect to load current. However, at higher temperature ($T_j = 50$ and 100 °C) it can be observed from Fig. 8(b) and (c), that $dI_{d1}/dt$ does not remain constant throughout the storage phase with respect to load current and tends to change before it reaches to peak reverse recovery current ($I_{rr}$). The change in the $dI_{d1}/dt$ during storage phase is termed as $dI^1_{d1}/dt$, and it increases with respect to $T_j$. Further, as per Fig. 5(a), at higher $T_j$, $V_{\text{ds1}}$ starts to rise before the body-diode current reaches to $I_{rr}$. This phenomena increases the reverse recovery loss at a higher temperature. For simplicity, in this article, it is assumed that $V_{\text{ds1}}$ rises after the $I_{rr}$ reaches to its peak at $t_2$ as shown in Fig. 4.

The body-diode's time constants $\tau_c$ and $T_m$ are found out as per the discussion in Section III-B and are shown in Fig. 7(a). The increment in $\tau_c$ and $T_m$ with respect to $T_j$ increases rapidly at lower temperature range but tends to reduce at higher temperature Fig. 7(a). The change in $Q_{rr}$, $Q^*_{rr}$, and $Q_{cj}$ with respect to temperature is shown in Fig. 7(b). The dynamics of $\tau_c$ and $T_m$ and $Q^*_{rr}$ from the experimental results can be expressed as per

$$\tau_c(\text{nSec}) = \alpha_1 T_j^{\beta_1} + \gamma_1$$
$$T_m(n\text{Sec}) = \alpha_2 T_j^{\beta_2} + \gamma_2 \tag{26}$$

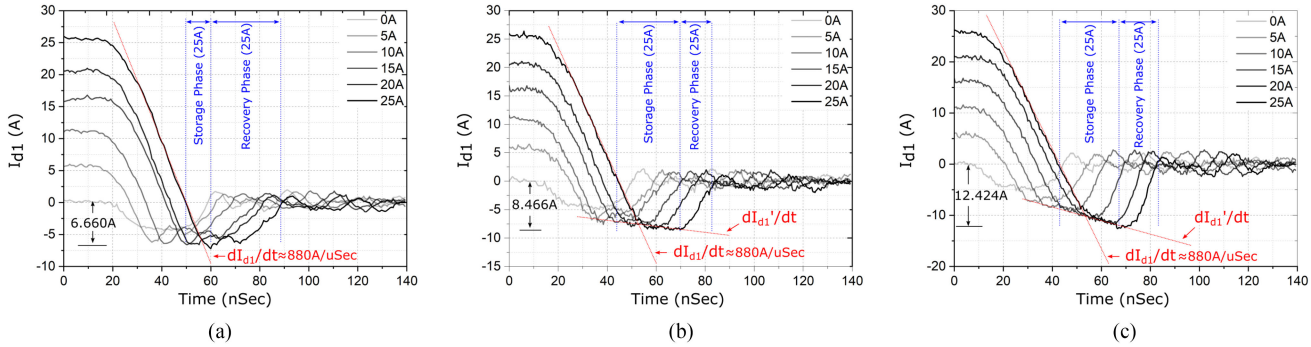


Fig. 8. (a) Reverse recovery current $I_{d1}$ at 25 °C. (b) Reverse recovery current at $I_{\mathrm{d1}}(t)$ at 50 °C. (c) Reverse recovery current at $I_{d1}(t)$ at 100 °C ($V_{dc} = 600$ V and $R_g = 9.98\,\Omega$).

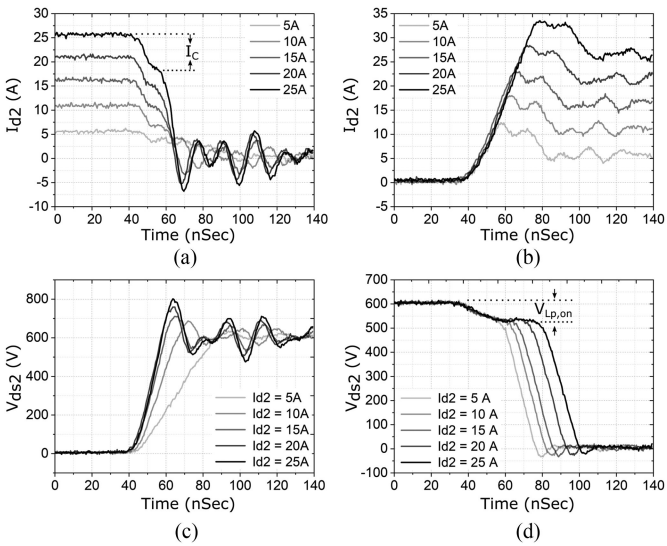


Fig. 9. (a) $I_{d2}$ fall transition at $T_j = T_{hs} = 25$ °C. (b) $I_{\mathrm{d2}}$ rise transition at $T_j = T_{hs} = 25$ °C. (c) $V_{\mathrm{ds2}}$ rise transition at different load current under $T_j = T_{hs} = 25$ °C. (d) $V_{\mathrm{ds2}}$ fall transition at different load current under $T_j = T_{hs} = 25$ °C ($V_{\mathrm{dc}} = 600\,V$, $I_{\mathrm{load}} = 5$–25 A and $R_g = 9.98\,\Omega$).

TABLE III
BODY-DIODE TIME CONSTANT FITTING PARAMETERS

| *Parameters* | $\alpha$ | | $\beta$ | | $\gamma$ | |
|---|---|---|---|---|---|---|
| | $R_g$ | | $R_g$ | | $R_g$ | |
| | 9.98Ω | 20Ω | 9.98Ω | 20Ω | 9.98Ω | 20Ω |
| $\tau_c(nSec)$ | -447.6 | -3.842 | -0.04924 | 0.6128 | 398.9 | -9.401 |
| $T_m(nSec)$ | -2.074e6 | -1799 | -3.55 | -1.059 | 39.12 | 75.85 |

$$Q_{rr}(\mathrm{nC}) = m_1 T_j + c_1$$
$$Q^*_{rr}(\mathrm{nC}) = m_2 T_j + c_2. \tag{27}$$

It should be noted that $Q_{rr}$ and $Q^*_{rr}$ at any given $T_j$ also depends upon the $R_g$. As $R_g$ increases, $dI_{d1}/dt$ and $dV_{ds1}/dt$ decrease. Due to this the $I_{rr}$, $Q_{rr}$, and $Q_{cj}$ decreases. The curve fitting parameters at $R_g = 9.98\,\Omega$ and $20\,\Omega$ for (26) and (27) are given in Tables III and IV, respectively.

### C. Energy Loss Verification

The loss estimation model presented in Section III is used for computing the turn-ON energy losses at different operating temperatures ($T_j$ = 25, 50, and 100). The experimental

TABLE IV
REVERSE RECOVERY CHARGE FITTING PARAMETERS

| *Parameters* | $m$ | | $c$ | |
|---|---|---|---|---|
| | $R_g$ | | $R_g$ | |
| | 9.98Ω | 20Ω | 9.98Ω | 20Ω |
| $Q_{rr}(nC)$ | 2.101 | 2.155 | 127.3 | 100.8 |
| $Q^*_{rr}(nC)$ | 2.101 | 2.155 | 2.54 | -9.155 |

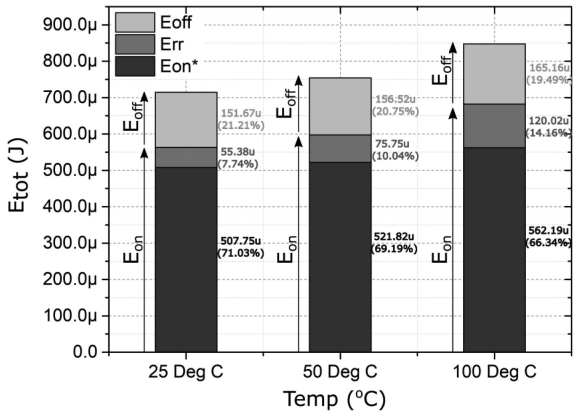


Fig. 10. Analytical energy loss segments under $T_j = 25$, 50, and 100 °C for $V_{\mathrm{dc}} = 600$ V, $I_{\mathrm{load}} = 25$ A, and $R_g = 9.98\,\Omega$.

energy losses are calculated by multiplying the $V_{ds2}$ and $I_{d2}$ during switching (see Fig. 9(b) and (d) for turn-ON and Fig. 9(a) and (c) for turn-OFF), and calculating the area under the curve. The analytical and experimental results of turn-ON loss at $R_g = 9.98\,\Omega$ and $20\,\Omega$ are compared and plotted in Fig. 11(a) and (d), respectively. Simulated $E_{\mathrm{on}}$ results from the manufacturer provided LT Spice model has also been compared with the developed analytical model, where it can be observed that LT Spice results for $E_{\mathrm{on}}$ does not vary with respect to temperature as it does not consider the temperature-dependent $E_{rr}$ contribution in $E_{\mathrm{on}}$.

The percentage estimation error in calculating $E_{\mathrm{on}}$ with different methods over a wide operating range has been shown in Fig. 11(b) and (e) for different $R_g$ (9.98 Ω and 20 Ω). It can be observed that at $I_{d2} = 5$ A, due to the absence of temperature dependencies in the $E_{\mathrm{on}}$ loss calculation, for $T_j = 100$ °C and $R_g = 9.98\,\Omega$, the absolute percentage error by the analytical model [9], LT Spice results are 31% and 58%; similarly, at $R_g = 9.98\,\Omega$ these errors are 29% and

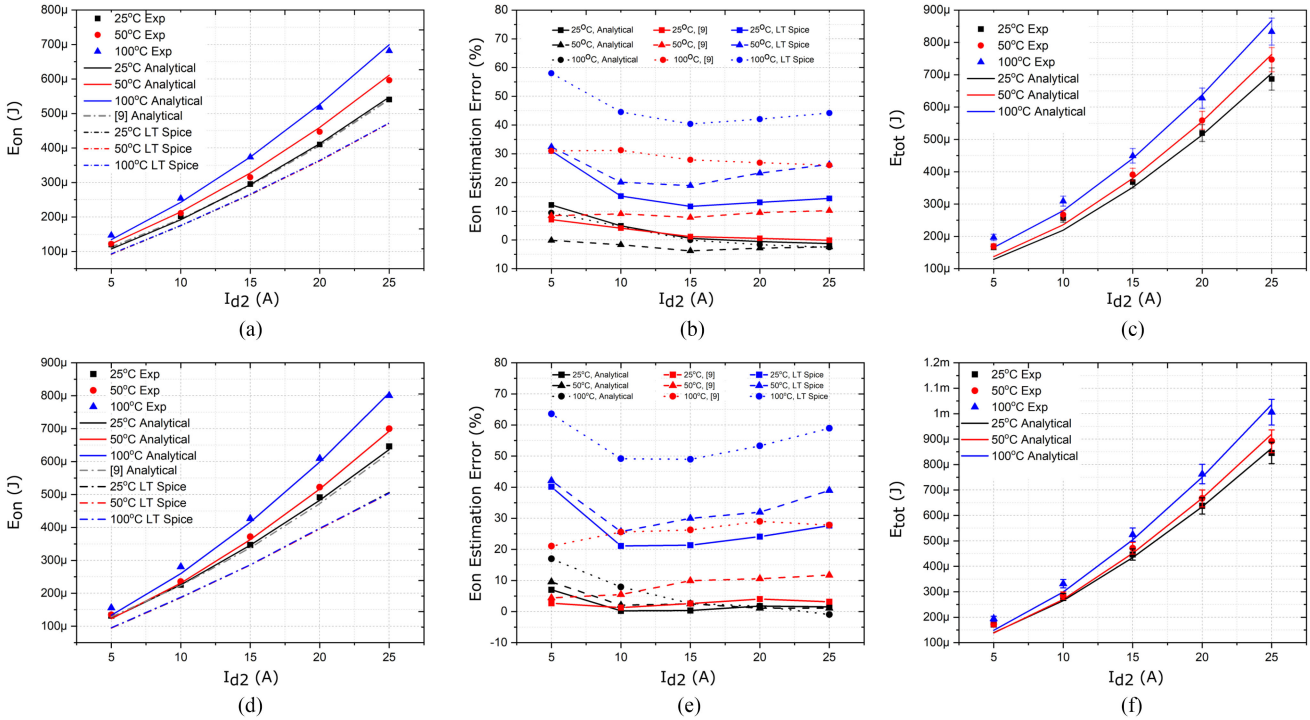


Fig. 11. (a) $E_{\text{on}}$ at $T_j = T_{hs} = 25, 50,$ and 100 °C and $R_g = 9.98\,\Omega$. (b) Comparison of $E_{\text{on}}$ estimation error at $T_j = 25, 50$, and 100 °C for $V_{\text{dc}} = 600$ V, $I_{\text{load}} = 5$–25 A and $R_g = 9.98\,\Omega$. (c) $E_{\text{tot}}$ at $T_j = T_{hs} = 25, 50,$ and 100 °C and $R_g = 9.98\,\Omega$. (d) $E_{\text{on}}$ at $T_j = T_{hs} = 25, 50,$ and 100 °C and $R_g = 20\,\Omega$. (e) Comparison of $E_{\text{on}}$ estimation error at $T_j = 25, 50$, and 100 °C for $V_{\text{dc}} = 600$ V, $I_{\text{load}} = 5$–25 A and $R_g = 20\,\Omega$. (f) $E_{\text{tot}}$ at $T_j = T_{hs} = 25, 50,$ and 100 °C and $R_g = 20\,\Omega$.

63.5%, respectively. However, due to the addition of the $T_j$ dependent parameters as per the proposed model, the maximum absolute error has been reduced to $\leq 12.1\%$ at $R_g = 9.98\,\Omega$ and $\leq 16.9\%$ at $R_g = 20\,\Omega$ ($I_{d2} = 5\,A$ and $T_j = 25$ °C). This estimation error further decreases to $\leq 2.5\%$ at $R_g = 9.98\,\Omega$ and $\leq 0.95\%$ at $R_g = 20\,\Omega$, at higher drain current ($I_{d2} = 25$ A).

For calculating $E_{\text{tot}}$, both $E_{\text{on}}$ and $E_{\text{off}}$ are required. The $E_{\text{on}}$ is being estimated as per the proposed model, while $E_{\text{off}}$ is estimated as per [9] and assumed to be constant at different $T_j$, since $E_{\text{off}}$ does not change substantially with respect to $T_j$. In the experimental results [see Fig. 11(c) and (f)], an accuracy band of $\pm 5\%$ has been created for $E_{\text{tot}}$ due to the measurement error introduced by the voltage and current probes. The error in the estimation of $E_{\text{tot}}$ increases at low value of $I_{\text{load}}$ due to the estimation error in $E_{\text{off}}$ at $0 \leq I_{\text{load}} \leq 2I_C$. At this current level, $I_{\text{ch2}}$ of $Q_2$ becomes zero, due to which, $dV_{\text{ds2}}/dt$ and $I_{\text{d2}}/dt$ decreases significantly as shown in Fig. 9(a) and (c). The loss distribution in $E_{\text{tot}}$ is shown in Fig. 10. The energy loss due to reverse recovery of $Q_1$ on $Q_2$ is subtracted from (14) and shown separately as $E_{rr}$. It can be seen that $E_{rr}$ increases by 116.7% (55.38–120.02 $\mu$J), when $T_j$ is increased from 25 to 100 °C.

## V. Conclusion

In this article, a combination of an analytical and behavioral model for estimating the temperature-dependent turn-ON switching energy losses $E_{\text{on}}$ of a SiC MOSFET in a half-bridge configuration is presented. Due to the nonavailability of the $T_j$ dependent reverse recovery data in the device data-sheet, an experiment based parameter extraction routine has been proposed for modeling the SiC MOSFET and its body diode characteristics. The impact of temperature on the charge carrier lifetime of the SiC MOSFETs' body-diode has been discussed and determined through experimental results for developing the $E_{\text{on}}$ loss model. Furthermore, the impact of the displacement current $I_{cj}(t)$ due to the SiC MOSFETs parasitic capacitance on estimating the reverse-recovery charge of the body-diode has been analyzed. The proposed model can also give the segmented turn-ON energy losses, including the device nonidealities.

For $E_{\text{tot}}$, $E_{\text{off}}$ has been estimated as per the model available in the literature, as $E_{\text{off}}$ does not show significant temperature dependency. However, in order to improve the accuracy in $E_{\text{tot}}$, further improvement in the $E_{\text{off}}$ modeling is required.

DPT has been conducted at different temperature (25, 50, and 100 °C) for validating the proposed model. The analytically estimated $E_{\text{on}}$ from the developed model at different $T_j$ closely matches with the experimental results over a wide operating range of device current. Additionally to show the effect of $R_g$ variation on $E_{\text{on}}$, the estimation has been performed for two different $R_g$ and experimentally validated. The estimation error from the proposed model at higher temperature drastically reduces compared with the other existing techniques. Moreover, the proposed model can estimate the $E_{\text{on}}$ at $I_{\text{load}} = 25$ A with a minimum accuracy of less than 2.5%.

## REFERENCES


[1] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si-evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[2] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[3] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, "Modeling of wide bandgap power semiconductor devices-part I," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 423–433, Feb. 2015.

[4] R. Kraus and A. Castellazzi, "A physics-based compact model of SiC power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5863–5870, Aug. 2016.

[5] S. Potbhare, N. Goldsman, A. Lelis, J. M. McGarrity, F. B. McLean, and D. Habersat, "A physical model of high temperature 4H-SiC MOSFETs," *IEEE Trans. Electron. Devices*, vol. 55, no. 8, pp. 2029–2040, Aug. 2008.

[6] B. N. Pushpakaran, S. B. Bayne, and A. A. Ogunniyi, "Electro-thermal transient simulation of silicon carbide power MOSFET," in *Proc. 19th IEEE Pulsed Power Conf.*, San Francisco, CA, USA, 2013, pp. 1–6.

[7] P. Alexakis, O. Alatise, L. Ran, and P. Mawby, "Modeling power converters using hard switched silicon carbide MOSFETs and Schottky barrier diodes," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Lille, France, 2013, pp. 1–9.

[8] A. Merkert, T. Krone, and A. Mertens, "Characterization and scalable modeling of power semiconductors for optimized design of traction inverters with Si- and SiC-devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2238–2245, May 2014.

[9] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for MOSFETs in a half-bridge," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.

[10] S. K. Roy and K. Basu, "Analytical estimation of turn on switching loss of SiC mosfet and Schottky diode pair from datasheet parameters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9118–9130, Sep. 2019.

[11] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[12] Y. Ren, M. Xu, J. Zhou, and F. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[13] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical methodology for loss calculation of SiC MOSFETs," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 71–83, Mar. 2019.

[14] S. Jahdi *et al.*, "An analysis of the switching performance and robustness of power MOSFETs body diodes: A technology evaluation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2383–2394, May 2015.

[15] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Berlin, Germany: Springer, 2007.

[16] "Efficiency of buck converter," Apr. 2016. [Online]. Available: https://fscdn.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/buck_converter_efficiency_app-e.pdf

[17] "An accurate approach for calculating the efficiency of a synchronous buck converter using the MOSFET plateau voltage," Jul. 2020. [Online]. Available: https://www.ti.com/lit/an/slvaeq9/slvaeq9.pdf

[18] "C2M0080120D mosfet datasheet," 2020. [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/C2M0080120D.pdf

[19] R. Perret, *Power Electronics Semiconductor Devices*. New York, NY, USA: Wiley, 2013.

[20] P. Lauritzen and C. Ma, "A simple diode model with reverse recovery," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 188–191, Apr. 1991.

[21] C. L. Ma, P. O. Lauritzen, and J. Sigg, "Modeling of power diodes with the lumped-charge modeling technique," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 398–405, May 1997.

[22] D. Nayak, M. Kumar, and S. Pramanick, "Analysis of switching loss reduction of SiC MOSFET in presence of antiparallel SiC schottky diode," in *Proc. IEEE Int. Conf. Power Electron., Smart Grid Renewable Energy*, 2020, pp. 1–6.

[23] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9307–9318, Dec. 2017.

[24] "Xyzs of oscilloscopes." [Online]. Available: https://download.tek.com/document/03W_8605_7_HR_Letter.pdf

[25] L. Zhang, S. Guo, X. Li, Y. Lei, W. Yu, and A. Q. Huang, "Integrated SiC MOSFET module with ultra low parasitic inductance for noise free ultra high speed switching," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, Blacksburg, VA, USA, 2015, pp. 224–229.

[26] "C2M0080120D silicon carbide power mosfet LTSpice model," [Online]. Available: https://www.wolfspeed.com/document-library/?documentType=ltspice-and-plecs-models&productLine=power


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