Systematic Analysis and Characterization of Extreme Failure for IGCT in MMC-HVdc System—Part II: Failure Mechanism and Short Circuit Characteristics

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***Abstract*—Short circuit failure mode (SCFM) of integrated gate commutated thyristor (IGCT) under extreme failure is of vital importance in high voltage direct current power transmission based on modular multilevel converter technology. Due to the sealing housing package of IGCT, the short circuit mechanism is hard to be clarified. Considering this limitation, the current density changes in IGCT with different failure modes are studied under different current levels in a built integrated test system with the placed magnetic sensor array and thermal couple array. Then, the short circuit mechanism of failed IGCT is proposed based on the experimental results. IGCT with turn-OFF failure performs self-triggering effect due to the focused short current and increased temperature in the initial destruction area, which is usually located in a single position of the outer cathode rings. While IGCT with surge current failure shares the short current among multiple initial destruction areas, which are usually distributed evenly in the wafer area. Scanning electron microscope picture and energy dispersive X-Ray spectroscopy (EDX) analysis show that the formed conducting alloy has spread into the molybdenum plate deeply and the phenomenon of atom diffusion (molybdenum, silicon and aluminum) near the interface is observed. Finally, long term short circuit tests of more than 12 h with both turn-OFF failure and surge current failure under 3000 A prove the stable SCFM of IGCT.**

***Index Terms*—Integrated gate commutated thyristor (IGCT), modular multilevel converter (MMC), short circuit failure mode (SCFM), surge current failure, turn-OFF failure.**

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I. Introduction

RECENT years, technology of modular multilevel converter (MMC) has developed rapidly [1], [2]. When the bypass switch of a faulty MMC submodule (MMC-SM) loses control, the MMC-SM needs to rely on the power devices' stable short circuit failure mode (SCFM) for reliable bypassing.

In the early high voltage direct current power transmission based on MMC technology (MMC-HVdc), the insulated gate bipolar transistor (IGBT), especially the plastic module IGBT (PMI) is commonly applied due to its low cost and loss. However, when the PMI gets destroyed, it cannot guarantee SCFM for long term. This is because that the bonding wires may fall off from the chips when it is destroyed [3], [4]. As a result, a lot of electrical and mechanical bypassing methods are added to the design of MMC based on PMIs [5].

Considering this problem, main power device manufacturers focus on press-pack IGBTs (PPI), which is more reliable than PMIs. And most study about short circuit characteristics of power devices for MMC-HVdc system is focused on PPIs in recent years, including the tests based on the whole device and the single IGBT chip [6]–[10]. Recently, the integrated gate commutated thyristor (IGCT) becomes a promising high power device and attracts much attention in applications of MMC [11]–[13] due to its lower voltage drop, smaller production cost and higher reliability compared with PPIs [14], [15]. But there is almost no analysis of IGCT's short circuit characteristics with different failure modes considering current redistribution changes during the long term, although turn-OFF failure mechanism of IGCT has been proposed based on detailed device simulation before [16], [17]. And this is due to the lack of relative experiment results, which is limited by IGCT's sealing housing package structure with the whole wafer.

The rest of this article is organized as follows. In Section I of this article, the device structure and explosion proof of IGCT has been introduced for the extreme failure in MMC-HVdc system. Reliable explosion proof and SCFM of IGCT are both of importance for the reliable operation under the extreme failure in MMC-HVdc system. This article gives the comprehensive experiments and analysis of the short circuit characteristics of IGCT with different failure modes for the extreme failure in MMC-HVdc system. Section II gives the basic introduction of

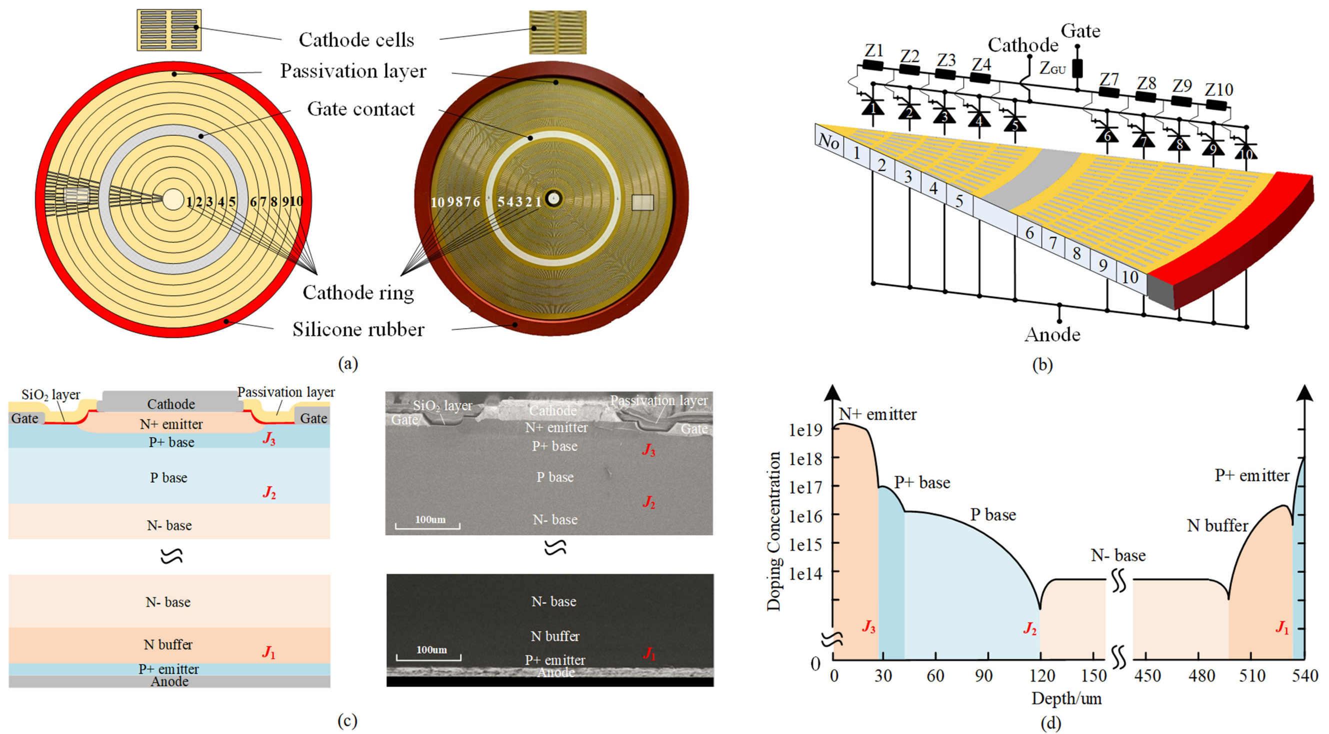


Fig. 1. Structure of the GCT chip in IGCT. (a) Schematic diagram and picture of the GCT chip. (b) Illustration of the GCT chip's gate metalization impedance using an equivalent circuit model. (c) Schematic diagram and SEM picture of the cathode cell's cross section. (d) Typical doping density of the cathode cell.

IGCT and introduces the typical failure mechanism of IGCT including turn OFF failure and surge current failure in MMC-HVdc system. Section III proposes an integrated test system for the short circuit characteristics of IGCT with the placed magnetic sensor array and thermal couple array and the theoretical analysis is given. Section IV gives the detailed experiment results and discussion of IGCT with different failure modes. Based on these, Section V proposes the short circuit mechanism of IGCT. Finally, long term short circuit tests of IGCT with different failure modes are carried out to prove the stable SCFM of IGCT for the extreme failure in MMC-HVdc system in Section VI. Finally, Section VII concludes this article.

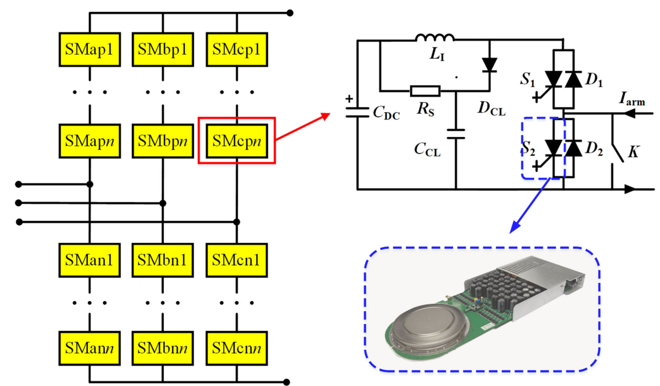


Fig. 2 . Typical schematic of IGCT based MMC-HVdc system and the IGCT based MMC submodule.

II. Failure Mechanism of IGCT in MMC-HVdc System

A. Introduction of IGCT

IGCT is an improved thyristor device including the integrated gate driver, the housing package and the gate commutated thyristor (GCT) chip. The structure of GCT chip in IGCT is shown in Fig. 1(a). The cathode side includes many striped cathode cells which are arranged in concentric rings. The gate contact is usually located between the fifth cathode ring and the sixth cathode ring. The regions besides the cathode cells and the gate contact are covered by the passivation layer for electrical insulation and pollution protection. Besides, silicone rubber is wrapped around the edge of the GCT chip for protection.

Due to the concentric distribution of the cathode cells in the GCT chip, there exist asymmetric electrical parameters among different rings during the GCT chip's operation. Fig. 1(b) gives the illustration of the GCT chip's gate metalization impedance using an equivalent circuit model. Inductances Z_1, Z_2, …, Z_{10} represent the gate metalization impedance loading of the cathode cells lying in different rings and Z_{GU} represents the impedance loading in the integrated gate driver. It can be seen that cathode cells in rings far from the gate contact have a larger impedance loading during the GCT chip's operation.

Fig. 1(c) shows the illustration and scanning electron microscope (SEM) picture of a cathode cell's cross section. There are N+ emitter region, P+ base region, P base region, N- base region, N buffer region, and P+ emitter region from the cathode to the anode in a cell. The SiO_2 layer is made between the gate and the cathode for insulation, which is below the passivation layer. PN junctions between N+ emitter region and

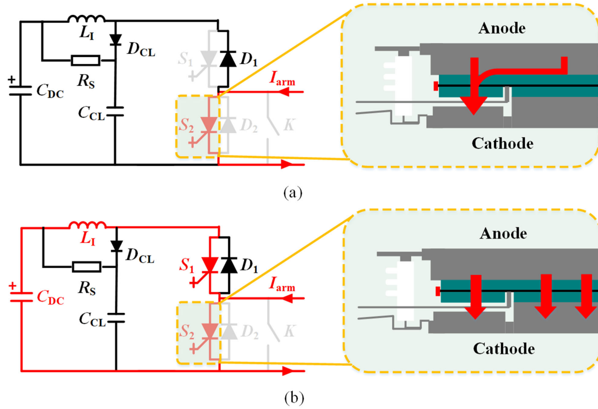


Fig. 3. Typical failure modes of IGCT in MMC-HVdc system. (a) Turn-OFF failure of S_2 in the overcurrent event of IGCT-SM. (b) Surge current failure of S_2 in the shoot-through fault event of IGCT-SM.

P+ base region, P base region and N- base region, N buffer region, and P+ emitter region are noted as J_3, J_2 and J_1. Fig. 1(d) presents the typical doping density of a cathode cell in the GCT chip, which is corresponding to Fig. 1(c).

B. Turn-OFF Failure Mechanism of IGCT in MMC-HVdc System

The typical schematic of IGCT based MMC-HVdc system and the IGCT based MMC submodule (IGCT-SM) is shown in Fig. 2. For IGCT-SM, S_1 and S_2 are IGCTs, meanwhile D_1 and D_2 are freewheeling diodes matched with S_1 and S_2. C_{DC} is the dc-link capacitor. L_{I} is the anode inductance, which is used to protect D_1 and D_2 from being destroyed by the high di/dt rate during the reverse recovery period. D_{CL}, R_{S} and C_{CL} make up the clamping circuit, which is used to limit the overvoltage caused by L_{I} when IGCT turns OFF. K represents the bypass switch of IGCT-SM. I_{arm} represents the output current of IGCT-SM.

Different from IGBTs, the maximum controllable current of commercial 4-in IGCT is 6.5 kA and there is no desaturation process in IGCT. Therefore, there are great risks for IGCT to turn-OFF a higher current than the nominal value of the manual. IGCT may not turn OFF successfully when an overcurrent fault event occurs in IGCT-SM. As a result, the turn-OFF failure of IGCT may happen in the MMC submodule. Fig. 3(a) shows the situation where S_2 fails to turn OFF I_{arm}. In this situation, IGCT-SM need to rely on SCFM of S_2 if the bypass switch K cannot work successfully.

When IGCT turns OFF, the cathode current is commutated to the gate terminal with the applied reverse voltage between the gate and the cathode. Fig. 4(a) gives the equivalent circuit model in the GCT chip's cross section, which is corresponding to that in Fig. 1(b). The maximum controllable current is usually affected by the uniformity of differnet rings' current [18] paths and current densities when IGCT turns OFF. For example, the cathode current's commutation path of the ninth ring with higher current density is marked red and the larger commutation inductance in the marked current path can be identified compared to those in the rings near the gate contact. Due to this, the cathode current will be commutated more slowly in the rings with larger commutation inductance and higher current density. As a result, the total current is easily crowded in these positions and IGCT may get damaged during IGCT's turn-OFF process, as shown in Fig. 4(b).

C. Surge Current Failure Mechanism of IGCT in MMC-HVdc System

For the surge current failure of IGCT, it mainly happens in the shoot-through fault events of IGCT-SM [19]. And this is usually caused by the problem of the controlling system and both the upper and lower IGCTs in the IGCT-SM turn ON at the same time. When a shoot-through fault occurs, the rise rate of fault current is almost unlimited in IGCT-SM due to the lack of desaturation process in IGCT compared to IGBT. So it is almost impossible for IGCT to turn OFF the fault current successfully and the destruction of IGCTs is almost inevitable. Fig. 3(b) shows the situation where S_1 is triggered by mistake during S_2's conducting period. In this situation, IGCT-SM also needs to rely on SCFM of S_2 if the bypass switch K cannot work successfully.

When IGCT conducts the surge current, it is usually limited by the transient temperature increase caused by the produced heat. Due to the differences of the pressure states and the ON-state voltages of cathode cells, the ON-state current densities are usually different, as shown in Fig. 4(c) [20]. As the surge current increases, positions with higher current densities achieve thermal limitation earlier than other positions. As a result, there are usually multiple destruction positions in the destroyed GCT chip, as shown in Fig. 4(d).

III. Integrated Test System for Short Circuit Characteristics of IGCT

A. Comparison of Different Methods

SCFM of IGCT under extreme failure in MMC-HVdc system is of vital importance for safe and reliable operation. However, the mechanism of IGCT's short circuit characteristics is not clear, which is limited by the sealing housing package of IGCT. Especially, it is hard to observe the short current density distribution and changes.

Table I compares different methods of detecting the current density distribution of press-pack devices with sealing housing packages. Measurement with Rogowski coils is broadband and accurate without contacting the sample. However, the closed loops of Rogowski coils make it hard to get the current density distribution unless a special designed housing package with multiple coils is adopted [20], [21]. Measurement with magnetic field sensors is another broadband method, which is like Rogowski coils. Compared with Rogowski coils, magnetic field sensors can be placed around the sample without any special designed housing package. However, the current paths need to be designed carefully because the magnetic field information is affected by these current paths around the sample easily.

Besides methods based on the principle of electromagnetic induction, the current density dsitrbution can also be detected according to the electrothermal effect, especically in high power semiconductor devices. There are mainly two kinds of methods.

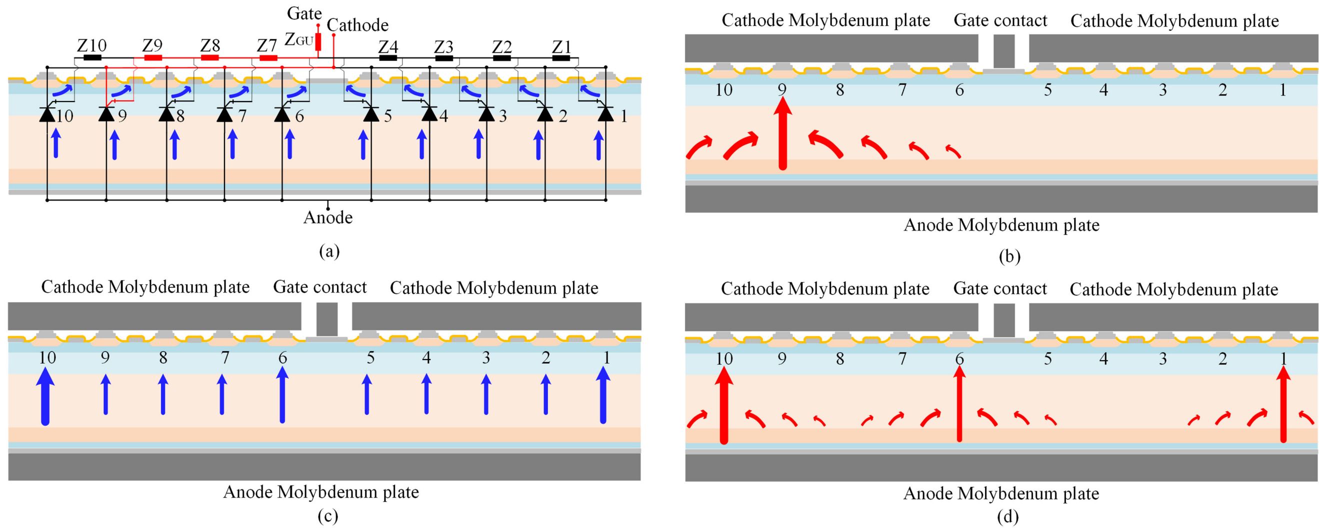


Fig. 4. Illustration of the failure mechanism of IGCT. (a) Equivalent circuit model in the GCT chip's cross section during turn-OFF process of IGCT. (b) Current crowding phenomenon and destruction position of IGCT during turn-OFF process. (c) Current distribution during ON-state process of IGCT. (d) Multiple destruction positions of the GCT chip with surge current failure.

TABLE I
COMPARISON OF DIFFERENT METHODS FOR DETECTING THE CURRENT DENSITY DISTRIBUTION IN IGCT

Method	Advantages	Disadvantages
Rogowski coil	Broadband measurement; Accurate current information of the measured area	Special designed housing package with multiple coils; only AC current can be detected effectively
Magnetic field sensor	Non-invasive and broadband measurement; Both AC and DC current information can be detected;	Multiple sensors; Affected by other current paths easily; Hard to get the accurate current density distribution in the device
Infrared thermography	Non-contact measurement; Observation of large areas at the same time	Special designed housing package with observation window; Affected by the surface state of the sample easily; Slow response to the current transient change
Thermal couple	Non-invasive measurement;	Multiple thermal couples; Isolation when measuring positions with high voltage; Slow response to the current transient change

The first kind is to use the infrared thermography technology. This method can obtain the temperature picture in a large area at the same time. However, the housing package must be replaced by a special designed infrared observation window partly to observe the surface of the chip [22], [23]. Another method is a kind of non-invasive measurement using thermal couples. This method does not need any changes of the housing package. But the thermal couples need to be islolated when they are placed at positions with high voltage. When the sample conducts a certain current, the voltage is usually very low. As a result, this method is suitable for study of the short current density distribution and changes in a failed IGCT.

According to the comparison, an integrated test system is built for detecting the short current density distribution and changes of the failed IGCT.

B. Introduction of the Integrated Test System

The built test system adopts the measurement using the thermal couple array and the magnetic field sensor array at the same time. Fig. 5 shows the picture of the test system. The test system includes the press-pack components with the tested IGCT, the cooling components and the high current source. The voltage information (including the anode-cathode voltage V_{ak}, the gate-cathode voltage V_{gk} and the anode-gate voltage V_{ag}), the temperature information (including T_1–T_{13}) and the magnetic field information (including B_{t1}–B_{t6}) of the failed IGCT during the test are detected using the voltage probes, the thermal couple array, and the magnetic field sensor array.

Illustration of the thermal couple array on the surface of IGCT and the magnetic field sensor array in the areas around IGCT from the top view is shown in Fig. 6.

According to this structure of the integrated test system, the 3-D simulation model can be built in COMSOL Multiphysics to simulate the magnetic field distribution around the device, as shown in Fig. 7(a). Fig. 7(b) gives the 2-D bottom view of the magnetic field distribution around the device under 1000 A. Positions where monitor magnetic fields B_{t1}–B_{t5} are also marked in Fig. 7(b). The current density of the device is assumed totally uniform in the simulation. It can be noticed that B_{t2} and B_{t5} are obviously larger than the magnetic fields of other four positions. This phenomenon is caused by the current paths of the copper bars A and B shown in Fig. 7(a). The magnetic fields produced by the copper bars A and B are in the same direction of those produced by the device. As a result, there are larger superimposed magnetic fields at the positions monitoring

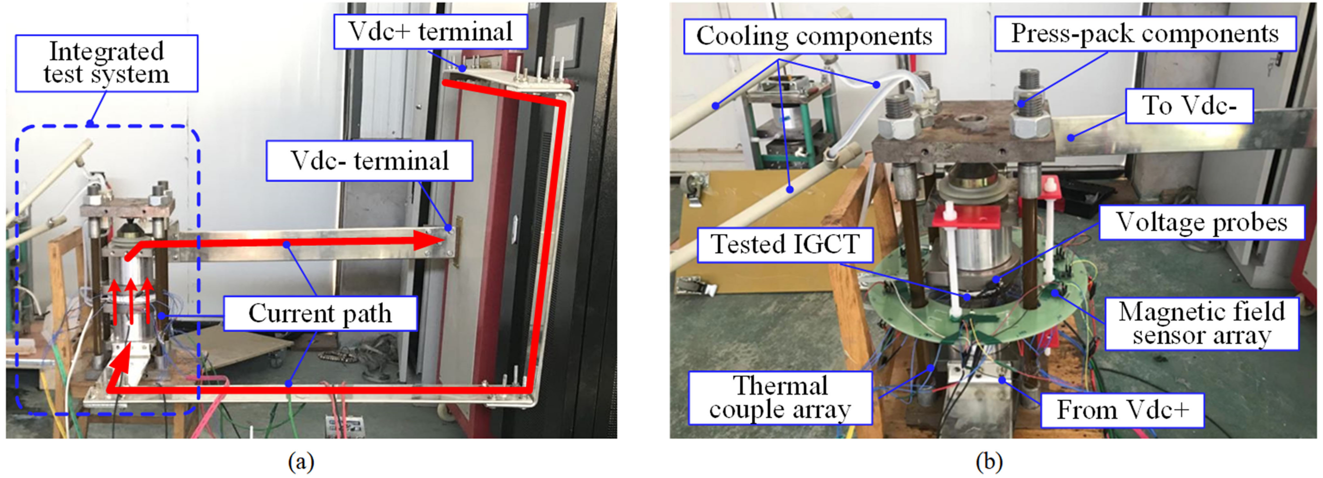


Fig. 5. Picture of the integrated test system for the study of the short circuit characteristics in IGCT during long term. (a) Illustration of the integrated test system as well as the current paths around it. (b) Detailed components of the integrated test system.

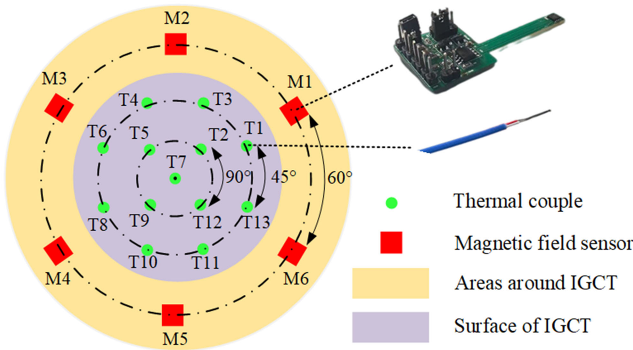


Fig. 6. Illustration of the thermal couple array on the surface of IGCT and the magnetic field sensor array in the areas around IGCT from the top view.

B_{t2} and B_{t5}. Nevertheless, the component of the magnetic field generated by the copper bar is fixed under a constant current and the difference in the magnetic fields induced by the changes in the device's current density can still be used to determine whether the current has been effectively transferred.

Meanwhile, the areas which conduct the current can perform as the heat sources and produce heat continuously due to the Joule effect in the short circuit test. As a result, there will be a certain temperature gradient distribution to ensure the balance of heat output and transfer. Due to the effects of the uneven heat sources which are corresponding to the conducting areas distributed in the device, the temperature of the device surface may be uneven. According to this, the main conducting areas where current focuses can also be identified.

IV. Short Circuit Developing Characteristics of IGCT

To study the short circuit developing characteristics of the IGCT with different failure modes, different dc currents are applied to monitor changes of the sample's voltage, temperature and magnetic field information.

The average rate current of the tested IGCT is nearly 3000 A. And when IGCT is applied in the MMC submodule, the maximum average rated current during the overload period may be higher than 2500 A. This also means that the failed IGCT need withstand such average short current to bypass the faulty MMC submodule. As a result, the applied dc current I_{dc} during the study is increased from 500 to 3000 A at 500 A intervals during different test stages.

To get the proper test period for the test stages, the thermal parameters of IGCT is analyzed. Materials of IGCT's different components are shown in Fig. 8 and the equivalent circuit of the IGCT thermal model is shown in Fig. 9. Heat conduction through the thin-layer components in the 4-in IGCT can be represented by the 1-D heat conduction in (1), where P_{in} is the produced heat power, T is the temperature, t is the time, A is the area of the layer, h is the thickness of the layer, ρ is the density of materials, c is the thermal capacity, and λ is the thermal conductivity. Then thermal resistances R and capacitances C of different layers can be derived from formulas (2) and (3). The calculated results are listed in Table II

$$P_{in} = -\lambda A \frac{\partial T}{\partial h} + \rho c A h \frac{\partial T}{\partial t} \tag{1}$$

$$R = \frac{h}{A\lambda} \tag{2}$$

$$C = \rho c A h. \tag{3}$$

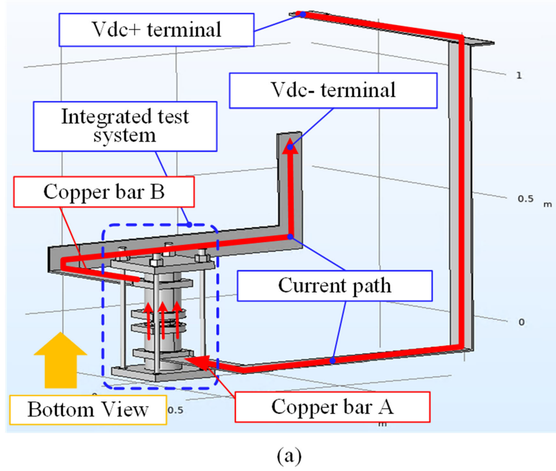
According to the analyzed thermal parameters of IGCT, the test period of the failed IGCT in each stage is finally set for 15 min to achieve thermal stability and this period is also long enough for observing the possible changes of the tested devices.

A. IGCT With Turn-OFF Failure

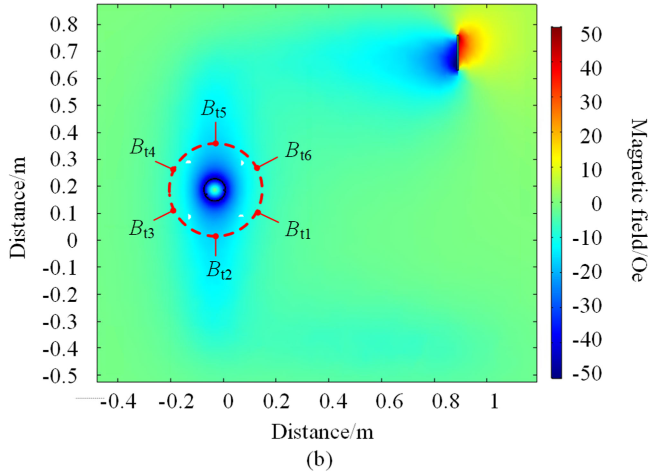
Picture and test results of the sample with turn OFF failure are shown in Figs. 10 and 11, respectively. In both stage 1 (I_{dc} = 500 A) and stage 2 (I_{dc} = 1000 A), the temperature T_1 and T_{13} is much higher than that of other positions and the monitored magnetic fields B_{t1} –B_{t6} perform stable, which means that the current focuses on the initial failure positions. Beisdes, the sample's anode–cathode voltage V_{ak} shows the same change trend as the sample's temperature, especially for T_1 and T_{13}. This result indicates that the sample's resistance, which equals to

TABLE II
PARAMETERS OF THE IGCT THERMAL MODEL

IGCT	Material Parameter			Anode Parameter				Cathode Parameter			
	c(J/gK)	ρ(g/cm^3)	λ(W/cmK)	A(cm^2)	h(cm)	R(K/W)	C(J/K)	A(cm^2)	h(cm)	R(K/W)	C(J/K)
Si (GCT chip)	0.70	2.33	1.30	51.50	0.038	0.00057	3.19	51.50	0.038	0.00057	3.19
Al (electrode)	0.90	2.70	2.38	51.50	0.0012	9.79e-6	0.15	12.65	0.0022	7.31e-5	0.068
Mo (Mo plate)	0.25	10.20	1.38	51.50	0.25	0.0035	32.83	51.50	0.25	0.0035	32.83
Cu (housing case)	0.39	8.94	4.00	59.40	1.015	0.0043	210.21	59.40	1.015	0.0043	210.21



(a)



(b)

Fig. 7. Simulation of magnetic field distribution around the tested device. (a) Three-dimensional simulation model of the integrated test system. (b) Two-dimensional bottom view of the magnetic field distribution with the marked positions that monitor B_{t1}–B_{t5}.

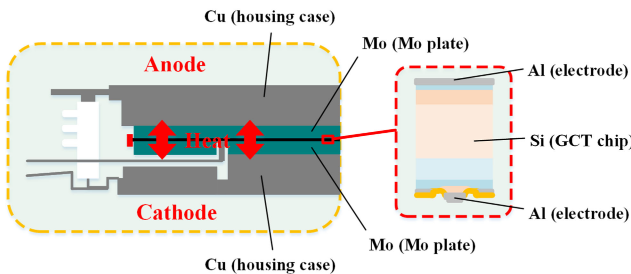


Fig. 8. Materials of IGCT's different components.

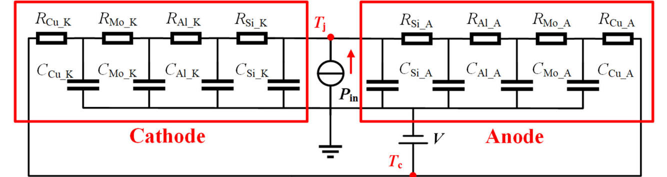


Fig. 9. Equivalent circuit of the IGCT thermal model.

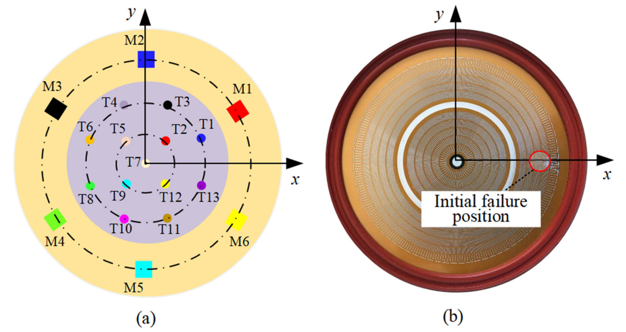


Fig. 10. Illustration of the tested IGCT sample with turn-OFF failure. (a) Positions of the magnetic sensors and thermal couples. (b) IGCT sample with turn-OFF failure and the area in the red circle is the initial failure position.

V_{ak}/I_{dc}, is up to the sample's temperature in stage 1 and stage 2. And when the test goes into stage 2 from stage 1, more generated heat helps the area of the conducting alloy spread and then the resistance gets dereased.

When the test period goes into stage 3 ($I_{dc} = 1500$ A), the sample's resistance in the intial serveral minutes performs like that during stage 1 and stage 2. And it is noted that there is slight increase of the gate-cathode voltage V_{gk} during this period. As V_{ak} increases, there is a jump of V_{gk} at t_1. This is an important signal which means that the sample's J_3 junction is forward biased. The short circuit current triggers the sample's undamaged cathode cells, which performs like a triggering current. The decreased anode-gate voltage V_{ag} also indicate these cathode cells are triggered and help to share the short circuit current. At this time, T_1 and T_{13} get decreased and temperatures of other monitored positions get increased. Finally, the temperature distribution of the sample tends to be uniform.

According to the analysis in Section III-B, the effects of the curent paths around the sample make B_{t2} and B_{t5} are larger than other monitored magnetic fields during the test. But the changes of the monitored magnetic fields under certain test currents can

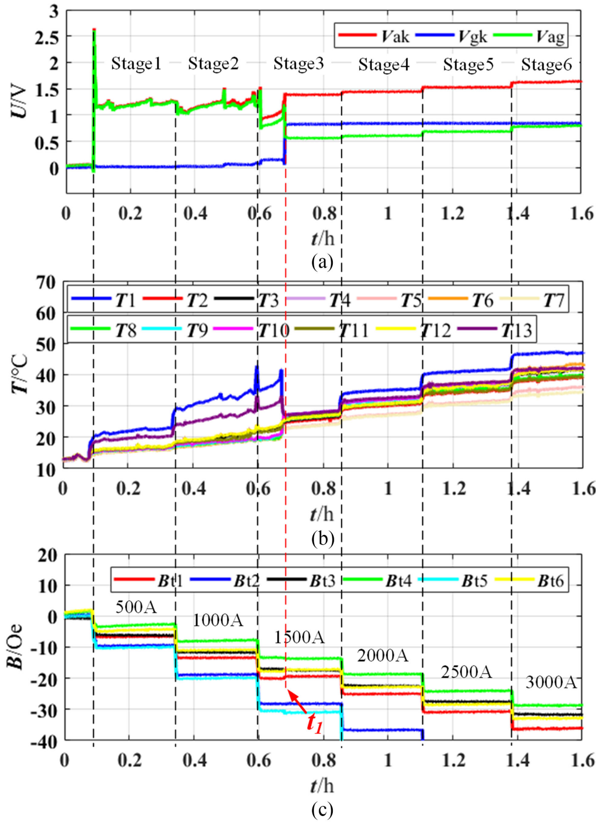


Fig. 11. Test results of the IGCT sample with turn-OFF failure under different dc current levels. (a) Monitored V_{ak}, V_{gk}, and V_{ag} of IGCT. (b) Monitored temperature results T_1–T_{13} of IGCT's surface. (c) Monitored magnetic field results B_{t1}–B_{t6} around IGCT.

be used to analysis the changes in current density. The triggering effect at t_1 during the test process can also be observed from the monitored magnetic fields. When the sample is triggered at t_1, B_{t1} and B_{t6} get decreased and B_{t3}, B_{t4} and B_{t5} get increased. This phenomenon shows that the current density gets redistributed. During this process, the conducting area expands from the intial alloy positions to other regions of the sample due to the triggering effect.

From stage 4 ($I_{\mathrm{dc}} = 2000$ A) to stage 6 ($I_{\mathrm{dc}} = 3000$ A), the triggering effect makes the normal cathode cells share the short circuit current continously and the monitored temperatures and magnatic field signals keep stable without sudden changes.

B. IGCT With Surge Current Failure

To compare with the short circuit developing characteristics of IGCT with turn-OFF failure, the IGCT sample with surge current failure is tested under the same dc current conditions after destruction. The picture of the IGCT sample after test and test results and are shown in Figs. 12 and 13, respectively.

In stage 1, the monitored temperature T_{11} around position 1 is higher than other temperatures, which means that the current density is mainly focused on position 1. When the test period goes into stage 2, position 3 begins to share more of the short circuit current and the monitored temperatures T_2, T_3, T_4, and T_5 around this position get increased. During stage 2, the increased V_{ak} shows that the sample's resistance, which equals to $V_{\mathrm{ak}}/I_{\mathrm{dc}}$,

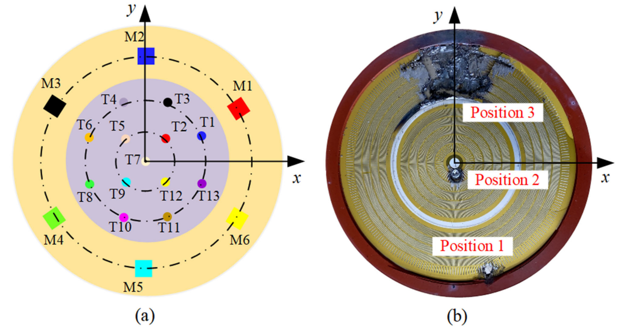


Fig. 12. Illustration of the tested IGCT sample with surge current failure. (a) Positions of the magnetic sensors and thermal couples. (b) IGCT sample with surge current failure after test and three failure positions are marked.

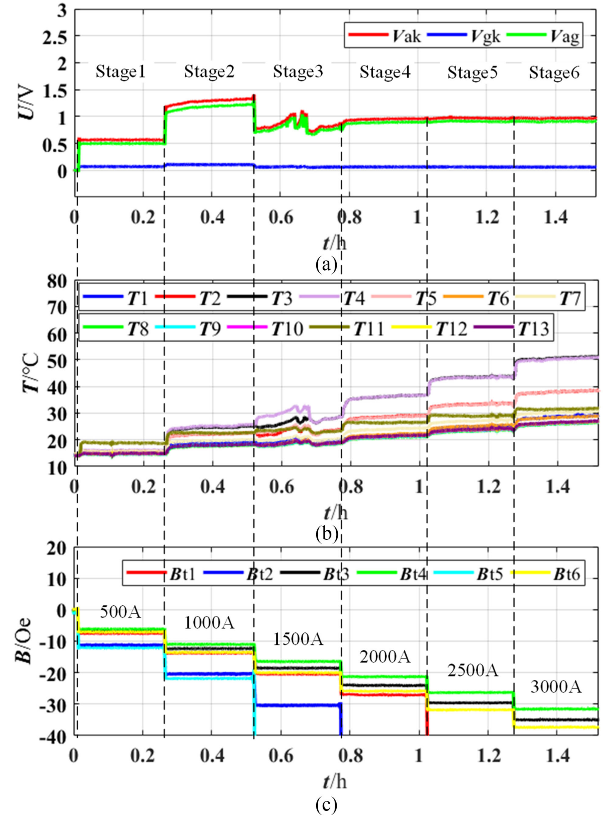


Fig. 13. Test results of the first IGCT sample with surge current failure under different dc current levels. (a) Monitored V_{ak}, V_{gk}, and V_{ag} of IGCT. (b) Monitored temperature results T_1–T_{13} of IGCT's surface. (c) Monitored magnetic field results B_{t1}–B_{t6} around IGCT.

is almost unchanged. While when the test period goes into stage 3, there is a severe decrease of V_{ak} and all the temperatures get decreased in the latter part. This indicates that the sample's resistance goes down and the sufficient melting and diffusion between the silicon wafer and the molybdenum plate around position 3 is the main cause.

From stage 4 to stage 6, V_{ak} remains stable although the current increases. This means that the sample's resistance keeps going down and the sample shows stable short circuit developing characteristics. T_2, T_3, T_4, and T_5 during these stages show that the current density is mainly focused on position 3. And T_7 and T_{11} show that position 1 and 2 also share a part of the short circuit current.

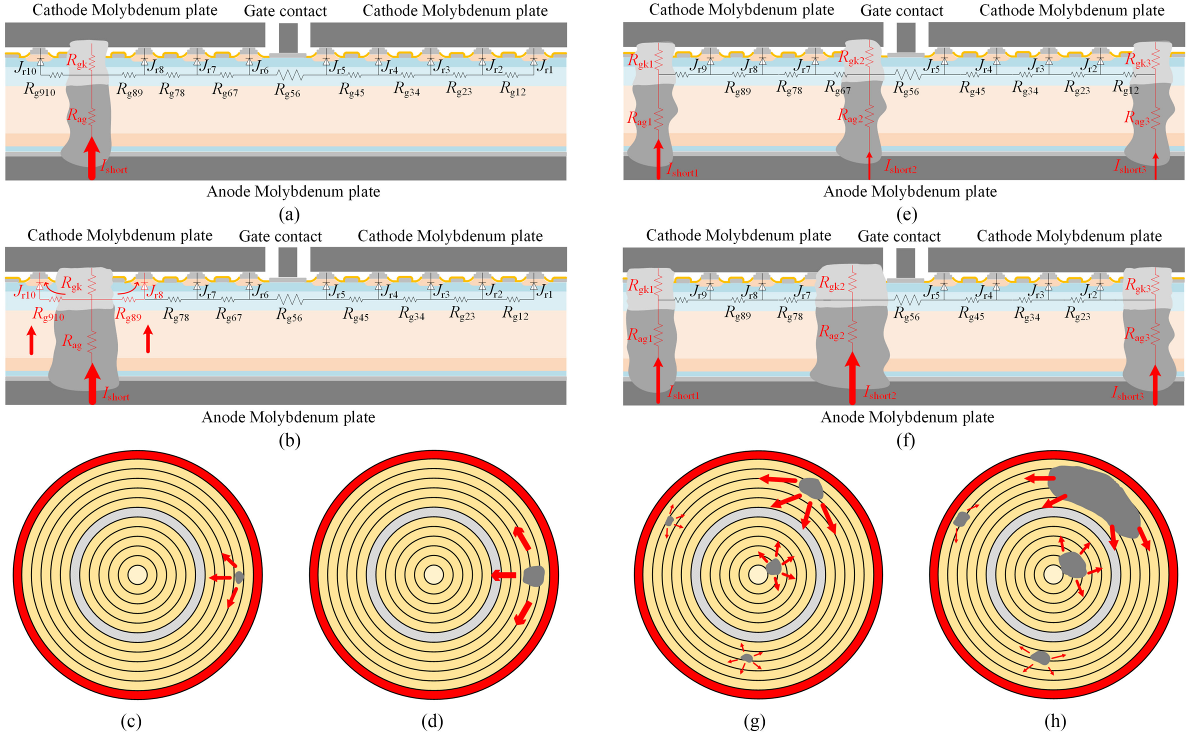


Fig. 14. Illustration of the short circuit mechanism of failed IGCT. (a) Equivalent circuit model of the short circuit characteristics of IGCT with turn-OFF failure. (b) Illustration of I_{short} paths when IGCT is self-triggered. (c) Initial destruction position of IGCT with turn-OFF failure. (d) Development of the conducting alloy area of IGCT with turn-OFF failure. (e) Equivalent circuit model of the short circuit characteristics of IGCT with surge current failure. (f) Current redistribution in different I_{short} paths. (g) Initial destruction position of IGCT with surge current failure. (h) Development of the conducting alloy area of IGCT with surge current failure.

During the test, V_{gk} does not exceed the threshold voltage and V_{ag} is almost the same to V_{ak}, which means that the sample's cathode cells are not triggered. And there is no obvious sudden change caused by the triggering effect in the monitored magnetic fields like that of the sample with turn-OFF failure. The magnetic field results remain stable in each stage and this indicates the stable current distribution focusing in the formed destruction areas during the surge current failure.

V. Short Circuit Mechanism of IGCT

Based on the test results in Section IV, the short circuit mechanism of IGCT can be concluded as follows.

A. *IGCT With Turn-OFF Failure*

Fig. 14(a)–(d) illustrates the short circuit mechanism of IGCT with turn-OFF failure. When IGCT fails during the turn-OFF process, a low-resistance conducting path forms in the destruction position. Then an equivalent circuit model can be built in Fig. 14(a). R_{gk} and R_{ag} stand for the resistance of the parts which are paralleled with the gate-cathode area and the anode-gate area in the undamaged chip part, respectively. J_{r1} to J_{r10} stand for the J_3 junctions of the cathode cells in ring 1 to ring 10, which are expressed as diodes in the circuit model. R_{12} to R_{910} stand for the horizontal resistance in the P+ base and P base regions between two adjacent cathode rings in the undamaged chip part.

When IGCT conducts a low short circuit current I_{short}, the voltage drop on the conducting alloy mainly focuses on R_{ag} and the voltage drop on R_{gk} is rather low. During this period, the changes of the voltage drop mainly depends on the temperature and the resistance changes of R_{ag}. When I_{short} increases, the voltage drop on R_{gk} increases gradually. During this period, because the heat mainly focuses on the anode-gate part of the conducting alloy, the further melting and spreading of this region causes the decrease of R_{ag} and the voltage drop between anode and gate V_{ag} decreases.

However, the new formed conducting alloy region does not achieve thermal stability and the temperature increases contiously. This will cause the increase of R_{gk} and block the short circuit current. Then the short circuit current will transfer to the nearby path of the undamaged cathode cell. Once the voltage drop on R_{gk} exceeds the voltage threshold of the J_3 junction (usually between 0.7–0.8 V) of the nearby undamaged cathode cells, part of I_{short} is transferred into these cells successfully and IGCT performs like being triggered by the short circuit current, as shown in Fig. 14(b). Then, the gate-cathode voltage is clamped immediately and I_{short} partly is shared by the normal cathode cells in IGCT. Besides, the temperature around the conducting alloy goes down quickly and the electrical characteristics of the conducting alloy becomes stable. Then, the conducting alloy will spread slowly around the initial failure region under thermal effects of the short current during long term tests, shown in Fig. 14(c)–(d).

Fig. 15(a) and (b) shows pictures of the IGCT sample with turn-OFF failure and the magnified conducting alloy expansion area after the short circuit current test, respectively. It can be

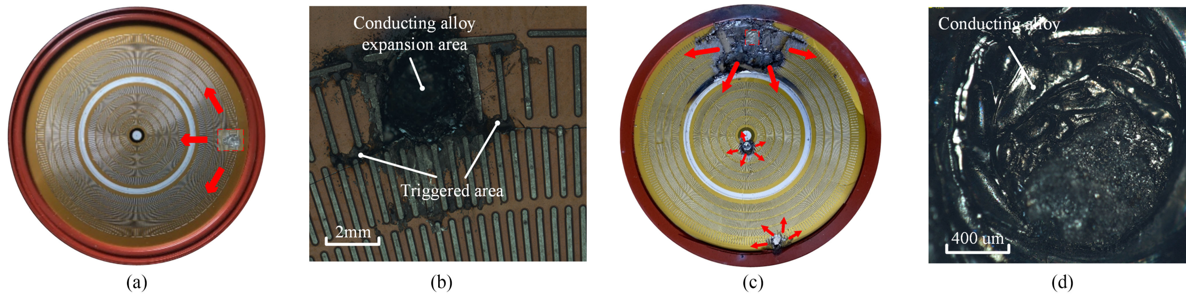


Fig. 15. Pictures of failed IGCTs after the short circuit current test. (a) Whole wafer of IGCT with turn-OFF failure. (b) Magnified conducting alloy expansion area in IGCT with turn-OFF failure. (c) Whole wafer of IGCT with surge current failure. (d) Magnified conducting alloy surface in IGCT with surge current failure.

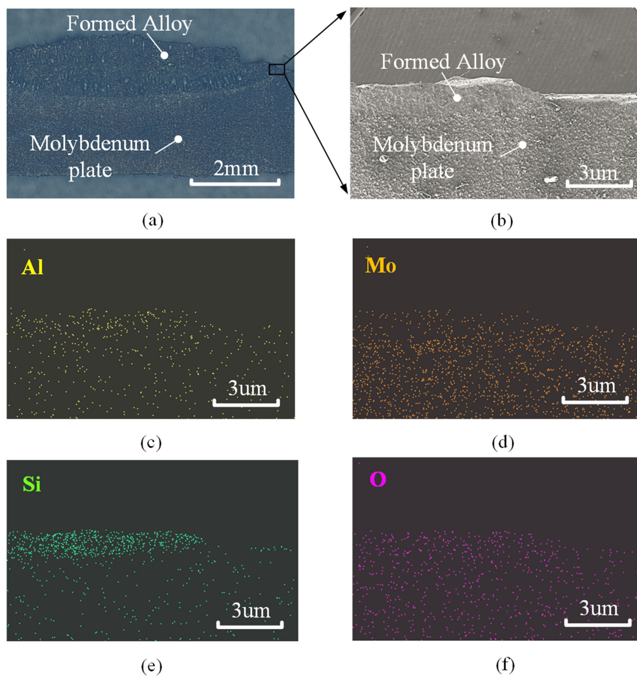
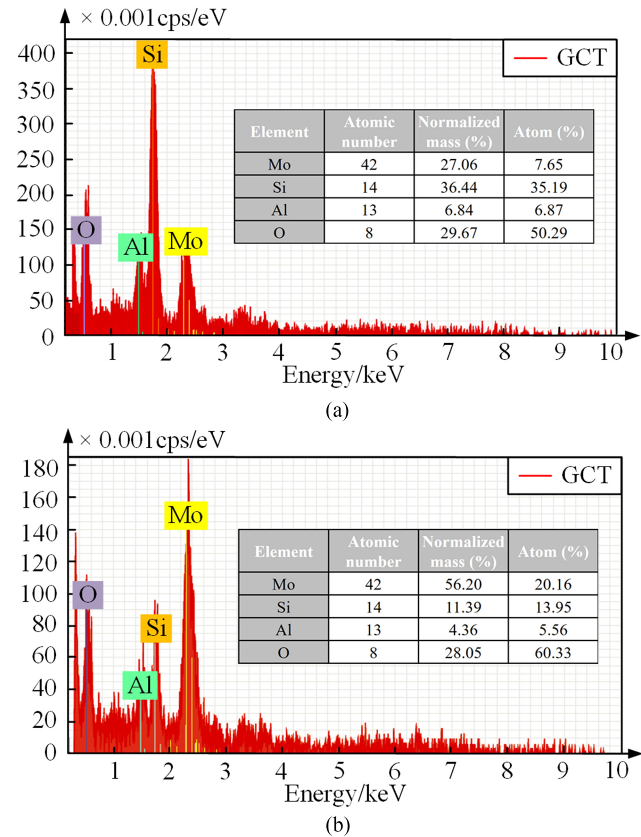


Fig. 16. EDX signal maps of the interface between the formed alloy and the molybdenum plate. (a) Cross section of the formed alloy areas on the molybdenum plate. (b) SEM picture of the magnified interface region. (c)–(f) EDX signal maps of Al, Mo, Si, and O.



Element	Atomic number	Normalized mass (%)	Atom (%)
Mo	42	27.06	7.65
Si	14	36.44	35.19
Al	13	6.84	6.87
O	8	29.67	50.29

Element	Atomic number	Normalized mass (%)	Atom (%)
Mo	42	56.20	20.16
Si	14	11.39	13.95
Al	13	4.36	5.56
O	8	28.05	60.33

Fig. 17. Element quantitative analysis of the formed alloy and molybdenum plate areas near the interface. (a) Formed alloy area. (b) Molybdenum plate area.

clearly seen that the expanded alloy area develops from the initial failure point and the burned surface area near this region indicates the large gate current which performs the triggering function of the nearby cathode cells.

B. IGCT With Surge Current Failure

Then, the short circuit mechanism of IGCT with surge current failure is illustrated in Fig. 14(e)–(h). Like that of Section V-A, a similar equivalent circuit model can be built in Fig. 14(e). Different from IGCT with turn-OFF failure, the total short circuit current is shared by the multiple destruction positions in IGCT with surge current failure, including I_{short1}, I_{short2}, and I_{short3} in Fig. 14(e). And this means that the temperature of the conducting alloy areas are more uniform and the electrical characteristics of the conducting alloy performs more stable. Consequently, it is harder to achieve the condition of self-triggering effect. As the total short circuit current increases, the current redistribution among these independent conducting alloy areas due to the different resistance changes, as shown in Fig. 12(f). And the low resistancce of the whole wafer can be kept under different short circuit current levels with the multiple conducting alloy areas.

Fig. 14(g) and (h) illustrate the spreading of the conducting alloy areas in IGCT with surge current failure. The shared shortcurrent in the destruction areas helps the spread of the conducting alloy areas around them.

Pictures of the conducting alloy area in IGCT with surge current failure after the short circuit current test are shown in Fig. 15(c) and (d). It can be seen that the formed alloy has metal-like surface state, which means that the silicon and the metal materials have been melt fully under the high temperature

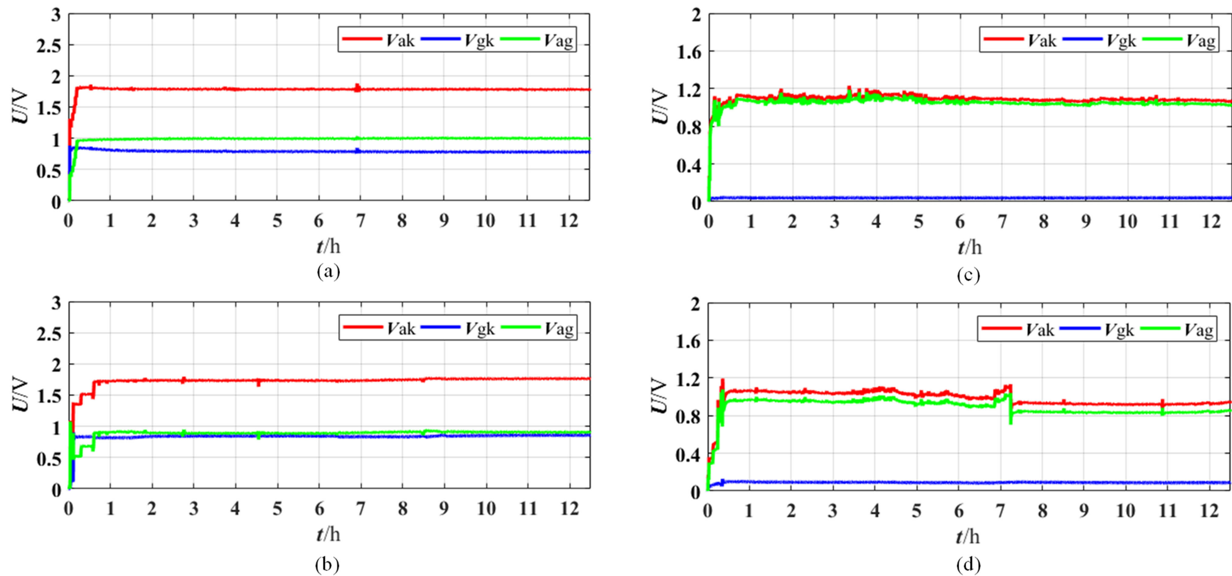


Fig. 18. Results of the long term short circuit characteristics of IGCT samples with different failure modes. (a) Sample A with turn-OFF failure. (b) Sample B with turn-OFF failure. (c) Sample C with surge current failure. (d) Sample D with surge current failure.

caused by the high current. Fig. 16(a) gives the cross section picture of the formed conducting alloy including the molybdenum plate. It can be seen that the formed alloy has picture of the formed conducting alloy including the molybdenum plate. It can be seen that the formed alloy has spread into the molybdenum plate deeply and the boundary between the formed conducting alloy and the molybdenum is clear in the picture.

Fig. 16(b) gives the scanning electron microscope (SEM) picture of the magnified interface between the formed alloy and the molybdenum plate and Fig. 16(c)–(f) give the further energy dispersive X-Ray spectroscopy (EDX) analysis of the magnified interface region. The signal maps of different elements show that the formed alloy is mainly composed of silicon and a certain amount of aluminum and molybdenum. The uniform oxygen in the EDX signal map is caused by the surface oxidation of the sample after sample preparation.

Element quantitative analysis of the formed alloy and molybdenum plate areas near the interface is given in Fig. 17. It can be seen that the silicon atom ratio of area in the conducting alloy region above the interface is about 35.19%. The molybdenum and aluminum atom ratios are about 7.65% and 6.87%, respectively. While in the molybdenum plate region below the interface, the silicon atom ratio is about 13.95%. And the molybdenum and aluminum atom ratios are about 20.16% and 5.56%, respectively. The results illustrate the phenomenon of atom diffusion (molybdenum, silicon, and aluminum) near the interface between the formed alloy and the molybdenum plate during the short circuit test periods.

VI. Long Term Experimental Validation of IGCT's Short Circuit Characteristics

A. IGCT With Turn-OFF Failure

To ensure the reliable long term short circuit characteristics of IGCT with turn-OFF failure. Another two IGCT samples are tested for more than 12 h under the dc current of 3000 A. The results are shown in Fig. 18(a) and (b). It can be seen that both the samples perform self-triggering effects, which are indicated by the gate-cathode voltages V_{gk} and the recorded voltage drops V_{ak} are stable during the test periods. Pictures of the IGCT samples after the short ciruit test are shown in Fig. 19(a) and (b). The conducting alloy area has been formed around the initial failure point. It is noted that both conducting alloy areas of the tested samples do not spread into the inner cathode rings of the chips. This is the effects of the horizontal resistance R_{56} in the P+ base region and P base regions under the gate contact in Fig. 14(a). Due to this, the nearby cathode cells will be triggered first during the spreading of the conducting alloy area. And the conducting alloy area develops along the circular path in the outer ring region.

B. IGCT With Surge Current Failure

Like IGCT with turn-OFF failure, extra IGCT samples with with surge current failure are prepared are also tested for more than 12 h under the dc current of 3000 A. The final results are shown in Fig. 18(c) and (d). It can be seen that both the gate-cathode voltages V_{gk} of the samples are very low, which mean that the self-triggering effects do not happen. Meanwhile, the recorded voltage drops V_{ak} remain low and stable. Photographs of the IGCT samples after the short circuit tests are shown in Fig. 19(c) and (d). There are multiple conducting alloy areas in both the samples which are distributed evenly in both the inner regions and outer regions.

For the test results of samples with turn-OFF failure, V_{ak} of sample A is a little higher voltage drop than that of sample B and this is mainly caused by the larger spread conducting alloy area in sample B. A similar phenomenon is also observed in the test results of sample C and sample D with surge current failure. Besides, after 7 h of the test, V_{ak} and V_{ag} of sample D both have a sudden drop. As analyzed in Section IV-B, the sufficient melting and diffusion between the silicon wafer and

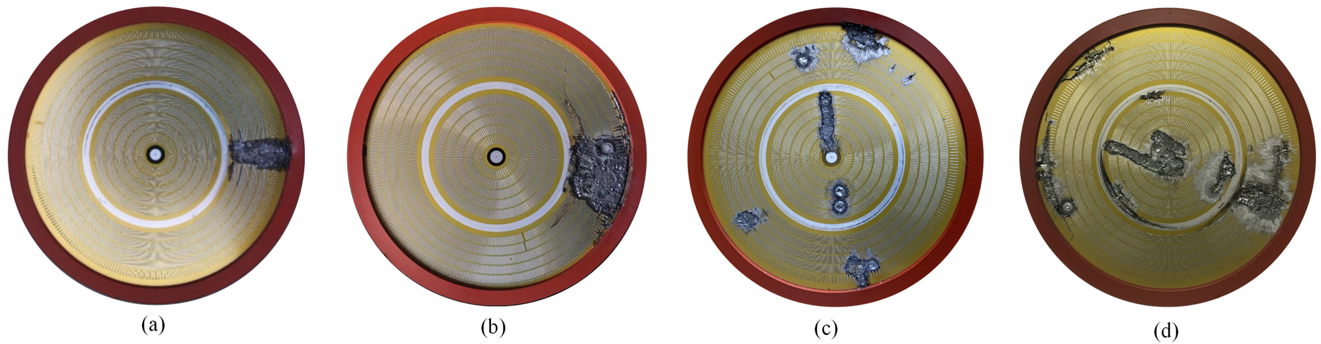


Fig. 19. Pictures of the tested IGCT samples with different failure modes after 12 h test under the dc current of 3000 A. (a) Sample A with turn-OFF failure. (b) Sample B with turn-OFF failure. (c) Sample C with surge current failure. (b) Sample D with surge current failure.

the molybdenum plate in some areas is the main cause and the short current is redistributed after the drop of V_{ak} and V_{ag}.

VII. Conclusion

SCFM of power devices are of vital importance for the reliable and safe operation of MMC-HVdc system. This article gives the comprehensive experiments and analysis of the short circuit characteristics of IGCT with different failure modes for the extreme failure in MMC-HVdc system. And IGCTs of two typical failure modes, including turn-OFF failure, and surge current failure, are compared.

IGCT with turn-OFF failure can conduct a certain short circuit current below 1000 A with the help of the initial destruction area, which is usually located in a single position of the outer regions. As the short current increases, IGCT performs self-triggering effect due to the current injecting into the gate-cathode junction, which is caused by the transient increased temperature in the initial destruction area. Then the undamaged cathode cells help share the short circuit current and the temperature of the whole IGCT tends to be uniform. While for IGCT with surge current failure, the evenly distributed multiple initial destruction areas can share the short circuit current together and the temperature is more uniform than that of IGCT with turn-OFF failure. As a result, it is hard to achieve the self-triggering condition. But the resistance can also be rather low with the formed multiple strong conducting alloy areas. Further long term short circuit tests of IGCTs with both failure modes under 3000 A prove the stable SCFM of IGCT under the extreme failure in MMC-HVdc system.

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