Startup Control to Eliminate Inrush Current for Star-Connected Cascaded H-Bridge STATCOM

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***Abstract*—Soft startup is essential to the operation of the star-connected cascaded H-bridge (CHB) STATCOM. The conventional startup stage involves only uncontrolled rectifier process in which the dc voltages are charged by inserting startup resistors to limit the inrush current. Nevertheless, another inrush current is induced at the beginning of normal operation due to the low charged dc voltages during the startup stage. In this article, to eliminate this inrush current, a novel startup control is proposed for further charging the dc voltages after the uncontrolled rectifier process. During this controlled charging process, the startup resistors are not bypassed so as to smoothen the dc voltages and limit the inrush current. In this scenario, the overall dc voltage control with constant charging current is proposed by establishing a relationship between the overall dc voltage and the positive sequence modulation index. Besides, the cluster dc voltage balancing control based on the negative sequence voltage injection is proposed by redistributing the active power of the STATCOM. Moreover, the charging current is designed to reduce the active power of the startup resistors and increase the charging speed. Due to the flexibility of the startup control, it can be applied to any voltage-source-based ac/dc grid-connected converter. Finally, the performance of the proposed control is verified by the simulation and experimental results.**

***Index Terms*—Cascaded H-bridge (CHB) statcom, controlled charging process, startup control.**

I. Introduction

With THE increasing penetration of renewable energy into the grid, Static Synchronous Compensator (STATCOM) has been widely used in the power system for power factor control and grid voltage regulation [1]–[2]. The star-connected cascaded H-bridge (CHB) converter has been often adopted in medium/high-voltage STATCOM since it features modular structure and lower number of components compared with the other widely used multilevel topologies, such as neutral-point-clamp topologies, flying-capacitors topologies, and modular multilevel converter (MMC) [3], [4]. However, the star-connected CHB STATCOM has separated dc-links, and thus the dc voltage control under the normal operation has been intensively studied [5]–[10]. The hierarchical voltage control structure has been widely employed to control the dc voltages well, which consists of overall dc voltage control, cluster dc voltage balancing control, and cell dc voltage balancing control. Regarding the overall dc voltage control, *dq* frame current controller with proportional–integral (PI) regulator, or *abc* frame current controller with PR regulator are usually adopted to control the total active power from the grid [5]. For the cluster dc voltage balancing control, negative sequence voltage/current, and zero sequence voltage injection are the typical control methods [6], [7]. In [8], in the CHB PV applications, the zero sequence harmonic voltages injection was explored to further enhance the capability of balancing three-cluster active powers. For the cell dc voltage balancing, the control methods can be generally classified into two different categories: sorting algorithm based on the switching redundancies and the active power control by adjusting the modulation reference voltages [9]. Square-wave compensation methods were proposed to extend the operation range for each cell of the PV power generation system [10].

The dc voltage control under the startup stage is more challenging since the initial voltages of dc capacitors are zero, potentially causing serious inrush current at the start point, thereby threatening the stable operation of the system or even damaging the switching devices [10]–[13]. Therefore, to guarantee the normal operation of the CHB STATCOM, the dc capacitors should be charged to their nominal voltage value without any inrush current during the startup stage. To achieve this objective, a straightforward technique employs additional dc source to charge the dc capacitors one-by-one [14], which, however, significantly increases system cost. To reduce the cost, a low-voltage dc source is employed for the MMC to accomplish the precharging by utilizing the existing power devices and filter inductors to configure them into boost circuits [15]. However, the cost is still high and the system structure is also complex. Charging the dc capacitors via the power grid is very suitable for the grid-connected CHB STATCOM. Nonetheless, when the grid-connected contactor is closed, an inrush charging current is induced during the startup stage (named as Startup Inrush Current, SIC) due to 0 V on the dc links. To suppress the SIC, a step-variable soft start control method was proposed for the STATCOM by inserting additional thyristors between the

Manuscript received June 27, 2021; revised September 10, 2021 and October 21, 2021; accepted November 27, 2021. Date of publication December 13, 2021; date of current version January 19, 2022. This work was supported by the National Natural Science Foundation of China under Grant 52007081. Recommended for publication by Associate Editor J. Acero. *(Corresponding author: Haibing Hu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3134278.

Digital Object Identifier 10.1109/TPEL.2021.3134278

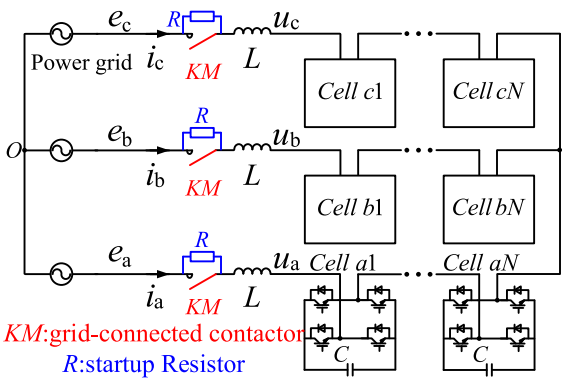

Fig. 1. Circuit configuration of the star-connected CHB STATCOM.

STATCOM and the power grid [16]. Nevertheless, in medium/high-voltage applications, the thyristors with high-voltage stress are expensive. A typical cost-effective method of inserting startup resistors is usually utilized to suppress the SIC [17], as shown in Fig. 1, where the startup resistors (*R*) are paralleled with grid-connected contactors (*KM*). The grid-connected contactors are in an OFF-state at the beginning of startup. Thereupon, the dc capacitors are charged in an uncontrolled way via startup resistors and antiparallel diodes of power switches, until the dc voltages are stable. However, each dc voltage remains far below the nominal voltage, thereby resulting in another inrush current when the CHB STATCOM turns into the normal operation [named as normal operation inrush current, (NIC)] [18]. To limit the NIC, increasing the inductance of the filters is an easy method for CHB STATCOM in practical applications, however, it is costly [5]. To reduce the cost, the grid voltage feedforward compensation method and the slow ramp dc voltage reference method [19] were proposed, respectively. However, the inrush current remains large since the CHB STATCOM fails to generate sufficient voltages by the precharged dc voltages to counteract the grid voltages.

To completely eliminate the NIC, the dc voltages should be further charged after the uncontrolled rectifier process. Many studies introduced a controlled charging process in which *the startup resistors are bypassed* and the gate drives are activated [20]–[25]. In [20], for three-phase two-level PFC rectifier, during the controlled charging process, the dc voltage was boosted by regulating one phase current with only one switch chopping and the controlled phase sequence is determined by the zero-crossing detection of the grid voltages. A duty-cycle soft start control was proposed by linearly ramping up the duty cycle of the switches in lower arms in [21]. However, these control methods require the power transistors to operate at high switching frequency, which is not suitable for the CHB converter with high-power low-frequency IGBTs. Moreover, the control methods are very complex when used for multilevel converters with many switches. For multilevel converters, many researchers have devoted their talents to exploring the startup control. Li *et al.* [22] proposed two closed-loop control methods for MMC applications by linearly charging the dc voltages with a constant charging current from the dc- and ac-side of MMC, respectively. Furthermore, Shi *et al.* [23] derived the small-signal model of the capacitor charging loop, and based on this model, an averaging capacitor voltage control was proposed by implementing a submodule as a boost converter. Wang *et al.* [24] proposed a unified startup strategy for MMC-HVDC based on deadbeat predictive current control from either ac or dc side. Unfortunately, these control methods cannot be applied to CHB STATCOM due to the different structures of MMC and CHB. Zhang *et al.* [25] proposed a generalized precharging strategy by regulating the number of the blocked and bypassed submodules with the capacitor voltage sorting algorithm, which can be applied to any modular converters, such as MMC and CHB. However, this method is an open-loop control and all the capacitors fail to be charged at the same time, increasing the complexity of the voltage balancing control.

In this article, different from the aforementioned methods, the available startup resistors are still inserted during *the controlled charging process*. On this basis, a simple and effective startup control method for the CHB STATCOM is proposed to charge all the dc capacitors to their nominal value without any inrush current during the controlled charging process. Under this new operating condition, the negative sequence voltage injection is further explored to maintain all the dc voltages balanced during the charging process. In addition, the charging current is designed to reduce the active power of the startup resistors and increase the charging speed. Compared with the conventional methods, the proposed method is cost effective with lower dc voltage balancing requirement since all the capacitors are charged at the same time. Besides, the proposed method can be applied to any ac/dc grid-connected converter. Finally, the proposed startup control is validated by the simulation and experimental results.

The rest of this article is organized as follows. The uncontrolled rectifier process of the CHB STATCOM is presented and the cause of the NIC is analyzed in Section II. In Section III, the dc voltage control under the controlled charging process is formulated. In Section IV, the charging current is optimized to achieve a tradeoff between the charging power and the active power of the startup resistor. Section V makes a comparison of the proposed method and the conventional methods. To verify the proposed control, the simulation and experimental results are presented in Sections VI and VII, respectively. Finally, Section VIII concludes this article.

II. Analysis of the NIC

A. System Description

Fig. 1 illustrates the circuit of a general star-connected CHB STATCOM with *N* identical H-bridge cells per cluster. Notably, the grid voltages $e_{\rm k}$ (k = a, b, c) are given as follows:

$$e_{\rm k} = E_{\rm m} \cdot \cos\left(\omega t - x{\cdot}2\pi/3\right) \tag{1}$$

where $x = 0, 1, 2$ for phase a, b, c, respectively. $E_{\rm m}$ denotes the magnitude of three-phase grid voltages. ω is the fundamental frequency of the grid voltages. $u_{\rm k}$ and $i_{\rm k}$ are the three-phase STATCOM voltages and output currents. $U_{\rm dckj}$ (j = 1, …,N) are the dc capacitor voltages of three-phase H-bridge cells. Cluster

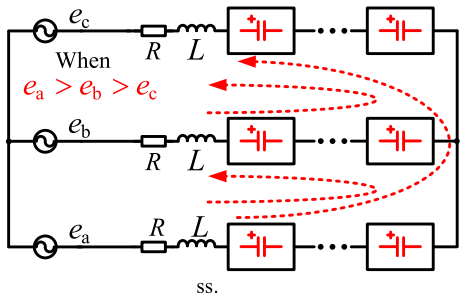

Fig. 2. Uncontrolled rectifier process.

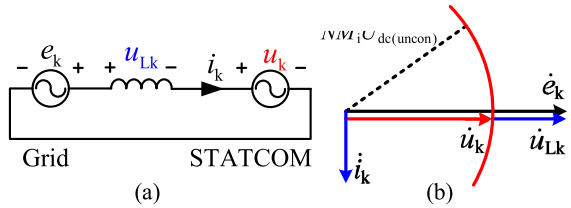

Fig. 3. (a) Equivalent circuit during normal operation. (b) Phasor diagram of the equivalent circuit.

dc voltages U_{dck} are defined as the sum of the dc capacitor voltages in phase k. U_{dcall} is the overall dc voltage, which equals the sum of all the capacitor voltages.

B. Uncontrolled Rectifier Process

Fig. 2 presents the uncontrolled rectifier process when the grid-connected contactors are in an OFF-state and the gate drivers are inactivated. In this scenario, the grid line-to-line voltages charge the dc capacitors of two clusters through the startup resistors and the antiparallel diodes of the switches. Hence, when dc voltages are stable, the dc voltage of each capacitor $U_{\mathrm{dc(uncon)}}$ meets

$$U_{dc(uncon)} \le \sqrt{3}E_m \Big/ (2N). \tag{2}$$

Note that if the dc capacitors are paralleled with bleeder resistors or supply the power to the hardware circuits in practice the dc voltages decrease.

The nominal dc voltage of each capacitor during the normal operation U_{nom} should be designed as

$$U_{nom} = E_m/(N \cdot M_{\mathrm{i}}) \tag{3}$$

where M_{i} ($0 \le M_{\mathrm{i}} \le 1$) is the modulation index. Based on (2) and (3), the relationship between $U_{\mathrm{dc(uncon)}}$ and U_{nom} is derived as

$$U_{dc(uncon)} \le \sqrt{3}M_i U_{nom} \Big/ 2. \tag{4}$$

In (4), M_{i} is usually around 0.9 when CHB STATCOM compensates rated currents; hence, $U_{\mathrm{dc(uncon)}}$ has a more than 22% voltage difference away from nominal voltage U_{nom}.

C. Cause of the NIC

When the dc voltages are stable during the uncontrolled rectifier process, the CHB STATCOM turns into the normal operation in which the startup resistors are bypassed and the gate drivers are activated. To explain the NIC at the start of normal operation, the equivalent circuit and its phasor diagram are illustrated in Fig. 3, where u_{Lk} denote the three-phase inductor voltages and their high switching frequency components are neglected. In Fig. 3(b), the circle represents the output voltage range of STATCOM. To minimize the inductor voltage and limit the STATCOM output current, the STATCOM output voltage should be in phase with the grid voltage and M_{i} is equal to 1. As a result, the amplitude of the inductor voltage U_{L} can be derived as

$$U_L = E_m - NM_{\mathrm{i}}U_{dc(uncon)} \ge 0.134E_m. \tag{5}$$

For multilevel converters, due to the superior harmonic performance, the rated inductor voltage drop is usually designed below 10% of the grid voltage. Hence, according to (5), the NIC will occur at the start of normal operation.

III. Proposed Startup Control Scheme

Based on (3) and (5), charging the dc voltage to its nominal value before normal operation can eliminate the NIC. In addition, the dc voltages of all capacitors should maintain balanced during the charging process to avoid overvoltage protection. Therefore, a controlled charging process is introduced after the uncontrolled process. During the controlled charging process, the typical three-layer control structure, which consists of overall dc voltage control, cluster dc voltage balancing control, and cell dc voltage balancing control is implemented, as illustrated in Fig. 4(a). From Fig. 4(a), moving averaging filter is employed to suppress the double-line frequency ripples of the dc capacitors. The overall dc voltage control charges U_{dcall} to its reference without inrush current by generating the positive sequence modulation voltages (m_{ap}, m_{bp}, m_{cp}), while the negative sequence modulation voltages (m_{an}, m_{bn}, m_{cn}) are regulated for the balance of three-cluster dc voltages. These two-layer control strategies are analyzed and formulated in the following two sections. For the cell dc voltage balancing control, the active voltage vector superposition method, proposed in [26], is adopted to balance the dc voltage of each cell, which is shown in Fig. 4(b). The active voltage means the voltage is in phase with or opposite to the current, and thus it is calculated by multiplying the dc voltage error with the phase current. In addition, the dc voltage feedforward compensation method is introduced in the modulation stage to avoid output voltage and current distortion [27]. Finally, the modulation voltage m_{kj} for each cell is modulated to generate the gate signals by using carrier phase shift (CPS) SPWM.

A. Proposed Overall DC Voltage Control

During the controlled charging process, to further increase the overall dc voltage, active currents should be generated. By analyzing the phasor diagram in Fig. 3(b), active current can be induced if the startup resistor *R* is in series with the inductor. The

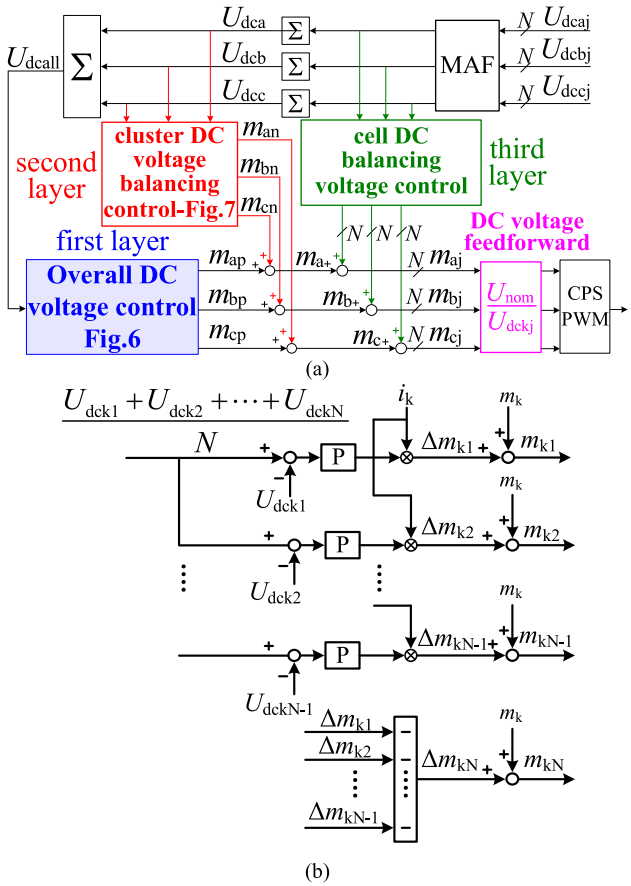

Fig. 4. (a) Whole startup control system. (b) Cell dc voltage balancing control.

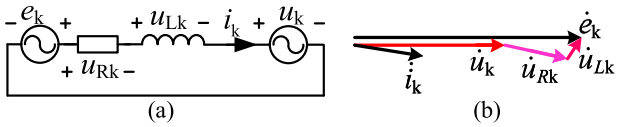

Fig. 5. (a) Equivalent circuit. (b) Phasor diagram when the startup resistors are connected.

equivalent circuit and phasor diagram are redrawn as Fig. 5(a) and (b) where u_{Rk} are the three-phase resistor voltages. Since $R>>\omega L$, the STATCOM almost absorbs active power, which will charge the dc capacitors.

Based on the idea of Fig. 5, the gate drivers are activated while the grid-connected contactors remain in an OFF-state during the controlled charging process. In this scenario, the startup resistors are utilized to generate the active currents and limit the inrush current. Based on Fig. 5, when neglecting the inductor voltages, the amplitude of the active current I_{p} can be derived as

$$I_{\mathrm{p}} = (E_m - NM_{\mathrm{p}}U_{dc(con)})/R \tag{6}$$

where $U_{\mathrm{dc(con)}}$ is the dc voltage of each capacitor during the controlled charging process. M_{p} is the modulation index of the positive sequence modulation voltage. From (6), as the dc voltages increase, the active current gradually decreases. Theoretically, when the active current I_{p} is equal to zero, the

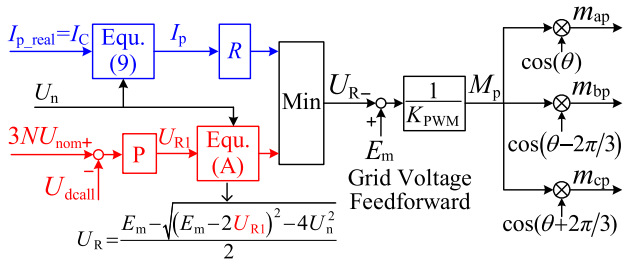

Fig. 6. Proposed overall dc voltage control method.

overall dc voltage is stable which can be derived as

$$U_{dcall} = 3NU_{dc(con)} = 3E_m/M_{\mathrm{p}}. \tag{7}$$

According to (7), the lower the modulation index (M_{p}), the larger the overall dc voltage. Based on this idea, M_{p} can be controlled to charge the overall dc voltage to its nominal value. However, in practice, the active current I_{p} is higher than zero in steady state since the negative sequence voltage from the second layer, interacting with the negative sequence current, will reduce the charging power of the dc capacitors. Therefore, the practical charging current should take into account the active power generated by negative sequence voltage and current, which can be considered as a perturbation. Based on principle of conservation of energy, the practical charging current (denoted as $I_{\mathrm{p\_real}}$) meet

$$\frac{(E_{\mathrm{m}} - I_p R)\cdot I_p}{2} - \frac{U_{\mathrm{n}}^2}{2R} = \frac{(E_{\mathrm{m}} - I_{p\_real} R)\cdot I_{p\_real}}{2} \tag{8}$$

where U_{n} is the amplitude of negative sequence voltage, which is derived in the next section. Based on (8), the relationship between the practical charging current $I_{\mathrm{p\_real}}$ and the active power current I_{p} can be derived as

$$I_p = \frac{E_{\mathrm{m}} - \sqrt{(E_{\mathrm{m}} - 2I_{p\_real}R)^2 - 4U_{\mathrm{n}}^2}}{2R}. \tag{9}$$

Based on (6) and (9), a closed-loop control scheme with a constant charging current is proposed, as shown in Fig. 6 where I_{C} is the constant charging current, K_{PWM} is the gain of the modulation stage, which is equal to the cluster dc voltage when CPS PWM is used, U_{R} is the amplitude of three-phase resistor voltages, and θ is the phase angle of the A-phase grid voltage.

As observed from Fig. 6, the regulation of the startup resistor voltage U_{R} has two branches, the bule one and red one. The bule branch represents the open-loop control with constant resistor voltage output, and the red branch represents the closed-loop control. At first, the overall dc voltage error is very large, leading to high output of high P regulator. Therefore, the open-loop control with constant output voltage is selected via Min function, which generates constant charging current. As the overall dc voltage increases and becomes close to its reference, the P regulator works and the closed-loop control is selected to maintain the overall dc voltage. Note that (A) in Fig. 6 is introduced to directly eliminate the perturbation of the negative sequence voltage, whose derivation is similar to (9). Finally, the trigonometric values (cos) make the STATCOM voltages

in phase with the grid voltages, thereby generating the positive sequence voltages.

B. Proposed Cluster DC Voltage Balancing Control

Ideally, the cluster dc voltage balancing control can be removed since all the capacitors are charged at the same time. However, in practice, the active power losses of the cells are unbalanced due to the nonuniformity of the IGBTs, the bleeder resistors and the active powers supplied for the hardware circuit of all cells. Besides, the active powers of the cells absorbed from the ac side are imbalanced due to the nonuniformity of the capacitors and the PWM signal delay time. Therefore, under serious conditions, the dc voltages deviate from each other during the controlled charging process, thereby causing the overvoltage protection and reducing the system reliability. Although the serious condition rarely happens, once it happens, the STATCOM must halt and we need to sort all the cells to maintain their balance, which is an extremely heavy work. Hence, to avoid the unnecessary shutdown and improve the STATCOM performance, a superior startup control should contain the voltage balancing control to maintain all the dc voltage balanced. Negative or zero sequence voltage injection is the typical cluster dc voltage balancing methods by redistributing three-cluster active powers. Nevertheless, the output currents are very limited during the startup stage, which lowers the active power regulating capability of the zero-sequence voltage injection method. Hence, the negative sequence voltage injection is adopted for the cluster dc voltage balancing during the startup stage, while the zero-sequence voltage injection is adopted during the normal operation due to the considerable output currents and good power quality for the grid.

Unfortunately, the conventional negative sequence injection methods under normal operation cannot be applied to this new operating condition with the connection of the startup resistors in the system. There are two major differences between the normal operation and the startup process, listed as follows.

1) In normal operation, the active power of the STATCOM is equal to that absorbed from the grid in each phase. However, in this startup process, the startup resistors in the main circuit generate three-phase unbalanced active powers due to the unbalanced three-phase currents. Therefore, we inject the negative sequence voltages to redistribute only the three-phase active powers of the STATCOM instead of the active powers from the grid.
2) In normal operation, the reactive current leads or lags the positive sequence voltage by 90°, and the negative sequence current lags the negative sequence voltage by 90° under balanced grid. However, in this startup process, the positive and negative sequence currents are both in phase with the positive and negative sequence voltages, respectively. As a result, the active powers redistributed by the negative sequence voltages are changed.

On this basis, a new negative sequence voltage injection method is formulated by deriving the input active powers of the STATCOM in the following.

When the negative sequence voltage is injected into the STATCOM, the three-phase output voltages and currents are expressed in the *dq* frame as given as follows:

$$\begin{aligned}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} &= \begin{bmatrix} x_{ap} \\ x_{bp} \\ x_{cp} \end{bmatrix} + \begin{bmatrix} x_{an} \\ x_{bn} \\ x_{cn} \end{bmatrix} \\ &= \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \cos(\omega t - 2\pi/3) & -\sin(\omega t - 2\pi/3) \\ \cos(\omega t + 2\pi/3) & -\sin(\omega t + 2\pi/3) \end{bmatrix} \begin{bmatrix} X_{dp} \\ X_{qp} \end{bmatrix} \\ &\quad + \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \cos(\omega t + 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t - 2\pi/3) & \sin(\omega t - 2\pi/3) \end{bmatrix} \begin{bmatrix} X_{dn} \\ X_{qn} \end{bmatrix} \\ x = u, i; X &= U, I \end{aligned} \tag{10}$$

where subscripts *p* and *n* denote the positive and negative sequence components, respectively; subscripts *d* and *q* denote the components in the *d*- and *q*-axis, respectively.

Based on (10), the input active powers of the STATCOM generated by the interaction between the positive sequence voltage and negative sequence current, and negative sequence voltage, and positive sequence current are expressed as (11), where P_{kn} are three-phase input active powers generated by the negative sequence components. Noted that the three-phase active powers generated by the interaction between the negative sequence voltage and current do not affect the balance of three-cluster dc voltages since they are equal and only affect the overall dc voltage.

$$P_{\mathrm{kn}} = \frac{\omega}{2\pi} \int_0^{2\pi/\omega} (u_{\mathrm{kn}} \cdot i_{\mathrm{kp}} + u_{\mathrm{kp}} \cdot i_{\mathrm{kn}}) dt. \tag{11}$$

In (11), the positive and negative sequence currents can be derived by the positive and negative sequence voltages based on Kirchhoff's voltage law, as shown in (12). Note that the inductor voltages are neglected since impedance $R >> \omega L$.

$$I_{dp} = \frac{E_{\mathrm{m}} - U_{dp}}{R}, I_{qp} = \frac{-U_{qp}}{R}, I_{dn} = \frac{-U_{dn}}{R}, I_{qn} = \frac{-U_{qn}}{R}. \tag{12}$$

Substituting (10) and (12) into (11) yields

$$\begin{aligned}&\begin{bmatrix} P_{an} \\ P_{bn} \\ P_{cn} \end{bmatrix} \\ &= \frac{1}{4R} \begin{bmatrix} 2E_m - 4U_{\mathrm{dp}} & 2U_{\mathrm{qp}} \\ 2U_{\mathrm{dp}} - E_m + 2\sqrt{3}U_{\mathrm{qp}} & 2\sqrt{3}U_{\mathrm{dp}} - \sqrt{3}E_m - 2U_{\mathrm{qp}} \\ 2U_{\mathrm{dp}} - E_m - 2\sqrt{3}U_{\mathrm{qp}} & \sqrt{3}E_m - 2\sqrt{3}U_{\mathrm{dp}} - 2U_{\mathrm{qp}} \end{bmatrix} \\ &\quad \begin{bmatrix} U_{dn} \\ U_{qn} \end{bmatrix}. \end{aligned} \tag{13}$$

As observed from (13), P_{kn} are unequal but their summation is equal to zero, which indicates that three-phase active powers generated by the negative sequence components are capable of balancing three-cluster dc voltages by redistributing the overall active power among three clusters. To simplify (13), based on Fig. 7, by using PARK transformation, the positive sequence

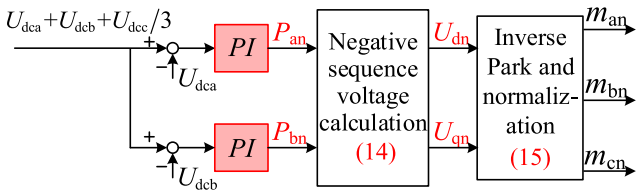

Fig. 7. Proposed cluster dc voltage balance control method.

voltage ($U_{\rm dp}$, $U_{\rm qp}$) can be derived as follows:

$$U_{dp} = M_{\rm p} \cdot K_{\rm PWM}, U_{qp} = 0. \tag{14}$$

Therefore, based on (13) and (14), the negative sequence voltage ($U_{\rm dn}$, $U_{\rm qn}$) is derived as

$$\begin{bmatrix} U_{dn} \\ U_{qn} \end{bmatrix} = \begin{bmatrix} \frac{2R}{E_{\rm m}-2M_{\rm p}K_{\rm PWM}} & 0 \\ \frac{2R}{2\sqrt{3}M_{\rm p}K_{\rm PWM}-\sqrt{3}E_{\rm m}} & \frac{4R}{2\sqrt{3}M_{\rm p}K_{\rm PWM}-\sqrt{3}E_{\rm m}} \end{bmatrix} \begin{bmatrix} P_{\rm an} \\ P_{\rm bn} \end{bmatrix}$$

$$U_n = \sqrt{U_{dn}^2 + U_{qn}^2}. \tag{15}$$

Based on (15), $U_{\rm dn}$ and $U_{\rm qn}$ are normalized with respect to $K_{\rm PWM}$ and then by using inverse Park transformation, the negative sequence modulation reference voltages in the *abc* frame are obtained as

$$\begin{bmatrix} m_{an} \\ m_{bn} \\ m_{cn} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \cos(\omega t + 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t - 2\pi/3) & \sin(\omega t - 2\pi/3) \end{bmatrix} \begin{bmatrix} U_{dn}/K_{\rm PWM} \\ U_{qn}/K_{\rm PWM} \end{bmatrix}. \tag{16}$$

In (15) and (16), only the active powers in phase A and B are utilized, which decouples the cluster dc voltage balancing control from the overall dc voltage control. To achieve the active powers of phase A and B in (15), the PI regulators are applied on the cluster dc voltage errors. As a result, the cluster dc voltage balancing control is proposed as shown in Fig. 7.

In summary, the whole startup stage, including the uncontrolled and controlled charging process, can be illustrated in the flowchart shown in Fig. 8. Based on the proposed control implemented during the controlled charging process, all capacitor dc voltages can be charged to the nominal values. Then, the grid-connected contactors are closed and the CHB STATCOM turns into the normal operation in which the dc voltages and the output currents are controlled by the dc voltage and current dual closed-loop control [7].

C. Stability Analysis of the Proposed Startup Control Strategy

Based on the aforementioned analysis, the first layer, overall dc voltage control, regulates the positive sequence voltage, while the negative sequence voltage is regulated in the second layer to balance three-cluster dc voltages. The active powers generated by positive and negative sequence components are shown in

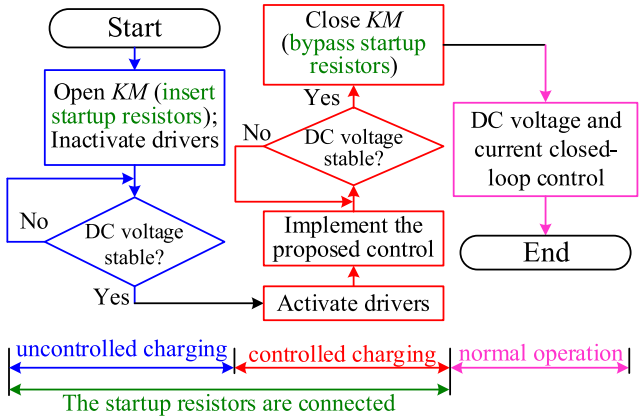

Fig. 8. Flowchart of the whole startup stage.

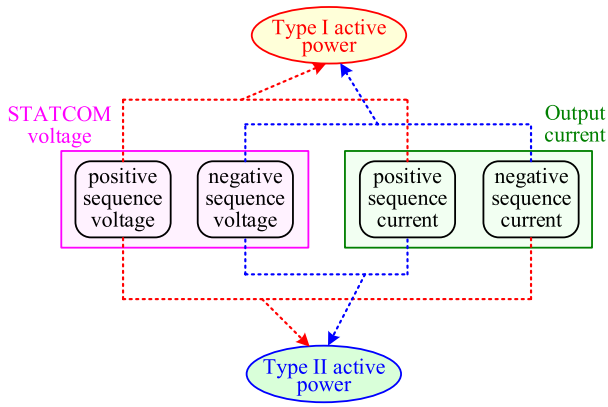

Fig. 9. Interaction between the positive sequence components and negative sequence components.

Fig. 9. As observed, type I active power, generated by the interaction between the positive sequence voltage and current, or the negative sequence voltage and current, features that three-phase active powers are equal. Type II active power, generated by the interaction between the positive sequence voltage and negative sequence current, or negative sequence voltage and positive sequence current, features that three-phase active powers are unequal but their summation equals zero. Therefore, positive sequence voltage and current are controlled to regulate the type I active power in the overall dc voltage control, while based on the positive sequence voltage and current, negative sequence voltage and current are controlled to regulate the type II active power to realize the balance of three-cluster dc voltages. The type II active power does not affect the type I active power since the sum of three-phase type II active powers equals zero. However, the negative sequence voltage and current from the cluster voltage balancing control will generate the type I active power to disturb the overall dc voltage control, which can be considered as a perturbation. Therefore, the overall dc voltage control takes the negative sequence voltage into account to eliminate this active power perturbation.

For the third layer control, the active voltage vector superposition method is employed to balance cell dc voltage, which is

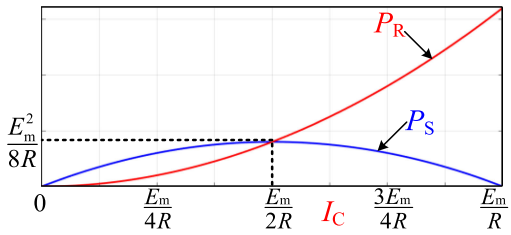

Fig. 10. Relationship between the active powers P_S (P_R) and I_C.

shown in Fig. 4(b). As observed, the sum of all the superposed active voltage vector Δm_{kj} is equal to zero, which does not change m_k. That is, the cell dc voltage balancing control is decoupled from the cluster dc voltage balancing control. In conclusion, the proposed startup control scheme has a good stability.

IV. Design of the Charging Current

According to (6) and Fig. 6, to increase the charging power and shorten the charging time of dc capacitors, the charging current can be increased by reducing the STATCOM voltages. Nevertheless, the increased charging current may reduce the absorbed active power of STATCOM, which approximately equals the charging power of dc capacitors. In particular, when the STATCOM voltage is reduced to zero, the charging current is very high while the charging power is equal to zero. Moreover, a high charging current also increases the active power of the startup resistors, thus increasing the volume and cost of the startup resistors. Therefore, to increase the charging power and reduce the active power of the startup resistor, the constant charging current I_C in Fig. 6 should be designed.

Assuming that the active powers among three clusters are balanced, the charging power of dc capacitors and the active power of the startup resistor in each phase are expressed as

$$P_S = (E_m - I_C R) \cdot I_C/2, P_R = {I_C}^2 R/2 \tag{17}$$

where Ps and P_R denote the charging power and the active power of the startup resistor in each phase, respectively. The charging power in (17) determines the charging time. Assuming there is no power loss in the dc links, the charging time can be derived as follows with the law of energy conservation:

$$T_s = \frac{N \cdot C\left(U_{nom}^2 - U_{dc(uncon)}^2\right)}{(E_m - I_C R) \cdot I_C} \tag{18}$$

where T_s is the charging time of the dc capacitors, which can be considered as a function of I_C. C is the capacitance of the dc capacitor of each cell.

Based on (17), P_S and P_R can be considered as the functions of I_C. Hence, P_S and P_R with varying value of I_C are plotted as Fig. 10. As seen from Fig. 10, when I_C increases from 0 to $E_m/2R$, the charging power P_S and the active power of the startup resistor P_R both increase. As I_C increases from $E_m/2R$ to E_m/R, P_R still increases but P_S is reduced. That is, compared with the range [$E_m/2R$, E_m/R], when the I_C is limited into the range [0, $E_m/2R$], the dc capacitors can be charged with the same P_S but with lower active power of the startup resistors. Therefore, the constant charging current I_C in Fig. 6 must be less than $E_m/2R$. On this basis, when I_C is equal to $E_m/2R$, the charging time and the active power of startup resistor are maximum (denoted as T_{s_max} and P_{R_max}), which can be derived as

$$\begin{aligned} T_{s\_max} &= 4N \cdot R \cdot C\left(U_{nom}^2 - U_{dc(uncon)}^2\right)\Big/\left(E_m^2\right) \\ P_{R\_max} &= E_m^2/(8R). \end{aligned} \tag{19}$$

To further determine the constant charging current I_C, the P_S and P_R are analyzed at the range $I_C \in [0, E_m/2R]$. In fact, when I_C varies from 0 to $E_m/2R$, we expect that P_S becomes larger to reduce the charging time of all dc capacitors while P_R becomes smaller to reduce the cost and volume. However, P_S and P_R both exhibit a monotone increasing trend when $I_C \in$ [0, $E_m/2R$] according to Fig. 10. When I_C is equal to $E_m/2R$, the charging power is maximum at the cost of large active power of the startup resistors. When I_C equals 0, the active power of the startup resistors is reduced to zero but the charging power is also reduced to zero. Therefore, the I_C should be designed to achieve a tradeoff between the charging power of the dc capacitors and the active power of the startup resistors.

In practical applications, to achieve the tradeoff, the upper limits of the active power of startup resistor and the charging time (denoted as P_{R_up} and T_{s_up}, respectively) are provided as constrains of I_C. Based on (18), T_s is lower than T_{s_up}, which yields

$$\begin{aligned} T_s = \frac{N \cdot C\left(U_{nom}^2 - U_{dc(uncon)}^2\right)}{(E_m - I_C R) \cdot I_C} \le T_{s\_up} \le T_{s\_max} \\ I_C \in \left[0\ E_m/2R\right]. \end{aligned} \tag{20}$$

Based on (20), the lower limit of charging current (denoted as I_{C_low}) can be solved as

$$I_C \ge I_{C\_low} = \frac{E_m - \sqrt{E_m^2 - \frac{4RNC\left(U_{nom}^2 - U_{dc(uncon)}^2\right)}{T_{s\_max}}}}{2R}. \tag{21}$$

Moreover, the active power of startup resistor P_R is lower than P_{R_up}, leading to the upper limit of the charging current I_{C_up} as follows:

$$I_C \le I_{C\_up} = \sqrt{2P_{R\_up}/R}, (P_{R\_up} \le P_{R\_max}). \tag{22}$$

As a result, the range of I_C are obtained. In practice, I_{C_low} may be higher than I_{C_up}, which requires the engineers to increase the active power of the startup resistor or the charging time until I_{C_up} is higher than I_{C_low}.

V. Comparison With the Conventional Startup Control Methods

To clarify the advantages of the proposed control, a comparison of the proposed control method and the conventional control methods is summarized in Table I .

The method in [14] employs an additional dc source to charge the dc capacitors one-by-one, where the dc source voltage is equal to the nominal voltage of cell capacitors. When this method

TABLE I
Comparison of the Proposed Control Method and the Conventional Control Methods

Method	Cost	Inrush current	Requirements for voltage balance	Charging speed	Applications
Ref [14]	High	None	Medium	Slow	All AC/DC grid-connected converters
Ref [15]	Medium	None	Medium	Slow	All AC/DC grid-connected converters
Ref [19]	Low	High	Low	Fast	All AC/DC grid-connected converters
Ref [25]	Low	Medium	High	Medium	AC/DC converters with modular structure
Ref [22]	Low	None	Low	Fast	Only MMC
Ref [28]	High	None	Low	Medium	Transformerless hybrid active power filter
This paper	Low	None	Low	Medium	All AC/DC grid-connected converters

TABLE II
Circuit Parameters for Simulation Results

Variable	Symbol	Value
Nominal DC voltage	U_{nom}	750 V
Cascaded cell number	N	12
AC filter inductor	L	20 mH
DC capacitor	C	1 mF
Startup resistor	R	1 kΩ

TABLE III
Circuit Parameters for Experimental Results

Variable	Symbol	Value
Nominal DC voltage	U_{nom}	85 V
Cascaded cell number	N	5
AC filter inductor	L	6 mH
DC capacitor	C	3 mF
Startup resistor	R	20 Ω

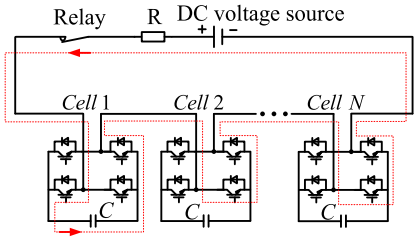

Fig. 11. Startup method in [14].

is applied to the CHB STATCOM, the charging process of each phase can be illustrated as Fig. 11. From Fig. 11, when the cell 1 is blocked and all other cells are bypassed, the capacitor of the cell 1 gets charged. Following this principle, all the capacitors can be charged one-by-one. However, the precharging process takes too long especially when the number of the cells is large. In addition, the cost is increased compared with the case of inserting the startup resistors.

To reduce the cost of above-mentioned startup method, a low-voltage dc source is employed to accomplish the precharging by utilizing the existing power devices and filter inductors to configure them into boost circuits [15]. As shown in Fig. 12, to charge the capacitor of the cell 1 to the nominal value, the cell 1 works in PWM mode while all other cells remain bypassed. The other capacitors can be charged by the similar way. Nevertheless, all the capacitors are not charged at the same time, which makes all the capacitor voltages imbalanced.

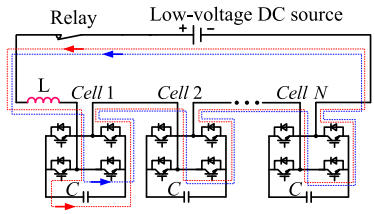

Fig. 12. Startup method in [15].

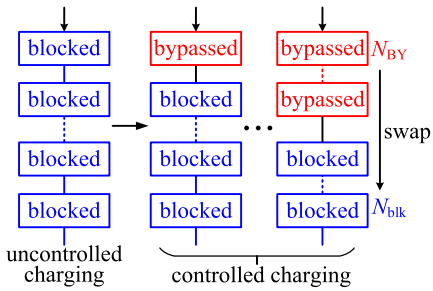

Fig. 13. Startup method in [25].

A dc voltage slope controller is proposed in [19] based on the conventional fixed voltage controller to suppress the inrush current, which increases the dc voltage reference from the initial value to the setting reference with a certain slope. This method is a fast startup method since the CHB STATOCM directly turns into the normal operation after the uncontrolled rectifier process. However, the inrush current still exists due to the large difference between the cluster dc voltage and the peak value of grid voltage at the beginning of normal operation. In addition, the precharging control is applied to only the two-level converter. This article is the further study of [19], and a new startup method is proposed for the multilevel converter (i.e., CHB) by inserting the startup resistors during the controlled charging process. Thereupon, not only the overall dc voltage control but also the dc voltage balancing control is proposed to evenly charge all the capacitors to their nominal value without any inrush current, which achieves the safe and reliable startup of the CHB STATCOM.

The method in [25] is suitable for the ac/dc multilevel converters with modular structure, which gradually increases the number of the bypassed cells to charge the capacitor voltage of the blocked cells after the uncontrolled rectifier process, as shown in Fig. 13. However, all the capacitors fail to be charged

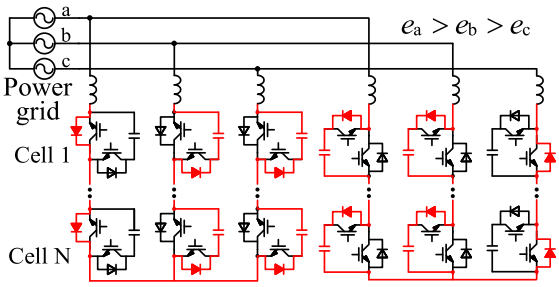

Fig. 14. Startup method in [22].

at the same time, which makes the dc voltage balancing control more challenging.

The method in [22] takes full advantage of the topology structure of MMC. As shown in Fig. 14 where the red lines represent the current paths, the MMC is considered as two CHB converters with half bridge cells, and thus the capacitor voltage is doubled compared with that of CHB converter with full bridge cells during the uncontrolled charging process. Hence, the filter currents can be controlled to further charge all the capacitors by dividing the grid voltages into six regions. However, this method is limited to the MMC applications.

The method in [28] charges the dc voltages to their nominal value by controlling the reactive power without inrush current since the ac capacitor filters in the main circuit offer high impedance to the fundamental grid voltage. However, this method is only suitable for the transformerless hybrid active power applications since the ac capacitor filters are available. If this method is applied to the CHB STATCOM, additional ac capacitors should be inserted, which significantly increases the cost and volume of the system.

Compared with the conventional methods, the proposed method has the following features.

1) Without introducing any additional dc sources, the proposed method can completely eliminate the inrush current by inserting the startup resistors during the controlled charging process.
2) The proposed method charges all the capacitors at the same time, lowering the requirement for dc voltage balancing. Ideally, the dc voltage balancing control can be removed, which highly reduces the control complexity of the system.
3) Although the startup resistors limit the charging currents and reduce the charging speed of the capacitors, all the capacitors are charged at the same time, which is advantageous when the number of the cells is large.
4) Due to the inserted startup resistors the STATCOM can absorb the active power from the grid to charge the capacitors, which is independent of the topology structure. Hence, the proposed method can be applied to any ac/dc grid-connected converters.

VI. Simulation Results

A star-connected CHB STATCOM rated at 1 MVAr/10 kV was simulated using MATLAB/Simulink to verify the proposed startup control strategy. The circuit parameters are listed in Table II.

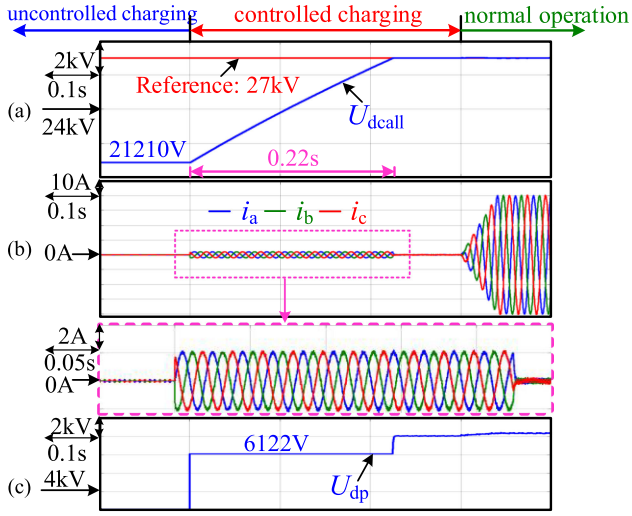

Fig. 15. Simulation waveforms with the proposed overall dc voltage control when $I_C = E_m/4R$.

A. Verification of the Proposed Overall DC Voltage Control

To verify the proposed overall dc voltage control, three comparative cases with different charging current were carried out in the following.

Case I: I_C equaled $E_m/4R$ (2 A). As shown in Fig. 15, the waveforms are divided into three stages. During the uncontrolled charging stage, the overall dc voltage can be stable at 21 210 V, as shown in Fig. 15(a). Then, the CHB STATCOM turns into the controlled charging stage where the proposed control method is implemented. Therefore, the overall dc voltage is linearly charged and reaches to the nominal value of 27 kV after about 0.22 s, which is close to the theoretical value of 0.21 s calculated by (18). This linear and fast charging is attributed to the constant active currents with the amplitude of 2 A, as shown in Fig. 15(b). Note that there is no inrush current induced due to the startup resistors. The active power of each startup resistor is 4 kW (0.4% of the rated reactive power). From Fig. 15(c), during the rise process of the overall dc voltage the STATCOM voltage (U_{dp}) is controlled to be $3E_m/4$ (6123 V), while U_{dp} is equal to E_m when the overall dc voltage is stable. Finally, the CHB STATCOM turns into the normal operation stage in which the reactive currents are controlled without NIC, as shown in Fig. 15(b), which is due to the high STATCOM voltage U_{dp} generated by the nominal dc voltages, as shown in Fig. 15(c).

Case II: I_C equaled $E_m/2R$ (4 A). According to the analysis in Section IV, the charging power reaches the maximum value, reducing the charging time of dc capacitors. However, the active power of the startup resistors is increased. As shown in Fig. 16(a), when the STATCOM turns into the controlled charging stage, the charging time shortens to 0.17 s, which is a reduction of 26% compared with the charging time in Fig. 15(a). However, the active currents are doubled, as shown

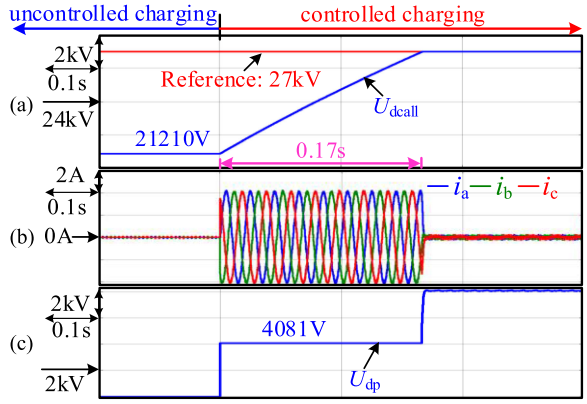

Fig. 16. Simulation waveforms with the proposed overall dc voltage control when $I_C = E_m/2R$.

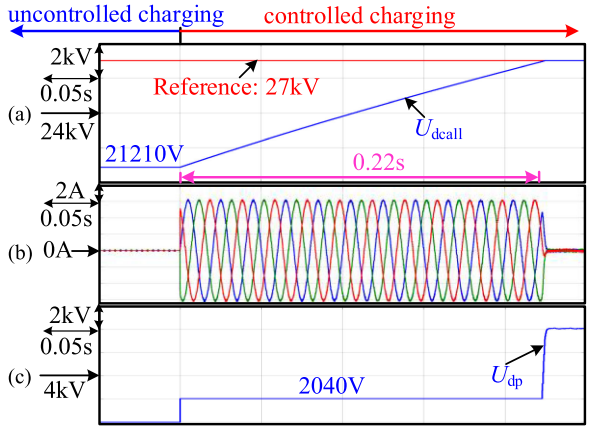

Fig. 17. Simulation waveforms with the proposed overall dc voltage control when $I_C = 3E_m/4R$.

in Fig. 16(b), thereby increasing the active power of the startup resistors by 300% compared with the case in Fig. 15(b). Fig. 16(c) shows the STATCOM voltage U_{dp}, which is equal to $E_m/2$ (4081 V).

Case III: We further increased the charging current I_C to $3E_m/4R$ (6 A). According to the analysis of Fig. 10, the charging powers are same when I_C is equal to $E_m/4R$ and $3E_m/4R$. Therefore, as shown in Fig. 17(a), the charge time of the dc capacitors is equal to 0.22 s, which is same as the case in Fig. 15(a). However, as shown in Fig. 17(b), the amplitude of the active current reaches up to 6 A that is three times larger than that in Fig. 15(b). Hence, the active power of the startup resistors are nine times larger than that in case *I*. Therefore, I_C should be limited into the range [0, $E_m/2R$].

B. Verification of the Cluster DC Voltage Balancing Control

To verify the proposed cluster dc voltage balancing control during the controlled charging process, the CHB STATCOM deliberately connected different power resistors to the dc-link of each H-bridge cell (phase A: 4 kΩ, phase B: 50 kΩ, phase C: 50 kΩ, for each cell). In addition, the three-phase startup resistors were deliberately set to be 0.9, 1, and 1.1 kΩ. As shown in Fig. 18(a), during the uncontrolled charging process, cluster dc

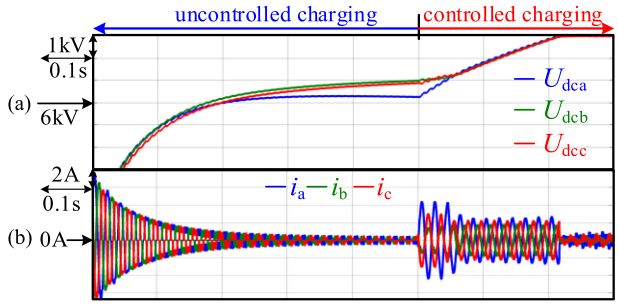

Fig. 18. Simulation waveforms with the proposed cluster dc voltage balancing control.

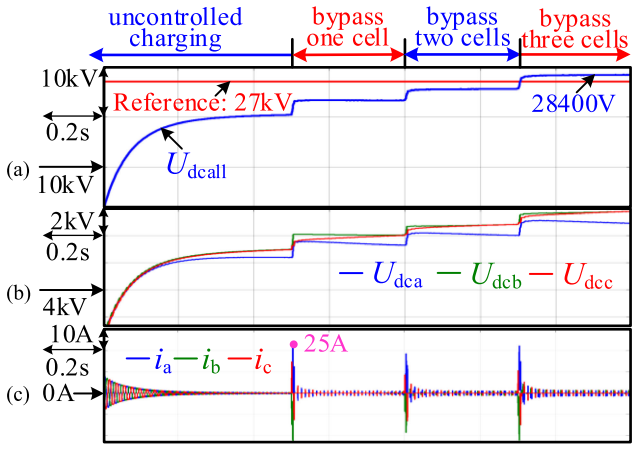

Fig. 19. Simulation waveforms with the typical startup control [25].

voltage in phase A deviates from those in phase B and C due to the different power losses in dc-links. When the STATCOM turns into the controlled charging process with the implementation of the proposed cluster dc voltage balancing control, three-cluster dc voltages begin to converge and balance, which is achieved by the injection of the negative sequence voltage and current. The three-phase unbalanced currents are shown in Fig. 18(b).

To compare the proposed startup control with the typical method presented in [25], which has been widely used in MMC applications, another simulation was carried out with the same operating conditions in Fig. 18. The idea of the typical startup control is based on the control of the number of blocked and bypassed cells. As shown in Fig. 19(a), after the uncontrolled charging process, the grid-connected contactors are closed and then a part of cells are bypassed by means of dynamic grouping. Note that the startup resistors are bypassed to avoid long charging time after bypassing each cell or swapping the cells since the startup resistors significantly limit the charging current. As analyzed in (2), the overall dc voltage is charged as the number of bypassed cells in each phase increases. When three cells are bypassed in each phase, the overall dc voltage reaches 28 400 V but it cannot be accurately controlled to its reference. Fig. 19(b) shows the three-cluster dc voltages, which cannot be balanced by the control method. As shown in Fig. 19(c), inrush currents with an amplitude of 25 A are generated at the instant of bypassing the cells. Although the peak value is lower than the rated current value, it is unfavorable for the system reliability.

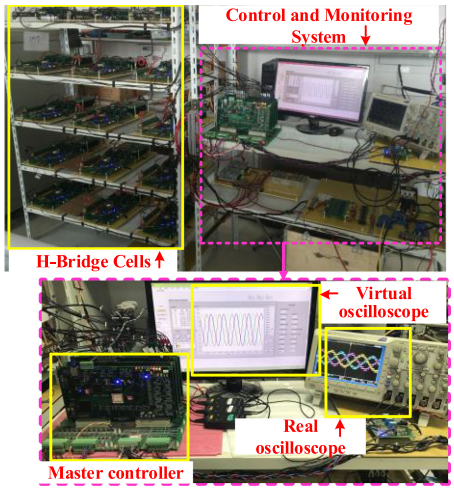

Fig. 20. Schematic diagram of the experimental test bench.

VII. Experimental Results

To verify the proposed startup control experimentally, a three-phase down-scaled star-connected CHB STATCOM rated at 380 V/7.5 kVAr was designed, as shown in Fig. 20, whose circuit parameters are listed in Table III. With regard to the control system, the DSP (TMS320F28335) and FPGA (EP3C25Q240C8N) were integrated for the master controller and CPLD (10M02SCE144C8G) for the cell controller. Currents and voltages were sampled by the DSP and FPGA-based controllers and all the sampled signals were sent to the computer via Ethernet. To display the currents and voltages, besides the real oscilloscope, a virtual oscilloscope was developed in LabVIEW.

Fig. 21 shows the performance of the overall dc voltage control method, where the voltage balancing controls from the second and third layers were removed since all the dc capacitors are charged at the same time with lower requirement for voltage balancing. From Fig. 21(a), the overall dc voltage can only be precharged to 788 V in the beginning. Then, the CHB STATCOM turns into the controlled charging process when the proposed control method is implemented ($I_C = E_m/4R$). As shown, during the whole controlled process, the overall dc voltage is charged smoothly and stabilized at the nominal value of 1275 V after about 0.076 s, which is basically same with the theoretical value of 0.075 s calculated by (18), while the inrush current is eliminated and the peak value of the active currents is about 3.9 A, as shown in Fig. 21(b). Fig. 21(c) shows three-phase cluster dc voltages, which are almost balanced even if the cluster balancing control was absent. In addition, all the cell dc voltages are stable with maximum 1 V voltage difference due to the inherent discrepancies of all the cells, as shown in Fig. 21(d)–(f). After the controlled charging process, the CHB STATCOM turns into the normal operation, where the phase currents are controlled without NIC since the CHB STATCOM can generate sufficient voltages by the nominal dc voltages, as shown in Fig. 21(b). Under the normal operation, since another control scheme [7] was implemented, the reactive current command I_q was set to zero at first, where the CHB STATCOM mainly controlled the dc voltage. To guarantee the

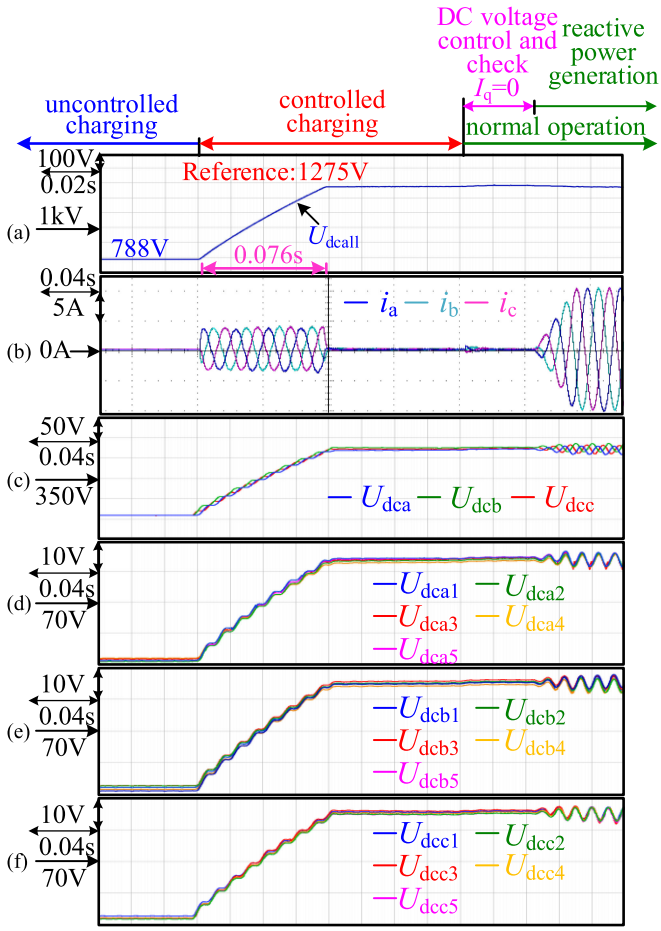

Fig. 21. Experimental waveforms with the proposed overall voltage control.

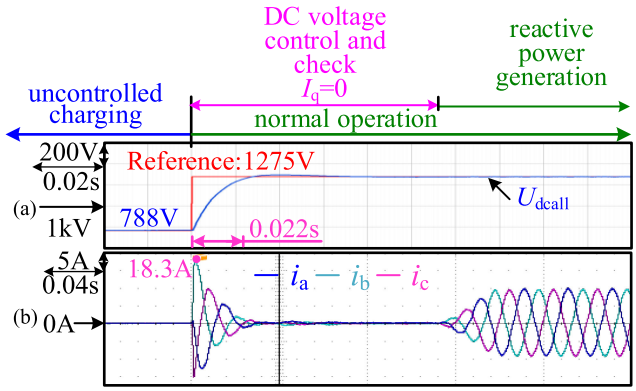

Fig. 22. Experimental waveforms with the conventional control [17].

reliable compensation of reactive current, the STATCOM did many checks during this time, such as the state of hardware, the stability and balance of all dc voltages, etc. Then, if everything was ready, the reactive current command was implemented.

To compare the proposed control with the conventional control presented in [17], another experimental test was conducted, as shown in Fig. 22 where the controlled charging process is removed. As seen, after the uncontrolled charging process, the CHB STATCOM directly turns into normal operation where the startup resistors were bypassed, and the overall dc voltage is

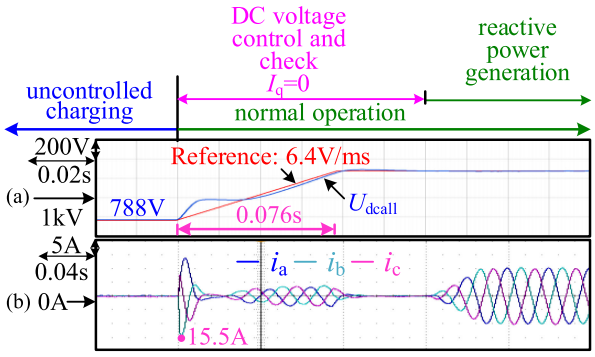

Fig. 23. Experimental waveforms with the conventional control [19].

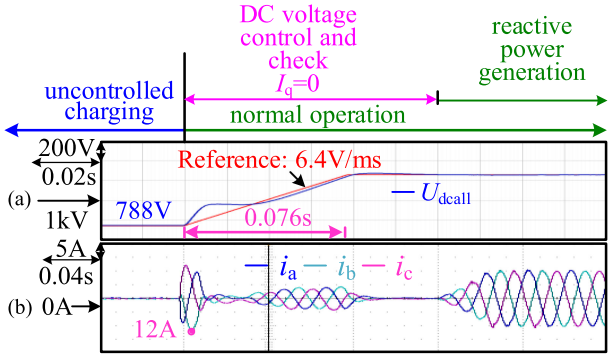

Fig. 24. Experimental waveforms with the increased inductance.

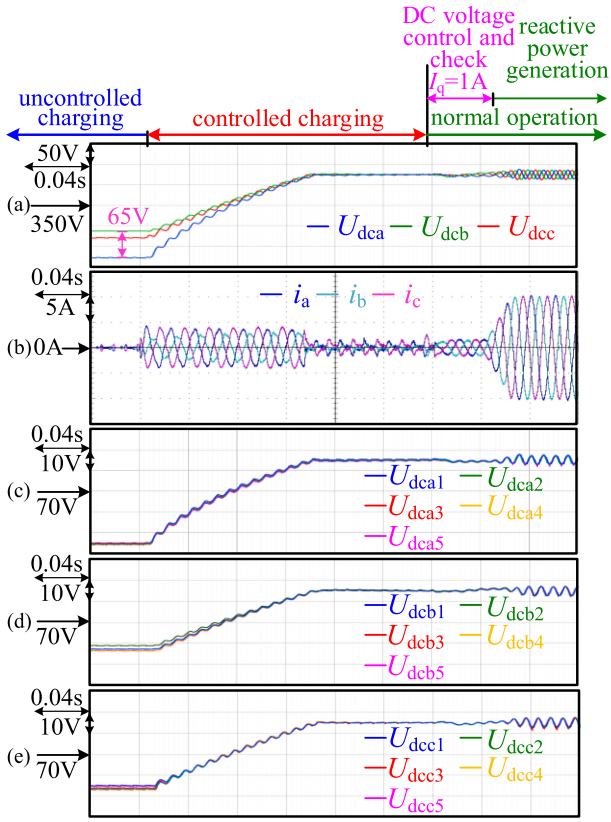

Fig. 25. Experimental waveforms with the proposed cluster dc voltage balancing control.

charged to the nominal value with only 0.022 s, much faster than that in Fig. 21(a) (0.076 s). However, as shown in Fig. 21(b), the peak value of the NIC is up to 18.3 A, much larger than that in Fig. 21(b), thereby seriously threatening the system safety.

For further comparison with the conventional method, another experimental test is performed with a dc voltage slope controller presented in [19]. As shown in Fig. 23(a), after the uncontrolled charging process, the reference of dc voltage was set to 6.4 V/ms, which is same as the rising slope in Fig. 21(a). As shown in Fig. 23(b), the peak value of the NIC decreases to 15.5 A at the cost of increasing the charging time, however, the NIC is still larger than the rated current value of 15 A, thereby reducing the reliability of the system. Note that the overall dc voltage cannot rise linearly at the beginning of normal operation due to the uncontrollable inrush current.

In practical applications, increasing the inductance of the filters is usually adopted to limit the NIC despite the increased cost. Therefore, the inductance in Fig. 23 is increased from 6 to 12 mH, and all other operating conditions are the same as those in Fig. 23. As shown in Fig. 24, although the NIC is not eliminated, the peak value of NIC (12 A) is lower than the rated current value of 15 A.

As shown in Fig. 21, if the design of all cells is good enough, the voltage balancing control can be removed. However, under serious conditions, a superior startup control should still maintain dc voltage balanced to guarantee the system reliability. Hence, to verify the proposed cluster dc voltage balancing control, another experiment test was performed with different power resistors paralleled with the dc capacitors (phase A: 300 Ω, phase B: 1600 Ω, phase C: 500 Ω, for each cell). As shown in Fig. 25(a), at the end of the uncontrolled charging stage, three-cluster dc voltages deviate from each other with around 65 V due to the different power losses generated by the power resistors in dc links. When the STATCOM turns into the controlled charging process, three-cluster dc voltages begin to rapidly converge to their reference by injecting the negative sequence voltages and currents, which is shown in Fig. 25(b). In addition, the cell dc voltages in each cluster are balanced well, as shown in Fig. 25(c)–(e). Finally, the STATCOM turns into the normal operation and three-cluster dc voltages also maintain balanced by using zero sequence voltage injection method presented in [7]. Note that during the dc voltage control and check period, the reactive current is set to 1 A to improve the active power regulating capability of the zero-sequence injection method.

To further verify the effectiveness of the proposed cluster dc voltage balance control, a comparative case with the same operating conditions as those of Fig. 25 were carried out but the cluster dc voltage balancing control was removed. As observed from Fig. 26 , during the controlled charging stage, three-cluster dc voltages cannot be balanced and they diverge from their reference. Finally, the cluster dc voltage in phase B reaches to the overvoltage protection point preset to be 480 V, which halted the converters and turned the system into the protection status.

To verify the effectiveness of the proposed startup control under unbalanced and distorted grid, the grid voltage in phase A drops 30% and the THDs of three-phase grid voltage are

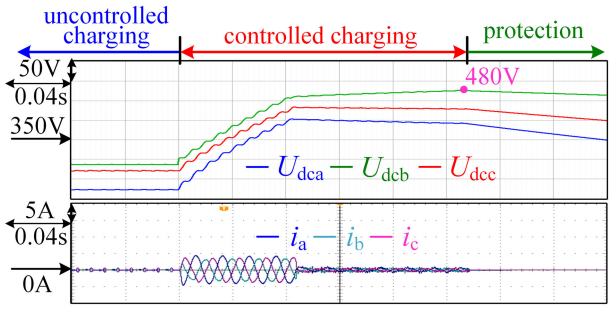

Fig. 26. Experimental waveforms without cluster voltage balancing control.

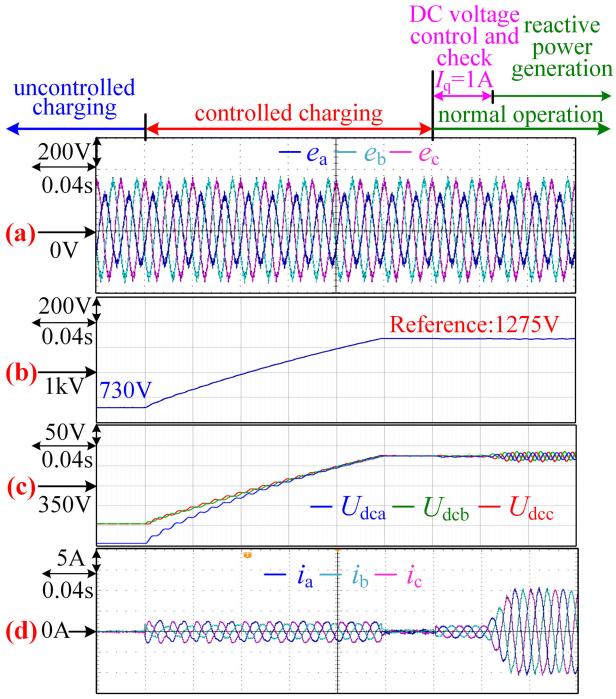

Fig. 27. Experimental waveforms under unbalanced and distorted grid.

6.84%, 5.29%, and 5.29%, respectively, as shown in Fig. 27(a). In this scenario, during the uncontrolled charging process, the overall dc voltage is only charged to 710 V, lower than the under balanced grid (788 V). In addition, three-cluster voltages are unbalanced due to the unbalanced grid voltages, as shown in Fig. 27(b) and (c). When the proposed control is implemented during the controlled charging process, the overall dc voltage is charged to the reference smoothly and three-cluster dc voltages are balanced during the charging process. Fig. 27(d) shows three-phase currents. It can be seen that there is no inrush current at the beginning of the controlled charging process and normal operation stage.

VIII. Conclusion

In this article, a novel startup control method was proposed for the star-connected CHB STATCOM by inserting the startup resistors into the main circuit during the controlled-charging circuit. The advantages of the proposed control method are: requiring no additional dc source, elimination of inrush current, constant charging current to achieve the tradeoff between the charging time and the active power of the startup resistor, and dc voltage balancing of all cells. Moreover, the proposed startup control method can be applied to any ac/dc grid-connected converters. The proposed control method was verified based on the simulation results on a three-phase 1 MVAr/10 kV CHB STATCOM and the experimental results on the 7.5 kVAr/380 V down-scaled CHB STATCOM, which proved that the proposed startup method is a good candidate for the star-connected CHB STATCOM.

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