Review, Analysis, and Design of Four Basic CPT Topologies and the Application of High-Order Compensation Networks

Yao Wang, *Graduate Student Member, IEEE*, Hua Zhang, *Member, IEEE*, and Fei Lu, *Member, IEEE*

***Abstract*—This article reviews existing capacitive power transfer (CPT) systems and aims to provide a universal methodology to systematically construct CPT topologies with zero-phase angle (ZPA) and load-independent output property. There are three contributions. First, *y*, *z*, *g*, and *h* parameters of a two-port network are adopted to model the capacitive coupler for four basic CPT compensations, which facilitates the resonant circuit analysis by forming parallel or series *LC* resonance. Second, four basic CPT compensations, series–series (SS), series–parallel (SP), parallel–series, and parallel–parallel (PP), are developed and analyzed. ZPA frequencies are identified with a load-independent output, and a unified efficiency analysis is also provided. Third, by selectively deploying high-order T/ΠΠ-type *LCL/CLC* networks and the SS mutual inductance with basic CPT compensations, a universal CPT design methodology is provided. In total, 144 feasible CPT topologies are derived with ZPA property and constant-current (CC) or constant-voltage output, which not only summaries existing ones but also predicts new topologies. Considerations are provided to guide the topology selection, from which ten typical CPT topologies are elaborated and recommended. A 500-W *LCL–PP–LCL* compensated CPT circuit is implemented. Experiments validate the proposed methodology by a ZPA property and a load-independent CC output, and a peak dc–dc efficiency of 87.76% is also achieved at 478 W.**

***Index Terms*—Basic CPT, capacitive power transfer (CPT), high-order CPT, load-independent constant-current/constant-voltage (CC/CV).**

I. Introduction

CAPACITIVE power transfer (CPT) technology uses alternate electric fields to transfer power [1]–[4]. Due to the lightweight, low-cost, and good metal tolerance, CPT is an alternative option of inductive power transfer (IPT) [5]–[10].

For both IPT and CPT, compensation networks are required to cancel reactive power, achieving zero-phase angle (ZPA). In IPT, four basic compensation topologies are constructed by two capacitors, namely series–series (SS), series–parallel (SP), parallel–series (PS), and parallel–parallel (PP) [11]. Besides, high-order IPT compensations are also developed [12]–[13].

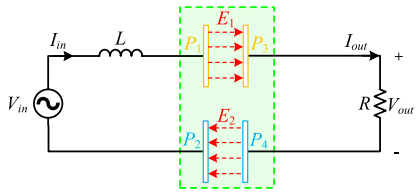

Fig. 1. Single-inductor-compensated CPT circuit.

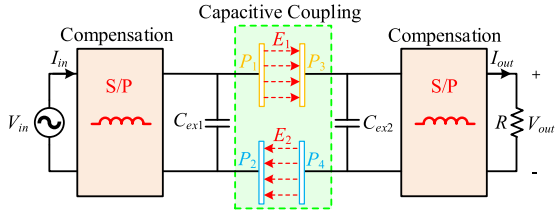

Fig. 2. Structure of the two-inductor compensated CPT.

In CPT, the simplest single-inductor compensation is shown in Fig. 1 [2], [14]–[15], where P_1, P_2, P_3, and P_4 comprise a capacitive coupler. Due to the small coupler capacitance, it is usually used in low-power systems and high-frequency (MHz) applications [16]–[17], otherwise, the large compensation inductance is difficult to handle. To mitigate this issue, external shunt capacitors are used to compensate the self-capacitance [18]. Considering the duality with IPT, four basic CPT topologies, SS, SP, PS, and PP, can be developed with two compensation inductors in series (S) or parallel (P) with the capacitive coupler [19]–[26], demonstrated in Fig. 2.

The double-sided *LC* compensated CPT topology with two series inductors [19]–[22] is considered as an SS CPT topology. It can work in both CC and CV modes and has a frequency splitting phenomenon [19], showing duality with SS IPT. Meantime, PS and SP CPT systems have shown step-up and step-down constant-voltage (CV) outputs [25]–[26], which are in duality with PS and SP IPT systems. Recently, high-order CPT circuits have been proposed, such as *LCL*, *LCLC*, and *CLLC* [27]–[35], which improve the system performance and promote applications of the CPT technology. However, there lacks a systematic method to design appropriate CPT topologies for different applications.

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The authors are with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA 19104 USA (e-mail: yw696@drexel.edu; hua.zhang@drexel.edu; fei.lu@drexel.edu).

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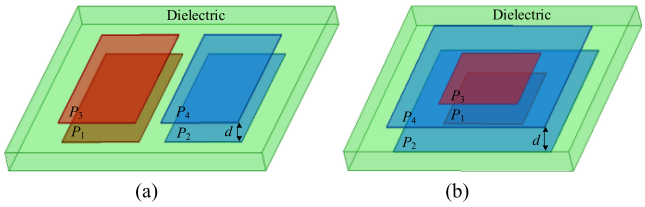


Fig. 3. Capacitive coupler configuration. (a) Parallel. (b) Stacked.

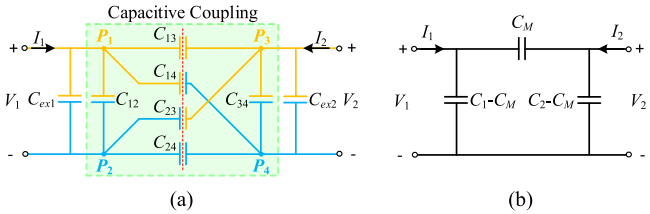


Fig. 4. Coupler circuit model. (a) Six-capacitor model. (b) Equivalent Π type.

This article aims to provide a universal methodology to systematically construct basic and high-order CPT topologies. There are three contributions. First, *y*, *z*, *g*, and *h* parameters of a two-port network are accordingly used to model the capacitive coupler for four basic CPT compensations, which facilitates the circuit resonance analysis by forming series or parallel *LC* resonant tanks. Second, based on the two-port parameters, four basic two-inductor CPT compensations are developed and investigated. ZPA frequencies are identified with the load-independent output, and unified efficiency analysis is also provided for four topologies. Third, by selectively deploying T/Π-type *LCL*/*CLC* networks and the SS mutual inductance circuit with the four basic CPT topologies, a universal CPT design methodology is provided, and 144 feasible CPT topologies are derived, which covers existing ones and predicts new candidates. Considerations are provided to guide the topology selection for different applications, and ten typical CPT topologies are elaborated and recommended. A 500-W *LCL-PP-LCL* compensated system is implemented to validate the proposed design methodology by showing ZPA property and load-independent CC output

$$\begin{cases} C_1 = C_{ex1} + C_{12} + \frac{(C_{13}+C_{14})\cdot(C_{23}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_2 = C_{ex2} + C_{34} + \frac{(C_{13}+C_{23})\cdot(C_{14}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_M = \frac{C_{13}\cdot C_{24}-C_{23}\cdot C_{14}}{C_{13}+C_{14}+C_{23}+C_{24}}. \end{cases} \tag{1}$$

II. Analysis of Four Basic CPT Topologies

A. Capacitive Coupler Modeling

Fig. 3 shows two typical configurations of the four-plate capacitive coupler: parallel [19] and stacked [27]. A six-capacitor model can represent the capacitive couplings between different plates, as shown in Fig. 4(a). C_{13} and C_{24} are the main couplings, C_{14} and C_{23} are the cross-couplings, and C_{12} and C_{34} are the internal shunt capacitances. $C_{\rm ex1}$ and $C_{\rm ex2}$ are external shunt capacitors. Usually, in a parallel coupler, cross-couplings C_{14} and C_{23} and shunt capacitances C_{12} and C_{34} are very small and can be neglected compared to the main coupling C_{13} and C_{24}.

According to [27], the six-capacitor model is simplified as a Π-type circuit, shown in Fig. 4(b). C_1 and C_2 are primary and secondary self-capacitances and C_M is the mutual capacitance, which is respectively expressed in (1).

The coupling coefficient k_C is defined as $k_C = C_M/(C_1C_2)^{0.5}$. Parameters C_M, C_1, C_2, and k_C specify the capacitive coupling, which is in uniformity with magnetic coupling, verifying the duality between IPT and CPT.

The capacitive coupler circuit can be analyzed as a two-port network, which is described by four variables: V_1, I_1, V_2, and I_2. Each port has an independent input excitation, which is either voltage or current. The other two variables are dependent and can be expressed by excitations and four two-port parameters based on the superposition theorem. In different combinations, totally, four categories of two-port parameters can be derived, referred to as *y*, *z*, *g*, and *h* parameters. For example, in the *y*-parameter model, V_1 and V_2 are two independent excitations, and I_1 and I_2 can be described by V_1 and V_2 and four parameters, y_{11}, y_{12}, y_{21}, and y_{22}.

The description, calculation, and the equivalent behavior-source circuits of two-port parameters are provided in Table I.

Particularly, the *y* parameter is used in [19] and [27], and *z* parameter is proposed in [31]. The *g* and *h* parameters are, respectively, used in [25] and [26].

With four basic CPT compensations, two-port parameters are selected accordingly to model the capacitive coupler and form parallel or series *LC* resonance, which helps to determine the ZPA resonant frequency and facilitate the circuit analysis. Specifically, *y*, *z*, *g*, and *h* parameters are, respectively, suitable to analyze PP, SS, PS, and SP compensations.

B. Analysis of Four Basic CPT Compensation

Four basic two-inductor CPT compensations are shown in Table II. *R* represents the secondary-sided load. The input excitation has two options: $V_{\rm in}$ or $I_{\rm in}$, which, respectively, represents a CV or constant-current (CC) input source. When *y*, *z*, *g*, and *h* parameter models, respectively, applied to PP, SS, PS, and SP compensations, behavior-source-based equivalent circuits are derived in which compensation inductors connect to the capacitor in either series or parallel form. To fully cancel the reactive power, it is straightforward to achieve *LC* resonance in double sides of the equivalent circuits. Then, the ZPA frequency is determined, and a resistive input impedance $Z_{\rm in}$ is calculated. The expressions of output current/voltage of four CPT circuits are also provided in Table II.

1) PP CPT Compensation: The PP compensation can achieve CC output from a CV source and CV output from a CC source. The resonance frequency and output are independent of k_C, which facilitates parameter tuning. Due to the parallel resonant tanks, the PP compensation is more suitable for the CC input excitation.

2) SS CPT Compensation: The SS CPT compensation has been studied in [19]–[22]. It also achieves the conversion between CC and CV. With given capacitance C_M, the output can be regulated by adjusting $C_{\rm ex1}$, $C_{\rm ex2}$, and the coupling coefficient k_C.

TABLE I
FOUR TWO-PORT PARAMETER MODELS OF THE CAPACITIVE COUPLING

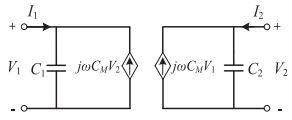
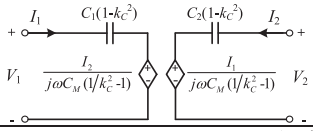
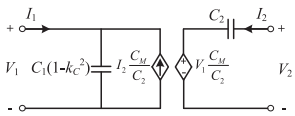
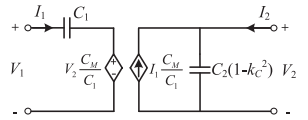
***y*-parameters**	***z*-parameters**	***g*-parameters**	***h*-parameters**
Description			
$\begin{cases} I_1 = y_{11}V_1 + y_{12}V_2 \\ I_2 = y_{21}V_1 + y_{22}V_2 \end{cases}$	$\begin{cases} V_1 = z_{11}I_1 + z_{12}I_2 \\ V_2 = z_{21}I_1 + z_{22}I_2 \end{cases}$	$\begin{cases} I_1 = g_{11}V_1 + g_{12}I_2 \\ V_2 = g_{21}V_1 + g_{22}I_2 \end{cases}$	$\begin{cases} V_1 = h_{11}I_1 + h_{12}V_2 \\ I_2 = h_{21}I_1 + h_{22}V_2 \end{cases}$
Calculation			
$\begin{cases} y_{11} = \left.\frac{I_1}{V_1}\right\|_{V_2=0} = j\omega C_1 \\ y_{12} = \left.\frac{I_1}{V_2}\right\|_{V_1=0} = -j\omega C_M \\ y_{21} = \left.\frac{I_2}{V_1}\right\|_{V_2=0} = -j\omega C_M \\ y_{22} = \left.\frac{I_2}{V_2}\right\|_{V_1=0} = j\omega C_2 \end{cases}$	$\begin{cases} z_{11} = \left.\frac{V_1}{I_1}\right\|_{I_2=0} = \frac{1}{j\omega C_1(1-k_C^2)} \\ z_{12} = \left.\frac{V_1}{I_2}\right\|_{I_1=0} = \frac{1}{j\omega C_M(1/k_C^2-1)} \\ z_{21} = \left.\frac{V_2}{I_1}\right\|_{I_2=0} = \frac{1}{j\omega C_M(1/k_C^2-1)} \\ z_{22} = \left.\frac{V_2}{I_2}\right\|_{I_1=0} = \frac{1}{j\omega C_2(1-k_C^2)} \end{cases}$	$\begin{cases} g_{11} = \left.\frac{I_1}{V_1}\right\|_{I_2=0} = j\omega C_1(1-k_C^2) \\ g_{12} = \left.\frac{I_1}{I_2}\right\|_{V_1=0} = -\frac{C_M}{C_2} \\ g_{21} = \left.\frac{V_2}{V_1}\right\|_{I_2=0} = \frac{C_M}{C_2} \\ g_{22} = \left.\frac{V_2}{I_2}\right\|_{V_1=0} = \frac{1}{j\omega C_2} \end{cases}$	$\begin{cases} h_{11} = \left.\frac{V_1}{I_1}\right\|_{V_2=0} = \frac{1}{j\omega C_1} \\ h_{12} = \left.\frac{V_1}{V_2}\right\|_{I_1=0} = \frac{C_M}{C_1} \\ h_{21} = \left.\frac{I_2}{I_1}\right\|_{V_2=0} = -\frac{C_M}{C_1} \\ h_{22} = \left.\frac{I_2}{V_2}\right\|_{I_1=0} = j\omega C_2(1-k_C^2) \end{cases}$
Expression			
$\begin{cases} I_1 = j\omega C_1 V_1 - j\omega C_M V_2 \\ I_2 = -j\omega C_M V_1 + j\omega C_2 V_2 \end{cases}$	$\begin{cases} V_1 = \frac{I_1}{j\omega C_1(1-k_C^2)} + \frac{I_2}{j\omega C_M(1/k_C^2-1)} \\ V_2 = \frac{I_1}{j\omega C_M(1/k_C^2-1)} + \frac{I_2}{j\omega C_2(1-k_C^2)} \end{cases}$	$\begin{cases} I_1 = V_1 \cdot j\omega C_1(1-k_C^2) - I_2 \cdot \frac{C_M}{C_2} \\ V_2 = V_1 \cdot \frac{C_M}{C_2} + \frac{I_2}{j\omega C_2} \end{cases}$	$\begin{cases} V_1 = \frac{I_1}{j\omega C_1} + V_2 \cdot \frac{C_M}{C_1} \\ I_2 = -I_1 \cdot \frac{C_M}{C_1} + V_2 \cdot j\omega C_2(1-k_C^2) \end{cases}$
Behavior-source circuit model			
			
Applicability			
PP Compensation	SS Compensation	PS Compensation	SP Compensation

TABLE II
MODELS AND PROPERTIES OF FOUR BASIC CPT COMPENSATIONS

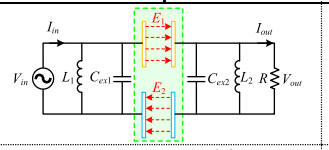
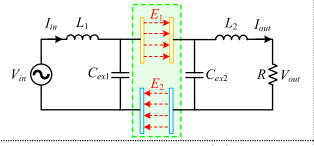
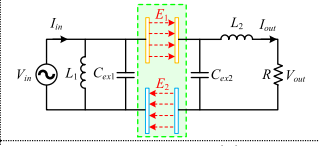
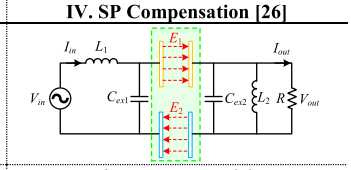
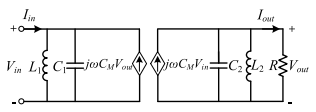
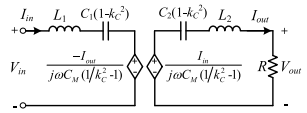
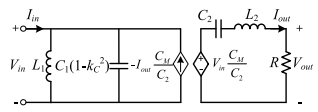
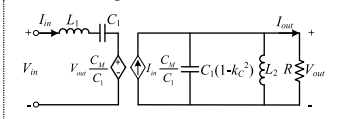
Four basic CPT compensations			
I. PP Compensation	**II. SS Compensation [19]-[22]**	**III. PS Compensation [25]**	**IV. SP Compensation [26]**
			
y-parameter model	*z*-parameter model	*g*-parameter model	*h*-parameter model
			
ZPA frequency			
$\omega = \frac{1}{\sqrt{L_1C_1}} = \frac{1}{\sqrt{L_2C_2}}$	$\omega = \frac{1}{\sqrt{L_1C_1(1-k_C^2)}} = \frac{1}{\sqrt{L_2C_2(1-k_C^2)}}$	$\omega = \frac{1}{\sqrt{L_1C_1(1-k_C^2)}} = \frac{1}{\sqrt{L_2C_2}}$	$\omega = \frac{1}{\sqrt{L_1C_1}} = \frac{1}{\sqrt{L_2C_2(1-k_C^2)}}$
Equivalent input impedance Z_{in} ($Z_{in}=V_{in}/I_{in}$)			
$Z_{in} = \frac{1}{(\omega C_M)^2 R}$	$Z_{in} = \frac{1}{[\omega C_M(1/k_C^2-1)]^2 R}$	$Z_{in} = (C_2/C_M)^2 R$	$Z_{in} = (C_M/C_1)^2 R$
CV Input Mode			
CC output	CC output	CV output	CV output
$I_{out} = V_{in} \cdot j\omega C_M$	$I_{out} = V_{in} \cdot j\omega C_M(1/k_C^2-1)$	$V_{out} = V_{in} \cdot C_M/C_2$	$V_{out} = V_{in} \cdot C_1/C_M$
CC Input Mode			
CV output	CV output	CC output	CC output
$V_{out} = -I_{in}/j\omega C_M$	$V_{out} = I_{in}/[j\omega C_M(1/k_C^2-1)]$	$I_{out} = I_{in} \cdot C_2/C_M$	$I_{out} = I_{in} \cdot C_M/C_1$

TABLE III
CIRCUIT TOPOLOGY OF INVERSION STAGE

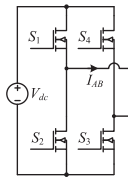
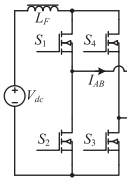
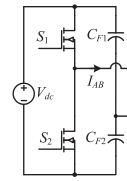
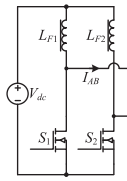
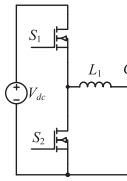
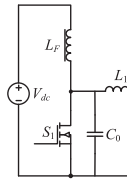
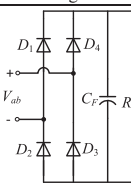
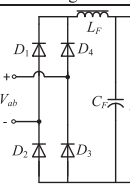
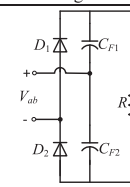
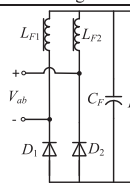
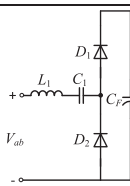
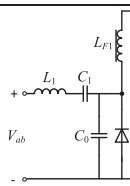
	Full-bridge VSI [19]	Full-bridge CSI [36]	Half-bridge VSI [37]	Half-bridge CSI [38]	Class D amplifier [39]	Class E amplifier [40]
Circuit topology						
Application	SS and SP	PS and PP	SS and SP	PS and PP	SS, SP, PS, PP	SS, SP, PS, PP
AC side	$V_{AB,1}=\frac{2\sqrt{2}}{\pi}V_{dc}$	$V_{AB}=\frac{\pi}{2\sqrt{2}}V_{dc}$	$V_{AB,1}=\frac{\sqrt{2}}{\pi}V_{dc}$	$V_{AB}=\frac{\pi}{\sqrt{2}}V_{dc}$	$V_{AB}=\frac{\sqrt{2}}{\pi}V_{dc}$	Load-dependent

TABLE IV
CIRCUIT TOPOLOGY OF RECTIFICATION STAGE

	Full-bridge VSR [19]	Full-bridge CSR [33]	Half-bridge VSR [36]	Half-bridge CSR [41]	Class D rectifier [42]	Class E rectifier [42]
Circuit topology						
Application	SS and PS	SP and PP	SS and PS	SP and PP	SS, SP, PS, PP	SS, SP, PS, PP
AC side	$V_{ab,1}=\frac{2\sqrt{2}}{\pi}V_{L}$	$V_{ab}=\frac{\pi}{2\sqrt{2}}V_{L}$	$V_{ab,1}=\frac{\sqrt{2}}{\pi}V_{L}$	$V_{ab}=\frac{\pi}{\sqrt{2}}V_{L}$	$V_{ab,1}=\frac{\sqrt{2}}{\pi}V_{L}$	Load-dependent

Note: $V_{AB,1}$ and $V_{ab,1}$: the first-order harmonics; VSI: voltage-source inverter; CSI: current-source inverter; VSR: voltage-source rectifier; CSR: current-source rectifier.

3) PS CPT Compensation: The PS CPT compensation performs as a step-down transformer. Its output has the same property as the input. It can achieve voltage step-down and current boosting function.

4) SP CPT Compensation: The SP CPT compensation also performs as a step-up transformer. It can boost voltage and decreases current.

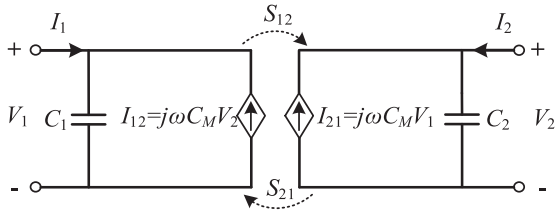


Fig. 5. Simplified *y*-parameter circuit of the capacitive coupling.

C. Inversion and Rectification Circuits Design

1) Inversion Stage: The inversion stage is the excitation of a CPT system. The commonly applicable inverter circuit structures are classified into three categories, i.e., full-bridge circuits, half-bridge circuits, and power amplifiers, as shown in Table III.

For a full-bridge inverter, there are two options: voltage-source inverter (VSI) and current-source inverter (CSI). A VSI generates a square-wave voltage V_{AB}, whereas a CSI requires a dc-link inductance to generate a square-wave current I_{AB}. By comparison, half-bridge circuits only use two switching devices, and additional two capacitors or inductors are needed.

It is noticed that a VSI is not compatible with PP and PS topologies because the primary-sided parallel capacitor cannot follow a square-wave voltage, otherwise, the *dv/dt* causes a huge rush current. Meantime, a CSI is also not compatible with SS and SP topologies because the primary series inductor cannot follow a square-wave input current.

Other than the full/half-bridge structure, the Class D and E power amplifiers can also achieve inversion. An additional *LC* resonant network is used to achieve sinusoidal output voltage.

For different inverters, the applicable CPT topologies and the expressions of ac voltages are also provided in Table III.

2) Rectification Stage: The rectification stage achieves the conversion from ac to dc. The rectification circuit can be constructed in an identical structure as the inverter by using uncontrolled diodes to replace the active switching device. Therefore, the full-bridge, half-bridge, and Class D/E rectifiers are designed as shown in Table IV. The applicable topologies and ac voltage expressions are also provided.

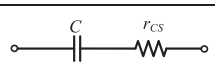
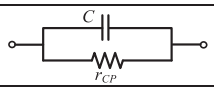
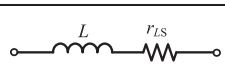
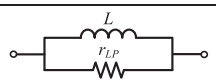
D. Power Transfer Capability Analysis

For a capacitive coupler, the *y*-parameter model is shown in Fig. 5. The voltage V_1 is chosen as the reference phasor, and the phase angle of V_2 is defined as θ, leading to

$$V_2 = |V_2|\,(\cos\theta + j\sin\theta). \tag{2}$$

In Fig. 5, the complex power transferred from the primary to secondary side is defined as S_{12} and calculated by V_1 and the

TABLE V
CIRCUIT MODELS OF INDUCTOR AND CAPACITOR WITH PARASITIC RESISTANCE

	Capacitor		Inductor	
Circuit model				
Parasitic resistance	$r_{CS} = 1/(\omega C \cdot Q_C)$	$r_{CP} = Q_C/(\omega C)$	$r_{LS} = (\omega L)/Q_L$	$r_{LP} = Q_L \cdot \omega L$

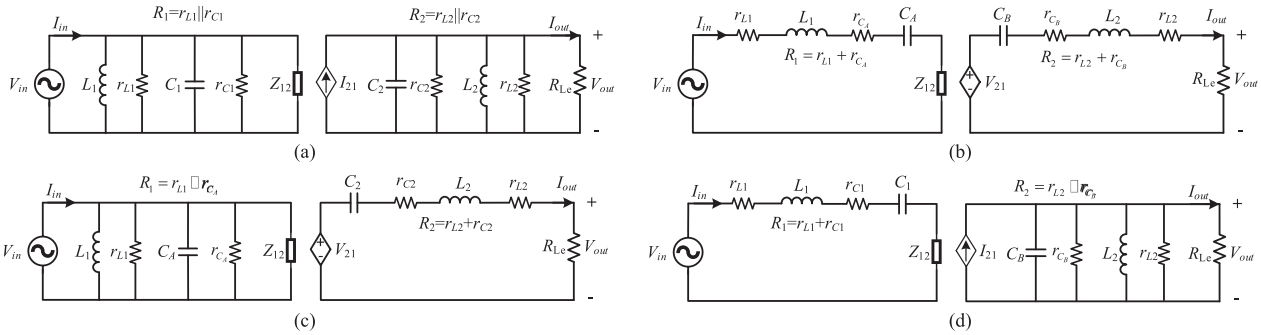


Fig. 6. Equivalent circuits of CPT topologies with parasitic resistances. (a) PP CPT topology. (b) SS CPT topology. (c) PS CPT topology. (d) SP CPT topology.

conjugation of I_{12}

$$S_{12} = V_1 \cdot (-I_{12}^*) = \omega C_M |V_1||V_2| \sin\theta + j\omega C_M |V_1||V_2| \cos\theta. \quad (3)$$

The active and reactive power P and Q are expressed as

$$\begin{cases} P = \mathrm{Re}[\mathrm{S}_{12}] = |V_1||V_2|\,\omega C_M \sin\theta \\ \mathrm{Q} = \mathrm{Im}[\mathrm{S}_{12}] = |V_1||V_2|\,\omega C_M \cos\theta. \end{cases} \quad (4)$$

The reactive power generated by C_2 is canceled by the secondary compensation inductance, therefore the phase angle θ of V_2 is around 90°. Then, the active power P is simplified as

$$P \approx |V_1||V_2|\,\omega C_M. \quad (5)$$

The active power P is proportional to ω, C_M, V_1, and V_2. Due to the limited capacitance C_M, V_1, and V_2 need to be high enough to achieve sufficient power transfer.

In SS, SP, and PS compensations, the series inductor is used to boost the voltage V_1 or V_2. However, in a PP topology, the capacitive coupler voltage is directly limited by the input and output voltages, resulting in a poor power transfer capability. With CV input, I_{out} of a PP CPT system is shown as

$$I_{\mathrm{out}} = V_{\mathrm{in}} \cdot j\omega C_M. \quad (6)$$

It is tens of times smaller than that of an SS circuit, showing the inferiority of the basic PP CPT in power transfer under a specific voltage source input mode.

III. EFFICIENCY ANALYSIS OF BASIC CPT TOPOLOGIES

Considering parasitic resistances, practical circuit models of passive capacitor and inductor are built in Table V. Quality factors are represented by Q_C and Q_L and r_{CS}, r_{CP}, r_{LS}, and r_{LP} define the parasitic resistances, which are built in either a series or parallel form.

Four basic CPT topologies are remodeled with parasitic resistances, shown in Fig. 6. The primary-sided reflected impedance Z_{12} is provided in Table VI. Particularly, in a SS CPT topology, C_A and C_B are used to represent the primary and secondary equivalent capacitance as

$$C_A = C_1(1-k_C^2),\ C_B = C_2(1-k_C^2). \quad (7)$$

r_{L1}, r_{L2}, r_{C1}, r_{C2}, r_{CA}, and r_{CB} are the parasitic resistances of inductors and capacitors. Total primary and secondary resistances are defined as R_1 and R_2. For the rectifier, the equivalent ac load is defined as R_{Le}. The efficiency $\eta(R_1, R_2, Z_{12}, R_{\mathrm{Le}})$ is provided in Table VI.

Q_1 and Q_2 are used to define the quality factors of primary and secondary circuits. a is the ratio between R_{Le} and R_2. Based on the definition of k_C, Q_1, Q_2, and a, for four basic CPT topologies, the system efficiency η is rewritten as

$$\eta = \frac{1}{1 + \frac{1}{a} + \frac{1}{Q_1 Q_2 k_C^2}(a + \frac{1}{a} + 2)}. \quad (8)$$

Equation (8) is also in uniformity with an IPT system [43]. The efficiency is only determined by k_C, Q_1, Q_2, and a. With given values, the maximum achievable efficiency is defined as $\eta_{\max}$, which is achieved at an optimal load condition $a_{\eta\max}$

$$a_{\eta\max} = \sqrt{1 + k_C^2 Q_1 Q_2}. \quad (9)$$

With $a = a_{\eta\max}$, $\eta_{\max}$ is calculated as

$$\eta_{\max} = \frac{k_C^2 Q_1 Q_2}{\left[1 + \sqrt{1 + k_C^2 Q_1 Q_2}\right]^2}. \quad (10)$$

Assuming $Q = Q_1 = Q_2$, $\eta_{\max}$ is shown in Fig. 7. It should be noticed that the power loss in the inverter and rectifier is not considered, which means the ac–ac efficiency is analyzed.

TABLE VI
SYSTEM EFFICIENCY OF FOUR CPT TOPOLOGIES

Circuit	I_{21} or V_{21}	Z_{12}	η (R_1, R_2, Z_{12}, R_{Le})	Q_1, Q_2, a	$\eta(k_C, Q_1, Q_2, a)$
PP CPT	$I_{21}=V_{in}\cdot j\omega C_M$	$Z_{12}=\frac{R_{Le}+R_2}{(\omega C_M)^2 R_{Le}R_2}$	$\eta_{PP}=\frac{1/Z_{12}}{1/Z_{12}+1/R_1}\cdot\frac{1/R_{Le}}{1/R_{Le}+1/R_2}$	$Q_1=\omega C_1R_1$ $Q_2=\omega C_2R_2$ $a=R_2/R_{Le}$	$\eta=\frac{1}{1+\frac{1}{a}+\frac{1}{Q_1Q_2k_C^2}(a+\frac{1}{a}+2)}$
SS CPT	$V_{21}=\frac{I_1}{j\omega C_M(1/k_C^2-1)}$	$Z_{12}=\frac{1}{[\omega C_M(1/k_C^2-1)]^2(R_{Le}+R_2)}$	$\eta_{SS}=\frac{Z_{12}}{Z_{12}+R_1}\cdot\frac{R_{Le}}{R_{Le}+R_2}$	$Q_1=1/(\omega C_1R_1)$ $Q_2=1/(\omega C_2R_2)$ $a=R_{Le}/R_2$	
PS CPT	$V_{21}=V_1\cdot C_M/C_2$	$Z_{12}=(C_2/C_M)^2(R_{Le}+R_2)$	$\eta_{PS}=\frac{1/Z_{12}}{1/Z_{12}+1/R_1}\cdot\frac{R_{Le}}{R_{Le}+R_2}$	$Q_1=\omega C_1R_1$ $Q_2=1/(\omega C_2R_2)$ $a=R_{Le}/R_2$	
SP CPT	$I_{21}=I_{in}\cdot C_M/C_1$	$Z_{12}=(C_M/C_1)^2\frac{R_{Le}R_2}{R_{Le}+R_2}$	$\eta_{SP}=\frac{Z_{12}}{Z_{12}+R_1}\cdot\frac{1/R_{Le}}{1/R_{Le}+1/R_2}$	$Q_1=\omega C_1R_1$ $Q_2=1/(\omega C_2R_2)$ $a=R_2/R_{Le}$	

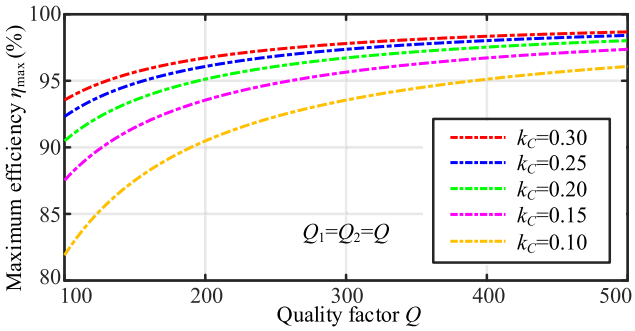


Fig. 7. Theoretical maximum achievable system efficiency.

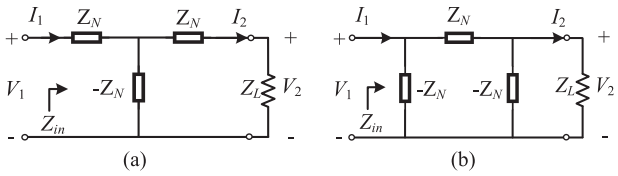


Fig. 8 Impedance network of (a) T type and (b) Π type.

IV. UNIVERSAL CPT DESIGN METHODOLOGY

The four basic CPT topologies have the advantage of structure simplicity, which also means few adjustable resonant parameters. The addition of high-order compensation provides more degrees of freedom to improve the system performance, which helps to satisfy all CPT system design criteria.

A. High-Order Compensation Network

When adding high-order compensations with basic CPT topologies, two premises need to be considered. First, the addition of high-order compensations should not damage the ZPA property. Second, the load-independent output property should still be maintained. Considering this, T- and Π-type impedance networks are adopted [44]–[45], as shown in Fig. 8.

As shown in Fig. 8, V_1 and V_2 are two voltage sources. Z_N is the reactance constructed by either a capacitor or inductor. Based on the superposition theorem, currents I_1 and I_2 in both T- and Π-type networks are given by

$$I_1=-\frac{V_2}{Z_N},I_2=\frac{V_1}{Z_N}. \tag{11}$$

Input impedance Z_{in} is given as

$$Z_{in}=\frac{V_1}{I_1}=\frac{|Z_N|^2}{Z_L}. \tag{12}$$

According to (11) and (12), when V_1 works as the input excitation, the output current I_2 is independent of load condition and the ZPA of input impedance is reserved when the load Z_L is resistive.

The reactance Z_N can be constructed by L or C, therefore, the applicable T/Π -type *CLC*/*LCL* compensation networks are derived, as shown in Table VII. Particularly, the SS mutual inductance circuit can be considered a special T-type *CLC* network, viewed as the fifth compensation network.

In a resonant condition of $\omega=(LC)^{0.5}$, these five networks all can achieve the conversion between CC and CV property without affecting the ZPA. This conversion is described in the last column of Table VII.

B. Universal CPT Structure

A practical CPT circuit can be configured by a basic CPT compensation with the primary and/or secondary T/Π/M-type networks. The basic inductor compensation is necessary to cancel the reactive power generated by the capacitive coupler. The high-order compensation is optional, which is used to increase power and change CC or CV output property. A general structure of the CPT system is shown in Fig. 9.

Based on the proposed design methodology, 144 feasible CPT topologies can be developed or predicted in total, as shown in Table VIII. Among these 144 circuits, the basic PP topology has the poor capability to transfer power under CV input, which is not recommended. With a CV input, the output property of each topology is also provided.

C. Considerations of Topology Selection

1) Preferred VSI and VSR in Inversion and Rectification: The applicable inversion and rectification circuits have been provided in Tables III and IV. The typical full-/half-bridge

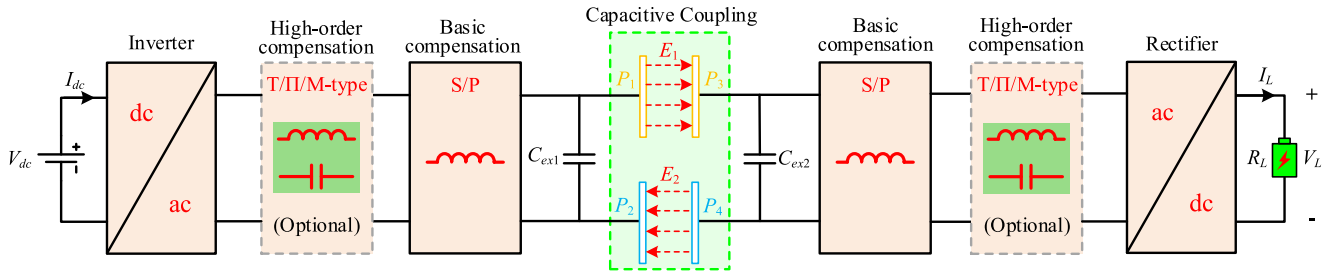


Fig. 9. General structure of the capacitive power transfer system.

TABLE VII
HIGH-ORDER COMPENSATION NETWORKS FOR CPT

Networks	Frequency	Output property
I. T-type *LCL*	$\omega=\frac{1}{\sqrt{LC}}$	I. CC output from CV source $\lvert I_{out}\rvert=\frac{\lvert V_{in}\rvert}{\omega L}=\lvert V_{in}\rvert\cdot\omega C$ II. CV output from CC source $\lvert V_{out}\rvert=\lvert I_{in}\rvert\cdot\omega L=\frac{\lvert I_{in}\rvert}{\omega C}$
II. T-type *CLC*		
III. Π-type *LCL*		
IV. Π-type *CLC*		
V. Mutual inductance (M-type) T-model		I. CC output from CV source $\lvert I_{out}\rvert=\frac{\lvert V_{in}\rvert}{\omega M}$ II. CV output from CC source $\lvert V_{out}\rvert=\lvert I_{in}\rvert\cdot\omega M$

TABLE VIII
FEASIBLE CPT TOPOLOGY

Classification	Topology structure	Number		IN-OUT
Basic CPT topology	SS [18]-[22]	1	4	CV-CC
	SP [26]	1		CV-CV
	PS [25]	1		CV-CV
	PP (**Not recommended**)	1		CV-CC
High-order CPT topology (I)	T/Π/M-SS [29], [31]	5	20	CV-CV
	T/Π/M-SP	5		CV-CC
	T/Π/M-PS	5		CV-CC
	T/Π/M-PP	5		CV-CV
High-order CPT topology (II) (**Not recommended**)	SS-T/Π [33]	5	20	CV-CV
	SP-T/Π/M	5		CV-CC
	PS-T/Π/M	5		CV-CC
	PP-T/Π/M	5		CV-CV
High-order CPT topology (III)	T/Π/M-SS-T/Π/M [27]-[28], [30], [32]	25	100	CV-CC
	T/Π/M-SP-T/Π/M	25		CV-CV
	T/Π/M-PS-T/Π/M	25		CV-CV
	T/Π/M-PP-T/Π/M	25		CV-CC

inverters/rectifiers include two categories: voltage-source and current-source types. Compared with the VSI/VSR, the CSI/CSR requires a large dc filter inductance in the input/output dc sides, which is not desirable in practice. Besides, when implementing a CSI in medium- or high-power applications, external diodes are generally series-connected to the CSI MOSFETs to prevent a rush circulating current [38], causing a complicated structure. Therefore, the VSI and VSR are preferred to the CSI and CSR.

The usage of VSI and VSR also guides the CPT selection. For example, the VSI is not compatible with a front-end parallel capacitor loop because capacitor voltage cannot follow a square-wave input, otherwise, the *dv*/*dt* causes a huge rush current to damage the circuit. Therefore, the basic PS and PP CPT circuits are not recommended when VSI is used.

2) Power Transfer Capability Versus Structural Complexity: The four basic CPT compensations have the advantage of great simplicity, which also means less freedom to improve the system power level. For example, in the basic SS CPT compensation, with the given input voltage $V_{\rm in}$, frequency ω, and coupled capacitance C_M, to increase the system power level, we have to reduce the coupling coefficient k_C, which means a sacrifice of efficiency. However, in the *CLC-SS* and *CLC-SS-CLC* topologies, by adjusting the capacitance in the T-type *CLC* compensation, it is easy to achieve a high power without sacrificing k_C.

With the addition of high-order networks, the system performance improves as the structural complexity increases. Therefore, the selection of CPT topology should take comprehensive considerations of the power requirements and system complexity. For low-power cases, the basic SS and SP CPT topologies are recommended because of their good simplicity. In medium power cases, with the T/Π-type networks only used on the primary side, a balance between power capability and compact receiver side is achieved. In high-power applications, the T/Π-type compensation can be used in double sides to further improve the power level.

3) Preferred T-Type Network to Π *Type:* The VSI and VSR are preferred in practice, which also guides the selection of T- and Π-type networks when designing high-order CPT topology. First, the Π-type *CLC* network is not compatible with VSI and VSR due to the front-end parallel capacitor. Second, when the Π-type *LCL* network is used with PS and PP CPT compensation, a parallel capacitor loop is also formed in the front end, which also causes the compatibility issue with a VSI. Third, when a Π-type *LCL* network is used with SS compensation, the

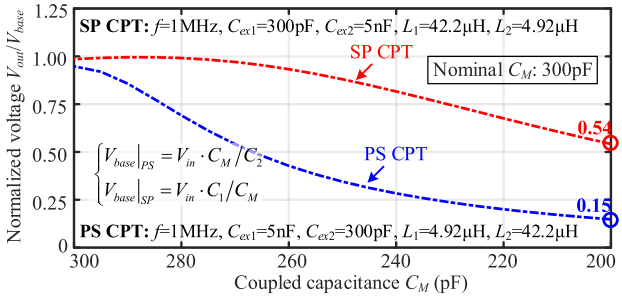


Fig. 10. Simulated normalized output voltage of PS and SP CPT under different coupling variations.

Π-SS/Π-SS-Π topologies is relatively more complicated than the counterparts constructed by a T-type network, because, in T-SS/T-SS-T topologies, the series-connected components can be merged, resulting in fewer circuit components.

4) Compactness: When the T-type *LCL/CLC* networks are used with an SS CPT compensation, the second compensation inductor or capacitor is in series connection with the inductor L_1 or L_2 of the SS CPT circuit, which can be merged to reduce the number of components, improving system compactness. A similar principle is also suitable for the mutual inductance network connected with an SS CPT circuit. Meantime, because fewer inductors are needed in the T-type *CLC* network than that in the *LCL* circuit, it tends to enable higher compactness.

Besides, a compact receiving-side circuit is also expected in practice. The category of "high-order CPT topology (II)" uses a single inductor in the transmitting side but complicated high-order compensation on receiving side, which is undesirable and generally not recommended when compared with the "high-order CPT topology (I)."

5) Misalignment Tolerance: In a CPT system, the misalignment will cause two negative impacts: 1) it will reduce the mutual capacitance C_M; and 2) it will detune the CPT system. The detuning condition always tends to deteriorate the output voltage/current. However, because of different output relationships with C_M, the misalignment tolerance of different CPT circuits varies.

For example, the output voltage expression of the basic PS and SP CPT compensations are, respectively, proportional and reverse proportional to C_M, as given in (13). Therefore, in a PS CPT system, reducing C_M tends to reduce the output voltage with an additional decrease from parameter detuning. However, in an SP CPT system, reducing C_M tends to increase the output voltage, which helps cancel the impact from parameter detuning, meaning a better misalignment tolerance.

$$V_{\text{out}}|_{\text{PS}} = V_{\text{in}} \cdot C_M/C_2,\ V_{\text{out}}|_{\text{SP}} = V_{\text{in}} \cdot C_1/C_M\,. \quad (13)$$

LTspice simulation is conducted to compare the misalignment tolerance of PS and SP CPT compensations with the same coupling variation of C_M, as shown in Fig. 10. It shows that at a nominal C_M of 300 pF, the SP and PS CPT circuits achieve their respective V_{base} as defined in (13). When C_M varies from 300 to 200 pF, the output voltage of an SP CPT system is much more stable than that of a PS CPT system, validating a better misalignment tolerance.

Therefore, when the CPT topology achieves a reverse output relationship with mutual capacitance C_M, the system tends to have a better misalignment tolerance.

D. Typical CPT Topologies

According to the proposed general CPT structure, 144 applicable topologies can be derived in total. Based on the considerations discussed above, ten typical CPT circuits are selected and recommended to be applied in practice, which are provided in Table IX.

1) Basic SS and SP CPT Topologies: Among the four basic CPT topologies, the SS and SP compensations tend to have better performance than the others because of their compatibility with a VSI and a good misalignment tolerance. Besides, the SS and SP CPT systems, respectively, achieve a CC and CV output, which is suitable for low-power applications due to high simplicity, therefore, they are selected as the first and second recommended CPT candidates. It is noticed that the SP CPT requires a dc filter inductance L_F in the rectification stage, which is a drawback compared to SS CPT. The high-frequency switching condition may help mitigate the impact of L_F.

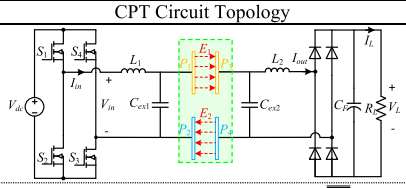
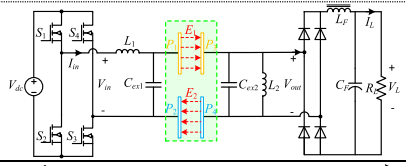
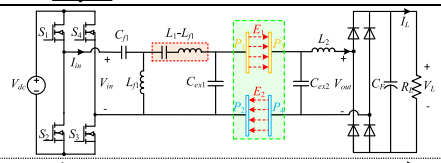
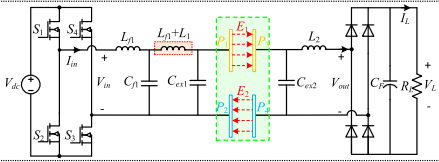
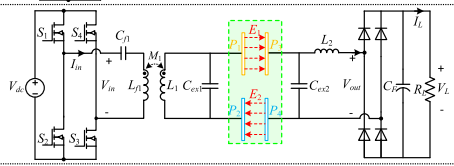
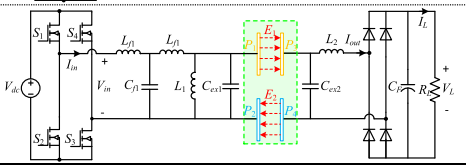
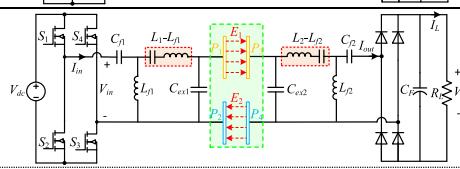
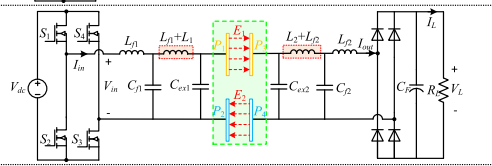
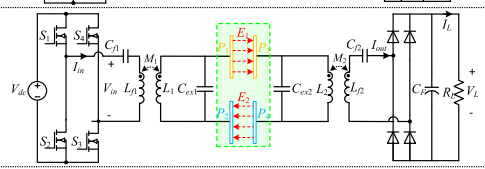
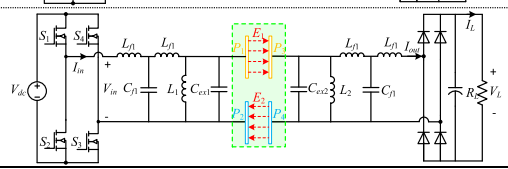
2) Primary-Sided T-Type Network Compensated Topologies: As discussed before, when constructing the high-order CPT system, T-type networks are preferred over Π-type networks, which include T-type *CLC/LCL* and the SS mutual inductance. With the T-type networks only used at the primary side, SS and PS basic compensations are recommended because of their compatibility with a VSR.

With SS basic compensation, the high-order *CLC-SS*, *LCL-SS,* and M_1*-SS* topologies are selected as the third to fifth recommended CPT candidates, as shown in Table IX, which achieve CV output, and C_{f1} or M_1 can help improve the power level. In the *CLC-SS* and *LCL-SS* topologies, the second capacitor/inductor of the T-type network can merge with the series-connected L_1, which reduces the number of components. Similar integration is also conducted for the M_1*-SS* CPT topology, in which the secondary self-inductance of the magnetic mutual coupling also works as the series inductance compensation for the CPT system.

With basic PS compensation, the T-type *CLC* network will be incompatible, otherwise, a front-end capacitor loop will be formed, which disables the VSI. The SS mutual inductance will be too complicated because no component can be merged. Therefore, the *LCL-PS* topology is recommended, listed as the sixth candidate, which achieves a CC output, and the reverse relationship with coupled capacitance C_M enables a relatively good misalignment tolerance.

It is noticed that the output voltage of the third to fifth circuits shows a proportional relationship with C_M, which may lead to undesirable misalignment tolerance. To solve the problem, one solution is to reversely use these topologies. Then, the misalignment tolerance is improved with CV output property, which belongs to the category of "high-order CPT topology (II)."

TABLE IX
TEN TYPICAL CPT TOPOLOGIES

Compensation	CPT Circuit Topology	ZPA frequency	Output Property
I Series-Series [18]-[22]		$\begin{cases} C_1 = C_M + C_{ex1} \\ C_2 = C_M + C_{ex2} \\ k_C = C_M/(C_1C_2)^{0.5} \\ \omega^2 L_1 C_1 (1\text{-}k_C^2) = 1 \\ \omega^2 L_2 C_2 (1\text{-}k_C^2) = 1 \end{cases}$	CC output $I_{out} = V_{in} \cdot j\omega C_M \left(\frac{1}{k_C^2} - 1\right) \approx V_{in} \cdot j\omega \frac{C_1 C_2}{C_M}$ **(Good misalignment tolerance)**
II Series-Parallel [26]		$\begin{cases} \omega^2 L_1 C_1 = 1 \\ \omega^2 L_2 C_2 (1\text{-}k_C^2) = 1 \end{cases}$	CV output $V_{out} = V_{in} \cdot \frac{C_1}{C_M}$ **(Good misalignment tolerance)**
III. *CLC-SS* [31]		$\begin{cases} \omega^2 L_1 C_1 (1\text{-}k_C^2) = 1 \\ \omega^2 L_2 C_2 (1\text{-}k_C^2) = 1 \\ \omega^2 L_{f1} C_{f1} = 1 \end{cases}$	CV output $V_{out} = \frac{V_{in} C_{f1}}{(1/k_C^2 - 1) C_M} \approx V_{in} \frac{C_{f1} C_M}{C_1 C_2}$
IV. *LCL-SS* [29]		$\begin{cases} \omega^2 L_1 C_1 (1\text{-}k_C^2) = 1 \\ \omega^2 L_2 C_2 (1\text{-}k_C^2) = 1 \\ \omega^2 L_{f1} C_{f1} = 1 \end{cases}$	CV output $V_{out} = -\frac{V_{in} C_{f1}}{(1/k_C^2 - 1) C_M} \approx -V_{in} \frac{C_{f1} C_M}{C_1 C_2}$
V. Coupled M_1-*SS*		$\begin{cases} \omega^2 L_1 C_1 (1\text{-}k_C^2) = 1 \\ \omega^2 L_2 C_2 (1\text{-}k_C^2) = 1 \\ \omega^2 L_{f1} C_{f1} = 1 \end{cases}$	CV output $V_{out} = \frac{V_{in}}{\omega^2 M_1 C_M (1/k_C^2 - 1)} \approx \frac{V_{in} C_M}{\omega^2 M_1 C_1 C_2}$
VI. *LCL-PS*		$\begin{cases} \omega^2 L_1 C_1 (1\text{-}k_C^2) = 1 \\ \omega^2 L_2 C_2 = 1 \\ \omega^2 L_{f1} C_{f1} = 1 \end{cases}$	CC output $I_{out} = -V_{in} \frac{j\omega C_{f1} C_2}{C_M}$ **(Good misalignment tolerance)**
VII. *CLC-SS-CLC* [32]		$\begin{cases} \omega^2 L_1 C_1 (1\text{-}k_C^2) = 1 \\ \omega^2 L_2 C_2 (1\text{-}k_C^2) = 1 \\ \omega^2 L_{f1} C_{f1} = 1 \\ \omega^2 L_{f2} C_{f2} = 1 \end{cases}$	CC output $I_{out} = V_{in} \frac{j\omega C_{f1} C_{f2}}{(1/k_C^2 - 1) C_M} \approx V_{in} j\omega C_M \frac{C_{f1} C_{f2}}{C_1 C_2}$
VIII. *LCL-SS-LCL* [27]-[28]		$\begin{cases} \omega^2 L_1 C_1 (1\text{-}k_C^2) = 1 \\ \omega^2 L_2 C_2 (1\text{-}k_C^2) = 1 \\ \omega^2 L_{f1} C_{f1} = 1 \\ \omega^2 L_{f2} C_{f2} = 1 \end{cases}$	CC output $I_{out} = V_{in} \frac{j\omega C_{f1} C_{f2}}{(1/k_C^2 - 1) C_M} \approx V_{in} j\omega C_M \frac{C_{f1} C_{f2}}{C_1 C_2}$
IX. M_1-*SS*-M_2 [5], [46]		$\begin{cases} \omega^2 L_1 C_1 (1\text{-}k_C^2) = 1 \\ \omega^2 L_2 C_2 (1\text{-}k_C^2) = 1 \\ \omega^2 L_{f1} C_{f1} = 1 \\ \omega^2 L_{f2} C_{f2} = 1 \end{cases}$	CC output $I_{out} = \frac{jV_{in}}{\omega^3 M_1 M_2 C_M (1/k_C^2 - 1)} \approx \frac{jV_{in} C_M}{\omega^3 M_1 M_2 C_1 C_2}$
X. *LCL-PP-LCL*		$\begin{cases} \omega^2 L_1 C_1 = 1 \\ \omega^2 L_2 C_2 = 1 \\ \omega^2 L_{f1} C_{f1} = 1 \\ \omega^2 L_{f2} C_{f2} = 1 \end{cases}$	CC output $I_{out} = -V_{in} \cdot \frac{j\omega C_{f1} C_{f2}}{C_M} = -V_{in} j\omega C_M \frac{C_{f1} C_{f2}}{C_M C_M}$ **(Good misalignment tolerance)**

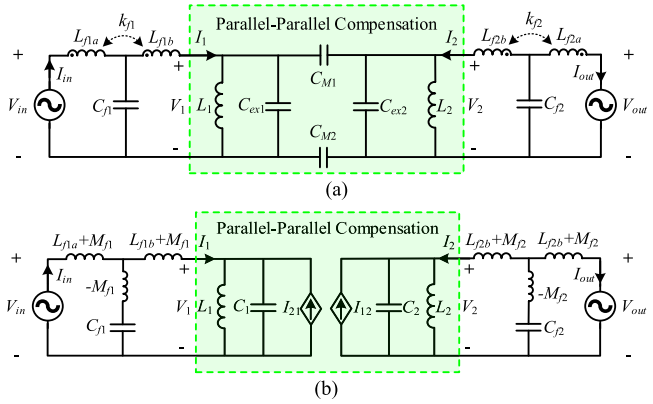


Fig. 11. Proposed *LCL-PP-LCL* compensated CPT system. (a) Circuit topology. (b) Equivalent circuit based on *y*-parameter model.

In this case, the only drawback is the complicated secondary compensation circuit.

3) Double-Sided T-Type Network Compensated Topologies: When double-sided T-type compensation networks are implemented with basic PS and SP CPT compensations, the systems will achieve CV output, which overlaps with the third to fifth CPT circuits. Therefore, they are not recommended here. With basic SS and PP compensations, four double-sided compensated high-order CPT circuits are recommended in total, listed as the seventh to tenth recommended CPT circuits. For the *CLC-SS-CLC*, *LCL-SS-LCL*, and M_1*-SS-*M_2 topologies, they have similar working principles and output expressions, which have been explored to achieve high power with CC output property for EV applications. According to the proposed general CPT structure, a new *LCL-PP-LCL* topology is further developed in this article with CC property. Compared with the other three circuits, the *LCL-PP-LCL* topology needs two more inductors because the component integration is no longer available. This issue can be mitigated by making the inductors of T-type *LCL* networks cross-coupled. On the other hand, the *LCL-PP-LCL* topology tends to have better misalignment tolerance because of the reverse output relationship with C_M. Meantime, according to the output expression, with identical circuit parameters, the *LCL-PP-LCL* topology will achieve a much higher output current than the others, meaning a higher power transfer capability.

E. LCL-PP-LCL *Compensated CPT Topology*

To validate the proposed design methodology, an *LCL*-PP-*LCL* compensated CPT topology is designed, shown in Fig. 11. There are three considerations in selecting the *LCL-PP-LCL* topology.

First, the *LCL-PP-LCL* topology is one of the most complicated high-order CPT topologies, which can fully verify the proposed universal design methodology.

Second, compared with SS, SP, and PS CPT compensations, the PP CPT compensation has not been investigated in the existing literature. The implemented *LCL-PP-LCL* topology can fill in the technical gap.

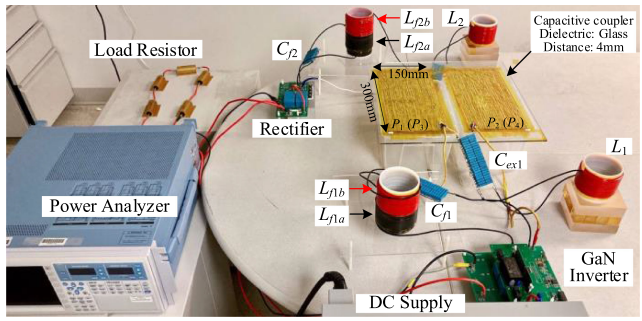


Fig. 12. Implemented *LCL-PP-LCL* compensated CPT prototype.

Third, the *LCL-PP-LCL* topology is new and has not been investigated in the existing literature. Meantime, it also shows good potential for misalignment tolerance and high-power transfer capability.

In Fig. 11(a), C_{M1} and C_{M2} are the main coupled capacitances between plates. C_1 and C_2 are self-capacitances, defined as

$$\begin{cases} C_M = C_{M1} \cdot C_{M2}/(C_{M1} + C_{M2}) \\ C_1 = C_{\text{ex1}} + C_M,\ C_2 = C_{\text{ex2}} + C_M. \end{cases} \tag{14}$$

To improve the compactness of the *LCL-PP-LCL* topology, the inductors of the T-type *LCL* network are cross-coupled, and the mutual couplings are represented by k_{f1} and k_{f2}. The T model is used to decouple. Fig. 11(b) provides an equivalent circuit based on *y*-parameters.

For T-type *LCL* network parameters are specified as

$$\begin{cases} L_{f1a} = L_{f1b} = L_{f1},\ M_{f1} = k_{f1} \cdot \sqrt{L_{f1a} L_{f1b}} \\ L_{f2a} = L_{f2b} = L_{f2},\ M_{f2} = k_{f2} \cdot \sqrt{L_{f2a} L_{f2b}}. \end{cases} \tag{15}$$

The resonant relationship is given as

$$\omega = \frac{1}{\sqrt{L_{f1} C_{f1}}} = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} = \frac{1}{\sqrt{L_{f2} C_{f2}}}. \tag{16}$$

Based on the working property of a T-type *LCL* network and a PP CPT compensation, the load-independent CC output is achieved as

$$I_{\text{out}} = -jV_{\text{in}} \cdot \frac{\omega C_{f1} C_{f2}}{(1 + k_{f1})(1 + k_{f2}) C_M}. \tag{17}$$

The compensation capacitors C_{f1} and C_{f2} are generally much larger than C_M. Therefore, by using the high-order *LCL* network, the output current can be significantly increased, enhancing the power transfer capability.

V. Experimental Validation

A. LCL-PP-LCL *Compensated CPT Prototype*

A 500-W *LCL-PP-LCL* compensated system is implemented in Fig. 12. The plate size is 300 mm × 150 mm. A glass insulator is used with the size of 400 mm × 400 mm × 4 mm. A coupling capacitance C_M is 300 pF, and the external shunt capacitance is 1.05 nF, enabling a coupling coefficient k_C of 0.22.

The detailed parameters are provided in Table X. The input dc voltage is 200 V and a full-bridge inverter uses gallium nitride (GaN) MOSFETs (GS66506T) to generate 1-MHz ac excitation.

TABLE X
SYSTEM SPECIFICATIONS OF THE PROPOSED CPT PROTOTYPE

Parameter	Value	Parameter	Value
V_{dc}	200 V	f	1 MHz
Transfer distance	4 mm	R_L	20 Ω~100 Ω
C_{M1}, C_{M2}	600 pF	C_{ex1}, C_{ex2}	1.05 nF
C_M	300 pF	C_1, C_2	1.35 nF
k_C	0.22	L_1, L_2	18.8 μH
L_{f1a}	21.5 μH	L_{f2a}	19.6 μH
L_{f1b}	19.6 μH	L_{f2b}	19.5 μH
k_{f1}	0.262	k_{f2}	0.254
C_{f1}	1.3 nF	C_{f2}	1.3 nF

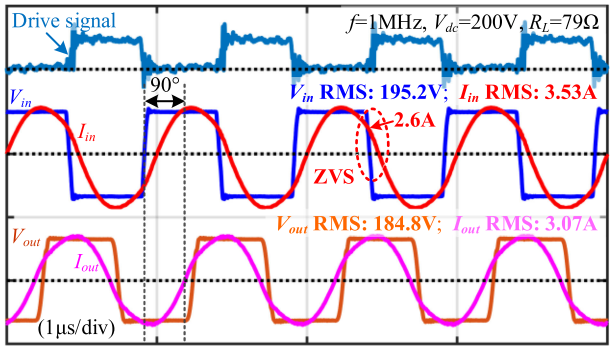


Fig. 13. Experimental waveforms at load resistance of 79 Ω.

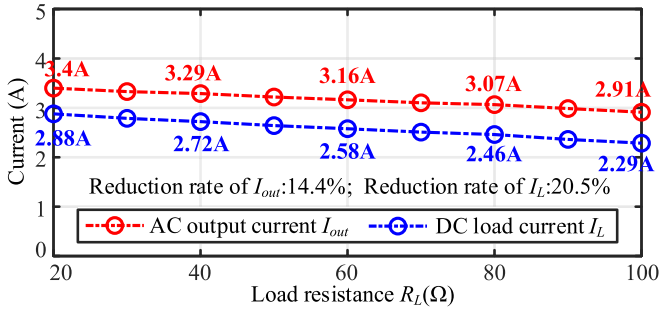


Fig. 14. Output currents versus load resistance.

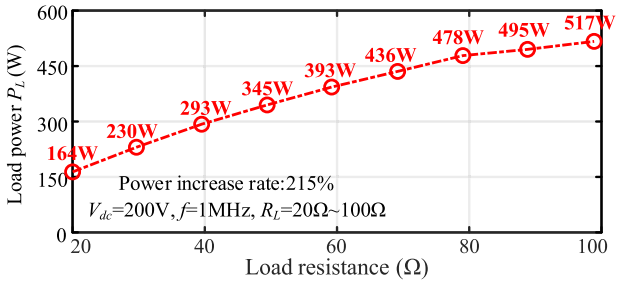


Fig. 15. Load power versus load resistance.

A full-bridge rectifier is designed based on silicon carbide (SiC) diodes (IDW30G65C5). Inductors are wound by 2180-strand AWG46 Litz wires. Two inductors of each T-type *LCL* network are coupled, shown as $L_{f1\,a}$ and $L_{f1\,b}$, $L_{f2\,a}$, and $L_{f2\,b}$. Particularly, $L_{f1\,a}$ is around 10% larger than the designed value to guarantee zero-voltage switching (ZVS).

B. Experimental Results

1) ZPA Property: With $f = 1$ MHz, $V_{\rm dc} = 200$ V, and $R_L = 79$ Ω, the experimental waveforms are provided in Fig. 13. It shows that the output current $I_{\rm out}$ lags input voltage $V_{\rm in}$ by 90°, which is consistent with (17). Meantime, $V_{\rm in}$ and $I_{\rm in}$ are almost in phase, which means a near ZPA condition, and the input reactive power is significantly suppressed. The slight phase shift between $V_{\rm in}$ and $I_{\rm in}$ is a deliberate parameter design aiming at achieving ZVS. As shown in Fig. 13, the inverter MOSFET turns OFF with a positive turn-OFF current of 2.6 A, the turn-OFF current is used to discharge the junction capacitors of the other MOSFET in the same leg within the dead time, guaranteeing ZVS turn-ON condition. The ZVS operation not only reduces switching loss of the inverter but also eliminates output voltage oscillation and avoids ringing in driver signals, which is greatly important for the MHz high-frequency inverter. In the experiment, L_{f1a} is set at 21.5 μH, which is 10% larger than the designed value, guaranteeing the ZVS operation.

2) Load-Independent Output Property: According to (17), in the *LCL-PP-LCL* CPT system, the output current is independent of load resistance R_L. Based on the parameters in Table X, with an ideal lossless circuit and a well-tuned resonant condition, the current ac output current $I_{\rm out}$ is calculated as 4.02 A.

The measured ac and dc output currents versus different load resistances are shown in Fig. 14. When load resistance R_L varies from 20 to 100 Ω with a variation of 400%, the measured ac output current $I_{\rm out}$ slightly reduces from 3.4 to 2.91 A by 14.4%. The difference between the measured $I_{\rm out}$ and the calculated one is mainly attributed to two factors. First, the parasitic resistances of passive circuit components will cause inevitable current attenuation as power increases, which has been revealed in the existing literature [25]–[26]. Second, the system detuning for ZVS operation also accounts for the difference from the ideal current value. The dc output current I_L experiences a reduction rate of 20.5% from 2.88 to 2.29 A. The larger reduction rate of I_L than $I_{\rm out}$ is caused by the parasitic capacitance of the rectifier diode, which cannot be neglected at MHz switching frequency and is in parallel with load resistance, increasing dc output fluctuation as the load varies.

Compared with the large load variation of 400%, both the ac and dc output current fluctuations are much smaller. Considering the impact of parasitic resistance and system detuning, the output current can be considered as load-independent.

3) Power and Efficiency Performance: With load resistance varying within 20–100 Ω, the system power P_L is provided in Fig. 15. It shows that the maximum power achieves 517 W and 100 Ω. System efficiency is provided in Fig. 16. The maximum dc–dc efficiency achieves 87.76% at 79 Ω and the maximum ac–ac efficiency achieves 89.31% at 60 Ω. The difference between ac–ac and dc–dc efficiency is caused by inverter and rectifier loss. At the peak dc–dc efficiency point of $R_L = 79$ Ω, the measured power is provided in Fig. 17, in which the load power achieves 478 W. The parasitic resistances of the CPT circuit account for most of the power loss. In the future research, high-quality passive components will be selected to further improve the system efficiency.

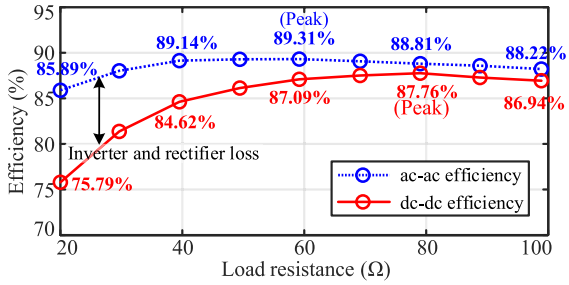


Fig. 16. Efficiency versus load resistance.

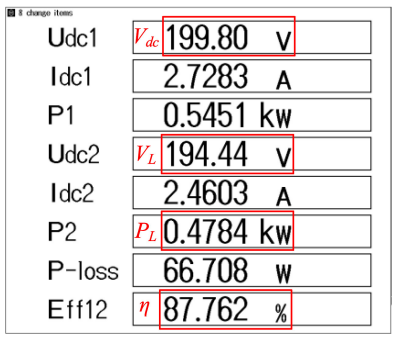


Fig. 17. Power at the peak efficiency.

VI. Conclusion

This article reviews the recent progress of CPT technology and aims to provide a methodology to systematically construct applicable CPT compensation circuits. Considering the duality with IPT, four basic two-inductor CPT compensations, SS, SP, PS, and PP, are developed and *y, z, g,* and *h* parameters are applied to model different CPT compensation. ZPA frequencies are identified with load-independent output property, and unified system efficiency is also investigated. By combining high-order T- and Π-type *LCL*/*CLC* networks with basic CPT compensations, a universal design methodology is proposed. In total, 144 feasible CPT topologies are derived, which covers existing ones and also predicts new candidates. Finally, ten typical CPT topologies are recommended and elaborated, and a 500-W *LCL-PP-LCL* compensated topology is designed and implemented with experimental validation.

Acknowledgment

The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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Yao Wang (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Northwestern Polytechnical University, Xi'an, China, in 2017 and 2020, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Drexel University, Philadelphia, PA, USA.

His research interests include wireless power transfer technology and resonant converters.

Hua Zhang (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Northwestern Polytechnical University, Xi'an, China, in 2011, 2014, and 2017, respectively.

From September 2014 to August 2015, she was a joint Ph.D. student funded by the China Scholarship Council with the University of Michigan, Dearborn, MI, USA. Since September 2015, she has been with San Diego State University, San Diego, CA, USA. She is currently an Assistant Research Professor with Drexel University, Philadelphia, PA, USA.

Her research reseach interests include wireless power transfer.

Fei Lu (Member, IEEE) received the B.S. and M.S. degrees from the Harbin Institute of Technology, Harbin, China, in 2010 and 2012, respectively, and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA, in 2017, all in electrical engineering.

He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA, USA. His research interests include power electronics and the application of electric vehicle charging.