

# Reduction in Circulating Current With Improved Secondary Side Modulation in Isolated Current-Fed Half Bridge AC–DC Converter

Manish Kumar , Student Member, IEEE, Sumit Pramanick , Member, IEEE, and B. K. Panigrahi , Senior Member, IEEE

**Abstract**—Current-fed half bridge converter with bidirectional switches on ac side and a full bridge converter on dc side of a high frequency transformer is an optimal topology for single stage galvanically isolated ac–dc converter for onboard vehicle charging application. The ac side switches are actively commutated to achieve zero current switching (ZCS) using single phase shift modulation (SPSM) and discontinuous current phase shift modulation (DCPSM). Furthermore, zero voltage turn-ON (ZVS) is achieved for dc side switches. Compared with SPSM, DCPSM maintains a constant peak current in the converter throughout the grid cycle of ac mains voltage. However, constant peak current contributes to a high circulating current near the zero crossings of ac mains voltage and also at light load conditions. This article proposes an improved discontinuous current phase shift modulation to increase the efficiency of the converter across different loading conditions. A dual control variable is adopted to actively reduce the circulating current while maintaining soft switching of both ac and dc side switches across the grid cycle of ac mains voltage. A 1.5-kW laboratory prototype has been developed to experimentally validate the analysis, design, and improvement in performance for different loading conditions.

**Index Terms**—AC–DC converter, current-fed half bridge, improved discontinuous current phase shift modulation (IDCPSM), single stage.

## I. INTRODUCTION

**E**LECTRIC vehicles (EVs) have gained tremendous popularity against their internal combustion engine (ICE) counterparts over the past decade. As EVs are becoming more common, ac–dc power converters are being explored for onboard charging applications (OBCs). OBCs provide the user with the convenience of using an ac utility outlet to charge the EV battery. The design of an OBC is mainly driven by electrical and volumetric efficiency [1]. These ac–dc power converters

should meet power quality standards on the grid side as per IEEE 519 [2]. Such converters should also have galvanic isolation between the ac side (grid) and the dc side (vehicle battery) as per Underwriters Laboratories (UL) 2202 safety standard [3].

The most general approach to attain the above requirements is a two-stage solution. An active power factor correction circuit as the first stage followed by an isolated dc–dc converter as the second stage [4], [5]. The isolated dc–dc converter is realized by a dual active bridge (DAB) in [4] and series resonant converter in [5]. However, the two-stage approach increases device count and losses, contributing to lower efficiency, along with increase in control complexity and volume. To overcome the disadvantages of two-stage solution, several single-stage ac–dc converter, have been reported in the literature [6]–[10].

A DAB-based single stage ac–dc converter with open-loop power factor correction and soft switching is presented in [6]. It consisted of matrix converter on ac side and full bridge converter on dc side. A combined frequency and phase shift modulation on a similar half-bridge matrix convert is presented in [7]. Another DAB-based converter with optimal zero voltage switching (ZVS) modulation in proposed in [8], which requires a line frequency synchronous rectifier on the ac side. A half bridge series resonant converter (HB-SRC)-based electrolytic capacitorless ac–dc converter with sinusoidal battery charging is reported in [9]. A resonant converter with multiwinding transformer is presented [10]. Single-stage bridgeless ac–dc converter with reduced component count and power factor correction has also been reported in the literature [11] and [12] for vehicle charging applications. However, these converters does not have galvanic isolation between the ac (grid) and dc (vehicle battery) side as per safety standard requirements.

A new class of current-fed isolated converters have gained popularity due to its distinct advantages over the voltage-fed isolated converters, such as lower input current ripple, inherent short-circuit protection, wide soft-switching operating range, and ease of current control [13], [14]. Work presented in [15] exhaustively compared the various isolated current-fed (ICF) topologies in terms of electrical and volumetric efficiency and reported that the L–L type isolated current-fed half-bridge (ICFHB) is an optimal topology among the different ICF topologies. Thus, an L–L type single stage single phase ICFHB ac–dc converter using bidirectional switches proposed in [16] is the focus of this article. This converter shown in Fig. 1 is conceptually

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The authors are with Power Electronics Lab, Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi 110016, India (e-mail: manish.kumar@ee.iitd.ac.in; sumit.pramanick@ieee.org; bkpanigrahi@ee.iitd.ac.in).

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TABLE I  
SINGLE STAGE AC–DC CONVERTER COMPARISON

Topology	DAB based Matrix Converter [6]	HB Matrix Converter [7]	DAB based [8]	HB SRC [9]	Resonant based [10]	Presented ICFHB Converter
No. of Active Components S+D <sup>1</sup>	12	8	12	8	22	8
No. of Passive Components L+C <sup>2</sup>	3	4	3	8	5	4
Soft Switching	ZCS on ac side ZVS on dc side	ZVS on dc side	ZVS on DAB	ZCS on SRC	ZCS on both ac and dc side	ZCS on ac side ZVS on dc side
Control Complexity	Simple duty ratio modulation	Complex frequency and phase shift modulation	Complex frequency, duty ratio and phase shift modulation	Simple phase shift modulation	Simple fixed duty ratio	Simple duty ratio modulation

<sup>1</sup> S+D: Total no. of switches and diodes, <sup>2</sup> L+C: Total no. of filter inductors, dc link and filter capacitors.

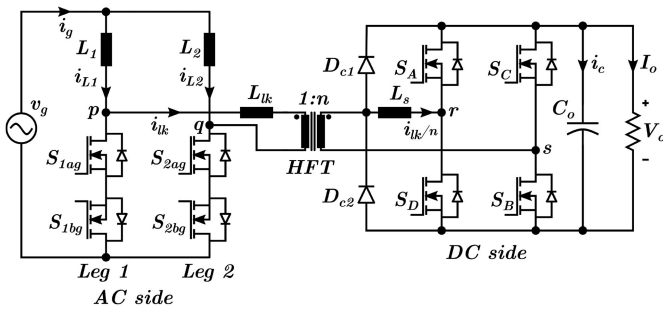


Fig. 1. L–L type current fed half bridge single stage ac–dc converter.

derived from an L–L type ICFHB dc–dc converter [17]. Table I highlights the advantage of ICFHB ac–dc converter in terms of lower component count, soft switching conditions, and simpler control over other single stage ac–dc converter.

However, one major drawback of such ICF converters is that a huge voltage spike appears at the switching node caused by an abrupt change in the current through the high-frequency transformer (HFT) winding. It occurs at the instant when the boost inductor current finds a path through the HFT windings. A common technique to mitigate the problem of voltage spike is to use an additional active clamp circuit. An active clamp circuit consisting of two active switches and a clamping capacitor was proposed in [18] for L–L type ICFHB. This clamp circuit assisted in zero voltage switching (ZVS) of all the switches. Another active clamp circuit consisting of a single switch, two diodes, a clamping capacitor, and a resonating inductor was proposed in [19] that ensures zero current switching (ZCS) of the main primary side switches. This increased component count in the auxiliary clamp circuit attributes to higher losses.

Another technique is the modulation-based approach also known as secondary side modulation (SSM) [17], [20]–[23]. The secondary side voltage-fed full bridge (VFFB) is used for active current commutation at the primary side current-fed half bridge (CFHB). This is achieved by using the reflected output voltage to completely transfer the boost inductor current from the commutating leg to the noncommuting leg through the HFT. The reflected output voltage is applied across the primary side of the HFT for a sufficiently long duration to force the

current through the commutating leg in the reverse direction, through the body diode. When the body diode current naturally reaches zero, the switch is turned OFF achieving ZCS. Also, body diode conduction in the secondary side ensures ZVS turn-ON of secondary side switches. The merit of this technique is that it does not require any additional circuits.

A single phase shift modulation (SPSM) for an L–L type ICFHB is proposed in [17]. The phase shift  $\phi$  is between the primary and secondary side bridge gating signals. Soft switching is achieved in both bridge switches for a wide operating range. However, when implemented in the case of the converter shown in Fig. 1 with ac input, the circulating current flowing through the switches and the HFT is substantially high near the zero crossing of the ac mains voltage and at light load conditions, attributing to poor efficiency of the converter.

A discontinuous current single phase shift modulation (DCPSM) is proposed in [20], where the current through the HFT drops to zero and a resonance occurs between the output capacitance of the dc side switches and the leakage inductance of the transformer. The circulating current flowing through the devices is still relatively large near the zero crossing of the ac mains voltage. A discontinuous current dual phase shift modulation (DCDPSM) for an L–L type ICFHB dc–dc converter is proposed in [21], where unsymmetrical switching pattern is applied to dc side switches to avoid resonance. However, a five control variable were adopted to reduce the circulating current value at light load conditions making the control architecture complex.

This article proposes an improved DCPSM (IDCPSM) with a simpler unsymmetrical switching pattern. The objective is to minimize the circulating current, flowing through the switches and the HFT across the grid cycle of ac mains voltage and also at different loading conditions. This is achieved by modulating the duty of the dc side VFFB in every switching interval. The duty of ac side CFHB is modulated to maintain unity power factor (UPF). This dual control variable approach keeps the control architecture simple and easy to implement. ZCS turn-OFF for ac side switches and ZVS turn-ON for dc side switches is maintained across the grid cycle. Reduced rms current through ac and dc side switches as well as through the HFT is achieved contributing to lower conduction losses with significant improvement in the efficiency of the converter.

TABLE II  
SWITCHING SCHEME IDCPSM

$v_g^{(k)}, i_g^{(k)}$	$v_g^{(k)} > 0, i_g^{(k)} > 0$	$v_g^{(k)} < 0, i_g^{(k)} < 0$
$S_{1ag}, S_{2ag}$	HFS at duty ratio $d_1^{(k)}$	Continuously on
$S_{1bg}, S_{2bg}$	Continuously on	HFS at duty ratio $d_1^{(k)}$
$S_A, S_D$	fixed duty ratio 0.5	fixed duty ratio 0.5
$S_B, S_C$	variable duty ratio $d_2^{(k)}$	variable duty ratio $d_2^{(k)}$

The rest of this article is organized as follows. Section II provides a detailed description of the schematic of ICFHB ac-dc converter. Operational stages with the proposed IDCPSM are described and compared with the conventional SSM in Section III. Section IV shows the experimental results of the implemented IDCPSM on the developed laboratory prototype and the comparative performance evaluation among the different SSM. Finally, Section V concludes this article.

## II. ICFHB AC–DC CONVERTER DESCRIPTION

The schematic of a single phase single stage galvanically isolated current-fed dual active bridge ac–dc converter is shown in Fig. 1. It consists of a current-fed half bridge converter with bidirectional switches on the ac side and a full bridge converter on the dc side, connected through a HFT.  $L_1$  and  $L_2$  are the two boost inductors.  $L_{lk}$  is the leakage inductance of the HFT. An external series inductor  $L_s$  is connected on the dc side to achieve the required total series inductance  $L_t = L_{lk} + L_s/n^2$ .  $C_o$  is the output filter capacitor. Diode clamps  $D_{c1}$  and  $D_{c2}$  are connected between the HFT terminals and external series inductor at dc side, to suppress this parasitic ringing, and clamping the ac side switch voltage to  $V_o/n$  during turn-OFF [24]. These diode clamps incur lower losses than the damping resistor used in [16].

The ac side switches are annotated as  $S_{xyg}$ , where  $x$  denotes leg number and  $y = a$  or  $b$ . The gate signals between ac side leg 1 and leg 2 switches are phase-shifted by  $180^\circ$ . The duty ratio  $d_1^{(k)}$  is always greater than 0.5, ensuring conduction overlap between the legs. Battery side switches are annotated as  $S_p$ , where  $p = A, B, C$ , or  $D$ .  $S_p$  turn-OFF is synchronized with the turn-OFF of  $S_{xyg}$  in the following way. In the positive half cycle of the grid voltage,  $S_{C,D}$  and  $S_{A,B}$  turn OFF is synchronized with  $S_{1ag}$  and  $S_{2ag}$ , respectively. In the negative half cycle,  $S_{C,D}$  and  $S_{A,B}$  turn OFF is synchronized with  $S_{2bg}$  and  $S_{1bg}$ , respectively. In case of SPSM, all the dc side switches are switched at duty ratio  $d_1^{(k)} - 0.5$ . Furthermore, in case of DCPSM, all the dc side switches are switched at fixed duty ratio  $d_2$ , irrespective of loading conditions. In the proposed IDCPSM, dc side switches  $S_{B,C}$  are switched at variable duty ratio  $d_2^{(k)}$  and  $S_{A,D}$  at fixed duty ratio of 0.5. Table II summarizes the switching scheme for IDCPSM.

## III. ICFHB AC–DC CONVERTER WITH IDCPSM

### A. Operational Stages

To simplify analysis, it has been assumed that the converter is operating at UPF. Furthermore, input ac mains voltage  $v_g^{(k)}(\tau)$  is assumed constant in a switching interval  $k$ . Variable with superscript  $k$  is changing every next switching interval and variable without the superscript  $k$  is assumed constant throughout the converter operation

$$v_g^{(k)}(\tau) = V_m \sin(\omega\tau) \quad (1)$$

$$i_g^{(k)}(\tau) = \frac{2P_o}{V_m} \sin(\omega\tau). \quad (2)$$

AC side duty cycle is given by

$$d_1^{(k)} = \frac{V_o - n |v_g^{(k)}(t)|}{V_o} \quad (3)$$

where,  $\tau = kT_s$  and  $T_s$  is the time period of a switching cycle,  $\omega = 2\pi/t_g$ ,  $t_g$  is the time period of a grid cycle,  $P_o$  is the output power, and  $V_o$  is the output voltage. Fig. 2(a) and (b) shows the operating waveform of the converter at the peak and near the zero crossing in the positive half cycle of ac mains voltage, respectively. Fig. 2(c) shows the ac side switch current  $i_{Sxyg}$  and dc side switch current  $i_{S_p}$  near the zero crossing in the positive half cycle of ac mains voltage. Inductor current  $i_{L1}^{(k)}(t)$  is given by

$$i_{L1}^{(k)}(t) = \begin{cases} \frac{1}{2} \left( i_g^{(k)} - \frac{v_g^{(k)}}{L_1} d_1^{(k)} T_s \right) + \frac{v_g^{(k)}}{L_1} [t - (k-1)T_s] & (k-1)T_s < t \leq (k-1 + d_1^{(k)}) T_s \\ \frac{1}{2} \left( i_g^{(k)} + \frac{v_g^{(k)}}{L_1} d_1^{(k)} T_s \right) + \frac{v_g^{(k)}}{L_1} [t - (k-1 + d_1^{(k)}) T_s] & -\frac{V_o}{nL_1} [t - (k-1 + d_1^{(k)}) T_s] & (k-1 + d_1^{(k)}) T_s < t < kT_s \\ \frac{1}{2} \left( i_g^{(k+1)} - \frac{v_g^{(k+1)}}{L_1} d_1^{(k+1)} T_s \right) & t = kT_s. \end{cases} \quad (4)$$

*Stage 1* ( $t_0, t_1$ ): Fig. 3(a) shows the equivalent circuit during this stage. At  $t_0$ , the HFT ac side winding current  $i_{lk}^{(k)}(t)$  equals boost inductor current  $i_{L2}^{(k)}(t)$ . The current through  $S_{2ag}$  body diode reaches zero and naturally turns-OFF achieving ZCS. The output parasitic capacitance of  $S_{2ag}$  charges to  $V_o/n$ , therefore  $v_{pq}^{(k)} = -V_o/n$ .  $S_{1ag}$  is ON in this stage.  $S_C$  and  $S_D$  are turned ON at  $t_0$  and their respective body diode current transfers to the channel of the devices thereby achieving ZVS.  $S_A$  and  $S_B$  are OFF during this stage and their respective device output capacitance are charged to  $V_o$ . The equation of  $i_{lk}^{(k)}(t)$  during stage 1 is given by (5) and at  $t_0$  is given by (6). The equation of ac side switch current and dc side switch current during this

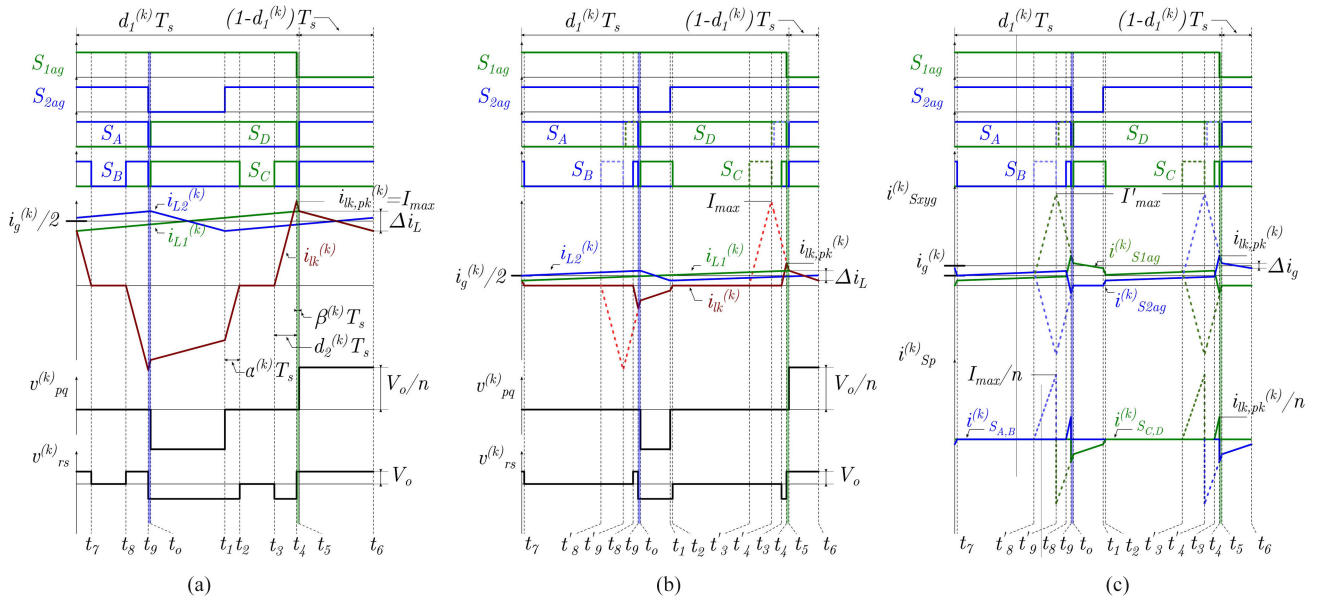


Fig. 2. Operating waveform of ICFHB ac-dc converter in a switching interval and in the positive half cycle of ac mains voltage (a) at  $\omega\tau = 90^\circ$  peak of ac mains voltage, (b) at  $\omega\tau = 10^\circ$  near zero crossing of ac mains voltage, (c) ac side switch current  $i_{Sx yg}$  and dc side switch current  $i_{S p}$  at  $\omega\tau = 10^\circ$  near zero crossing of ac mains voltage for DCPSM (dotted lines) and proposed IDCPSM (bold lines).

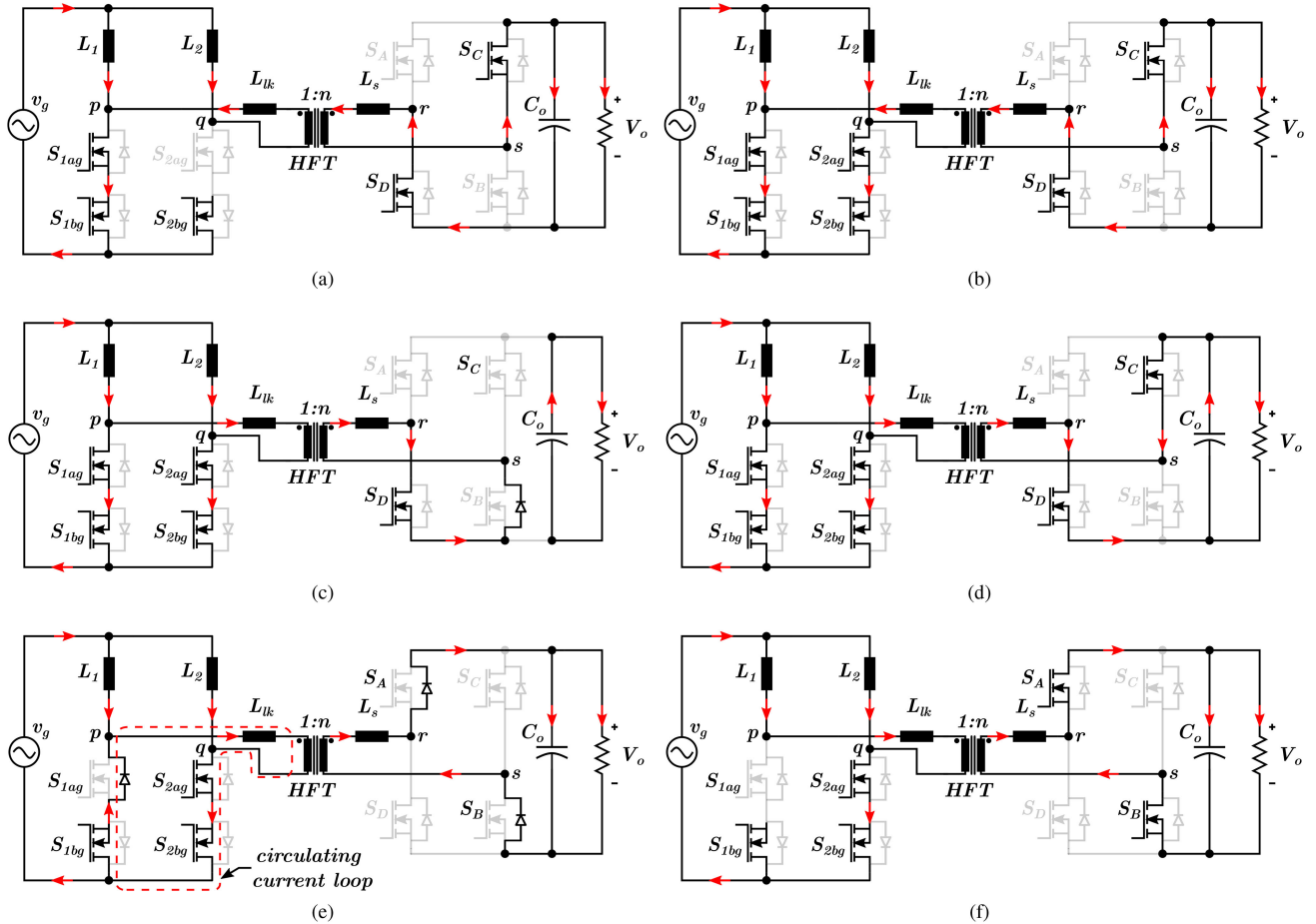


Fig. 3. Equivalent circuits of ICFHB ac-dc converter in a switching interval at various stages. (a) Stage 1 ( $t_0, t_1$ ). (b) Stage 2 ( $t_1, t_2$ ). (c) Stage 3 ( $t_2, t_3$ ). (d) Stage 4 ( $t_3, t_4$ ). (e) Stage 5 ( $t_4, t_5$ ). (f) Stage 6 ( $t_5, t_6$ ).

stage is give by (7) and (8), respectively

$$i_{lk}^{(k)}(t) = -\frac{(v_g^{(k)} - \frac{V_o}{n})}{L_2 + L_t}(t - t_0) + i_{lk}^{(k)}(t_0) \quad (5)$$

$$i_{lk}^{(k)}(t_0) = -\frac{1}{2} \left( i_g^{(k)} + \frac{v_g^{(k)}}{L_2} d_1^{(k)} T_s \right) \quad (6)$$

$$i_{S_{1ag}}^{(k)}(t) = i_{L_1}^{(k)}(t) + i_{lk}^{(k)}(t) \quad (7)$$

$$i_{S_C}^{(k)}(t) = i_{S_D}^{(k)}(t) = \frac{i_{lk}^{(k)}(t)}{n}. \quad (8)$$

*Stage 2* ( $t_1, t_2$ ): At  $t_1$ ,  $S_{2ag}$  is turned ON, as a result, its device output capacitance completely discharges in short duration.  $S_{1ag}$  is already on from stage 1, therefore  $v_{pq}^{(k)} = 0$ .  $S_C$  and  $S_D$  is also kept on from stage 1, and thus,  $v_{rs}^{(k)} = -V_o$ . Fig. 3(b) shows the circuit condition during this stage. The ac side HFT winding current gets transferred to switch  $S_{2ag}$  at a constant slope defined by the total series inductor  $L_t$  and  $v_{rs}^{(k)}$ . The equation of  $i_{lk}^{(k)}(t)$  during this stage is given by (9) and (10) and gives the value of  $i_{lk}^{(k)}(t)$  at  $t_1$ . AC side leg 1 switch current follows the same equation as (7) and leg 2 switch current is as per (11). DC side switch current in stage 2 is same as in stage 1

$$i_{lk}^{(k)}(t) = \frac{V_o}{nL_t}(t - t_1) + i_{lk}^{(k)}(t_1) \quad (9)$$

$$i_{lk}^{(k)}(t_1) = -\frac{1}{2} \left( i_g^{(k)} - \frac{v_g^{(k)}}{L_2} d_1^{(k)} T_s \right) \quad (10)$$

$$i_{S_{2ag}}^{(k)}(t) = -i_{lk}^{(k)}(t). \quad (11)$$

The duration of this stage is denoted as  $\alpha^{(k)}T_s$  as shown in Fig. 2(a) and is given by

$$\alpha^{(k)}T_s = \frac{nL_t \left| i_{lk}^{(k)}(t_1) \right|}{V_o}. \quad (12)$$

*Stage 3* ( $t_2, t_3$ ): At  $t_2$ , HFT winding current  $i_{lk}$  reaches zero as the line inductor current  $i_{L_2}$  gets completely transferred to switch  $S_{2ag}$ . Since both  $S_{1ag}$  and  $S_{2ag}$  is on,  $v_{pq}^{(k)} = 0$ .  $S_D$  is kept ON and gate pulse to  $S_C$  is removed. Since  $v_{rs}^{(k)} = -V_o$  at  $t_2$ , this voltage is kept applied across the winding of HFT for a short duration even after  $t_2$ . This rises the HFT winding current to a minimum value which in turn discharges the output device capacitance of  $S_B$  and charges the the output device capacitance of  $S_C$ . The body diode of  $S_B$  gets forward biased and the HFT winding current is maintained at that minimum value as  $v_{rs}^{(k)} = 0$ . This minimum current value is very small compared with the total load current and hence it is assumed to be zero. Fig. 3(c) shows the circuit condition during this stage.

*Stage 4* ( $t_3, t_4$ ): Fig. 3(d) shows the equivalent circuit during this stage.  $S_{1ag}$  and  $S_{2ag}$  is kept on and  $v_{pq}^{(k)} = 0$ . At  $t_3$ ,  $S_C$  is turned ON and its output device capacitance discharges and at the same time output device capacitance of  $S_B$  charges to  $V_o$ . Thus,  $v_{rs}^{(k)} = -V_o$  and is applied across the dc side winding of HFT, rising the current through it at a constant slope. The current

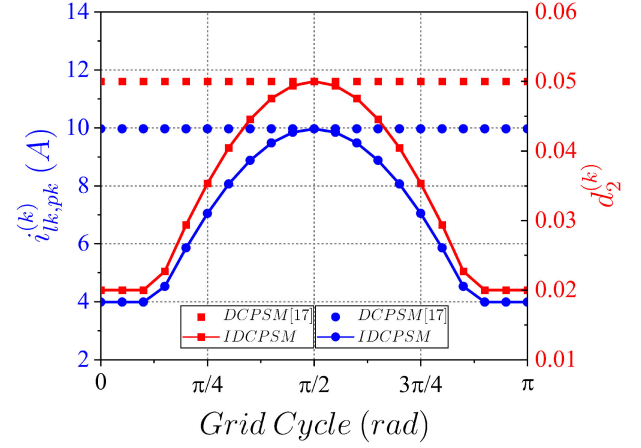


Fig. 4. DC side duty  $d_2^{(k)}$  and peak value of ac side HFT winding current  $i_{lk,pk}^{(k)}$  variation in a half grid cycle at  $P_o = 1.5$  kW and  $V_o = 345$  V.

through  $S_{1ag}$  falls at the same constant slope and through  $S_{2ag}$  rises at the same constant slope. This duration is kept sufficiently long enough for the current to go negative through  $S_{1ag}$  as shown in Fig. 2(c). The negative current flowing through the loop of ac side switches and the HFT is the circulating current  $i_{lk}^{(k)}$  as shown in Fig. 3(e) and is given by (13). The equation of  $i_{lk}^{(k)}(t)$  during this stage is given by (14). AC side leg 1 switch current and leg 2 switch current is as per (15) and (16), respectively. The dc side switch current equation in stage 4 is same as in stage 1

$$i_{cir}^{(k)} = i_{lk,pk}^{(k)} - \frac{1}{2} i_g^{(k)} \quad (13)$$

$$i_{lk}^{(k)}(t) = \frac{V_o}{nL_t}(t - t_3) \quad (14)$$

$$i_{S_{1ag}}^{(k)}(t) = i_{L_1}^{(k)}(t) - i_{lk}^{(k)}(t) \quad (15)$$

$$i_{S_{2ag}}^{(k)}(t) = i_{L_2}^{(k)}(t) + i_{lk}^{(k)}(t). \quad (16)$$

From Fig. 2(a) it can be noted that the duration of this stage  $d_2^{(k)}T_s$  is given by

$$d_2^{(k)}T_s = \frac{nL_t \left| i_{lk,pk}^{(k)} \right|}{V_o}. \quad (17)$$

It is clear from (17) that the peak value of ac side HFT winding current  $i_{lk,pk}^{(k)}$  is dependent on  $d_2^{(k)}$ . In the case of DCPSM, the value of  $d_2^{(k)}$  was decided for the maximum output power and was kept constant irrespective of the operating conditions [20]. Thus, for a fixed value  $d_2^{(k)} = 0.05$ ,  $i_{lk,pk} = I_{max}$  remained constant across the entire grid cycle of ac mains voltage as shown in Fig. 4. Therefore, from (13), it is evident that for a fixed value of  $I_{max}$ , the circulating current flowing through the converter is substantially high near the zero crossing of ac mains voltage and also at lighter load conditions. This high circulating current attributes to increased conduction losses in both ac and dc side switches and in the HFT. In the proposed IDCPSM, the ratio between  $i_g^{(k)}$  and  $i_{lk,pk}^{(k)}$  is kept fixed in the entire grid cycle of

ac mains voltage, i.e.,  $i_{lk,pk}^{(k)}$  follows the grid current sinusoidal envelope. This is achieved by varying  $d_2^{(k)}$  as a function of grid current in every switching interval as depicted in Fig. 4. The minimum secondary side duty  $d_{2,\min}^{(k)}$  is kept at 0.02, to ensure there is always minimum current available through the HFT winding for ZCS and ZVS in ac and dc side switches, respectively, as discussed in Section III-C.

Fig. 2(a) shows that, at the peak of ac mains voltage, i.e., at  $\omega\tau = 90^\circ$ , the winding current reaches  $I_{\max}$  during  $d_2T_s$ . In case of DCPSM, as shown by dotted lines  $(t'_4 - t'_3)T_s$  in Fig. 2(b), the peak winding current remained constant at  $I_{\max}$  near the zero crossing of ac mains voltage, i.e., at  $\omega\tau = 10^\circ$ . In the proposed IDCPSM,  $d_2^{(k)}$  is modulated as a function of grid current, and therefore the peak winding current is reduced to a much lower value of  $i_{lk,pk}^{(k)}$ , as shown by bold lines  $(t_4 - t_3)T_s$  in Fig. 2(b). The merits of the proposed IDCPSM can also be seen in Fig. 2(c). The peak current through the ac and dc side switches has also reduced substantially shown by bold lines as compared to DCPSM shown by dotted lines near the zero crossing of ac mains voltage. This reduced peak and circulating currents through the switches and the HFT across the grid cycle of ac mains voltage and at light load conditions, contributes to lower conduction losses, significantly improving the efficiency of the converter at lighter load conditions.

*Stage 5 ( $t_4, t_5$ ):* At  $t_4$ ,  $S_{1ag}$  is turned OFF and the negative current flowing through it shifts to its body diode.  $S_{2ag}$  continues to stay ON from the previous stage therefore  $v_{pq}^{(k)} = 0$ .  $S_C$  and  $S_D$  are turned OFF and its output parasitic capacitance charges to  $V_o$  and at the same time output parasitic capacitance of  $S_A$  and  $S_B$  discharges and their body diode starts conducting. Thus,  $v_{rs}^{(k)} = V_o$  and is applied across the dc side winding of HFT and current through it falls at a constant slope. The equation of  $i_{lk}^{(k)}(t)$  during this stage is given by (18) at  $t_4$  is given by (19). The ac side switch current follows the same equation as per stage 4. The dc side body diode current equation is given by (20)

$$i_{lk}^{(k)}(t) = \frac{-V_o}{nL_t}(t - t_4) + i_{lk}^{(k)}(t_4) \quad (18)$$

$$i_{lk}^{(k)}(t_4) = \frac{V_o d_2^{(k)} T_s}{nL_t} = i_{lk,pk}^{(k)} \quad (19)$$

$$i_{DA}^{(k)}(t) = i_{DB}^{(k)}(t) = -\frac{i_{lk}^{(k)}(t)}{n} \quad (20)$$

As represented in Fig. 2(a), this duration is  $\beta T_s$  and is given by

$$\beta^{(k)} T_s = \frac{nL_t \left| i_{lk}^{(k)}(t_5) - i_{lk}^{(k)}(t_4) \right|}{V_o} \quad (21)$$

*Stage 6 ( $t_5, t_6$ ):* At  $t_5$  the current through body diode of  $S_{1ag}$  falls to zero naturally turning OFF the device and achieving ZCS.  $S_{2ag}$  continues to stay on therefore  $v_{pq}^{(k)} = V_o/n$ .  $S_A$  and  $S_B$  are turned ON and the current through their body diode shifts to channel undergoing ZVS.  $v_{rs}^{(k)} = V_o$ . The equation of  $i_{lk}^{(k)}(t)$  during this stage is given by (22) and at  $t_5$  is given by (23). AC side leg 2 switch current equation is given by (24) and dc side

switch current equation is given by (25)

$$i_{lk}^{(k)}(t) = \frac{\left( v_g^{(k)} - \frac{V_o}{n} \right)}{L_1 + L_t} (t - t_5) + i_{lk}^{(k)}(t_5) \quad (22)$$

$$i_{lk}^{(k)}(t_5) = \frac{1}{2} \left( i_g^{(k)} + \frac{v_g^{(k)}}{L_1} d_1^{(k)} T_s \right) \quad (23)$$

$$i_{S_{2ag}}^{(k)}(t) = i_{L2}^{(k)}(t) + i_{lk}^{(k)}(t) \quad (24)$$

$$i_{SA}^{(k)}(t) = i_{SB}^{(k)}(t) = -\frac{i_{lk}^{(k)}(t)}{n} \quad (25)$$

Stage 1 to stage 5 describes the converter operation in a half switching interval. The other half is symmetrical to the above described stages as evident from stage 6. Table III presents the expressions of rms current through ac side HFT winding  $i_{lk,rms}^{(k)}$ , rms current through ac side switch  $i_{S_{xyg,rms}}^{(k)}$  and dc side switch  $i_{S_{p,rms}}^{(k)}$ , average current through the body diode of ac side switch  $i_{D_{xyg,avg}}^{(k)}$ , and dc side switch  $i_{D_{p,avg}}^{(k)}$  in a switching interval  $k$ . The corresponding rms ( $I_{xyg}, I_p, I_{lk}$ ) and average value ( $I_{xyg,bd}, I_{p,bd}$ ) in a grid cycle is obtained by substituting the current expression from Table III in (26) and (27), respectively

$$I_{rms} = \sqrt{\frac{1}{k} \sum_{k=1}^{t_g/t_{sw}} \left[ i_{rms}^{(k)}(t) \right]^2} \quad (26)$$

$$I_{avg} = \frac{1}{k} \sum_{k=1}^{t_g/t_{sw}} i_{avg}^{(k)}(t). \quad (27)$$

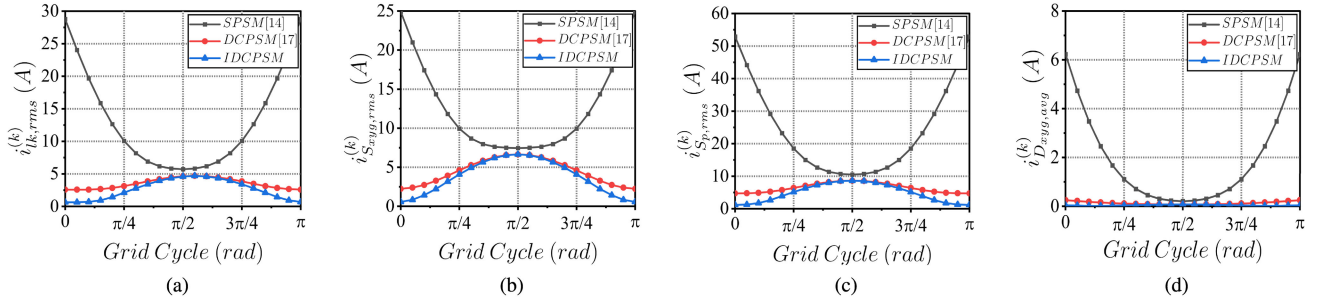
Assuming 20 switching intervals in half grid cycle, rms current through ac side HFT winding  $i_{lk,rms}^{(k)}$  for every switching interval  $k$  is estimated. The variation in a half grid cycle for SPSM, DCPSM, and proposed IDCPSM is shown in Fig. 5(a). It can be observed that  $i_{lk,rms}^{(k)}$  is maximum in switching intervals near the zero crossing of ac mains voltage for SPSM and is substantially low for DCPSM. In the proposed IDCPSM, this value is further reduced as the peak current through the windings of HFT is significantly reduced by modulating  $d_2^{(k)}$  across the grid cycle. Fig. 5(b) and (d) shows similar variation of rms current through ac side switch  $i_{S_{xyg,rms}}^{(k)}$ , dc side switch  $i_{S_{p,rms}}^{(k)}$ , and average current through the body diode of ac side switch  $i_{D_{xyg,avg}}^{(k)}$  in a half grid cycle. Here, too rms current through ac and dc side switches for the proposed IDCPSM has reduced. This amounts to lower conduction losses with considerable improvement in the converter's efficiency, especially at light load conditions.

## B. Diode Clamp $D_{c1}$ and $D_{c2}$ Functionality

At the beginning of stage 6, i.e.,  $t = t_5$  the current through body diode of  $S_{1ag}$  falls to zero and its output capacitance  $C_{oss,S1ag}$  starts charging. Fig. 6(a) shows the simplified circuit referred to ac side during this stage. Its a simple LC resonance circuit, wherein the device output capacitance starts resonating with total series inductance  $L_t$ . The voltage across ac side switch

TABLE III  
CURRENT EXPRESSIONS

Parameters	SPSM [17]	DCPSM [20]	Proposed IDCPSM
$i_{lk,rms}^{(k)}$	$\frac{i_g^{(k)}}{2} \sqrt{\frac{5}{3} - \frac{4d_1^{(k)}}{3}} + i_{lk,pk}^{(k)}$ $\sqrt{\frac{2d_1^{(k)}}{3} - \frac{1}{3} + \frac{i_g^{(k)}}{i_{lk,pk}^{(k)}} \left( \frac{1}{6} - \frac{d_1^{(k)}}{3} + \frac{2\beta^{(k)}}{3} \right)}$	$\frac{i_g^{(k)}}{\sqrt{2}} \sqrt{1 - d_1^{(k)} + \frac{\alpha^{(k)}}{3} + \frac{\beta^{(k)}}{3}}$ $+ I_{max} \sqrt{\frac{2d_2}{3} + \frac{2\beta^{(k)}}{3} + \frac{i_g^{(k)}}{I_{max}} \frac{\beta^{(k)}}{3}}$	$\frac{i_g^{(k)}}{\sqrt{2}} \sqrt{1 - d_1^{(k)} + \frac{4d_2^{(k)}}{3} + \frac{\alpha^{(k)}}{3} + \frac{7\beta^{(k)}}{3}}$
$i_{S_{xyg},rms}^{(k)}$	$\frac{i_g^{(k)}}{2} \sqrt{\frac{5}{3} - \frac{4d_1^{(k)}}{3}} + i_{lk,pk}^{(k)}$ $\sqrt{\frac{2d_1^{(k)}}{3} - \frac{1}{3} - \frac{\beta^{(k)}}{3} + \frac{i_g^{(k)}}{i_{lk,pk}^{(k)}} \left( \frac{\beta^{(k)}}{3} - \frac{d_1^{(k)}}{3} - \frac{1}{6} \right)}$	$\frac{i_g^{(k)}}{2} \sqrt{\frac{11}{3} - \frac{10d_1^{(k)}}{3} + \frac{4d_2}{3} + \frac{7\alpha^{(k)}}{3} + \frac{5\beta^{(k)}}{3}}$ $+ I_{max} \sqrt{\frac{2d_2}{3} + \frac{\beta^{(k)}}{3} + \frac{i_g^{(k)}}{I_{max}} \frac{2\beta^{(k)}}{3}}$	$\frac{i_g^{(k)}}{2} \sqrt{\frac{11}{3} - \frac{10d_1^{(k)}}{3} + \frac{4d_2^{(k)}}{3} + \frac{7\alpha^{(k)}}{3} + \frac{17\beta^{(k)}}{3}}$
$i_{D_{xyg},avg}^{(k)}$	$\left( i_{lk,pk}^{(k)} - \frac{i_g^{(k)}}{2} \right) \frac{\beta^{(k)}}{2}$	$\left( I_{max} - \frac{i_g^{(k)}}{2} \right) \frac{\beta^{(k)}}{2}$	$\frac{i_g^{(k)}}{2} \frac{\beta^{(k)}}{2}$
$i_{S_p,rms}^{(k)}$	$\frac{i_g^{(k)}}{2n} \sqrt{\frac{5}{6} - \frac{2d_1^{(k)}}{3}} + i_{lk,pk}^{(k)}$ $\sqrt{\frac{d_1^{(k)}}{3} - \frac{1}{6} + \frac{i_g^{(k)}}{i_{lk,pk}^{(k)}} \left( \frac{1}{12} - \frac{d_1^{(k)}}{6} + \frac{\beta^{(k)}}{3} \right)}$	$\frac{I_{max}}{n} \sqrt{\frac{d_2}{3}}$	$\frac{i_g^{(k)}}{2n} \sqrt{1 - d_1^{(k)} + \frac{4d_2^{(k)}}{3} + \frac{\alpha^{(k)}}{3} + \frac{7\beta^{(k)}}{3}}$
$i_{D_p,avg}^{(k)}$	0	$\frac{i_g^{(k)}}{2n} \left( 1 - d_1^{(k)} + \frac{\alpha^{(k)}}{2} + \frac{\beta^{(k)}}{2} \right) + \frac{I_{max}}{n} \frac{\beta^{(k)}}{2}$	0

Fig. 5. Variation of switching cycle rms and average value of current in a half grid cycle for different modulation scheme at  $P_o = 1.5$  kW and  $V_o = 345$  V. (a) RMS current through the ac side winding of HFT. (b) RMS current of ac side switch. (c) RMS current of dc side switch. (d) Average current of ac side body diode.

during resonating interval can be expressed by

$$v_{ds,S1ag}(t) = \frac{V_o}{n} (1 - \cos\omega_o(t - t_5)) \quad (28)$$

where  $\omega_o = 1/\sqrt{L_t C_{oss,S1ag}}$ . This can be represented in normalized state plane analysis by taking base voltage  $V_b = V_o/n$  and base current  $I_b = V_b/Z_o$ , where characteristics impedance  $Z_o = \sqrt{L_t/C_{oss,S1ag}}$  [25]. The normalized voltage  $m_{ds}(t)$  across the ac side switch and normalized current  $j_{lk}(t)$  through the total series inductor is given by

$$m_{ds}(t) = \frac{v_{ds,S1ag}(t)}{V_b}; j_{lk}(t) = \frac{i_{lk}(t)}{I_b}. \quad (29)$$

Fig. 6(b) shows the trajectories of  $m_{ds}$  and  $j_{lk}$  in a normalized state plane for an unclamped lossless circuit (dotted black) and with diode clamp (red). The starting point is at  $t = t_5$ , i.e.,  $v_{ds,S1ag} = 0$  and  $i_{lk} = I_{L1}$ , giving  $(0, J_1)$  in the normalized plane as starting point. The center of the circle is the steady-state solution  $(1, J_1)$ . In the absence of diode clamp, it is evident that

the peak voltage across the ac side switch is  $2m_{ds}$ , i.e.,  $2V_o/n$ . However, in the presence of diode clamp  $D_{c1}$ , the moment  $v_{ds,S1ag}(t)$  reaches  $V_o/n$ ,  $D_{c1}$  gets forward biased, clamping the dc side HFT terminal voltage to  $V_o$ . This reduces the characteristics impedance to  $Z_1 = \sqrt{L_{lk}/C_{oss,S1ag}}$  and the peak voltage across the ac side switch reduces to  $(1 + \sqrt{K})V_o/n$ , where  $K = L_{lk}/L_t < 1$ .

### C. ZCS/ZVS Condition Analysis

*AC Side:* It is evident that, during stage 5, the body diode of  $S_{1ag}$  will conduct only if the current through the HFT winding  $i_{lk}^{(k)}$  is greater than the peak value of inductor current  $i_{L1}^{(k)}$  which is clearly depicted in Fig. 2(c). Therefore, the necessary condition for ZCS turn-OFF of ac side switches  $S_{xyg}$  is given by (30). The minimum secondary side duty  $d_{2,min}^{(k)}$  to achieve ZCS across the grid cycle can be derived from ZCS conditions

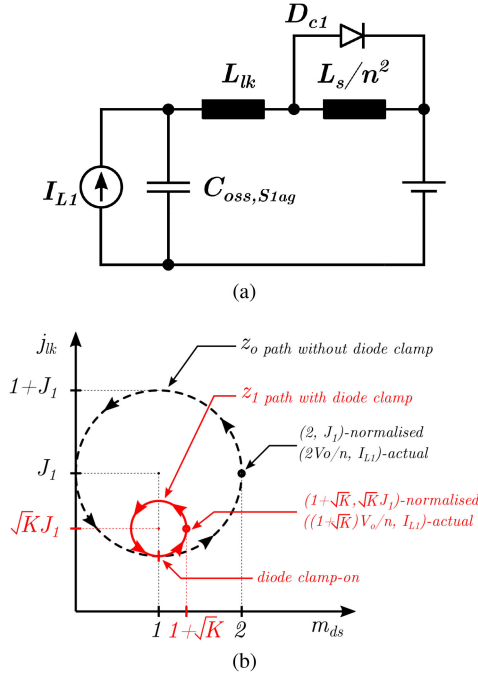


Fig. 6. ICFHB ac–dc converter. (a) Simplified equivalent circuit during stage 6 ( $t_5, t_6$ ). (b) Normalized state plane showing trajectories of  $m_{ds}$  and  $j_{lk}$ .

and is given by (31)

$$\begin{aligned}
 i_{lk}^{(k)}(t_4) &= i_{lk,pk}^{(k)} > i_{L1}^{(k)}(t_5) \\
 i_{lk}^{(k)}(t_9) &= -i_{lk,pk}^{(k)} > -i_{L2}^{(k)}(t_9) \\
 d_{2,\min}^{(k)} &> \frac{nL_t}{2V_oT_s} \left( \left| i_g^{(k)} \right| + \frac{|v_g^{(k)}|}{L_x} d_1^{(k)} T_s \right). \quad (31)
 \end{aligned}$$

*DC Side:* It can be observed from Fig. 2(a) that at  $t_4$ ,  $i_{lk,pk}^{(k)}/n$  simultaneously charges and discharges output capacitance of switches  $S_C, S_D$  and  $S_A, S_B$ , respectively. Therefore, the dead time  $t_{dt}$  maintained between the gating signals of  $S_A, S_B$  and  $S_C, S_D$  should satisfy the condition in (32), where  $T_c$  is the commutation interval (i.e., time required to completely charge and discharge the output capacitance of dc side switches)

$$t_{dt} > T_c. \quad (32)$$

The commutation interval  $T_c$  can be estimated using a charge-based model [26] and is given by (33), where,  $Q_{\text{coss}}(V_o)$  is the charge due to output voltage  $V_o$  across device output capacitance  $C_{\text{oss}}$

$$T_c = \frac{2nQ_{\text{coss}}(V_o)}{i_{lk}^{(k)}}. \quad (33)$$

#### IV. EXPERIMENTAL RESULTS

A 1.5-kW laboratory prototype was developed and is shown in Fig. 7. The performance of the converter with proposed modulation scheme is validated at different loading conditions. Table IV lists the parameters of the implemented prototype. The control

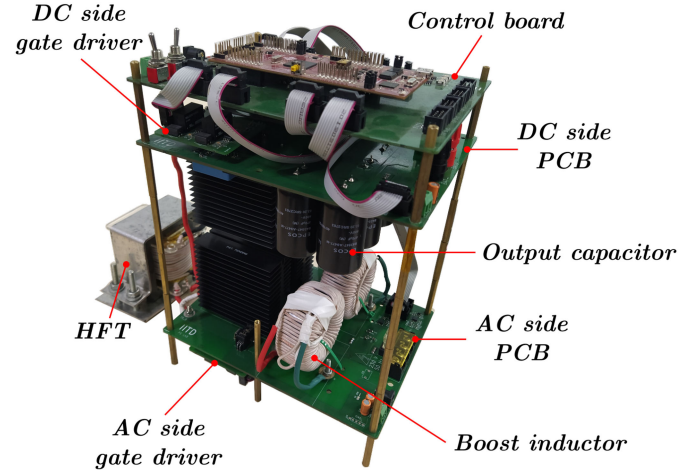


Fig. 7. Laboratory prototype of a L-L type ICFHB ac–dc converter.

TABLE IV  
PARAMETERS OF THE IMPLEMENTED HARDWARE PROTOTYPE

AC mains voltage	$V_g$	230 $V_{rms}$
AC mains frequency	$f_g$	50 Hz
Output Voltage	$v_o$	300 V...400 V
Output Power	$P_o$	1.5 kW
Switching Frequency	$f_{sw}$	100 kHz
Transformer ratio: 0.38		
Transformer	HFT	Prim: 26 turns, 135 wires, #40 SWG
		Sec: 10 turns, 260 wires, #40 SWG
		Core: Ferrite EE80/20 (2 stacked)
$L_{lk} = 600$ nH		
Boost Inductor	$L_1, L_2$	82 turns, 135 wires, #40 SWG
		Core: Kool M $\mu$ 77620
$7.5$ $\mu$ H		
Series Inductor	$L_s$	10 turns, 260 wires, #40 SWG
		Core: Kool M $\mu$ 77071
$940$ $\mu$ F		
Output Capacitor	$C_o$	4 parallel leg
		Each leg: 2 series connected 470 $\mu$ F (Electrolytic 400 V)
AC side SiC Mosfets	$S_{xyg}$	Cree C2M0080170P
DC side SiC Mosfets	$S_p$	UnitedSiC UF3C065030K4S

scheme is implemented in a TI TMS320F28397D launchpad and the combinational logic of gate pulses is generated using Xilinx XC6SLX4-based FPGA board.

#### A. Experimental Waveform

Fig. 8 shows the measured ac side HFT voltage  $v_{pq}$  and drain source voltage  $v_{ds,S1bg}$  with and without diode clamp. It can be observed that in presence of diode clamp, the peak voltage during turn-OFF across ac side switches has reduced by a ratio of  $(1 + \sqrt{K})$  along with substantial reduction in parasitic ringing.

Fig. 9(a) shows the measured ac grid voltage  $v_g$  along with the input grid current  $i_g$ , ac side HFT winding current  $i_{lk}$ , and

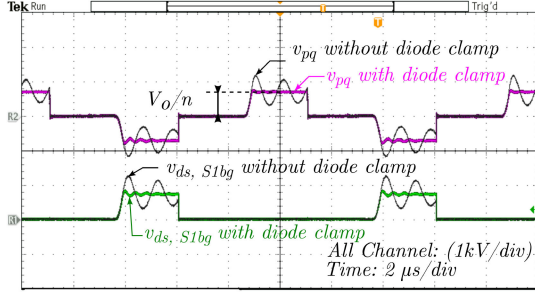


Fig. 8. Measured ac side HFT voltage  $v_{pq}$  and drain source voltage  $v_{ds,S1bg}$  with and without diode clamp.

output voltage  $V_o$  for DCPSM [20]. It can be observed that the peak value of the winding current is constant in the entire grid cycle of ac mains voltage. This is further depicted in Fig. 9(b) and (c) showing the zoomed waveform at the peak and near the zero crossing of the ac mains voltage, respectively. The peak value of the winding current is 10.2 A. This higher circulating current near the zero crossing of ac mains voltage, attributes to higher conduction losses and deteriorating efficiency.

Figs. 10(a) and 11(a) show the measured ac grid voltage  $v_g$ , grid current  $i_g$ , ac side HFT winding current  $i_{lk}$ , and output voltage  $V_o$  for proposed IDCPSM in few grid cycle at 1.5 and 0.5 kW, respectively. It is clear from the figure that converter is operating at 0.999 power factor. The total series inductor current now has a sinusoidal envelope with twice the ac mains voltage frequency. Its peak current value has reduced by almost 55% from the peak in Fig. 10(b) to near the zero crossing in Fig. 10(c) of the ac mains voltage. Furthermore, with the proposed IDCPSM the HFT winding peak current at light load condition of  $P_o = 0.5$  kW Fig. 11(b) has reduced to 6.1 A from 10.2 A at full load condition of  $P_o = 1.5$  kW in Fig. 10(b). This value remains constant for DCPSM across the grid cycle and at different loading conditions. The HFT winding peak current near the zero crossing of ac mains voltage remains constant at a much lower value of 4.6 A at different loading conditions in Figs. 10(c) and 11(c). This is because the minimum secondary side duty  $d_{2,min}^{(k)}$  is fixed at 0.02, to ensure that there is always a minimum current available through the HFT winding for ZCS at ac side and ZVS for dc side switches.

Fig. 12(a) and (b) shows the zoomed waveform of gate source voltage  $v_{gs,S1ag}$  and drain source voltage  $v_{ds,S1ag}$  of ac side switch  $S_{1ag}$ , along with the ac side HFT voltage  $v_{pq}$  at the peak and near the zero crossing of ac mains voltage, respectively. It can be observed that in the dotted region even though the gate voltage is at  $-5$  V, voltage across the switch is zero, indicating that its body diode is conducting as discussed in Section II. The switch naturally turns-OFF when the current through its body diode goes to zero, achieving ZCS across grid cycle.

Fig. 13(a) and (b) shows the zoomed waveform of gate source voltage  $v_{gs,S_D}$ , drain source voltage  $v_{ds,S_D}$  of dc side switch  $S_D$ , and dc side HFT voltage  $v_{rs}$  at the peak and near the zero crossing of ac mains voltage, respectively. It can be inferred that in the dotted region, voltage across the switch is zero, indicating

that its body diode is conducting and the gate voltage is applied after the dead time achieving ZVS across grid cycle.

## B. Loss Analysis

In order to estimate the total losses of the converter for proposed IDCPSM, DCPSM, and SPSM, semiconductor devices, boost inductor, series inductor, and HFT losses have been considered.

1) *Switching Devices*: Total conduction losses of ac side switches  $S_{xyg}$  and dc side switches  $S_p$  are estimated using

$$P_{\text{cond,ac}} = 4 (I_{xyg}^2 r_{on,xyg} + I_{xyg,bd} V_{xyg,bd}) \quad (34)$$

$$P_{\text{cond,dc}} = 4 (I_p^2 r_{on,p} + I_{p,bd} V_{p,bd}) \quad (35)$$

where  $r_{on,xyg}$  and  $r_{on,p}$  are the ON-state resistances,  $V_{xyg,bd}$  and  $V_{p,bd}$  are the forward voltage of ac and dc side body diodes, respectively. As ZCS is achieved for ac side switches  $S_{xyg}$ , switching losses are zero. Zero voltage turn-ON is achieved for dc side switches  $S_p$ , so only turn-OFF losses is considered and is given by

$$P_{sw,p} = f_{sw} E_{\text{off}}^* \frac{V_o}{V_{DS}} \quad (36)$$

where,  $E_{\text{off}}^*$  is the energy loss during turn-OFF which is a function of  $i_{lk,pk}/n$  obtained from datasheet [27] at specified drain-source voltage  $V_{DS}$ .

2) *Inductor*: Assuming,  $L_1 = L_2$ , the total copper loss of inductors is given by

$$P_{L_T,Cu} = 2I_{L1}^2 [r_{dc,L1} + r_{ac,L1}] \quad (37)$$

where,  $r_{dc,L1}$  and  $r_{ac,L1}$  are the equivalent ac and dc resistances of  $L_1$ , respectively. Total core loss density of inductors is estimated for every switching interval using (38) and is averaged out in a grid cycle

$$P_{L_T,\text{core}} = 2pB_{pk}^q f_{sw}^r \quad (38)$$

where parameters  $p$ ,  $q$ , and  $r$  can be obtained from datasheet [28].  $B_{pk}$  is half the flux density swing in a switching interval. Similarly, total losses in the series inductor  $L_s$  is estimated.

3) *HFT*: Copper loss occurred in HFT is given by

$$P_{\text{HFT,Cu}} = I_{lk}^2 [r_{dc,\text{HFT}} + r_{ac,\text{HFT}}] \quad (39)$$

where  $r_{dc,\text{HFT}}$  is sum of primary side and secondary side dc resistance referred to primary side. Similarly,  $r_{ac,\text{HFT}}$  is sum of primary side and secondary side ac resistance referred to primary side. Improved generalized Steinmetz (IGSE) equation is used to calculate core loss density of HFT [29] and is given by

$$P_{\text{HFT,core}} = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha} dt \quad (40)$$

where  $\Delta B$  is peak-to-peak flux density and

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos \theta|^\alpha 2^{\beta-\alpha} d\theta} \quad (41)$$

The parameters  $k$ ,  $\alpha$ , and  $\beta$  are the same parameters as used in the Steinmetz equation obtained from datasheet [30].

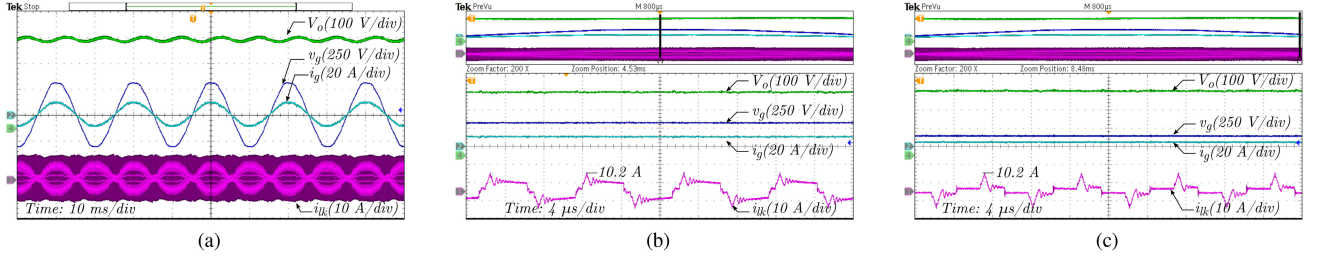


Fig. 9. Measured grid voltage  $v_g$ , grid current  $i_g$ , output voltage  $V_o$  and ac side HFT winding current  $i_{lk}$  for DCPSM in (a) grid cycle, (b) zoomed near peak of ac mains voltage, and (c) zoomed near zero crossing of ac mains voltage. ( $P_o = 1.5$  kW,  $v_g = 230$  V<sub>rms</sub>, and  $V_o = 345$  V).

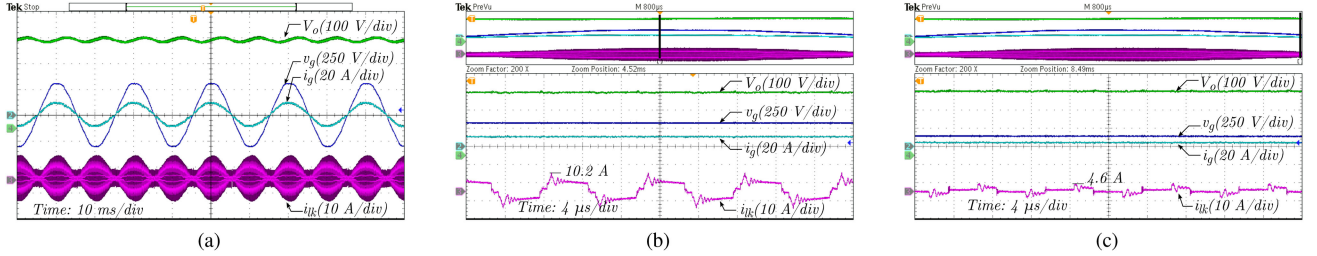


Fig. 10. Measured grid voltage  $v_g$ , grid current  $i_g$ , output voltage  $V_o$  and ac side HFT winding current  $i_{lk}$  for IDCPSM in (a) grid cycle, (b) zoomed near peak of ac mains voltage, and (c) zoomed near zero crossing of ac mains voltage. ( $P_o = 1.5$  kW,  $v_g = 230$  V<sub>rms</sub>, and  $V_o = 345$  V).

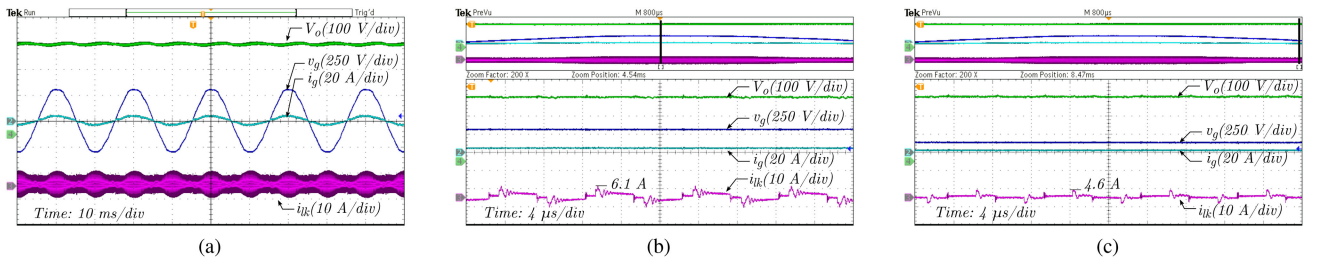


Fig. 11. Measured grid voltage  $v_g$ , grid current  $i_g$ , output voltage  $V_o$  and ac side HFT winding current  $i_{lk}$  for IDCPSM in (a) grid cycle, (b) zoomed near peak of ac mains voltage, (c) zoomed near zero crossing of ac mains voltage. ( $P_o = 0.5$  kW,  $v_g = 230$  V<sub>rms</sub>, and  $V_o = 345$  V).

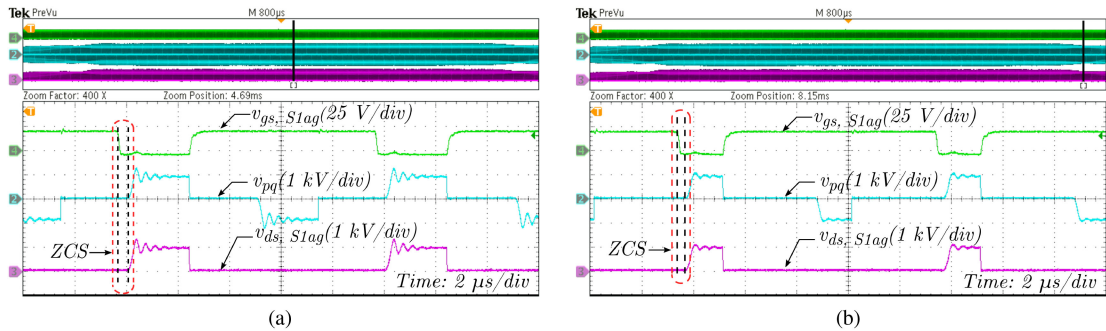


Fig. 12. Measured gate source voltage  $v_{gs,S1ag}$ , drain source voltage  $v_{ds,S1ag}$  and the ac side HFT voltage  $v_{pq}$  (a) zoomed near peak of ac mains voltage, (b) zoomed near zero crossing of ac mains voltage.

### C. Efficiency

Fig. 14 shows the efficiency curve for different SSM at nominal output voltage  $V_o = 345$  V. Power analyzer module of Tektronix MDO3104 DSO is used for measuring power. The measured efficiency is shown in bold lines and the theoretical estimated efficiency is shown in dashed line for different SSM.

Furthermore, it can be concluded that the proposed IDCPSM has the best performance among the compared SSM, with peak efficiency of 94.4%. The efficiency curve for IDCPSM remains nearly flat across different loading conditions. A substantial improvement of around 6.6% is seen at lighter loading condition of  $P_o = 0.5$  kW and 1.7% at full load  $P_o = 1.5$  kW from DCPSM. This improvement in performance is due to active control of the

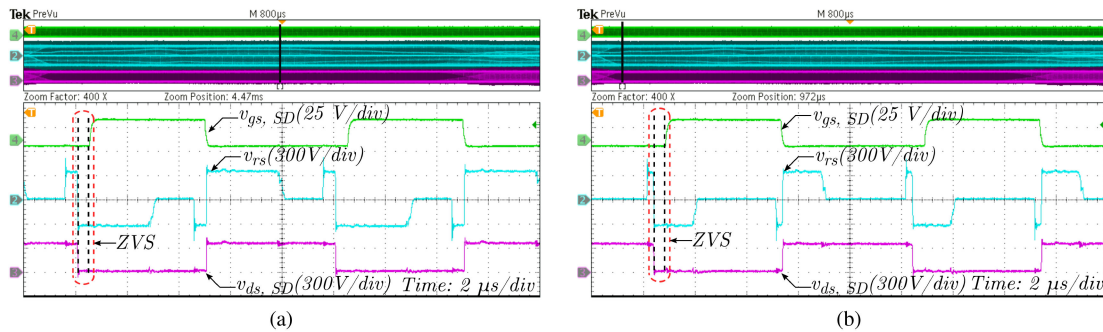


Fig. 13. Measured gate source voltage  $v_{gs,SD}$ , drain source voltage  $v_{ds,SD}$  and the dc side HFT voltage  $v_{rs}$  (a) zoomed near peak of ac mains voltage, (b) zoomed near zero crossing of ac mains voltage.

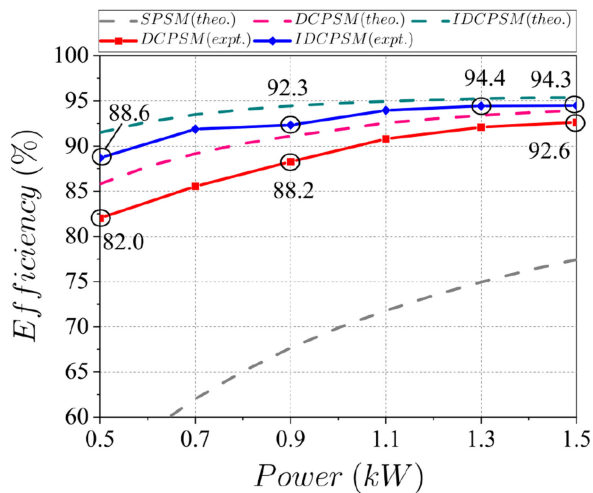


Fig. 14. Efficiency curve for different SSM at  $V_o = 345$  V.

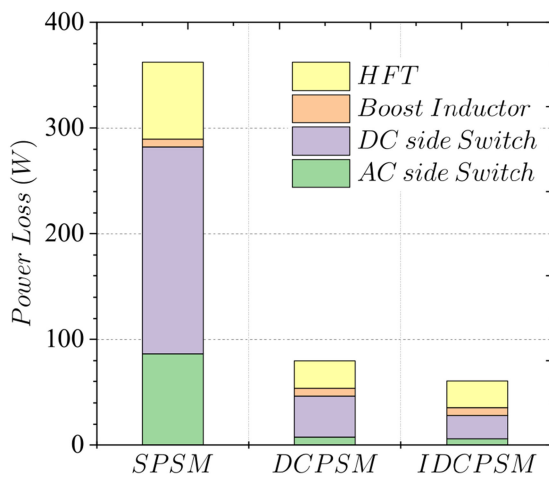


Fig. 15. Loss distribution among the components of L-L type ICFHB ac-dc converter at  $P_o = 1.5$  kW and  $V_o = 345$  V for different SSMs.

peak circulating across the grid cycle of the ac mains voltage and at different loading conditions. Fig. 15 shows the loss distributions among the components. The sum of switching and conduction loss is depicted as ac or dc side switch loss. HFT loss shows the total loss occurred in the HFT and the total series inductor. The reduction in peak value of circulating current with

the proposed IDCPSM reduces the conduction losses in ac side switch as depicted in Fig. 15. The total loss in the dc side switch is reduced by almost 42% from DCPSM. This is because both switching and conduction loss are reduced in the dc side switch. Furthermore, the total loss in the HFT is reduced by almost 20% with the proposed IDCPSM as both core loss and copper loss reduces in the HFT and the series inductor.

## V. CONCLUSION

This article proposed an IDCPSM for an L-L type ICFHB ac-dc converter. A dual control variable approach has been developed, where in ac side CFHB duty is modulated to maintain UPF and dc side VFFB duty is modulated to reduce the peak circulating current in a grid cycle of ac mains voltage and also at light load conditions. ZCS turn-OFF of ac side switches and ZVS turn-ON of dc side switches are maintained throughout the operating condition. This has significantly reduced the conduction and switching losses in both ac and dc side switches. A comparative performance analysis with different SSM reported in the literature is also presented. The proposed IDCPSM provides the best performance with peak efficiency of 94.4% and almost a flat efficiency profile across different loading conditions.

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**Manish Kumar** (Student Member, IEEE) received the B.E degree in electrical and electronics engineering from Visvesvaraya Technological University, Belgavi, India, in 2013, and the M.Tech. degree in power electronics and electrical drives from the Indian Institute of Technology Dhanbad, Dhanbad, India, in 2016. He is currently working toward the Ph.D. degree with Power Electronics, Electrical Machines and Drives Research Group, Indian Institute of Technology Delhi, New Delhi, India.

His research interests include high-frequency ac-dc and dc-ac bidirectional power electronics converters.



**Sumit Kumar Pramanick** (Member, IEEE) received the B.E. degree in electrical engineering from the Indian Institute of Engineering Science and Technology, Shibpur, India, in 2011, the M.Tech. degree in electronic systems engineering and the Ph.D. degree in power electronics and machine drives from the Indian Institute of Science, Bengaluru, India, in 2013 and 2017, respectively.

From 2016 to 2018, he was a Postdoctoral Fellow with Power Electronics, Microgrids and Subsea Electrical Systems (PEMSES) Center, University of Houston, Houston, TX, USA. In 2018, he joined the Indian Institute of Technology Delhi, New Delhi, India, where he is currently an Assistant Professor with the Department of Electrical Engineering. His research interests include multilevel converter, active filters, machine drives, and high-frequency power conversion.



**Bijaya Ketan Panigrahi** (Senior Member, IEEE) received the Ph.D. degree in power systems from Sambalpur University, Sambalpur, India, in 2004. He is currently a Professor with Department of Electrical Engineering, Indian Institute of Technology Delhi (IIT Delhi), New Delhi, India. He is heading the Centre for Automotive Research and Tribology, IIT Delhi. His research interests include soft computing, signal processing, power quality, renewable energy systems, power system protection, electric vehicles and charging infrastructure, cyber security of power

systems, and IoT.

Dr. Panigrahi is Associate Editor for *IET Smart Grid*, and the Editor of *IETE Journal of Research*.