

# Real-time Selective Harmonic Minimization Using a Hybrid Analog/Digital Computing Method

Jason Poon , *Member, IEEE*, Mohit Sinha, *Member, IEEE*, Sairaj V. Dhople , *Member, IEEE*,  
and Juan Rivas-Davila , *Senior Member, IEEE*

**Abstract**—We present a hybrid analog/digital computing circuit to solve a selective harmonic minimization problem. The approach leverages favorable attributes of digital and analog controllers to yield a fast and scalable optimization solver. A digital microcontroller programs the cost function and other user-defined inputs to the optimization problem. Voltages in the circuit represent switching angles. In steady state, the voltages converge to Karush–Kuhn–Tucker (KKT) points of the problem. We present a specific realization of the computing circuit that solves for eight independent switching angles for a quarter-wave symmetric pulsewidth modulation (PWM) driven two-level single-phase inverter. Seven undesired harmonics are minimized while retaining control over the modulation index. The proposed computing circuit is verified with simulations and a hardware implementation. The experimental results demonstrate that the proposed circuit can converge to the optimal solution in less than 5.0 ms, which is substantially faster than the existing methods and facilitates real-time implementation. Moreover, the steady-state power consumption of the hardware implementation is approximately 750 mW, which is also significantly lower than the published methods for comparable applications. The computing circuit is utilized to generate the PWM for a 2-kW single-phase inverter, which validates its feasibility in practical applications.

**Index Terms**—Analog computers, dc–ac power converters, optimization methods, power conversion harmonics, selective harmonic minimization.

## I. INTRODUCTION

NONLINEAR programming is an important method used in a variety of power and energy systems to solve optimization problems in which the objective function or constraints are nonlinear. Some examples of nonlinear programming control problems include model predictive control [1]–[3], optimal

power flow [4], [5], state and parameter estimation [6], and motor control [7], [8]. Another widely studied nonlinear programming control problem is selective harmonic minimization, which refers to a broad class of problems of optimally determining the pulsewidth modulation (PWM) of a power converter—typically a two-level or multilevel inverter—to precisely control or minimize the output harmonic content [9]–[14]. The technique generally improves harmonic spectra at reduced switching frequency, thereby yielding lower switching losses and designs with smaller filter components and heat sinks. Several variations of the selective harmonic minimization problem have been put forth for different inverter topologies and applications. For instance, various works consider nonequal dc-link voltages in multilevel inverters [15], the symmetry of the PWM waveform (e.g., quarter-wave, half-wave, nonsymmetrical) [16]–[18], and the consideration of cost functions that incorporate harmonic limits set by grid codes [19], [20].

A separate class of work, not considered in this article, is the selective harmonic *elimination* (SHE) problem, wherein a system of transcendental equations is solved to eliminate specific undesired harmonics [21]–[25]. These techniques utilize analytical solutions, approximations, or interpolations of the transcendental equations. These are typically solved on a digital microcontroller or field-programmable gate array to facilitate real-time implementation. While the underlying premise of SHE is similar to that of selective harmonic minimization, it does not permit the specification of an objective-based optimization problem (which provides added design and operational flexibility). This constrains its applicability outside settings where elimination of discrete, prespecified harmonics is the main goal. Further discussions of the similarities and differences between the selective harmonic minimization and SHE problems are available in [13] and [14].

Optimization-based selective harmonic minimization problems are typically implemented with precomputed solutions stored either as a lookup table (LUT) [15]–[20], [26]–[30] or as an artificial neural network (ANN) that is trained offline [31], [32] (see Table I for an overview of previous approaches). Many prior works do not provide data regarding the time required to obtain these precomputed solutions. Typical solution approaches are not tailored for online implementation, and they involve static LUTs or pretrained ANNs, which can also consume significant microcontroller resources and memory. For instance, a technique based on a particle swarm optimization [28] has been reported to require 290 ms to compute a single optimal solution, while other techniques using a genetic algorithm and bee algorithm have been reported to require 700 s and 10<sup>3</sup> s, respectively [26].

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Jason Poon and Juan Rivas-Davila are with the Electrical Engineering Department, Stanford University, Stanford, CA 94305 USA (e-mail: jason.poon@stanford.edu; jmrivas@stanford.edu).

Mohit Sinha is with Enphase Energy, Petaluma, CA 94954 USA (e-mail: msinha@enphaseenergy.com).

Sairaj V. Dhople is with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455 USA (e-mail: sdhople@umn.edu).

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TABLE I  
COMPARISON OF THE PROPOSED APPROACH WITH EXISTING SELECTIVE HARMONIC MINIMIZATION TECHNIQUES

	<b>This Work</b>	[25]	[14]	[26]	[27]	[28]	[29]	[30]
Number of angles optimized	8	3	3	15	5	3, 5, 7	6, 9	5
Optimization method	physics-based computing	BA	SA	SA	PSO	GA	hybrid GA	GA
Implementation method	analog/digital circuit	LUT	LUT	LUT	LUT	N/A	LUT	ANN
Time to optimal convergence	< 5 ms	1000 s	N/A	N/A	0.29 s	N/A	N/A	N/A
Real-time optimization?	<b>yes</b>	no	no	no	no	no	no	no

GA = genetic algorithm; BA = bee algorithm; SA = simulated annealing; PSO = particle swarm optimization; ANN = artificial neural network; LUT = lookup table; N/A = not indicated or implemented.

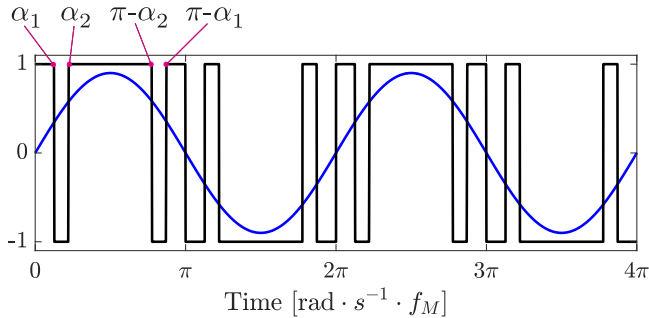


Fig. 1. Illustration of the switching angles  $\alpha = [\alpha_1, \alpha_2]$  for a quarter-wave symmetric PWM scheme with a fundamental modulation frequency  $f_M$ .

The response for the full range of anticipated signals and inputs has to be preprogrammed in LUT and ANN applications. This constrains the applicability of the approach to dynamically respond to conditions that are not preprogrammed.

Focusing on addressing limitations of the state-of-the-art methods surveyed above, we present a hybrid analog/digital circuit that solves the selective harmonic minimization problem in real-time. To focus ideas, we consider the design and analysis of a computing circuit for a quarter-wave symmetric PWM-driven two-level single-phase inverter. Fig. 1 illustrates an example PWM waveform with two switching angles. The cost function and desired modulation index are determined by the digital stage of the circuit, and these can be updated in real time. The voltages in the circuit correspond to the PWM switching angles, and in steady state, they are feasible solutions to the optimization problem [precisely, they are Karush–Kuhn–Tucker (KKT) points]. The proposed computing circuit is verified with a printed circuit board (PCB) hardware implementation that optimizes eight independent switching angles to eliminate seven undesired harmonics while maintaining control of the modulation index. The hardware implementation demonstrates convergence to the optimal solution in less than 5.0 ms, which is substantially faster than existing methods and facilitates real-time implementation. Moreover, the steady-state power consumption of the PCB implementation is approximately 750 mW, which is also significantly lower than published methods. The computing circuit is utilized to generate PWM signals for a 2-kW single-phase inverter, which validates its performance and feasibility in practical applications.

The remainder of this article is organized as follows. Section II presents the analysis and simulation of the hybrid analog/digital computing method for minimizing a single harmonic. Section III presents a generalized realization of the computing circuit for minimizing arbitrary numbers of harmonics while maintaining an arbitrary modulation index. Section IV presents a PCB

hardware implementation of the computing circuit that can minimize seven user-selected harmonics in real time for a two-level single-phase inverter, as well as simulations and experimental measurements that verify the functionality of the hardware implementation. Section V concludes this article.

## II. SPECIAL CASE: MINIMIZING ONE HARMONIC

In order to build intuition for the proposed hybrid analog/digital computing method, we consider a special case involving the minimization of a single harmonic for a two-level inverter subject to a quarter-wave symmetric PWM scheme [29].

### A. Problem Formulation

Consider the PWM switching waveform in Fig. 1, which illustrates switching angles  $\alpha = [\alpha_1, \alpha_2]$  for a quarter-wave symmetric PWM scheme with a fundamental modulation frequency  $f_M$ . In this example, we will focus on the goal of eliminating the third harmonic. The selective harmonic minimization problem takes the form

$$\min_{\alpha_1, \alpha_2} \varphi(\alpha) = (1 + 2(-\cos \alpha_1 + \cos \alpha_2) - m)^2 + (1 + 2(-\cos 3\alpha_1 + \cos 3\alpha_2))^2 \quad (1a)$$

$$\text{s.t. } f_1(\alpha) = \alpha_1 \geq 0, (\lambda_1) \quad (1b)$$

$$f_2(\alpha) = \alpha_2 - \alpha_1 \geq 0, (\lambda_2) \quad (1c)$$

$$f_3(\alpha) = -\alpha_2 + \pi/2 \geq 0, (\lambda_3). \quad (1d)$$

The constraints  $f_1(\alpha), f_2(\alpha), f_3(\alpha)$  ensure the correct ordering and bounds on the switching angles ( $0 \leq \alpha_1 \leq \alpha_2 \leq \frac{\pi}{2}$ ), and corresponding Lagrange multipliers are denoted by  $\lambda_1, \lambda_2, \lambda_3$ , respectively. In what follows, we will leverage the notation  $f(\alpha) = [f_1(\alpha), f_2(\alpha), f_3(\alpha)]^T$  and  $\lambda = [\lambda_1, \lambda_2, \lambda_3]^T$ .

For the modulation index,  $m = 0.9$ , Fig. 2 depicts the cost function  $\varphi(\alpha)$  from (1a) projected on a two-dimensional plane with the constraints in (1b)–(1d) shown as dashed lines. The function is nonconvex, but we can clearly visualize a minimum. Indeed, obtaining solutions from such visualizations is impossible when scaling the selective harmonic minimization problem to higher dimensions (i.e., when there are more than two switching variables). In general, however, multiple minima may exist, as has been discussed in previous literature (see, e.g., [13], [14]).

The proposed computing circuit physically realizes the KKT conditions [33]–[35] for the optimization problem in (1). The KKT conditions are first-order necessary conditions to guarantee a local minimum solution; such solutions are called KKT points. We denote these KKT points by  $\alpha^* = [\alpha_1^*, \alpha_2^*]^T, \lambda^* =$

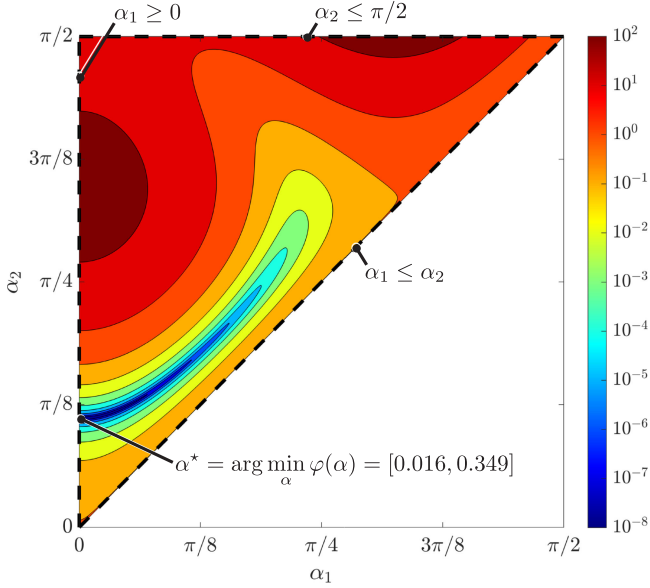


Fig. 2. Cost function  $\varphi(\alpha)$  in (1a) plotted as a function of  $\alpha_1$  and  $\alpha_2$ . The constraints in (1b)–(1d) bound the feasible solution space of  $\varphi(\alpha)$ . The cost function has a minimum at  $\alpha = [0.016, 0.349]$ .

$[\lambda_1^*, \lambda_2^*, \lambda_3^*]^T$ . The KKT conditions for (1) take the form

$$\frac{\partial \varphi(\alpha^*)}{\partial \alpha_\ell} + \sum_j \lambda_j^* \frac{\partial f_j(\alpha^*)}{\partial \alpha_\ell} = 0, \quad \ell = 1, 2 \quad (2a)$$

$$f_j(\alpha^*) \geq 0, \quad \lambda_j^* \leq 0, \quad \lambda_j^* f_j(\alpha^*) = 0, \quad j = 1, 2, 3. \quad (2b)$$

In particular, (2a) are the so-called stationarity conditions. Furthermore, in (2b),  $f_j(\alpha^*) \geq 0$  are primal feasibility conditions,  $\lambda_j^* \leq 0$  are dual feasibility conditions, and  $\lambda_j^* f_j(\alpha^*) = 0$  are complementary-slackness conditions. Given the constraints in (1b)–(1d), it follows that

$$\frac{\partial f_1}{\partial \alpha} = [1, 0], \quad \frac{\partial f_2}{\partial \alpha} = [-1, 1], \quad \frac{\partial f_3}{\partial \alpha} = [0, -1]. \quad (3)$$

It is relevant to note that the KKT conditions in (2a) and (2b) have been shown to be continuous or Lipschitz continuous for parametric optimization (the modulation index  $m$  being the exogenous parameter in this case) under a set of mild assumptions (see [36]). This is unlike the SHE problem, which involves solving harmonic transcendental equations, and have been shown to admit a discontinuous solution space for higher order multilevel converters (see [37]–[39]).

## B. Circuit Realization

We show next that, with an appropriate mapping and interpretation of the variables  $\alpha$  and  $\lambda$ , the circuit in Fig. 3 yields solutions of the KKT conditions (2a)–(2b). In this circuit, the primal variables,  $\alpha_1, \alpha_2$ , and dual variables,  $\lambda_1, \lambda_2, \lambda_3$ , are voltages at specific nodes; and constraints  $f_1, f_2, f_3$  are currents on specific branches. Moreover, note that resistors are labeled with conductances normalized to a 10-k $\Omega$  resistor ( $R_{\text{nom}}$ ), and negative resistors are realized by connecting one terminal of the resistor to an inverted output of the equivalent voltage [e.g., the  $-\alpha_\ell$  terminal in Fig. 4(a)]. The implementation of these inverted voltage rails is straightforward and involves an inverting op-amp network.

The resistor network on the bottom left of the figure encodes the sensitivities of the constraints with respect to the optimization variables (3). Likewise, the resistive network on the top left yields currents that capture the functional form of the constraints in (1b)–(1d). The cost function dynamics of  $\varphi(\alpha)$  are introduced to the circuit by time-varying controlled voltage sources with values precisely equal to  $\partial \varphi(\alpha) / \partial \alpha_\ell$ . The implementation of these controlled voltage sources is elaborated on Section III-B. As we will show through forthcoming developments, the circuit is constructed in a manner such that the steady-state values of these voltages and currents precisely satisfy the KKT conditions in (2a) and (2b). The integrator and nonlinear resistor blocks depicted in Fig. 4(a) and 4(b), respectively, are relevant to the operation of the circuit and are explained in detail here.

1) *Integrator Block*: The integrator block [Fig. 4(a)] is a transimpedance amplifier with the dynamics of a capacitor, that is, its output is a voltage that is proportional to the integral of the current at its input. The currents flowing into the integrators,  $i_\ell$ , originate from two sources. The first source is the term  $\partial \varphi(\alpha) / \partial \alpha_\ell$  (from the controlled voltage sources), while the second source is from the sum of terms  $\lambda_j \partial f_j(\alpha) / \partial \alpha_\ell$ .

2) *Nonlinear Resistor Block*: The nonlinear resistor [Fig. 4(b)] is a transimpedance amplifier with a voltage–current relationship shown in Fig. 4(b), specifically

$$\lambda = g(\mathcal{I}) = \begin{cases} 0 & \text{if } \mathcal{I} \leq 0 \\ -\mathcal{I}R & \text{if } \mathcal{I} > 0 \end{cases} \quad (4)$$

for some  $R$ , and where  $\mathcal{I}$  is the input current to the nonlinear resistor. A resistor network connects the input of the nonlinear resistors to voltages  $\alpha_1, \alpha_2, \alpha_3$  such that the currents flowing into the inputs of the nonlinear resistors are  $-f_1(\alpha), -f_2(\alpha), -f_3(\alpha)$ .

Having overviewed the subsystems of the circuit realization, we now examine its steady-state operation. First, consider that in steady state, the currents  $i_\ell$  are zero. Given the composition of the currents, we see that this precisely maps to the KKT stationarity condition (2a). Assume that in steady state,  $\alpha_j$  satisfy the constraints in (1b)–(1d); equivalently, the currents  $f_j(\alpha)$  satisfy the primal-feasibility constraints in (2b). With negative (or zero) input currents to the nonlinear resistors, the output voltages of the nonlinear resistors are  $\lambda_j = 0$ . With this, we see that the voltages  $\alpha_j, \lambda_j$  correspond to the KKT points,  $\alpha_j^*, \lambda_j^*$ , i.e., they satisfy all the KKT conditions in (2a) and (2b). It is relevant to note that while these KKT points represent local minima of (1), they are not necessarily the global minimum, as finding the global minimum of a nonconvex function such as (1a) is generally an NP-hard problem. Many conventional metaheuristic optimization techniques (e.g., genetic algorithms, particle swarm optimization, among others) introduce noise based on a Gaussian or Boltzmann distribution to the dynamics of the optimization variable to mitigate the likelihood of falling into undesirable local minima (e.g., [40]–[42]). In the simulation and experimental results that follow, we will evaluate the effectiveness of the solution obtained at the KKT points, which will depend on the initial condition of the circuit and the presence of noise. We will see that the proposed approach does not fall into undesired local minima and that the targeted harmonics are effectively minimized in the various tested scenarios. We hypothesize that the analog realization of the proposed circuit may provide a natural noise mechanism, similar to the artificial noise introduced in

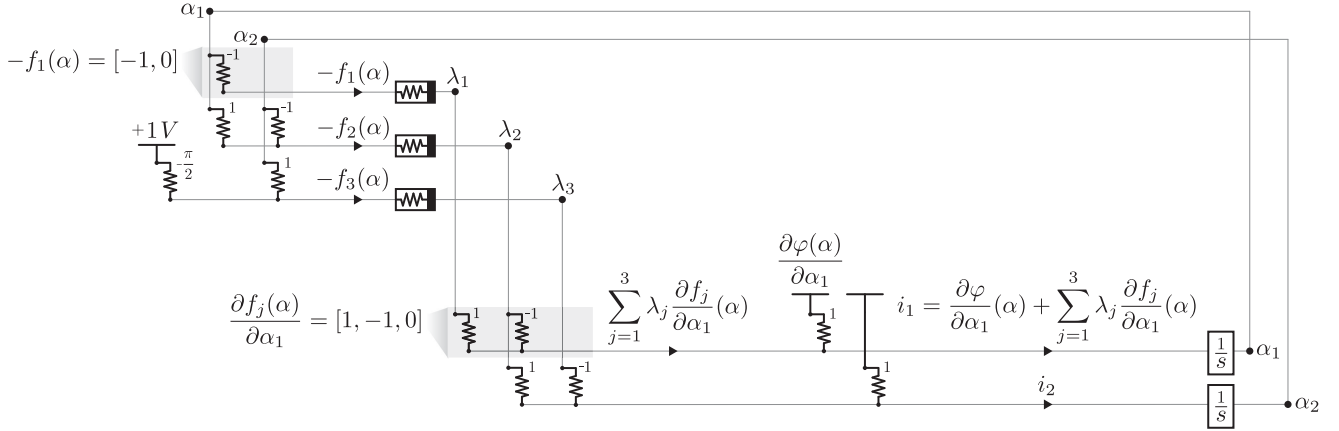


Fig. 3. Circuit implementation of the computing circuit that yields the optimal switching angles  $\alpha_1^*$  and  $\alpha_2^*$  that minimize the third harmonic in a two-level inverter. In particular, the circuit minimizes the cost function (1a) subject to constraints (1b)–(1d). The resistors are labeled with conductances normalized to a 10 k $\Omega$  resistor ( $R_{\text{nom}}$ ), and negative resistors are realized by connecting one terminal of the resistor to an inverted output of the equivalent voltage [e.g., the  $-\alpha_\ell$  terminal in Fig. 4(a)].

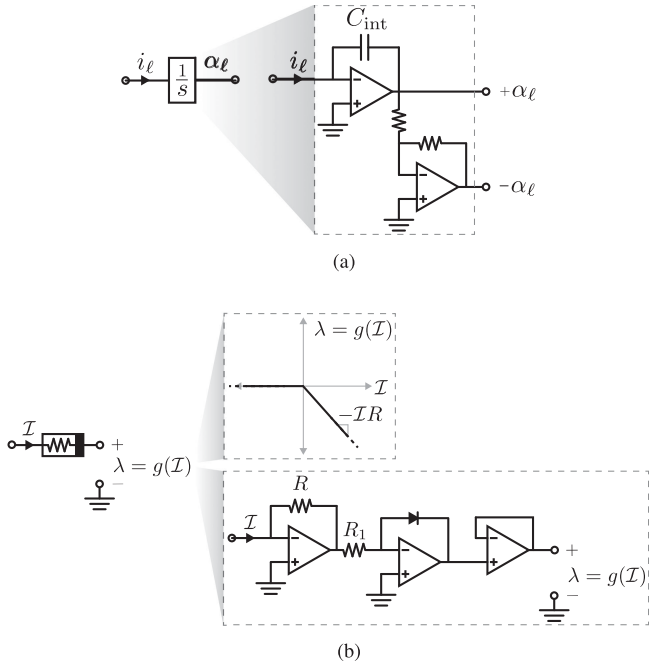


Fig. 4. Circuit implementations for elements in the computing circuits in Figs. 3 and 8. (a) Circuit implementation of the integrator blocks. (b) Dynamic behavior and circuit implementation of the nonlinear resistors.

conventional metaheuristic optimization techniques. Moreover, artificial noise or perturbations could be introduced to dynamics of the optimization variables by the digital microcontroller.

Alternatively, consider the scenario where, e.g., the constraint  $f_1(\alpha)$  is not satisfied, i.e., the voltage,  $\alpha_1$  is such that  $f_1(\alpha) < 0$ . In this case, the output of the first nonlinear resistor will be a negative voltage  $\lambda_1 = -f_1(\alpha)R$ . This produces a nonzero current  $i_1$  at the input of the first integrator, thereby perturbing the  $\alpha_1$  voltage. In all, the passive nonlinearity in (4) penalizes errors in the constraints  $f_j(\alpha)$  and perturbs the voltages  $\alpha_j$  in a direction to satisfy the constraints  $f_j(\alpha) \geq 0$ . The value of the resistance  $R$  in the nonlinear resistor block determines the magnitude of the perturbation and, thus, affects the rate of convergence to a steady-state solution that satisfies the constraints.

### C. Simulation Results

The computing circuit depicted in Fig. 3 is simulated using a SPICE-based simulation software. Results are shown in Fig. 5. Fig. 5(a) depicts the evolution of voltages (equivalently, switching angles),  $\alpha_1, \alpha_2$ . They approach the steady-state solution  $\alpha_1^* = 0.000099$  and  $\alpha_2^* = 0.349$ , in approximately 38  $\mu\text{s}$ . The simulated  $\alpha_2^*$  exactly matches the predicted minimum from Fig. 2, while the simulated value of  $\alpha_1^*$  is approximately the same, albeit with a 1.0% error within the  $[0, \pi/2]$  variable range. As will be shown, this error imposes no practical consequences on the effectiveness of the solution. The KKT multipliers,  $\lambda_j$ , are plotted in Fig. 5(b). They are driven to zero at around the same instance as the  $\alpha_j$  converge. The combination of these results indicates that all KKT conditions in (2a)–(2b) are satisfied in steady state. The resulting PWM time domain waveform is illustrated in Fig. 5(c) with the associated switching instances obtained from  $\alpha_1^*$  and  $\alpha_2^*$  appropriately labeled. An analysis of this waveform confirms that the modulation index is 0.90 as desired. Note that for this example, there are two switching instances per quarter period, resulting in eight switching instances per period (see Fig. 1). However, because the value of  $\alpha_1^* = 0.000099$  is below the minimum ON-time of the control logic, two of the switching transitions per period are suppressed. A frequency domain analysis of this waveform is shown in Fig. 5(d). The third harmonic is eliminated as desired, while all other odd harmonics remain.

### D. Transient Analysis

Next, we present a transient analysis of the switching-angle and KKT multiplier voltages as a function of the nominal resistance value ( $R_{\text{nom}}$ ) and the integrator capacitance ( $C_{\text{int}}$ ). The results of the simulation are illustrated in Figs. 6 and 7. Importantly, as shown, we see that while the values of  $R_{\text{nom}}$  and  $C_{\text{int}}$  affect the rate of convergence of the switching angles and KKT multiplier voltages in the circuit, they do not affect the final steady-state value. Therefore, the steady-state operation of the circuit will remain exactly the same. The simulation results illustrate that a larger  $R_{\text{nom}}$  and a larger  $C_{\text{int}}$  slow the convergence rate of the circuit, while the converse has the opposite affect.

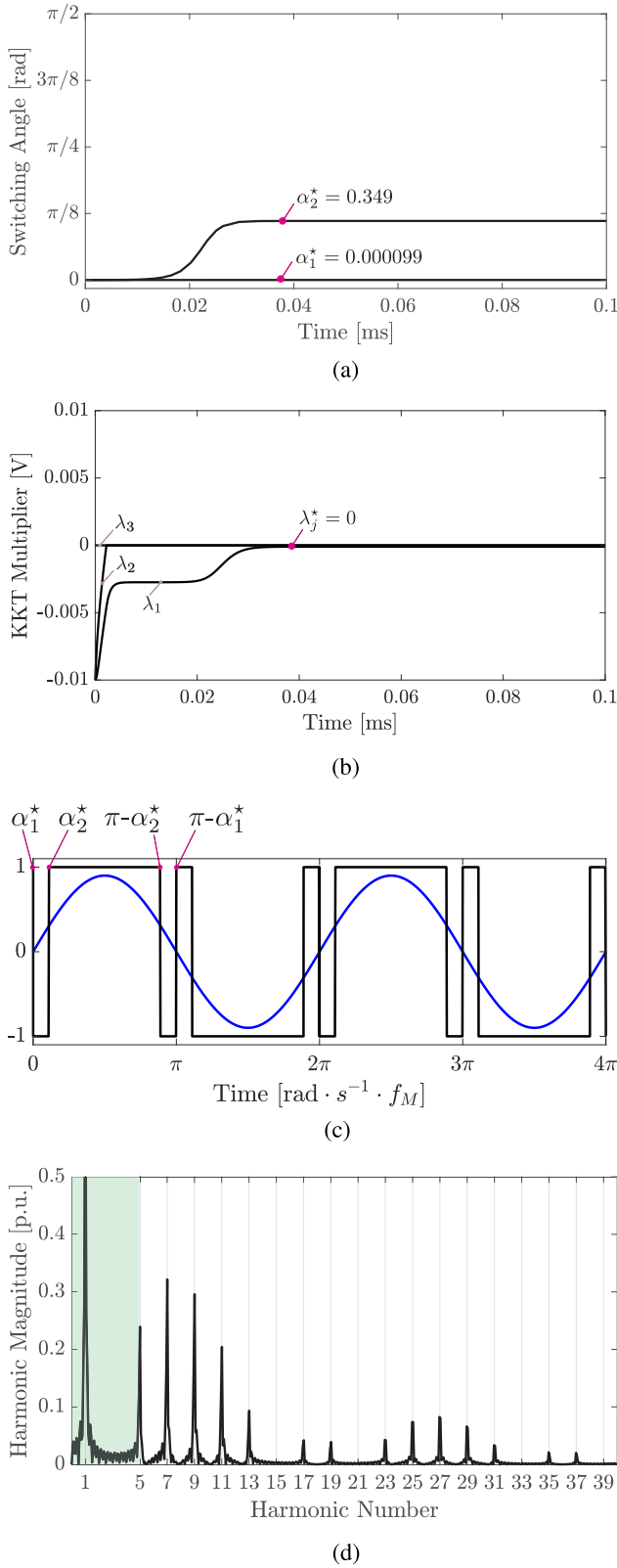


Fig. 5. Simulation of the computing circuit minimizing a single odd harmonic. (a) Switching angle voltages  $\alpha_1$  and  $\alpha_2$  converge to the optimal value in 38  $\mu\text{s}$ . These values closely match the expected minimum of the cost function  $\varphi(\alpha)$  in Fig. 2. (b) KKT multiplier voltages become zero in 38  $\mu\text{s}$ , indicating that the switching angle voltages satisfy the constraints in (1b)–(1d). (c) Optimal quarter-wave symmetric two-level waveform obtained by using the computed switching angles  $\alpha_1^*$  and  $\alpha_2^*$ . (d) Frequency domain analysis of the two-level waveform illustrates the minimization of the third harmonic.

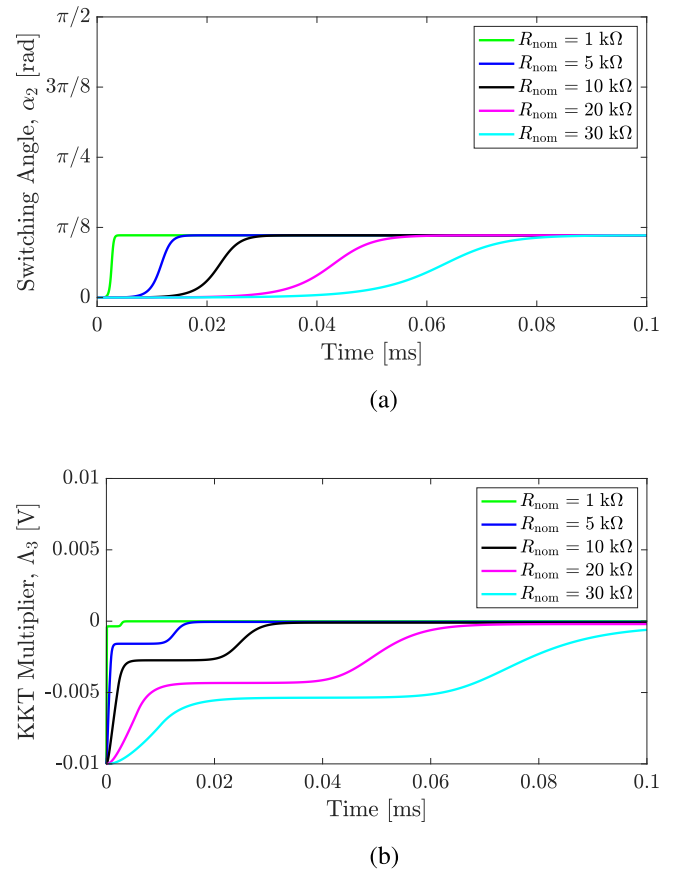


Fig. 6. Transient simulation of the proposed computing circuit with variations in the nominal resistance value  $R_{\text{nom}}$ . (a) Variations in the convergence of the switching angle voltage  $\alpha_2$  due to varying  $R_{\text{nom}}$ . (b) Variations in the convergence of the KKT multiplier voltage  $\Lambda_3$  due to varying  $R_{\text{nom}}$ .

Thus, the desired rate of convergence can be tuned by selecting  $R_{\text{nom}}$  and  $C_{\text{int}}$ . For example, a larger realization of the circuit may have more parasitics, and will require a slower transient in order to minimize ringing and to maintain the accuracy and stability. Conversely, if a design requires fast convergence, one would attempt to select the smallest possible  $R_{\text{nom}}$  and  $C_{\text{int}}$  while ensuring that layout parasitics are minimized as well. Such design considerations can be simulated *a priori* if the parasitics are modeled appropriately in the simulation model.

### III. GENERALIZED HYBRID ANALOG/DIGITAL COMPUTING CIRCUIT FOR SELECTIVE HARMONIC MINIMIZATION

In this section, we consider the generalized version of the selective harmonic minimization problem leveraging intuition gleaned from the special case of eliminating one harmonic considered in Section II.

#### A. Problem Formulation

The generalized version of the problem involves solving for the optimal values of  $N$  switching angles to minimize  $N - 1$  arbitrary harmonics while maintaining an arbitrary modulation index  $m$ . As before, we consider a quarter-wave symmetric PWM scheme for a two-level inverter. The precise formulation

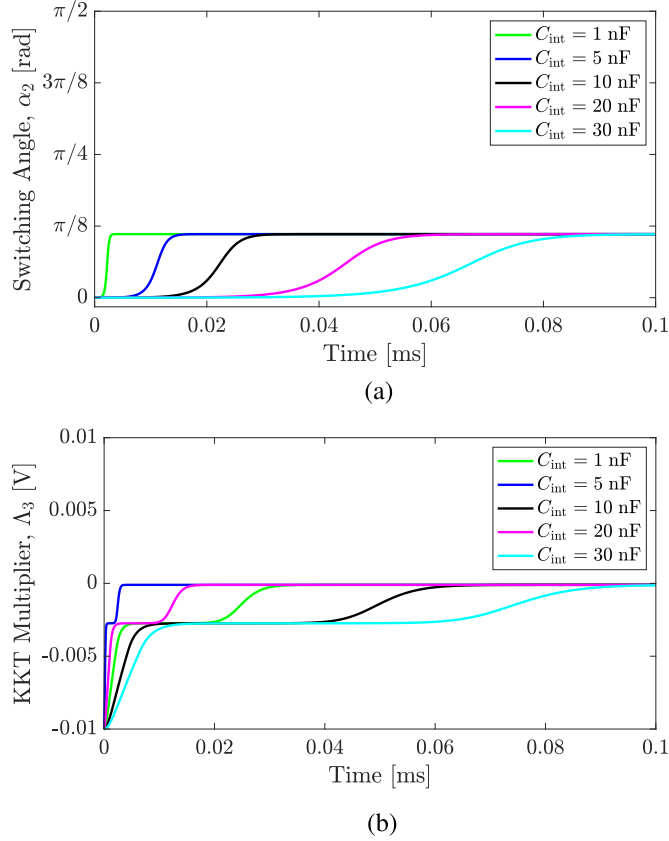


Fig. 7. Transient simulation of the proposed computing circuit with variations in the nominal resistance value  $R_{\text{nom}}$ . (a) Variations in the convergence of the switching angle voltage  $\alpha_2$  due to varying  $R_{\text{nom}}$ . (b) Variations in the convergence of the KKT multiplier voltage  $\lambda_3$  due to varying  $R_{\text{nom}}$ .

is given by

$$\min_{\alpha=[\alpha_1, \dots, \alpha_N]^T} \varphi(\alpha) = \left( 1 + 2 \sum_{\ell=1}^N (-1)^\ell \cos(\alpha_\ell) - m \right)^2 + \sum_{k=1}^{N-1} \left( 1 + 2 \sum_{\ell=1}^N (-1)^\ell \cos(h_k \alpha_\ell) \right)^2 \quad (5a)$$

$$\begin{aligned} \text{s.t. } f_1(\alpha) &= \alpha_1 \geq 0, (\lambda_1) \\ f_2(\alpha) &= \alpha_2 - \alpha_1 \geq 0, (\lambda_2) \\ &\vdots \\ f_N(\alpha) &= \alpha_N - \alpha_{N-1} \geq 0, (\lambda_N) \\ f_{N+1}(\alpha) &= -\alpha_N + \pi/2 \geq 0, (\lambda_{N+1}) \end{aligned} \quad (5b)$$

where  $\alpha = [\alpha_1, \dots, \alpha_N]^T$  are the  $N$  switching angles to be determined,  $\lambda = [\lambda_1, \dots, \lambda_{N+1}]^T$  are the Lagrange multipliers corresponding to the constraints  $f(\alpha) = [f_1(\alpha), \dots, f_{N+1}(\alpha)]^T$ , which enforce  $0 \leq \alpha_1 \leq \dots \leq \alpha_N \leq \frac{\pi}{2}$ ,  $m$  is the modulation index, and  $h_1, \dots, h_{N-1}$  are the orders of the undesired harmonics to be minimized. Depending on the application,  $h_1, \dots, h_{N-1}$  are typically chosen to be the lowest odd harmonics (i.e., 3, 5, 7, ...) or, for three-phase applications, the lowest odd nontriplen harmonics (i.e., 5, 7, 13, ...). The KKT conditions for problem (1) take the form

$$\nabla_{\alpha} \varphi(\alpha^*) + (\lambda^*)^T \nabla_{\alpha} f(\alpha^*) = 0 \quad (6a)$$

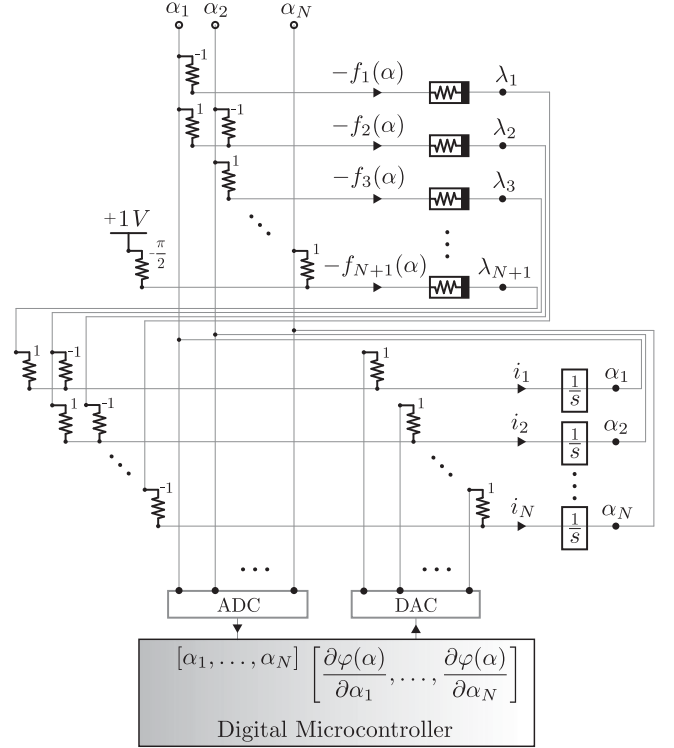


Fig. 8. Circuit implementation of the generalized computing circuit that yields  $N$  optimal switching angles  $\alpha_\ell^*$  that minimize  $N - 1$  arbitrary harmonics for a two-level inverter. The circuit minimizes the cost function of (5a) with the constraints of (5b). The resistors are labeled with conductances normalized to a 10-k $\Omega$  resistor, and negative resistors are realized by connecting one terminal of the resistor to an inverted output of the equivalent voltage.

$$f_j(\alpha^*) \geq 0, \lambda_j^* \leq 0, \lambda_j^* f_j(\alpha^*) = 0, j = 1, \dots, N + 1 \quad (6b)$$

where  $\nabla_{\alpha} \varphi(\cdot)$  captures the sensitivities of the cost function with respect to the optimization variables

$$\nabla_{\alpha} \varphi(\alpha) = \begin{bmatrix} \frac{\partial \varphi(\alpha)}{\partial \alpha_1} & \dots & \frac{\partial \varphi(\alpha)}{\partial \alpha_N} \end{bmatrix} \quad (7)$$

and  $\nabla_{\alpha} f(\cdot)$  is the Jacobian matrix corresponding to the constraints, given by

$$\begin{aligned} \nabla_{\alpha} f(\alpha) &= \begin{bmatrix} \frac{\partial f_1}{\partial \alpha_1} & \frac{\partial f_1}{\partial \alpha_2} & \dots & \frac{\partial f_1}{\partial \alpha_{N-1}} & \frac{\partial f_1}{\partial \alpha_N} \\ \frac{\partial f_2}{\partial \alpha_1} & \frac{\partial f_2}{\partial \alpha_2} & \dots & \frac{\partial f_2}{\partial \alpha_{N-1}} & \frac{\partial f_2}{\partial \alpha_N} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \frac{\partial f_N}{\partial \alpha_1} & \frac{\partial f_N}{\partial \alpha_2} & \dots & \frac{\partial f_N}{\partial \alpha_{N-1}} & \frac{\partial f_N}{\partial \alpha_N} \\ \frac{\partial f_{N+1}}{\partial \alpha_1} & \frac{\partial f_{N+1}}{\partial \alpha_2} & \dots & \frac{\partial f_{N+1}}{\partial \alpha_{N-1}} & \frac{\partial f_{N+1}}{\partial \alpha_N} \end{bmatrix} \\ &= \begin{bmatrix} 1 & 0 & \dots & 0 & 0 \\ -1 & 1 & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 0 \\ 0 & 0 & \dots & -1 & 1 \end{bmatrix}. \end{aligned} \quad (8)$$

## B. Circuit Realization

Fig. 8 illustrates the implementation of the generalized computing circuit to solve the optimization problem (5). In particular, the steady-state values of voltages  $\alpha_1, \dots, \alpha_N$  and

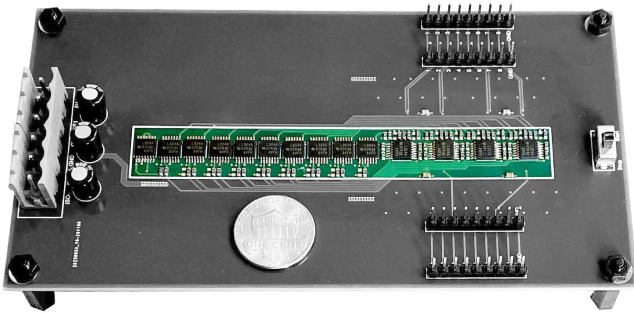


Fig. 9. Photograph of the hardware implementation of the proposed computing circuit with a US penny for scale. The active area of the circuit is shown in color and measures  $3.925 \times 0.535$  in.

$\lambda_1, \dots, \lambda_{N+1}$  converge to  $\alpha_1^*, \dots, \alpha_N^*$  and  $\lambda_1^*, \dots, \lambda_{N+1}^*$ , respectively, which satisfy the KKT conditions (6a)–(6b).

The computing circuit merges an analog system composed of a resistor network, integrators [Fig. 4(a)], and nonlinear resistors [Fig. 4(b)], with a digital system composed of a small microcontroller and associated analog-to-digital (ADC) and digital-to-analog converters (DACs). The resistor network on the bottom left of the figure encodes the sensitivities of the constraints with respect to the optimization variables as described by the Jacobian in (8). The resistor network on the top left yields currents that capture the functional form of the constraints in (5b). The microcontroller interfaces with particular nodes in the resistor network through the ADCs and DACs. The microcontroller computes  $\partial\varphi/\partial\alpha_\ell$  based on measurements of  $\alpha_\ell$ . The programmed cost function includes the harmonics  $h_1, \dots, h_{N-1}$  that are to be minimized, along with the modulation index  $m$  of the two-level waveform. Notably, these parameters can be changed in real time and the circuit will dynamically converge to a new solution.

The operation of this circuit is largely similar to that of the realization presented in Section II. In particular, steady-state values of the currents,  $i_\ell, \ell = 1, \dots, N$  are all zero, and the constitution of these currents implies that this steady-state operating condition satisfies the stationarity condition (6a). Furthermore, the nonlinear resistors operate in concert with the integrators to ensure that voltages,  $\lambda_1^* \leq 0, \dots, \lambda_{N+1}^* \leq 0$  and currents  $f_1(\alpha^*) \geq 0, \dots, f_{N+1}(\alpha^*) \geq 0$ .

#### IV. EXPERIMENTAL VALIDATION

In this section, we present a PCB implementation of the proposed computing circuit that solves the selective harmonic minimization problem with eight independent switching angles, that is,  $N = 8$ , for an effective switching frequency of  $8 \times 4 \times 60$  Hz = 1920 Hz. The PCB implementation, moreover, generates the associated PWM signals to control a 2-kW single-phase inverter, from which we measure the output voltage to verify the minimization of the seven ( $N - 1$ ) desired harmonics.

##### A. Hardware Details

The PCB implementation of the computing circuit is depicted in Fig. 9 with a US penny for scale. The active area of the analog and digital systems of the circuit is shown in color and measures 3.925 by 0.535 in. The remaining area of the PCB (shown in grayscale) is used for power connectors, voltage measurement test points, signal connectors to the single-phase inverter, and

a physical switch for starting the computation or resetting the voltages  $\alpha_\ell$  to a predefined initial condition.

The analog system is implemented with 14 LM324 general purpose quad op amps, 111 SMD 0603 resistors, 26 SMD 0603 capacitors, and 9 SOT-23 diodes connected to realize the circuit diagram in Fig. 8. The analog components used in the circuit are generally robust to temperature variations up to  $125^\circ\text{C}$  and other operating variations, and, moreover, can be implemented using robust automotive grade components if high precision or operation in harsh conditions is required. The analog system of the circuit is “fixed” (i.e., unchanged between different experiments) for  $N = 8$  and for the constraints  $f_j \geq 0$  from (5b). The digital system is implemented with a TI Delphino F28379D microcontroller, its internal ADCs, and an LTC2666 8-channel 16-bit DAC. The microcontroller samples  $\alpha_1, \dots, \alpha_8$  through the ADC, computes  $\partial\varphi/\partial\alpha_1, \dots, \partial\varphi/\partial\alpha_8$ , and feeds the result back to the analog system through the DAC. The function  $\varphi(\alpha)$  is programmed according to the harmonics to be minimized and the desired modulation index, and can be updated in real time. The microcontroller also contains logic to generate the quarter-wave symmetric PWM based on its measurements of  $\alpha_1, \dots, \alpha_8$ . The PWM output is connected to a custom-designed single-phase inverter with a dc-link voltage of 400 V, whose output is connected to a  $100\text{-}\Omega$  resistive load. In steady state, the overall power consumption of the computing circuit, including the analog and digital systems, is approximately 750 mW. While many previous works on selective harmonic minimization do not provide data with respect to power consumption, most metaheuristic optimizers (which many prior techniques utilize) are typically solved on a desktop computer using MATLAB or a similar software, which would consume on the order of 10’s or 100’s of watts. Therefore, the power consumption of the proposed computing circuit is substantially lower than such techniques. Further study is required to precisely benchmark the power consumption of existing methods used for selective harmonic minimization with the proposed circuit.

##### B. Verification of Hardware Implementation

We now present simulation and experimental verification of the hardware implementation discussed above. We conduct three verification tests that involve the minimization of the following:

- 1) the first seven odd harmonics;
- 2) the first seven odd nontriplen harmonics; and
- 3) the first seven odd nontriplen harmonics while the modulation index command,  $m$ , is time varying.

These verification tests demonstrate the speed of the proposed computing circuit in obtaining the optimal solution, as well as the programmability and generalizability of the implementation to minimize any set of harmonics that are specified by the user. Moreover, the test in which the modulation command is varied intentionally with time demonstrates the ability of the proposed circuit to dynamically respond to inputs and operating conditions that change the optimal solution. This is unique in the literature to the best of the authors’ knowledge.

1) *Minimization of First Seven Odd Harmonics*: In the first verification test, the digital system is programmed to minimize the first seven odd harmonics ( $h = 3, 5, 7, 9, 11, 13, 15$ ) while maintaining a constant modulation index  $m = 0.9$ . Fig. 10

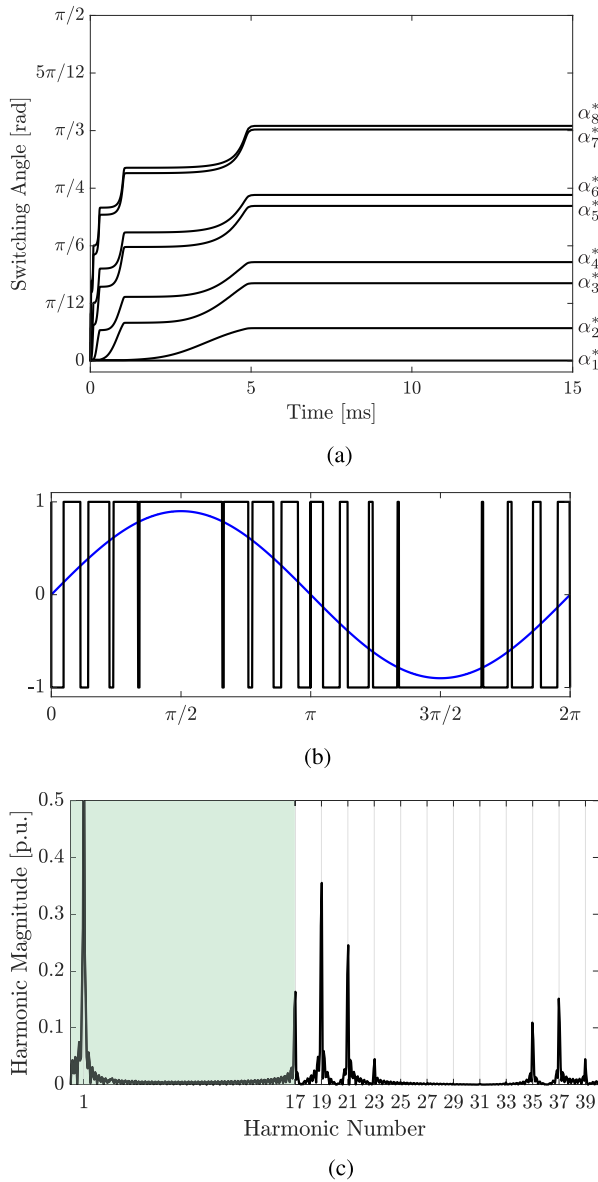


Fig. 10. Simulation of the computing circuit minimizing the first seven odd harmonics ( $h = 3, 5, 7, 9, 11, 13, 15$ ). (a) Switching angle voltage variables  $\alpha_\ell$  converge to the optimal value  $\alpha_\ell^*$  in approximately 5 ms. (b) Optimal quarter-wave symmetric two-level waveform obtained by using the computed switching angles  $\alpha_\ell^*$ . (c) Frequency domain analysis of the two-level waveform confirms the minimization of the first seven odd harmonics.

presents the results from a SPICE-based simulation of this scenario. As shown in Fig. 10(a), the eight switching angle voltage variables  $\alpha_\ell, \ell = 1, \dots, 8$  from the computing circuit converge in steady state to KKT points,  $\alpha_\ell^*, \ell = 1, \dots, 8$ . Fig. 10(b) illustrates one period of the inverter waveform obtained by using these computed switching angles. A frequency-domain analysis of this waveform [Fig. 10(c)] confirms that the first seven odd harmonics are minimized via these KKT points obtained in steady state,  $\alpha_\ell^*, \ell = 1, \dots, 8$ . Fig. 11 illustrates the measurements from the hardware implementation of this scenario. As shown in Fig. 11(a), voltage measurements of  $\alpha_\ell, \ell = 1, \dots, 8$  from the analog system illustrate that the circuit converges to a steady state value in 5.0 ms. The transient dynamics and

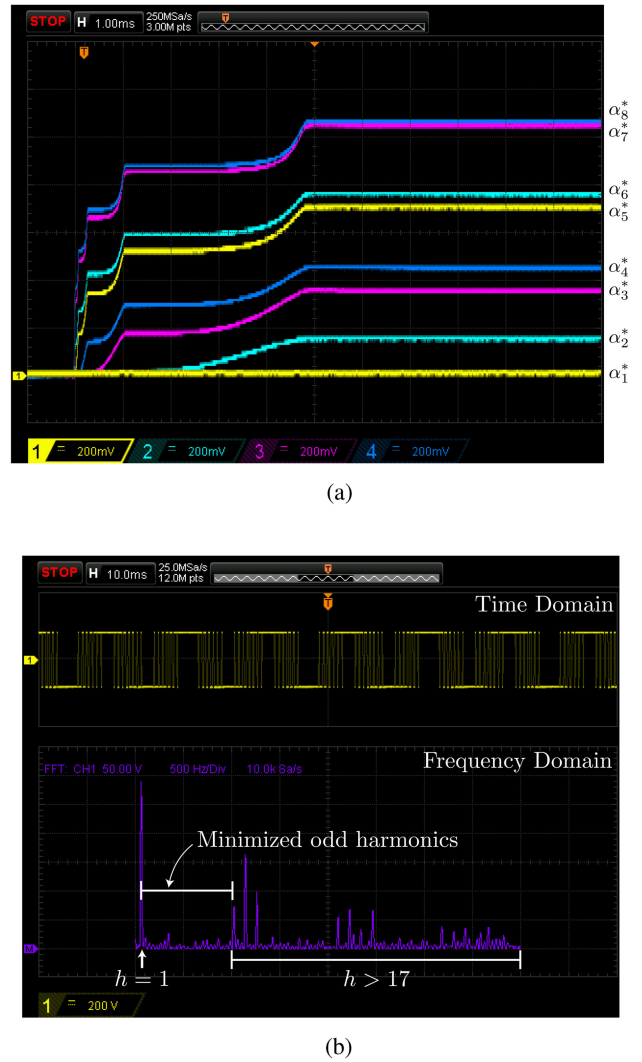


Fig. 11. Experimental measurements of the computing circuit minimizing the first seven odd harmonics ( $h = 3, 5, 7, 9, 11, 13, 15$ ). (a) Measurements of the switching angle voltage variables  $\alpha_\ell$  converge to the optimal value  $\alpha_\ell^*$  in 5.0 ms. (b) Time and frequency domain analysis of the two-level waveform confirms the minimization of the first seven odd harmonics.

steady-state values of  $\alpha_\ell, \ell = 1, \dots, 8$  closely match the simulation seen in Fig. 10(a). The resulting single-phase inverter waveform is shown in Fig. 11(b) in the time and frequency domains. As shown, the harmonics below  $h = 17$  are indeed minimized, while odd harmonics remain in the region  $h > 17$ .

2) *Minimization of First Seven Odd Nontriplen Harmonics:* In this verification test, the digital system is reprogrammed to minimize the first seven odd nontriplen harmonics ( $h = 5, 7, 11, 13, 17, 19, 23$ ). Note that there are no modifications to the analog system of the computing circuit. A SPICE-based simulation of this scenario is shown in Fig. 12. The circuit converges to a KKT point in steady state [Fig. 12(a)], while the frequency-domain analysis [Fig. 12(c)] again confirms that the specified harmonics are indeed minimized. The measurements from the hardware implementation of this scenario are shown in Fig. 13. In this case, we observe that the switching angle voltage variables converge to steady state in 3.7 ms [Fig. 13(a)]. The time- and frequency-domain analysis of the resulting inverter

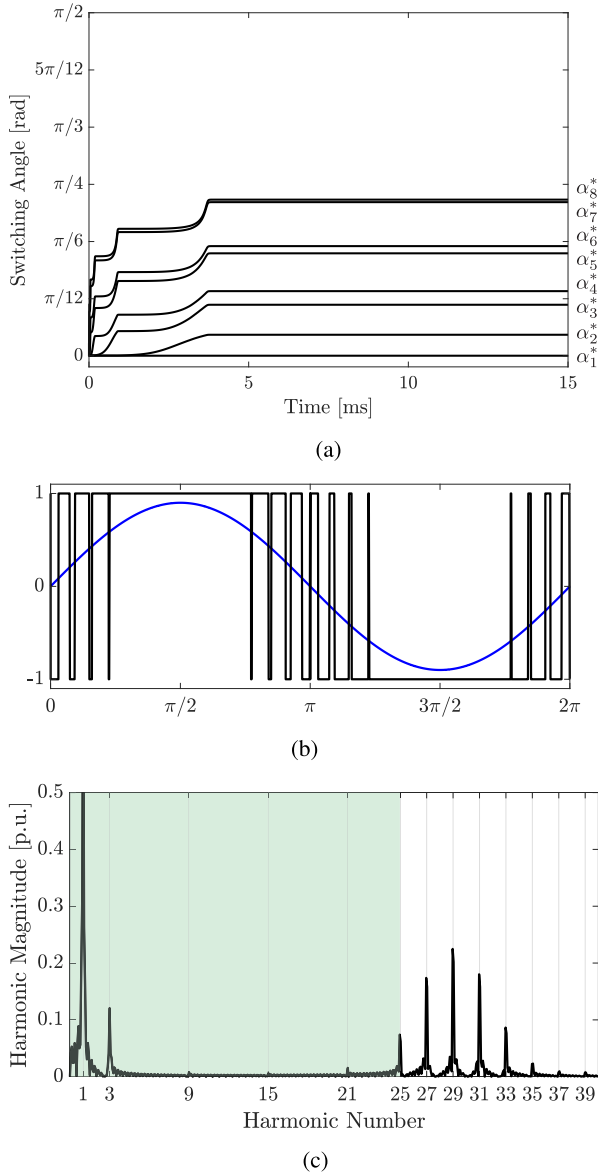


Fig. 12. Simulation of the computing circuit minimizing the first seven odd nontriplen harmonics ( $h = 5, 7, 11, 13, 17, 19, 23$ ). (a) Switching angle voltage variables  $\alpha_\ell$  converge to the optimal value  $\alpha_\ell^*$  in approximately 3.8 ms. (b) Optimal quarter-wave symmetric two-level waveform obtained by using the computed switching angles  $\alpha_\ell^*$ . (c) Frequency domain analysis of the two-level waveform confirms the minimization of the first seven odd nontriplen harmonics.

waveform in Fig. 13(b) confirms that the desired harmonics are minimized.

3) *Minimization of First Seven Odd Nontriplen Harmonics with Time-varying Modulation Index Command*: In the third verification test, the digital system is programmed to minimize the first seven odd nontriplen harmonics while the commanded modulation index,  $m$ , is continually varied. Fig. 14 illustrates the SPICE-based simulation for this scenario. As shown in Fig. 14(a),  $m$  is varied from 0 to 1 over 1 s from  $t = 0.2$  to  $t = 1.2$  s. Over this time period, the switching angle voltage variables [Fig. 14(b)] continuously evolve as the KKT points  $\alpha_\ell^*$  change as a function of  $m$ . Fig. 14(c) shows a waterfall plot that analyzes the time-varying frequency content of the resulting two-level inverter waveform. As shown, the first seven odd nontriplen harmonics are indeed continually minimized over

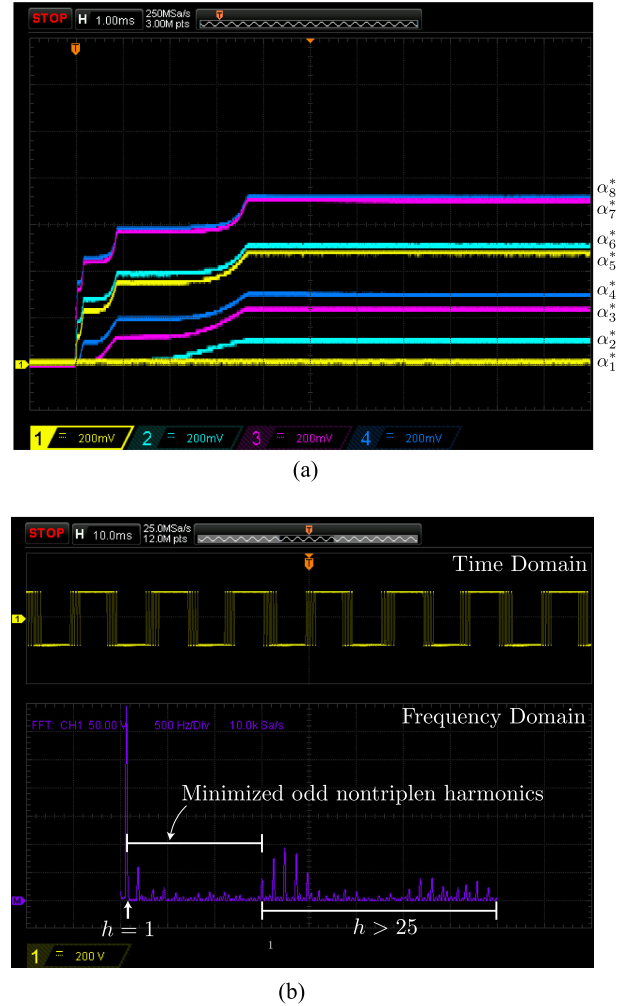


Fig. 13. Experimental measurements of the computing circuit minimizing the first seven odd nontriplen harmonics ( $h = 5, 7, 11, 13, 17, 19, 23$ ). (a) Measurements of the switching angle voltage variables  $\alpha_\ell$  converge to the optimal value  $\alpha_\ell^*$  in 3.7 ms. (b) Time and frequency domain analysis of the two-level waveform confirms the minimization of the first seven odd nontriplen harmonics.

the entire simulation period, while the fundamental frequency ( $h = 1$ ) increases in magnitude due to the control of the modulation index. This test validates the dynamic tracking capability of the proposed approach. As the commanded modulation index changes, the corresponding optimal switching angles will also change. Thus, the conventional methods that rely on LUTs or ANNs are unable to address these scenarios unless the response is preprogrammed into the system. On the contrary, the proposed computing circuit accepts the commanded modulation index as an input, and the switching angle voltage variables automatically converge to the new optimal solution.

## V. CONCLUSION

This article presented a hybrid analog/digital computing circuit capable of solving the selective harmonic minimization problem in a fast and power-efficient manner. The experimentally verified convergence speed ( $< 5.0$  ms) and power consumption (750 mW) of the computing circuit are substantially lower than previously published works where data are available.

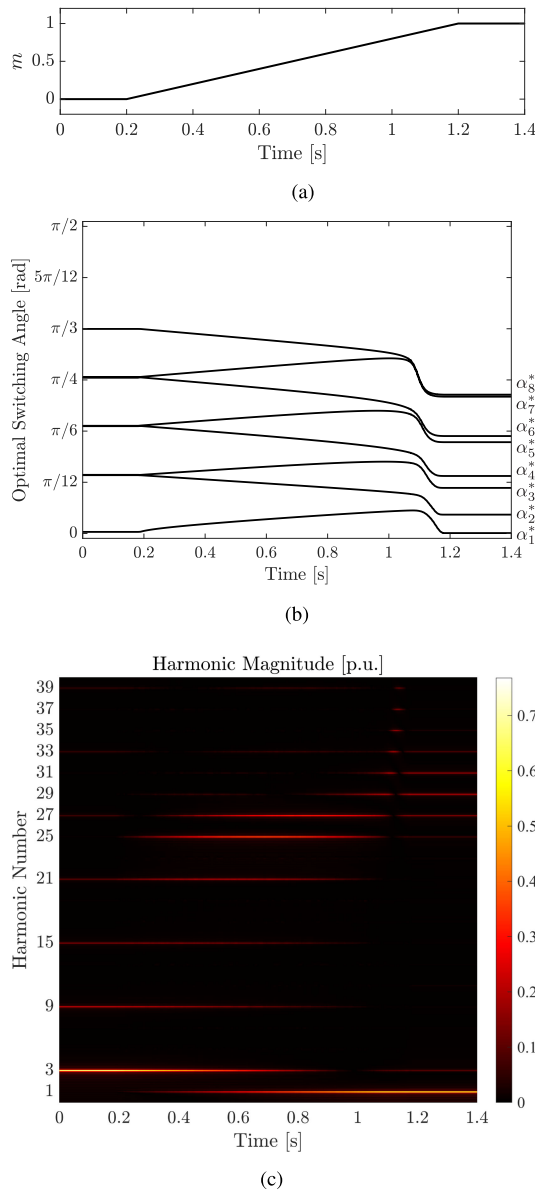


Fig. 14. Simulation of the computing circuit minimizing the first seven odd nontriplen harmonics ( $h = 5, 7, 11, 13, 17, 19, 23$ ) while dynamically controlling the modulation index,  $m$ . (a) Commanded modulation index,  $m$ , is varied from 0 to 1 from 0.2 to 1.2 s. (b) Switching angle voltage variables  $\alpha_l^*$  continuously evolve in response to the changing modulation index, which changes the corresponding optimal solution. (c) Waterfall plot of the resulting two-level waveform shows that the first seven odd nontriplen harmonics are continually minimized, while the fundamental frequency ( $h = 1$ ) increases in magnitude due to the control of  $m$ . The colors on the plot indicate the harmonic magnitude at the indicated harmonic number; the black color indicates that there is essentially no harmonic content at the particular frequency and time instance.

Moreover, the proposed circuit is capable of dynamically updating the optimization in realtime based on inputs and feedback—illustrated specifically in this article by dynamic control of the modulation index—which, to the best of the authors’ knowledge, is unique in the selective harmonic minimization literature.

There are a number of directions for future study. First, grid codes or uneven weighting function across the harmonics to be minimized could be incorporated by modifying the objective function. Second, while the experimental results shown here were targeted for a lower power single-phase inverter application, the proposed circuit could be generalized for

other converter configurations that have been explored in the context of selective harmonic minimization techniques, such as three-phase, multilevel, or unbalanced converters. Third, further study is required to precisely benchmark the performance of the proposed technique with existing methods for selective harmonic minimization, namely numerical-based optimization methods, with respect to speed and power consumption. This would potentially entail a register-transfer level simulation of metaheuristic-based optimization techniques to provide a fair hardware comparison and accurate power estimate. Finally, alternative all-digital, all-analog, or other hybrid analog/digital configurations of the proposed computing circuit can be considered to determine the resulting trade-offs in speed, energy consumption, and cost for various applications.

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**Jason Poon** (Member, IEEE) received the B.S. degree from the Olin College of Engineering, Needham, MA, USA, in 2012, and the M.S. and Ph.D. degrees from the University of California, Berkeley, CA, USA, in 2015 and 2019, all in electrical engineering.

He is currently a Visiting Scholar with the Department of Electrical Engineering, Stanford University, Stanford, CA, USA, and also an Affiliate Researcher with Lawrence Berkeley National Laboratory, Berkeley, CA, USA. His research interests include power electronics, renewable energy systems, and emergent

computing technologies.

Dr. Poon is the recipient of the 2019 EERE Postdoctoral Research Award and the Best Paper Award at the 2016 IEEE Workshop on Control and Modeling for Power Electronics for his work on distributed fault-tolerant power electronics.



**Mohit Sinha** (Member, IEEE) received the B.Tech. degree from the Indian Institute of Technology, Delhi, India, in 2011, and the Ph.D. degree from the University of Minnesota, Minneapolis, MN, USA, in 2018, both in electrical engineering.

He is currently a Senior Engineer with CTO Group, Enphase Energy, Petaluma, CA, USA. His research interests include control and modeling of power electronics, nonlinear system analysis, and networked dynamical systems.



**Sairaj V. Dhople** (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, USA, in 2007, 2009, and 2012, respectively.

He is currently an Associate Professor with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN, USA. His research interests include modeling, analysis, and control of power electronics and power systems with a focus on renewable integration.

Dr. Dhople is the recipient of the National Science Foundation CAREER Award in 2015, the Outstanding Young Engineer Award from the IEEE Power and Energy Society in 2019, and the IEEE Power and Energy Society Prize Paper Award in 2021.



**Juan Rivas-Davila** (Senior Member, IEEE) was born in Mexico City, Mexico. He received the B.A.Sc. degree from the Monterrey Institute of Technology, Monterrey, Mexico, in 1998, and the S.M. and Sc.D. degrees from the Laboratory of Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge, MA, USA, in 2003 and 2006, respectively.

From 2007 to 2011, he was a Power Electronics Engineer with High-Frequency Power Electronics Group, General Electric Global Research Center, Niskayuna, NY, USA. From 2011 to 2013, he was an Assistant Professor with the University of Michigan, Ann Arbor, MI, USA. Since 2014, he has been with Stanford University, Stanford, CA, USA, where he is currently an Associate Professor with Electrical Engineering Department, and is also with Stanford University Power Electronics Research Laboratory (SUPER-Lab), Stanford, CA, USA. His research interests include power electronics, RF power amplifiers, resonant converters, soft-switching topologies, and the design of air-core passive components for VHF power conversion.