Negative Gate Bias Induced Dynamic ON-Resistance Degradation in Schottky-Type *p*-Gan Gate HEMTs

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***Abstract*—In this article, the impacts of the OFF-state gate bias ($V_{GS,OFF}$) on dynamic ON-resistance (R_{ON}) are systematically investigated in commercial Schottky-type *p*-GaN Gate high-electron-mobility transistors. Double-pulse tester and pulsed *I–V* system are adopted to evaluate the dynamic R_{ON} with various OFF-state gate and drain bias ($V_{DS,OFF}$) under hard- and soft-switching conditions. More negative $V_{GS,OFF}$ can aggravate the dynamic R_{ON} degradation under both soft- and hard-switching, especially when switching with a high $V_{DS,OFF}$. The impacts of $V_{GS,OFF}$ on switching transients and OFF-state stress are investigated separately to reveal the underlying mechanisms, which are found to be associated with the generation and movements of holes. The OFF-state gate bias of the voltage-driving scheme needs to be carefully considered according to the identified mechanisms in terms of dynamic ON-resistance degradation.**

***Index Terms*—Dynamic ON-resistance, impact ionization, OFF-state gate bias, Schottky-type p-GaN gate high-electron-mobility transistor (HEMT).**

I. Introduction

GaN-BASED high-electron-mobility transistors (HEMTs) are superior candidates for high-efficiency power converter applications, owing to low ON-resistance (R_{ON}), fast switching speed and high-temperature operation capabilities [1]–[3]. Enhancement-mode (E-mode) devices are preferred for fail-safe operation of the power electronic systems. Presently, *p*-GaN gate HEMT is leading the commercialization of the single-chip E-mode GaN power devices, which adopts a *p*-type GaN layer on the AlGaN barrier to deplete two-dimensional electron gas (2-DEG) underneath the gate region, ensuring normally-OFF operation.

The contact between the gate metal and *p*-GaN layer is either an Ohmic- [4] or a Schottky-type contact [5] in the commercial devices. The Ohmic-type *p*-GaN gate HEMT [i.e., gate injection transistor (GIT)] has demonstrated attractive threshold voltage (V_{TH}) stability [6] and dynamic switching performance [7], but it requires a continuous gate current (i.e., current driving) to maintain ON-state, which enlarges the power consumption of gate driving and creates difficulties in GaN-based on-wafer integration. Another *p*-GaN gate HEMT technology, i.e., adopting a Schottky-type *p*-GaN gate, can effectively suppress the gate leakage current and thus enables a voltage-driving scheme. All-GaN integration of gate driver circuits with the Schottky-type *p*-GaN gate HEMTs has been demonstrated, which shows impressive high efficiency and high operation frequency [8].

To release the full potential of the Schottky-type *p*-GaN gate HEMTs, optimum OFF-state gate bias ($V_{GS,OFF}$) of the voltage-driving scheme needs elaborated consideration. When operated under a high switching speed, gate rings caused by parasitic inductance or miller capacitor could easily exceed the threshold voltage that is not sufficiently high (typically $<$ 2 V in Schottky-type *p*-GaN gate HEMTs [9]). False turn-ON could occur [10], [11]. Therefore, a negative OFF-state gate bias ($V_{GS,OFF}$ of -1 to -4 V), especially for high-power (e.g., 1 –100 kW) applications, is recommended to ensure the reliability of power system [12], [13]. Negative $V_{GS,OFF}$ can also bring other benefits. When switching with a high load current, negative $V_{GS,OFF}$ can obviously expedite the switching-OFF transition and reduce the turn-OFF switching loss [14]. In addition, sufficiently negative $V_{GS,OFF}$ was recommended to suppress the dynamic OFF-state leakage current degradation, which could be caused by photo-conductivity effect [15], electroluminescence emitted photon pumping of trapped electrons [16], or hole-assisted electron de-trapping [17]–[19] in the gate region.

However, adopting negative $V_{GS,OFF}$ could result in some drawbacks. One critical drawback of the negative $V_{GS,OFF}$ is larger reverse-conduction loss. In practical applications with an inductive load, the power devices during deadtime will be subjected to a reverse-conduction state to provide a freewheeling current path. The reverse conduction of GaN HEMTs is enabled by turning ON the drain-side channel with gate-to-drain bias (V_{GD}) higher than V_{TH}. Negative $V_{GS,OFF}$ will increase the reverse turn-ON voltage of GaN HEMTs, causing higher reverse-conduction loss [20]. Thus, $V_{GS,OFF}$ of 0 V is recommended by the manufacturers in low-voltage or low-power applications, or when the deadtime power loss is critical [21]. In addition, holes could be generated by impact ionization in the high electric-field region during high drain-bias stress [22]. Negative gate bias could accelerate the device degradation by attracting the flow

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of holes to the gate side [23]. Thus, negative $V_{\mathrm{GS,OFF}}$ should be limited to a certain operation range for better device reliability.

The impacts of $V_{\mathrm{GS,OFF}}$ have been considered from different angles, including switching transition [14], OFF-state leakage current [17]–[19], hole transport [22], [23], and hole-assisted detrapping [18]. These factors are also critical to dynamic ON-resistance (R_{ON}) performance. Due to the electron trapping in the buffer layer and at the barrier surface induced by high drain bias stress [24], the 2-DEG channel is partially depleted after switching back to ON-state, resulting in increased R_{ON} and enlarged conduction loss. In previous on-board dynamic R_{ON} characterizations, negative $V_{\mathrm{GS,OFF}}$ of –1∼ –4 V is often applied to ensure the stability of the circuit system [25]–[27]. However, the impacts of $V_{\mathrm{GS,OFF}}$ on dynamic R_{ON} degradation have not been investigated.

In this article, the influence of $V_{\mathrm{GS,OFF}}$ on dynamic ON-resistance (R_{ON}) is investigated under both hard- and soft-switching conditions in commercial E-mode *p*-GaN gate HEMTs. When switching with a large OFF-state drain bias (i.e., $V_{\mathrm{DS}} > 200$ V), more negative $V_{\mathrm{GS,OFF}}$ could greatly aggravate current collapse. The major reason is that the generation and movement of holes during the OFF-state stress are affected by negative $V_{\mathrm{GS,OFF}}$. Understanding the impacts of $V_{\mathrm{GS,OFF}}$ on the dynamic performance is of great significance for gate driver design.

The rest of this article is organized as follows. In Section II, test setups and configurations of dynamic R_{ON} measurements are introduced. In Section III, detailed test results are presented to show the impacts of $V_{\mathrm{GS,OFF}}$ on dynamic R_{ON} degradation. The underlying mechanisms are analyzed in Section IV. Finally, Section V concludes this article.

II. Dynamic R_{ON} Characterizations Method

The devices tested in this article are commercial Schottky-type *p*-GaN gate HEMTs with a voltage/current rating of 650 V/30 A [28]. Hard-switching tests were conducted on the commercial *p*-GaN gate HEMTs with a double-pulse tester to systematically characterize the impacts of $V_{\mathrm{GS,OFF}}$ on dynamic performance. In addition, soft-switching tests were also conducted using a high-speed pulsed *I*–*V* (PIV) system to verify the impacts of $V_{\mathrm{GS,OFF}}$ during OFF-state stress excluding the impacts of switching transients.

A. ON-State Gate Drive Bias Consideration

Transfer and output characteristics of the *p*-GaN gate HEMT are shown in Fig. 1, measured by the Agilent B1505A power device analyzer. The device features a static R_{ON} around 55 mΩ extracted from the linear region of output characters with V_{GS} of 6 V, and a V_{TH} of 1.24 V defined at I_{DS} of 1 mA. According to the static characteristics, a gate drive voltage of 4 V is enough to fully turn ON the GaN transistor. However, under high-power switching operations, a positive V_{TH} shift could occur due to hole deficiency [25] and electron trapping in the barrier/buffer layer [29]. The dynamic R_{ON} is significantly larger (compared with the static R_{ON}) under a low V_{GS} of 4 V as the result of the positive V_{TH} shifts. Considering the impacts of positive V_{TH} shift on

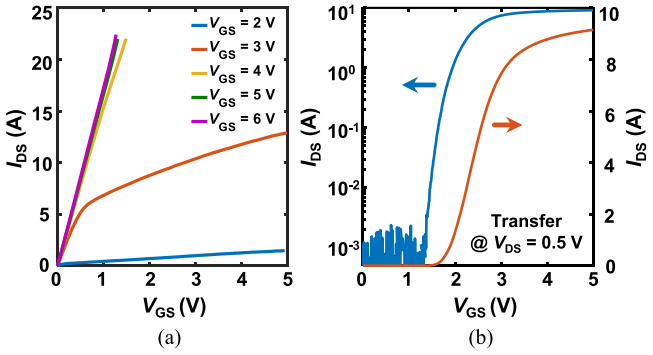

Fig. 1. (a) Output (I_{DS}-V_{DS}) and (b) transfer (I_{DS}-V_{GS}) characteristics of the commercial *p*-GaN gate HEMTs.

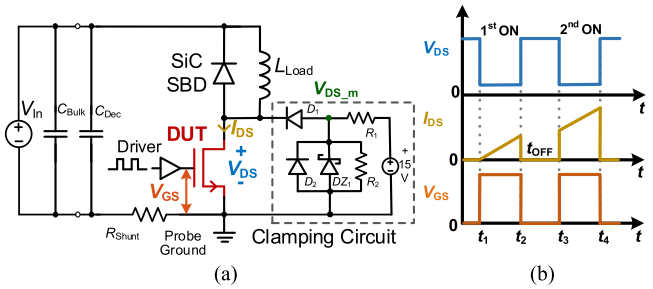

Fig. 2. (a) Schematic circuits of the double-pulse tester with a clamping circuit. (b) Waveforms of gate control signal (V_{GS}) and the corresponding drain voltage (V_{DS}) and current (I_{DS}).

R_{ON} and reliable gate operation [25], optimized ON-state gate bias of 6.1 V is adopted, which is clamped by a Zener diode.

B. Double-Pulse Test Setups

A double-pulse tester is built to evaluate the device switching performance under hard switching conditions. The test circuit schematic is shown in Fig. 2(a). A bulk capacitor bank C_{Bulk} with a large capacitance of 640 μF is adopted for a quick transfer of electric energy to the double pulse tester (DPT), as well as to maintain a smooth input power voltage (V_{In}) with a variation smaller than 0.1 V. The SiC Schottky barrier diode (SBD) serves as the freewheeling diode of the inductive load to facilitate fast commutation processes. A clamping circuit [27] is applied to block the high OFF-state V_{DS} and provide a good measuring resolution of the low ON-state drain voltage. The drain voltage is calculated by subtracting the turn-ON voltage of clamping diode D_1 (V_{F_D1}) from the measured drain-to-source voltage $V_{\mathrm{DS}(m)}$. The measuring delay time is around 100 ns. The gate control signals (V_{GS}) and the corresponding drain voltage (V_{DS}) and current (I_{DS}) waveforms are illustrated in Fig. 2(b).

As is shown in Fig. 3(a), the test setup contains a test board, a waveform generator, an oscilloscope, an auxiliary power supply, a dc power supply and a bulk capacitor bank. The test board is designed on a four-layers print circuit board (PCB) to reduce the parasitic parameters. A detailed overview of the PCB test board is depicted in Fig. 3(b). A double-side layout is designed to reduce the coupling between the high-voltage power loop (on the top side) and the low-power gate control and clamping circuits

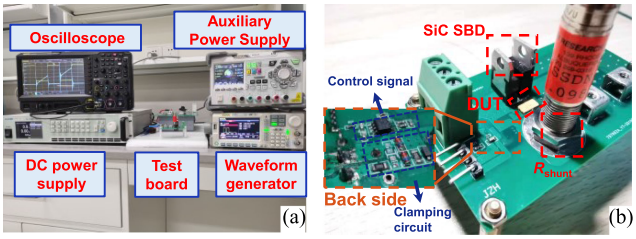

Fig. 3. (a) DPT setup for dynamic R_{ON} evaluation. (b) Photograph of the PCB test board used in the DPT.

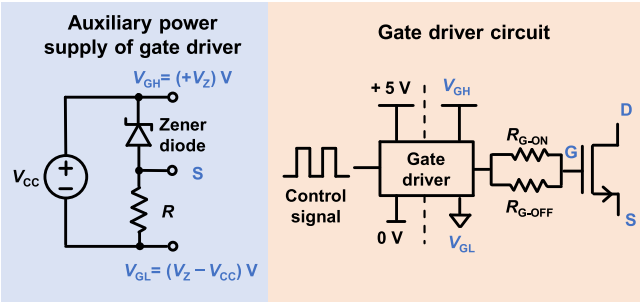

Fig. 4. Schematic gate driver circuits of the DPT.

(on the backside), which benefits a tight layout to minimize the stray inductance. The drain current is sensed using a 0.1-Ω coaxial shunt (SSDN-10) from T&M Research and then monitored by the oscilloscope. In particular, 50-Ω impedance matching is indispensable between the signal line of the coaxial shunt and the oscilloscope. The gate and drain voltages are measured using single-ended passive probes of the oscilloscope. A scope probe with a short ground clip is used for accurate measurement results.

The double-pulse gate control signals of the device under test (DUT) are provided by the waveform generator. Aimed at probing the impacts of $V_{GS,OFF}$ on dynamic R_{ON}, a gate drive circuit is designed, as shown in Fig. 4. The auxiliary power supply of the gate driver (V_{cc}) is divided into two parts by a 1-kΩ resistance and a Zener diode, which is employed to provide the turn-OFF gate voltages (V_{GL}) and turn-ON gate voltage (V_{GH}), respectively. V_{GH} is clamped to the breakdown voltage (V_Z) of the Zener diode, which is 6.1 V, to ensure adequate gate overdrive, as discussed in Section II-A; while various V_{GL} that equals $V_Z - V_{cc}$ is achieved by adjusting the auxiliary power supply. In more detail, an isolated half-bridge driver IC Si8271 is applied to provide a wide supply range and a fast propagation time of 60 ns [21]. External turn-ON gate resistor $R_{G\text{-}ON}$ of 27 Ω and turn-OFF gate resistor $R_{G\text{-}OFF}$ of 2 Ω are used to control the switching speed of the GaN power transistors.

C. DPT and Soft-Switching Test Configurations

DPT is an effective method to evaluate the dynamic performance of the device under operating conditions close to practical applications. Before double pulse tests, the prestressing time is controlled to be five minutes to eliminate the impacts induced by different prestressing time. Then, the DUT is turned ON and maintained at ON-state for 1 μs. The inductive load is charged up, and the load current (I_{load}) through the DUT keeps increasing.

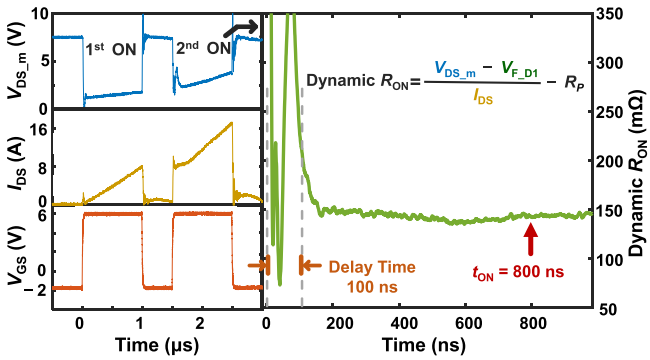

Fig. 5. Experimental waveforms for dynamic ON-resistance measurement and extraction. The illustrated waveforms are measured under hard-switching conditions with harsh hard-switching conditions with $R_{G\text{-}ON}$ of 27 Ω, $V_{DS,OFF}$ of 400 V and $V_{GS,OFF}$ of –2 V. R_P is the parasitic resistance between the S/D terminals on the DPT board, which is ~28 mΩ.

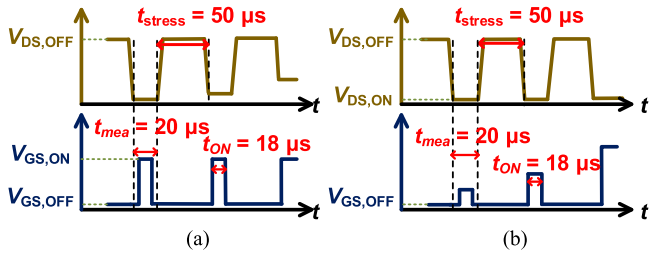

Fig. 6. Illustrated waveforms of gate and drain voltage during the pulsed (a) output and (b) transfer characteristics test using PIV system.

By adjusting the load inductance, the load current at the end of the first ON-state pulse can be maintained the same with different input power voltage. After that, the DUT is turned OFF and kept at the OFF-state for 0.5 μs with the SiC SBD serving as a freewheeling diode. Subsequently, the DUT turns ON again and dynamic R_{ON} is measured during this second ON-state pulse with a measuring delay time of 100 ns (see Fig. 5). To avoid switching noise or unexpected oscillation, dynamic R_{ON} after switching on for a sufficient delay of 800 ns is extracted from the waveforms and normalized to the static R_{ON}. To evaluate the impacts of $V_{GS,OFF}$ on dynamic R_{ON}, double pulse tests were conducted with $V_{GS,OFF}$ varying from 0 to –4 V.

Compared with the hard switching test, the soft switching test can exclude the influence of switching transients, so that the impacts of OFF-state stress on dynamic R_{ON} can be studied separately. The soft switching tests are conducted using an AMCAD 1000-V/30-A pulse IV (PIV) system. The waveforms of the gate and drain voltage during the pulsed output (I_D–V_{DS}) tests are illustrated in Fig. 6(a). The pulse period is 70 μs, and the pulse width of the gate and the drain bias is 18 and 50 μs, respectively. A delay time of 1 μs is set to ensure the soft switching operations. ON-state gate bias of 6.1 V, same as that used in DPT, is applied in pulsed output tests. $V_{DS,ON}$ sweeps up from 0 to 1.5 V, and dynamic R_{ON} is extracted from the linear region. In particular, dynamic R_{ON} degradation could partially recover during the long measurement delay, so a wide range of $V_{GS,OFF}$ from 0 to –8 V is used in the soft switching tests to

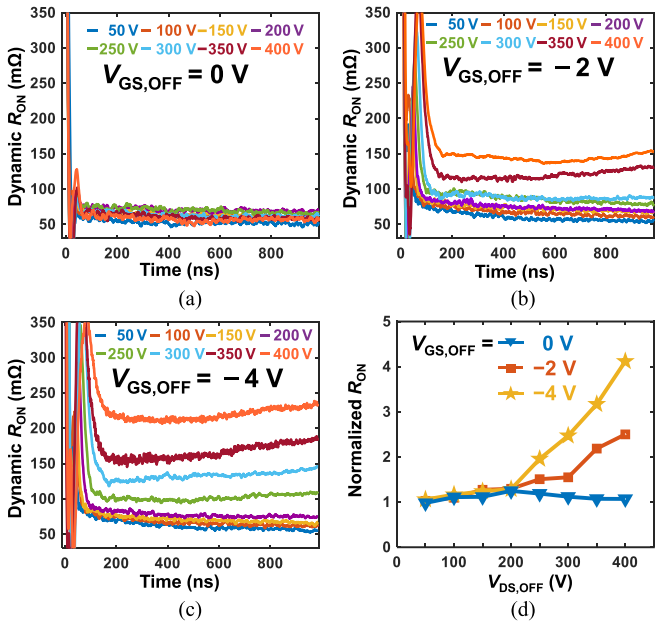

Fig. 7. R_{ON} of *p*-GaN gate Dynamic HEMTs with different drain bias stresses from 50 to 400 V and $V_{GS,OFF}$ of (a) 0 V, (b) –2 V, and (c) –4 V, respectively. The load current I_{load} is 8 A, and ON-state V_{GS} is 6 V. (d) Normalized dynamic R_{ON} after turning ON for 800 ns.

see clear dependence of dynamic R_{ON} on $V_{GS,OFF}$. Within the 10-μs measurement window, five data points are sampled and averaged to obtain the accurate results.

The high current resolution of the PIV system also enables pulsed transfer (I_D–V_{GS}) tests to extract V_{TH}, which provides more insight into the underlying R_{ON} degradation mechanism. The pulse width, period, delay time and measurement widow of the pulsed transfer (I_D–V_{DS}) tests are the same with that of the pulsed output tests [see Fig. 6(b)]. ON-state drain bias of 1 V is applied in the pulsed transfer tests with $V_{GS,ON}$ sweeping up from 0 to 4 V. Transient ON-state drain current I_D and V_{DS}/V_{GS} are sampled simultaneously after each OFF-to-ON switching event.

III. Experimental Results

Previous publications have paid much attention to the impacts of OFF-state drain bias [30], ON-state gate drive bias [25], temperature [31], substrate termination [24], etc., on dynamic R_{ON}, but few of them pay attention to the OFF-state gate bias. This section aims to show the impacts of $V_{GS,OFF}$ on the dynamic R_{ON} under different operation conditions. The OFF-state stress and switching transients during the double-pulse tests could be both affected by $V_{GS,OFF}$, of which the impacts on dynamic R_{ON} behaviors are characterized separately.

A. Impacts of $V_{GS,OFF}$ on Dynamic R_{ON}

Fig. 7 shows the dynamic ON-resistance measured with the same drain current of 8 A and different OFF-state gate and drain bias. With $V_{DS,OFF}$ exceeding a certain value (i.e., 200 V), more negative $V_{GS,OFF}$ aggravates the dynamic R_{ON} degradation, which is more obvious with higher $V_{DS,OFF}$. For example, with a drain bias of 400 V, the dynamic R_{ON} with $V_{GS,OFF}$ of −4 V

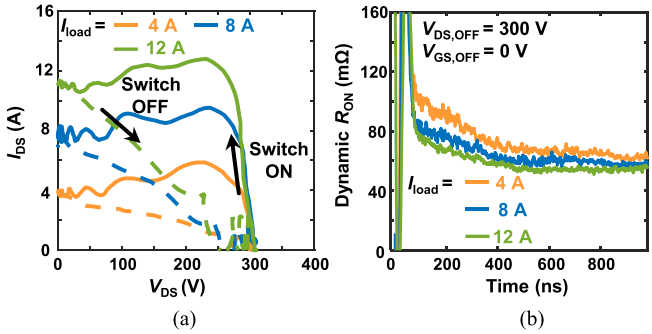

Fig. 8. (a) Switching transient load lines. (b) Dynamic R_{ON} with $V_{DS,OFF}$ = 300 V, $V_{GS,OFF}$ = 0 V and I_{load} = 4, 8, and 12 A, respectively.

is aggravated to 4 times larger than that with $V_{GS,OFF}$ of 0 V [see Fig. 7(d)], which is remarkable compared to the impacts of other factors, such as load current [27], OFF-state stress time [32], temperature [31], duty cycle and switching mode [33]. Taking a 300-kHz/3.3-kW totem-pole continuous conduction mode power factor correction application as an example, the conduction loss caused by dynamic R_{ON} is comparable to the switching loss, resulting in around 0.3% efficiency reduction. Therefore, the impacts of $V_{GS,OFF}$ on dynamic R_{ON} under switching operations are worth careful considerations in gate-driving scheme engineering.

In addition, the dependence of dynamic R_{ON} on drain stress bias changes with $V_{GS,OFF}$. With $V_{GS,OFF}$ of 0 V, the dynamic R_{ON} exhibits a nonmonotonic dependence on the OFF-state drain voltage ($V_{DS,OFF}$). Medium $V_{DS,OFF}$ (<150 V) results in monotonically increasing dynamic R_{ON}, but higher $V_{DS,OFF}$ (>200 V) enables alleviated dynamic R_{ON} degradation. Similar dynamic R_{ON} improvement under high $V_{DS,OFF}$ has also been reported in [32] and [34]. With negative OFF-state gate bias, the dynamic R_{ON} degradation turns to monotonically increase as $V_{DS,OFF}$ increases, consistent with other reported DPT results using the same setup with negative $V_{GS,OFF}$ [26], [27].

Five more devices and those with different voltage/current rating of 650 V/22.5 A [35] were also tested to check that the dependence of dynamic R_{ON} on $V_{GS,OFF}$ is a common behavior.

B. Impacts of Switching Transients on Dynamic R_{ON}

Switching transients, especially the turn-OFF transients, could be affected by $V_{GS,OFF}$. To verify the impacts of switching transients on dynamic R_{ON}, the load line is modified by adjusting the load current [see Fig. 8(a)], while maintaining the same OFF-state stress condition, i.e., the same OFF-state gate/drain bias and stress period. In addition to I_{load}, R_{G_OFF}, and R_{G_ON} can also affect the switching transients [27], thereby affecting the dynamic R_{ON}, but the impacts should be much weaker than that caused by varying I_{load}. As depicted in Fig. 8(a), switching load lines are greatly changed by adjusting the inductive load, causing harsher or softer switching transients than that with I_{load} of 8 A.

Dynamic R_{ON} measured with various load currents, $V_{DS,OFF}$ of 300 V and $V_{GS,OFF}$ of 0 V is shown in Fig. 8(b). Switching operation with higher I_{load} results in slightly reduced dynamic R_{ON} degradation. Similar trends are also observed with negative

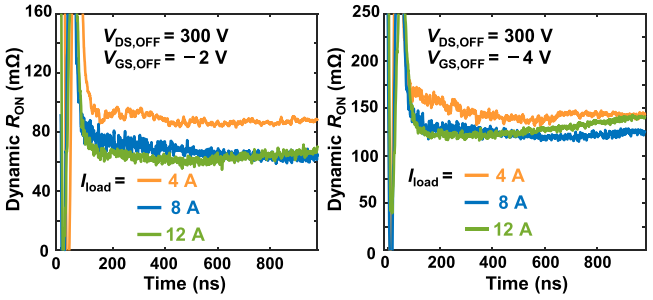

Fig. 9. Dynamic R_{ON} measured with different I_{load}, $V_{DS,OFF} = 300$ V. (a) $V_{GS,OFF} = -2$ V. (b) $V_{GS,OFF} = -4$ V.

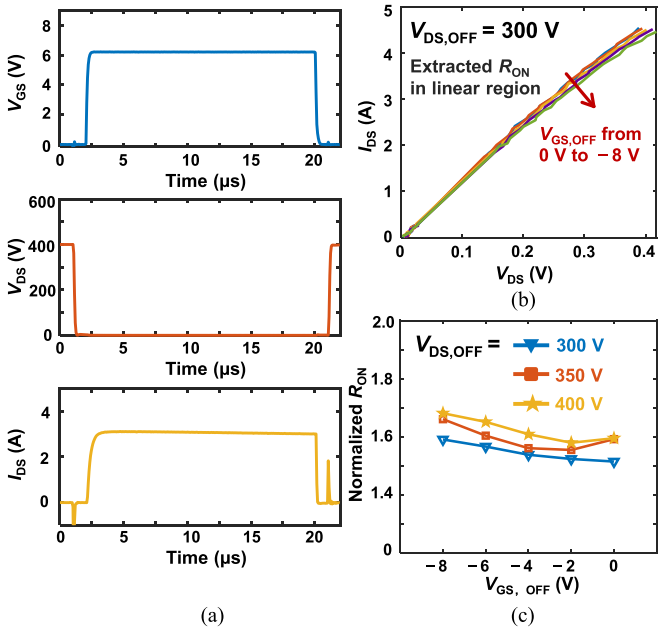

Fig. 10. (a) Waveforms of V_{GS}, V_{DS}, and I_{DS} during the soft-switching test with $V_{DS,OFF}$ of 400 V and $V_{GS,OFF}$ of 0 V. (b) Pulsed output under soft switching with $V_{DS,OFF} = 300$ V and various $V_{GS,OFF}$. (c) Dynamic R_{ON} measured with various $V_{GS,OFF}$ and $V_{DS,OFF}$.

OFF-state gate bias of −2 V [see Fig. 9(a)] and −4 V [see Fig. 9(b)]. In addition, in all the tests with various I_{load}, dynamic R_{ON} increases with more negative $V_{GS,OFF}$.

C. Impacts of OFF-State Stress on Dynamic R_{ON}

In contrast to its strong dependence on $V_{GS,OFF}$, the dynamic R_{ON} only shows slight distinction when load lines are largely changed [see Fig. 8]. The major impacts of $V_{GS,OFF}$ in hard-switching tests should arise mainly from OFF-state stress. To individually evaluate the impacts of OFF-state stress on dynamic R_{ON}, soft-switching tests were conducted excluding the impacts of switching transients. The tests were conducted using a PIV system with various $V_{GS,OFF}$ from 0 to −8 V and $V_{DS,OFF}$ of 300, 350, and 400 V, respectively (see Fig. 10). Fig. 10(a) shows the waveforms of I_{DS}, V_{DS}, and V_{GS} in the soft-switching test with $V_{DS,OFF}$ of 400 V and $V_{GS,OFF}$ of 0 V. With more negative $V_{GS,OFF}$ and the same $V_{DS,OFF}$, the increase in dynamic R_{ON}

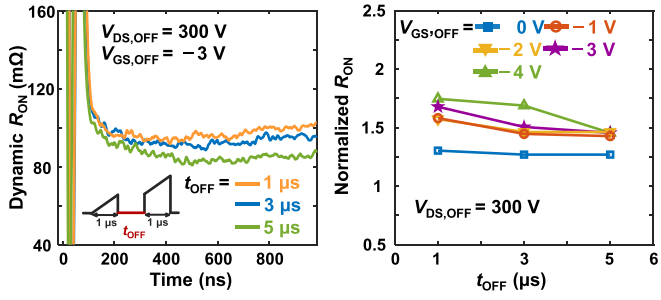

Fig. 11. Dynamic R_{ON} with different off-state stress time (t_{OFF}). (a) $V_{GS,OFF} = -2$ V. (b) Different $V_{GS,OFF}$.

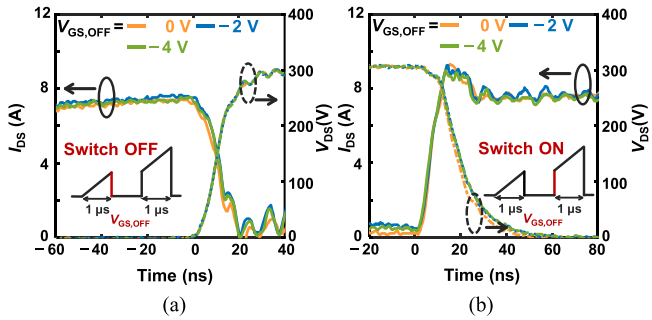

Fig. 12. (a) Turn-OFF and (b) turn-ON transient waveforms of V_{DS} and I_{DS} during the double pulse tests with different $V_{GS,OFF}$ and $V_{DS,OFF}$ of 300 V. The OFF-state stress time t_{OFF} is 0.5 μs.

was also observed with the impacts of switching transients excluded [see Fig. 10(c)], indicating that the OFF-state stress with different $V_{GS,OFF}$ has considerable impacts on the dynamic R_{ON} degradation.

The impacts of OFF-state stress time (t_{OFF}) on dynamic R_{ON} are also characterized, which was measured using DPT with various t_{OFF} (i.e., 1, 3, and 5 μs) and maintaining other operating conditions the same (i.e., $V_{GS,OFF}$, $V_{DS,OFF}$, t_{ON}) [see Fig. 11(a)]. The t_{OFF} corresponds to the switching frequency in the range of 100 kHz to 1 MHz, typically adopted in practical applications. With a longer OFF-state stress period, the dynamic R_{ON} degradation is alleviated [see Fig. 11(a)]. Similar trends are also observed under operations with different negative $V_{GS,OFF}$ [see Fig. 11(b)]. Dynamic R_{ON} shows a slightly stronger negative correlation with t_{OFF} as $V_{GS,OFF}$ becomes more negative. These trends further indicate the strong impacts of OFF-state stress on dynamic R_{ON} caused by different OFF-state gate bias.

IV. Mechanisms and Discussion

More negative OFF-state gate bias aggravates the dynamic R_{ON} degradation under different operation conditions, which could steam from the OFF-state stress and/or switching transients that could be both affected by $V_{GS,OFF}$. The underlying mechanisms are analyzed in this section to provide valuable information for device driving schemes design.

The impact of $V_{GS,OFF}$ on the OFF-state stress and switching transients should be analyzed separately to identify the dominant factor. Fig. 12 shows the switch-OFF and switch-ON transient

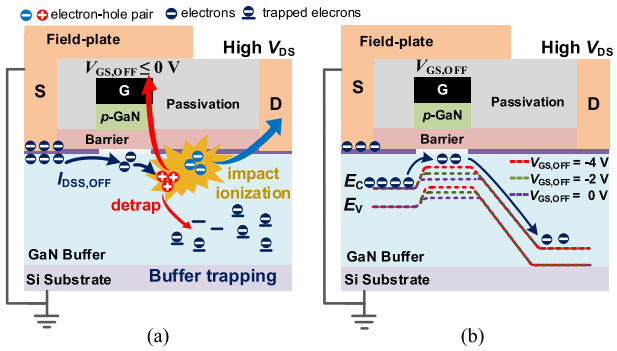

Fig. 13. (a) Schematic cross section to illustrate holes generation by impact ionization and transport of holes to the buffer and the gate side. (b) Schematic cross section and band diagrams under high drain voltage with different gate bias.

waveforms of V_{DS} and I_{DS} during the double-pulse tests with $V_{DS,OFF}$ of 300 V, I_{Load} of 8 A, and various $V_{GS,OFF}$. The switching transient waveforms almost entirely overlap and show insignificant differences with various $V_{GS,OFF}$, indicating that $V_{GS,OFF}$ has negligible influence on the load lines under the work conditions with moderate load current.

More evidence for excluding the influence of switching transients comes from the comparison between the dynamic R_{ON} variations caused by different $V_{GS,OFF}$ (see Fig. 7) and that caused by different load current (see Fig. 8). The dynamic R_{ON} shows much weaker dependence on load lines [see Fig. 8(b)] than on $V_{GS,OFF}$ [see Fig. 7(d)]. It indicates that the influence of various $V_{GS,OFF}$ on dynamic R_{ON} degradation should not be produced by affecting the load lines of switching transients. Moreover, in soft switching tests, which have excluded the impacts of switching transients, an increase of dynamic R_{ON} with more negative $V_{GS,OFF}$ was still observed [see Fig. 10(b)]. It is concluded that the $V_{GS,OFF}$ should mainly impact dynamic R_{ON} degradation during the OFF-state stress rather than via affecting the switching transients.

A closer look at the impacts of OFF-state stress with different gate and drain bias on dynamic R_{ON} could provide useful indications to reveal the role of $V_{GS,OFF}$ during OFF-state stress. As shown in Fig. 7(d), reduced dynamic R_{ON} degradation was observed with $V_{GS,OFF}$ of 0 V and $V_{DS,OFF}$ increasing from 200 to 400 V, indicating larger $V_{DS,OFF}$ contributes to the dynamic-R_{ON} alleviation process. However, more negative $V_{GS,OFF}$ aggravates the dynamic R_{ON} degradation, which becomes more serious with higher drain-bias stress. It suggests that the alleviation process of dynamic R_{ON} degradation could only occur with large $V_{DS,OFF}$, and be hindered by negative OFF-state gate bias.

At OFF-state with a high drain bias, trap states in the buffer layer could be filled by electrons injected from source and substrate, causing dynamic R_{ON} degradation. Meanwhile, impact ionization is also initiated by the injected electrons in the gate-to-drain access region, generating electron-hole pairs [see Fig. 13(a)] [36]. Considering source-connected field plates, impact ionization could occur mainly in the gate-drain edge and field-plate edges near the drain side, where the high electric field exists. The generated holes will be swept toward the lowest potential at substrate and gate side [37], while electrons will flow to the high-potential drain side. The holes flow to the gate side will be collected by the gate edge close to the drain side [38], or be blocked at the source end of the gate [39]. Few electrons could overcome the gate-to-source energy barrier and reach the source side access region. The holes flow to the buffer layer could assist detrapping of the electron traps, and thus reduce dynamic R_{ON} degradation [see Fig. 13(a)] [34]. With prolonged OFF-state stress time, more holes could be generated by impact ionization during OFF-state, and facilitate the suppression of current collapse, resulting in smaller dynamic R_{ON} as shown in Fig. 11(b). In addition to hole-assisted de-trapping, electron trapping occurs meanwhile during the OFF-state stress. The unchanged dynamic R_{ON} with $V_{GS,OFF}$ of 0 V after 1-μs stress indicates a dynamic equilibrium reached between the trapping and detrapping process.

The negative $V_{GS,OFF}$ has negligible impacts on the access-region electric field at the OFF-state [40]. However, negative $V_{GS,OFF}$ will raise the energy barrier under the gate [see Fig. 13(b)], and suppress the source-to-drain leakage current [18]. Thus, there will be fewer electrons causing impact ionization, and the subsequent hole-assisted current collapse alleviation process will be weakened. Meanwhile, negative $V_{GS,OFF}$ will also affect the movement of holes. As is depicted, holes mainly originate from impact ionization in the high electric field region, i.e., gate-drain edge and field-plate edge. The generated holes will be attracted to the gate side by negative $V_{GS,OFF}$ [23], then the holes flowing to the buffer layer are reduced. With more negative $V_{GS,OFF}$ at high drain bias, reduced holes generation and suppressed holes flow to the buffer result in fewer holes assisting the detrapping of buffer traps, so deteriorated dynamic R_{ON} degradation is observed as shown in Figs. 7 and 10. With temperature varying, the impacts of $V_{GS,OFF}$ on dynamic R_{ON} degradation are expected to be more complicated, since the electron trapping/de-trapping, impact ionization, carriers transport have different temperature dependencies.

Limited by the current resolution of the onboard test, hole leakage current cannot be directly tracked during the double pulse measurement. Nevertheless, the impacts of $V_{GS,OFF}$ on threshold voltage shifts (ΔV_{TH}) under the OFF-state stress add further weight to the suggested mechanism that hole flow can be attracted to the gate side by negative gate bias. The V_{TH} shifts are characterized by pulsed transfer test, and related test waveforms are illustrated in Fig. 6(b). The measurement result with a drain bias of 0 V shows a positive ΔV_{TH} when the negative gate bias is applied [see Fig. 14(a)]. However, with $V_{DS,OFF}$ of 100 V, negative $V_{GS,OFF}$ caused positive ΔV_{TH} to disappear [see Fig. 14(b)]. With higher $V_{DS,OFF}$ of 400 V, even negative ΔV_{TH} was observed with more negative $V_{GS,OFF}$ [see Fig. 14(c)]. To exclude the impacts caused by different drain-to-gate bias (V_{DG}) at high $V_{DS,OFF}$, pulsed transfer curves with different V_{DG} corresponding to $V_{GS,OFF}$ of 0, -2, -4, and -6 V were measured [see Fig. 14(d)]. Almost no V_{TH} difference was observed. Additionally, the $V_{DG,OFF}$ variations was proved to induce positive ΔV_{TH} like Fig. 14(a), as holes will emit from *p*-GaN and cannot be replenished timely when switched back to

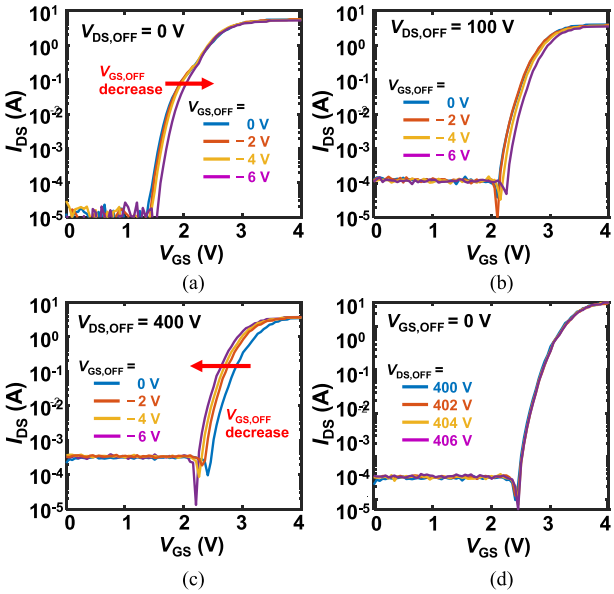

Fig. 14. Pulsed transfer measured using PIV system with various $V_{GS,OFF}$ and $V_{DS,OFF}$ of (a) 0 V, (b) 100 V, and (c) 400 V. (d) Pulsed transfer measured with different $V_{DG,OFF}$ and $V_{GS,OFF}$ of 0 V.

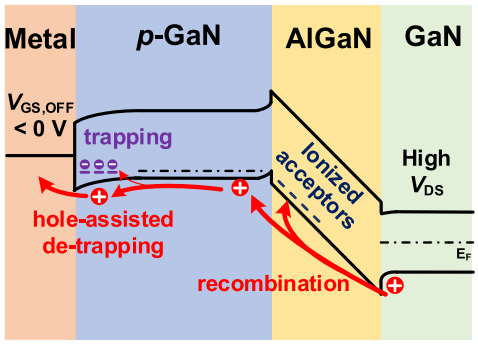

Fig. 15. Schematic band diagram along the p-GaN gate under a high V_{DS} and negative $V_{DS,OFF}$ to illustrate the role of holes in detrapping the trapped electrons and recombination with ionized acceptors.

ON-state [25]. So, the negative shifts of V_{TH} should be caused by $V_{GS,OFF}$ rather than different V_{DG}.

Due to large drain-bias stress, positive V_{TH} shifts could be caused by acceptor ionization in the AlGaN layer [29] and electron trapping in the p-GaN depletion region [41]. However, with a negative $V_{GS,OFF}$, the holes attracted to the gate side could be trapped in the AlGaN layer or assist the detrapping in the p-GaN layer (see Fig. 15), suppressing the positive ΔV_{TH}. With more negative $V_{GS,OFF}$, contributors causing positive ΔV_{TH} are restricted more by larger holes flow, so that negative V_{TH} shifts were observed compared with $V_{GS,OFF}$ of 0 V. The V_{TH} shifts characterization verifies the holes flow to the gate side with negative $V_{GS,OFF}$. After the device is turned ON, slightly increased R_{ON} was observed in the tests under harsh stress conditions, i.e., with high $V_{DS,OFF}$, large I_{load}, or negative $V_{GS,OFF}$ [see Figs. 7 and 9). One possible reason is the recovery of hole trapping in the AlGaN barrier near the gate edge or in the gate region.

The holes generated by impact ionization do not only play a key role in the $V_{GS,OFF}$-dependent dynamic R_{ON}, but also be applicable to explain the alleviated dynamic R_{ON} by larger load current (see Figs. 8 and 9). Larger load current results in more hot electrons during the switching transients, and triggers more intense impact ionization. Thus, more holes are generated to assist the electron detrapping, and alleviated dynamic R_{ON} degradation was observed. In soft-switching tests, load current is conducted with a low V_{DS} at ON-state. Due to the absence of high electric field, the hot electrons generation or impact ionization initiated by I_{load} is quite weak to affect R_{ON}. To draw a more general conclusion for different operating conditions [31], [42], the impacts of OFF-state stress and switching transients should be considered from two angles, i.e., electron trapping and hole-assisted de-trapping. These two factors compensate for each other and are both strongly dependent on current and voltage level. It is worthy of further systematical investigation to determine the dominant factor under specific operating conditions.

Compared with the Schottky-type p-GaN gate HEMT, the GIT introduces additional hole injection from the hybrid drain during hard-switching transients [7] or from the gate at ON-state [3]. The strong hole injection could overwhelm the impacts of the impact-ionization-induced holes during OFF-state stress, weakening the influence of $V_{GS,OFF}$ on dynamic R_{ON}.

V. Conclusion

In this article, the impacts of OFF-state gate bias ($V_{GS,OFF}$) on dynamic R_{ON} of Schottky-type p-GaN gate HEMTs are investigated. A strong dependence of dynamic R_{ON} degradation on $V_{GS,OFF}$ is observed. The influence of negative $V_{GS,OFF}$ is attributed to two different mechanisms. With a negative $V_{GS,OFF}$ during OFF-state stress, source-to-drain leakage current will be reduced, as well as the subsequent holes generation by impact ionization. In addition, the negative $V_{GS,OFF}$ will attract holes to the gate side, and the holes flow to the buffer layer will be further reduced. As a result, fewer holes arrived in the buffer layer to assist in de-trapping electrons, worsening dynamic R_{ON} degradation. By slightly prolonging OFF-state stress time, the dynamic R_{ON} degradation aggravated by negative $V_{GS,OFF}$ could be alleviated. In practical applications of GaN HEMTs, a larger $V_{GS,OFF}$ within the limits of converters reliability is recommended to weaken current collapse and to reduce conduction loss.

References

[1] K. J. Chen *et al.*, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[2] N. E. Posthuma *et al.*, "An industry-ready 200 mm p-GaN E-mode gan-on-Si power technology," in *Proc. IEEE 30th Int. Symp. Power Semicond. Devices ICS*, May 2018, pp. 284–287, doi: 10.1109/ISPSD.2018.8393658.

[3] Y. Uemoto *et al.*, "Gate injection transistor (GIT)—A normally-off AlGaN/GaN power transistor using conductivity modulation," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3393–3399, Dec. 2007, doi: 10.1109/TED.2007.908601.

[4] E. Mizuta *et al.*, "Single-event damage observed in gan-on-Si HEMTs for power control applications," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1956–1963, Aug. 2018, doi: 10.1109/TNS.2018.2819990.

[5] I. Hwang *et al.*, "*p*-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 202–204, Feb. 2013, doi: 10.1109/LED.2012.2230312.

[6] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold voltage instability in *p*-GaN gate AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2454–2460, Jun. 2018, doi: 10.1109/TED.2018.2828702.

[7] S. Kaneko *et al.*, "Current-collapse-free operations up to 850 v by GaN-GIT utilizing hole injection from drain," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC's*, May 2015, pp. 41–44, doi: 10.1109/ISPSD.2015.7123384.

[8] K. J. Chen *et al.*, "Planar GaN power integration – the world is flat," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2020, pp. 27.1.1–27.1.4, doi: 10.1109/IEDM13553.2020.9372069.

[9] J. O. Gonzalez, B. Etoz, and O. Alatise, "Characterizing threshold voltage shifts and recovery in Schottky gate and ohmic gate GaN HEMTs," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2020, pp. 217–224, doi: 10.1109/ECCE44975.2020.9235650.

[10] S. Jahdi, O. Alatise, J. O. Gonzalez, L. Ran, and P. Mawby, "Comparative analysis of false turn-on in silicon bipolar and SiC unipolar power devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 2239–2246, doi: 10.1109/ECCE.2015.7309975.

[11] H. Ishibashi, A. Nishigaki, H. Umegami, W. Martinez, and M. Yamamoto, "An analysis of false turn-on mechanism on high-frequency power devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 2247–2253, doi: 10.1109/ECCE.2015.7309976.

[12] How to drive GaN E-mode transistors, GaN Systems GN001, Ottawa, ON, Canada, 2020. [Online]. Available: http://www.gansystems.com

[13] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An analytical model for false turn-on evaluation of high-voltage enhancement-mode GaN transistor in bridge-leg configuration," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6416–6433, Aug. 2017, doi: 10.1109/TPEL.2016.2618349.

[14] J. L. Lu, R. Hou, and D. Chen, "Opportunities and design considerations of GaN HEMTs in ZVS applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 880–885, doi: 10.1109/APEC.2018.8341117.

[15] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, "Effect of hole-injection on leakage degradation in a *p*-GaN gate AlGaN/GaN power transistor," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1203–1206, Aug. 2018, doi: 10.1109/LED.2018.2849398.

[16] X. Tang, B. Li, and K. J. Chen, "On-chip optical pumping of deep traps in AlGaN/GaN-on-Si power HEMTs," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC's*, May 2015, pp. 201–204, doi: 10.1109/ISPSD.2015.7123424.

[17] Y. Wang *et al.*, "Dynamic off-state current (dynamic I_{OFF}) in *p*-GaN gate HEMTs with an ohmic gate contact," *IEEE Electron Device Lett.*, vol. 39, no. 9, pp. 1366–1369, Sep. 2018, doi: 10.1109/LED.2018.2852699.

[18] Y. Wang, J. Wei, S. Yang, J. Lei, M. Hua, and K. J. Chen, "Investigation of dynamic I_{OFF} under switching operation in Schottky-type *p*-GaN gate HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3789–3794, Sep. 2019, doi: 10.1109/TED.2019.2930315.

[19] Y. Wang *et al.*, "A physics-based empirical model of dynamic I_{OFF} under switching operation in *p*-GaN gate power HEMTs," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9796–9805, Sep. 2021, doi: 10.1109/TPEL.2021.3062450.

[20] S. Sun, "Does GaN have a body diode? – Understanding the third quadrant operation of gaN," Texas Instrum. Incorp., Dallas, TX, USA, 2019. [Online]. Available: https://www.ti.com/lit/an/snoaa36/snoaa36.pdf

[21] Gate driver design with GaN E-HEMTs, GaN Systems GN012, Ottawa, ON, Canada, 2020. [Online]. Available: http://www.gansystems.com

[22] M. Hua, J. Wei, Q. Bao, Z. Zhang, Z. Zheng, and K. J. Chen, "Dependence of V_{TH} stability on gate-bias under reverse-bias stress in E-mode GaN MIS-FET," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 413–416, Mar. 2018, doi: 10.1109/LED.2018.2791664.

[23] M. Hua, J. Wei, Q. Bao, Z. Zhang, Z. Zheng, and K. J. Chen, "Reverse-bias stability and reliability of hole-barrier-free E-mode LPCVD-SiN_x/GaN MIS-FETs," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2017, pp. 33.2.1–33.2.4, doi: 10.1109/IEDM.2017.8268489.

[24] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng, and K. J. Chen, "Impact of substrate bias polarity on buffer-related current collapse in algan/gan-on-Si power devices," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 5048–5056, Dec. 2017, doi: 10.1109/TED.2017.2764527.

[25] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V *p*-GaN gate HEMTs: Dynamic R_{ON} characterization and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017, doi: 10.1109/TPEL.2016.2610460.

[26] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic on-state resistance test and evaluation of GaN power devices under hard- and soft-switching conditions by double and multiple pulses," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1044–1053, Feb. 2019, doi: 10.1109/TPEL.2018.2844302.

[27] F. Yang, C. Xu, and B. Akin, "Experimental evaluation and analysis of switching transient's effect on dynamic on-resistance in GaN HEMTs," *IEEE Trans. Power Electron.,* vol. 34, no. 10, pp. 10121–10135, Oct. 2019, doi: 10.1109/TPEL.2019.2890874.

[28] GS66508T datasheet, GaN System Inc., Ottawa, ON, Canada, 2018. [Online]. Available: https://gansystems.com/wpcontent/uploads/2018/12/GS66502B-DS-Rev-181214.pdf

[29] L. Efthymiou, K. Murukesan, G. Longobardi, F. Udrea, A. Shibib, and K. Terrill, "Understanding the threshold voltage instability during off-state stress in *p*-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1253–1256, Aug. 2019, doi: 10.1109/LED.2019.2925776.

[30] T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2015–2020, Oct. 2003, doi: 10.1109/TED.2003.816549.

[31] Y. Li *et al.*, "Evaluation and analysis of temperature-dependent dynamic R_{DSON} of GaN power devices considering high-frequency operation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 111–123, Mar. 2020, doi: 10.1109/JESTPE.2019.2947575.

[32] C. Roy and B. Parkhideh, "Design consideration for characterization and study of dynamic on state resistance of GaN devices," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl.*, Oct. 2019, pp. 181–186, doi: 10.1109/WiPDA46397.2019.8998909.

[33] Y. Cai, A. J. Forsyth, and R. Todd, "Impact of GaN HEMT dynamic on-state resistance on converter performance," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 1689–1694, doi: 10.1109/APEC.2017.7930926.

[34] M. Cioni, N. Zagni, F. Iucolano, M. Moschetti, G. Verzellesi, and A. Chini, "Partial recovery of dynamic R_{ON} versus off-state stress voltage in *p*-GaN gate AlGaN/GaN power HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 4862–4868, Oct. 2021, doi: 10.1109/TED.2021.3105075.

[35] GS66506T Datasheet, GaN System, Ottawa, ON, Canada, 2020. [Online]. Available: https://gansystems.com/wp-content/uploads/2020/04/GS66506T-DS-Rev-200402.pdf

[36] B. Brar, K. Boutros, R. E. DeWarnes, V. Tilak, R. Shealy, and L. Eastman, "Impact ionization in high performance AlGaN/GaN HEMTs," in *Proc. IEEE Lester Eastman Conf. High Performance Devices*, Aug. 2002, pp. 487–491, doi: 10.1109/LECHPD.2002.1146791.

[37] B. Shankar and M. Shrivastava, "Safe operating area of polarization superjunction GaN HEMTs and diodes," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4140–4147, Oct. 2019, doi: 10.1109/TED.2019.2933362.

[38] Z. Zheng, M. Hua, J. Wei, Z. Zhang, and K. J. Chen, "Identifying the location of hole-induced gate degradation in LPCVD-SiN_x GaN MIS-FETs under high reverse-bias stress," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs*, May 2019, pp. 435–438, doi: 10.1109/ISPSD.2019.8757652.

[39] S. R. Bahl, M. Van Hove, X. Kang, D. Marcon, M. Zahid, and S. Decoutere, "New source-side breakdown mechanism in AlGaN/GaN insulated-gate HEMTs," in *Proc. 25th Int. Symp. Power Semicond. Devices IC's*, 2013, pp. 419–422, doi: 10.1109/ISPSD.2013.6694434.

[40] M. Hua *et al.*, "Hole-induced threshold voltage shift under reverse-bias stress in E-mode GaN MIS-FET," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3831–3838, Sep. 2018, doi: 10.1109/TED.2018.2856998.

[41] J. Chen *et al.*, "OFF-state drain-voltage-stress-induced V_{TH} instability in Schottky-type *p*-GaN gate HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3686–3694, Jun. 2021, doi: 10.1109/JESTPE.2020.3010408.

[42] G. Zulauf, M. Guacci, and J. W. Kolar, "Dynamic on-resistance in gan-on-Si HEMTs: Origins, dependencies, and future characterization frameworks," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5581–5588, Jun. 2020, doi: 10.1109/TPEL.2019.2955656.