Modeling and Design of High-Power, High-Current-Ripple Planar Inductors

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***Abstract*—This article is focused on modeling and design optimization of high-current-ripple planar inductors in liquid-cooled high-power applications, such as electric-vehicle drivetrain systems, where efficiency and power density are the key performance metrics. The planar-inductor optimization is facilitated by innovations in computationally efficient and accurate models of ac winding loss and thermal management. A novel approximate analytical model for the ac winding loss takes into account effects of inside-the-core versus outside-the-core winding geometry as well as the air-gap fringing effect. Furthermore, thermal management strategies are introduced to enhance the vertical thermal flow from the core and the windings to the cold plate, leading to 2.5–3 times higher peak power capability compared with standard solutions. The developed modeling and optimization techniques are applied to planar inductor design in a 16.5-kW-rated SiC-based zero-voltage-switching quasi-square-wave boost converter, and the insights of selecting the core dimensions, number of turns and inductance are discussed in detail. The designed ELP 43-based planar inductor achieves a power density of 175.7 kW/L, and is experimentally validated on the converter prototype, achieving 98.8% efficiency at the typical 9.45-kW point, and less than 60 °C of worst-case temperature rise with a winding loss of 68 W in full power operation.**

***Index Terms*—High-frequency inductors, optimization, planar inductors, thermal management.**

I. Introduction

ADVANTAGES of planar magnetics in power electronics applications include low profile, predictable parameters including parasitics, and ease of manufacturability, together with improved thermal characteristics and higher power density [1]. As a result, planar magnetics are routinely applied in high-density power converters at low and moderate power levels in the kW range. Advances in silicon carbide (SiC) MOSFETs have enabled higher switching frequencies and reductions in the size of magnetics at higher voltage and power levels. Increased power density is particularly important in electrified transportation applications, which motivates the need to extend modeling and design optimization techniques to planar magnetics for power conversion at high power levels.

Applying SiC devices to allow higher switching frequency at higher power levels is often accompanied by employing operating modes, such as zero-voltage-switching quasi-square-wave (ZVS-QSW) [2]–[4] or discontinuous conduction mode (DCM) [5], to reduce switching losses and to lower the required inductance. Such modes of operation result in relatively high inductor current ripple, which causes substantial ac loss and temperature rise in inductors, making the conventional design methods based on dc resistance and saturation flux density less effective [6]. A more practical method for high-ripple planar inductor design is numerical optimization with the objectives of minimizing power loss and volume, which critically requires loss models with excellent accuracy and speed in order to support large-scale parameter sweeps through a large design space. Furthermore, as temperature limitations impose a major constraint on the design, it is important to develop both thermal management improvements to enable further size reduction, and electrothermal models to validate the thermal performance during the design process.

A major challenge to the loss modeling for inductors lies in the fringing effect; the fringing field of the air gaps makes the current in planar windings more crowded near the gaps, which substantially contributes to the ac winding loss. The widely used 1-D analytical model of ac winding loss based on Dowell's study [7]–[9] cannot capture the fringing effect and will significantly underestimate the loss of gapped inductors. Several studies have developed 2-D analytical models to include the fringing effect [10]–[13] by assuming the fringing field crossing each conductor is uniform, which is valid for narrow conductors, but not for wide planar printed circuit board (PCB) turns utilizing the full window width that are commonly used in high-power applications. For such cases, 2-D or 3-D finite-element analysis (FEA) has proven to be an effective tool [1], but its long computation time makes it impractical for design optimization that relies on exhaustive parameter sweeping. It is possible to adopt more advanced optimization algorithms, such as the genetic algorithm used in [14], but the computation time would still be lengthy when wide ranges of parameters are considered. Alternatively,

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curvefitted models based on a series of FEA results [15], [16] are useful for well-defined problems with a limited number of design variables, but such models cannot be easily generalized to wider design ranges.

Although planar inductors offer improved thermal characteristics due to the high surface-area-to-volume ratio, effective thermal management is particularly challenging in high-density, high-power applications, such as electric-vehicle drivetrain power electronics. Liquid cooling is ubiquitous in such systems, but the standard cold plates with a flat surface can only effectively cool one side of the core and fall short of cooling the winding PCB. One direction is to introduce direct thermal interfaces between the winding and the heat sink, as demonstrated for a custom pot core in [17]. An alternative solution is to directly print windings on the liquid-cooled cold plate [18], but this approach is limited to two-layer designs. Effective thermal management solutions for planar magnetics optimized for high-power high-density applications, using cores such as ELP, are yet to be developed.

The contributions of the work of this article include extensions to loss and thermal analysis and modeling techniques necessary to support optimization of high-power, high-current-ripple planar inductors in high-density, liquid-cooled applications. First, the modeling accuracy of ac winding loss is improved by correcting a common misconception related to simplifying the 3-D inductor geometry into 2-D models. Furthermore, a novel closed-form approximate model is developed, which is able to effectively capture the fringing effect in a wide range of core and winding configurations, while achieving the same level of calculation speed as the simple 1-D models.

To address thermal management limitations, a series of techniques are proposed to substantially boost the peak power capability of the inductors by improving the thermal flow in the vertical direction. A corresponding lumped thermal resistance model is also developed to support the parameter sweeping and improve intuition around the thermal design.

Applications of the developed loss and thermal models are demonstrated in comprehensive optimization of a high-power high-current ripple planar inductor for a 66-kW-rated SiC-based four-phase ZVS-QSW boost converter for automotive drivetrain application, and the insights of selecting core and winding parameters are discussed in detail. The optimized inductor prototype achieves a power density of 175.7 kW/L, which is about three times higher compared with the power density of wire-wound inductors reported in [19], and is also higher than the power density reported for planar inductors in [20]. A comparable power density can be achieved using high temperature nanocrystalline cores by allowing higher operating temperature and reduced ambient temperature [19]. However, since such inductors are not well suited for operation with high current ripple at high switching frequency, the overall converter efficiency is inferior to converters with soft-switching ZVS-QSW operation using ferrite-based inductors.

The rest of this article is organized as follows. The case study converter and inductor specifications are summarized in Section II. The ac winding loss modeling is addressed in Section III, including a superposition-based modeling technique as well as an approximate analytical model for the fringing effect. The thermal management analysis and the proposed enhancement strategies are discussed in Section IV. With the aforementioned models and strategies, Section V is focused on the optimization of the inductor, with an in-depth analysis on the optimal properties of core geometry, number of turns, and inductance value. Experimental verification results are presented in Section VI. Finally, Section VII concludes this article.

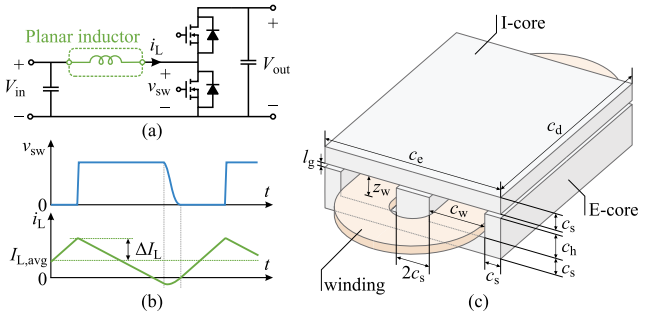


Fig. 1. (a) Planar inductor in a boost converter. (b) Inductor current and switch-node waveforms in ZVS-QSW mode of operation. (c) Dimensional parameters of an ELP-core planar inductor.

II. Case Study Design Specifications

The high-power high-current-ripple planar inductor to be designed is for a 66-kW SiC-based four-phase boost converter for automotive drivetrain application, as shown in Fig. 1(a). The peak operating point of each phase, which determines the worst-case operation of the inductor, is defined as: input voltage $V_{\text{in}} = 300$ V, output voltage $V_{\text{out}} = 630$ V, and power per phase $P = 16.5$ kW. The typical operating point of each phase, which is the basis for power loss and efficiency analysis, is defined as: Input voltage $V_{\text{in}} = 350$ V, output voltage $V_{\text{out}} = 580$ V, and power per phase $P = 9.45$ kW.

At most operating points, the converter is set to operate in ZVS-QSW mode, where the current ripple ΔI_{L} is approximately the same as the averaged inductor current $I_{\text{L,avg}}$, and the switching frequency is adjusted accordingly, as shown in Fig. 1(b). However, exceptions may apply due to the limits in the switching frequency (in this article, the converter switching frequency is limited between 100 and 350 kHz) and the saturation flux density, which may force the converter to operate in continuous conduction mode (CCM). The exceptions are further explained in Appendix A.

As shown in Fig. 1(c), the planar inductor design is based on the ELP core, which is selected for its simple geometry, convenience of stacking, and wide product line for high-power applications. For development of the design guidelines for the optimal specifications of the inductor, the dimensions of the core considered in this article are not confined to the few standard commercially available options. Instead, the design space includes various combinations of the core geometrical parameters in a wide range between the size of ELP 22 and ELP 102 cores, and the ranges of parameters to be considered in the design process are as follows.

1) *Core Dimensions:* 22 mm $\leq c_e \leq$ 100 mm, 2.5 mm $\leq c_s \leq 8$ mm, 3 mm $\leq c_h \leq 13$ mm, 16 mm $\leq c_d \leq$ 100 mm, where c_e, c_s, c_h, and c_d are defined as shown in Fig. 1(c).
2) *Number of turns n:* $2 \leq n \leq 8$.
3) *Inductance L:* $5\mu\text{H} \leq L \leq 20\,\mu\text{H}$.
4) *Copper Thickness:* 3 to 6 oz.

The required air gap can be found using standard techniques [21] in which the reluctance considering the 2-D fringing field is taken into account. Note that the contribution of the 3-D fringing effects is not considered for simplicity, since the width of the core legs is significantly shorter than their depth in ELP cores. The switching frequency is determined to achieve ZVS-QSW operation. Additionally, for simplicity, the following properties are fixed for all the designs: The winding PCB has only one turn per layer to maximize the width of the copper to boost the thermal and efficiency performance for high-power applications, and the PCB substrates are all set as 10-mil FR4 layers using FR406 material, with a 1-mm gap between the PCB edges and the core for isolation and dimensional tolerance. Finally, the N87 ferrite material is selected because of the wide availability of different core sizes. The modeling techniques and the design process presented in the following sections can be easily extended to address sweeping over a wider range of parameters, including alternative core materials.

Regarding the temperature limits, the coolant temperature is set to 65 °C, considered the standard for automotive applications. Based on the material properties, the temperature limits in the PCB winding and the ferrite core are, respectively, set as 140 °C and 115 °C, which, when another 10° C margin is considered, correspond to 65 °C and 40 °C of temperature rise.

Given the system specifications, the objective is to perform inductor design optimization based on volume and loss metrics. To better distinguish the optimal designs, these two objectives are converted into the following reciprocal terms to obtain a pair of "higher is better" metrics as follows.

1) $P_{\text{max}}/V_{\text{ind}}$: Evaluates the inductor volume V_{ind}, where the converter peak power $P_{\text{max}} = 16.5$ kW.
2) $P_{\text{nom}}/P_{\text{loss,nom}}$: Evaluates the inductor power loss $P_{\text{loss,nom}}$ at the nominal point, where $P_{\text{nom}} = 9.45$ kW.

III. Modeling of AC Winding Loss

The objectives in this section are to develop computationally efficient models to accurately predict ac winding losses by properly taking into account the PCB winding geometry and the fringing effect in a high-power planar inductor.

A. Superposition of 2-D Models

For the ac winding loss modeling of planar inductors, it is well known that 2-D simplification can significantly reduce the complexity of 3-D problems, but the conventional 2-D simplification approach is not able to preserve all of the physical properties in the entire inductor. Given the planar inductor structure shown in Fig. 2(a), the conventional approach is to develop a 2-D planar model based on the cross section at the middle of the inductor shown in Fig. 2(b), and the result of the 2-D

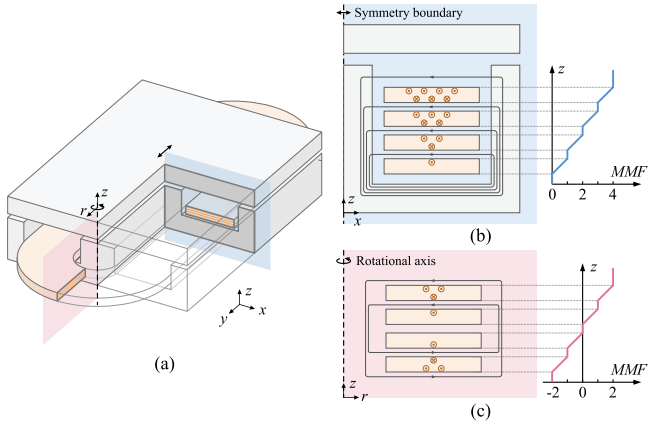


Fig. 2. ELP core-based planar inductor with (a) planar and axisymmetric cross-sections. (b) 2-D planar model in xz-coordinate system and its MMF distribution. (c) 2-D axisymmetric model in the cylindrical rz-coordinate system and its MMF distribution.

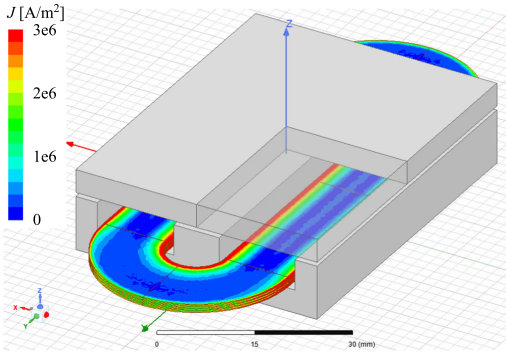


Fig. 3. 3-D FEA simulated current density of an ELP 43-based four-layer planar inductor with a 0.7-mm air gap, and a 300-kHz ac current excitation.

inside-the-core model is then simply scaled by the mean length per turn (MLT). Since the core has a large permeability, the magnetomotive force (MMF) induced in the core is negligible, and hence the MMF is zero underneath the winding bottom layer, and is n times the winding current on the top. However, this property does not apply to the portion of the winding outside of the core window, as illustrated in Fig. 2(c). Without the large-permeability core surrounding the winding, the H-field distribution is symmetrical around the middle of the winding, which is fundamentally different from the 2-D planar model. Fig. 3 shows a 3-D FEA simulated example, which illustrates the differences in the current distribution in the two portions of the winding.

An alternative, 2-D axisymmetric model, is developed to address this issue: For the generalized racetrack-shape winding shown in Fig. 2(a), the solution at the curved portion of the winding outside the core is similar to the solution for a toroidal coil, which can be simplified into a 2-D model rotating around the z-axis shown by Fig. 2(c). The result of the 2-D axisymmetric model can be considered equivalent to the sum of the contributions by the two 180° arcs of the winding. On the other hand, the conventional 2-D planar model shown by Fig. 2(b) is valid for the winding region inside the core window,

TABLE I
SIMULATED AC RESISTANCES OF THE EXAMPLE CASES BASED ON THE 3-D FULL MODEL, THE MLT-BASED 2-D MODEL, AND THE SUPERPOSITION-BASED 2-D MODEL

Case	3D FEA	2D MLT-based	2D superposition
4-turn ELP 43	35.2 mΩ	43.3 mΩ (+22.8%)	40.1 mΩ (+13.9%)
6-turn ELP 43	95.7 mΩ	129.9 mΩ (+35.7%)	107.8 mΩ (+12.6%)
4-turn ELP 64	32.4 mΩ	47.1 mΩ (+45.6%)	36.7 mΩ (+13.3%)
6-turn ELP 64	90.1 mΩ	146.4 mΩ (+62.5%)	100.6 mΩ (+11.7%)

[0]All cases have 5 oz copper weight, 0.7-mm air gap and 300 kHz as the frequency.

and the solution can be scaled by the y-direction depth of the core. Finally, the ac resistance of the entire winding is obtained by the superposition of the results from the aforementioned two models: The standard 2-D model for the winding inside the core, and the 2-D axisymmetric model for the winding outside the core.

The superposition-based approach is validated in a series of case studies detailed in Table I, where the computed ac resistance, R_{ac}, numbers based on 3-D and 2-D FEA simulations are compared. In all cases, the superposition-based approach is able to reduce the error substantially compared with the conventional 2-D MLT-based approach.

B. Approximate Modeling of Fringing Effect

While 2-D simplification significantly reduces complexity, the computational burden of 2-D FEA is still very high in the optimization process that relies on sweeping parameters over wide ranges. This motivates the development of simpler analytical models. Upon considering the difficulty of solving the eddy currents under the nonuniform fringing field analytically, one may develop an approximate model based on the assumption that the current density distribution approximately follows a certain pattern due to the fringing effect. The equivalent R_{ac} value can then be solved by taking into account the current density profile in the 1-D Dowell's analytical model. In this way, the model is applicable to a much wider range of parameters without the limitations imposed by curve fitting to the results coming from numerical analysis.

In the 2-D planar model shown in Fig. 2(b), when the skin depth is less or equal to the copper thickness, the fringing field is mostly shielded by the top surface of the top layer, leading to an assumption that it is only the current distribution in this part that needs to be modified, whereas for all of the other layers, the current density and loss profile can still be computed from the 1-D Dowell's analytical model. To find the current distribution in the top layer, the perpendicular fringing field H_{z} equation from [11] is written as follows, for reference:

$$H_{\text{z}}(x) = \frac{0.9nI}{2\pi l_{\text{g}}}\left[\tan^{-1}\frac{2xl_{\text{g}}}{x^2+z_{\text{w}}^2-l_{\text{g}}^2} - \tan^{-1}\frac{2x'l_{\text{g}}}{x'^2+z_{\text{w}}^2-l_{\text{g}}^2}\right] \tag{1}$$

where $x' = (c_{\text{w}} - x)$. When $l_{\text{g}} \ll z_{\text{w}}$, (1) can be simplified into

$$H_{\text{z}}(x) \approx \frac{0.9nI}{\pi}\left(\frac{x}{x^2+z_{\text{w}}^2} - \frac{x'}{x'^2+z_{\text{w}}^2}\right) \tag{2}$$

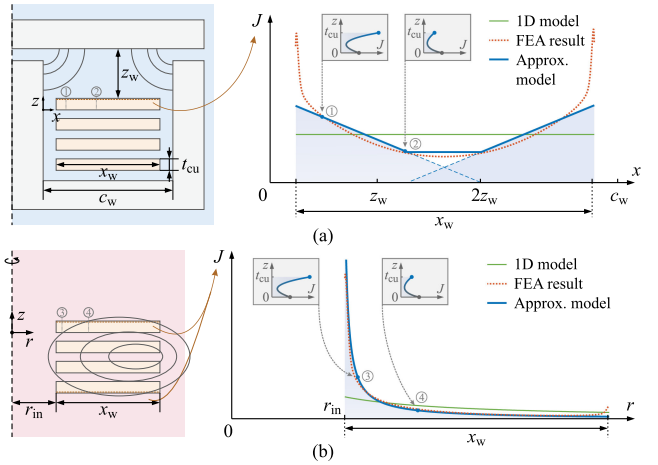


Fig. 4. Approximate current distribution on the top surface of the top PCB layer in (a) 2-D planar model and (b) 2-D axisymmetric model. The top surface current density curves are entered into into the 1-D model for the z-direction currents.

which suggests that the fringing field is mostly dependent on z_{w} rather than l_{g}. Furthermore, the derivative of $H_{\text{z}}(x)$ is

$$\frac{\text{d}H_{\text{z}}(x)}{\text{d}x} \approx \frac{0.9nI}{\pi}\left(\frac{z_{\text{w}}^2-x^2}{(x^2+z_{\text{w}}^2)^2} + \frac{z_{\text{w}}^2-x'^2}{(x'^2+z_{\text{w}}^2)^2}\right). \tag{3}$$

At the left-hand side of the winding, since x' is much larger than x, the second term in (3) can be neglected, which implies that the peak of H_{z} occurs near $x = z_{\text{w}}$. Similarly, on the right-hand side, the peak occurs at approximately $x' = z_{\text{w}}$, i.e., at $x = c_{\text{w}} - z_{\text{w}}$. Consequently, another assumption is made that the current is crowded at the two edges due to the two gaps, and the crowding effect is centered around the peak H_{z} points. For simplicity, the current density is assumed to follow linear functions of x, which intercept with the x-axis at $x = 2z_{\text{w}}$ and $x = c_{\text{w}} - 2z_{\text{w}}$, respectively, as shown by the blue dashed lines in Fig. 4(a). By combining the two linear dependencies, the approximate current distribution then follows the piecewise solid blue curve in Fig. 4(a). Finally, the slope and the magnitude parameters of the piecewise linear approximation are determined by the integration along the x direction and by equating the result to the same normalized value as the 1-D model. A detailed derivation is included in Appendix B. Fig. 4(a) shows how the approximate current density curve matches well with the red curve obtained by FEA solution for the specific case study.

It should be noted that (1) is a simplified model, which is only valid when the air gap is relatively small. In the work reported in this article, the length of the air gap is limited to $l_{\text{g}} \le c_{\text{h}}/2$ so that the model is generally applicable. If a wider air gap needs to be considered, 3-D reluctance modeling, as described in [22], can be used for improved accuracy.

In the outside-the-core axisymmetric model, as the gap is much farther away from the winding, the fringing effect is ignored for simplicity. However, the current distribution in the winding segments outside the core is greatly affected by another perpendicular magnetic field, which is produced by the winding current itself. As indicated by the FEA result shown in Fig. 4(b),

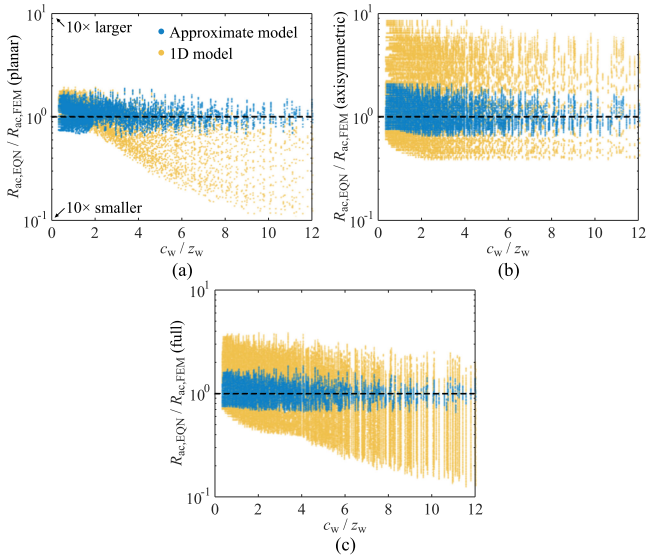


Fig. 5. Error analysis of the proposed approximate R_{ac} model compared with the 1-D model: $R_{ac,EQN}/R_{ac,FEA}$ data points between 100 and 500 kHz, respectively, for (a) 2-D planar model, (b) 2-D axisymmetric model, and (c) complete model.

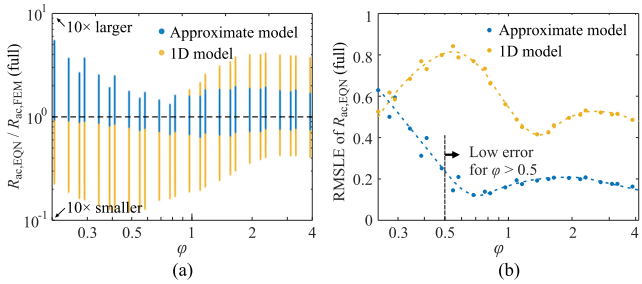


Fig. 6. Error of $R_{ac,EQN}$ generated by the approximate and the 1-D models as functions of the parameter φ defined in (4). (a) Sweeping points. (b) Root mean squared logarithmic error (RMSLE).

the normalized current distribution in dc and ac situations are notably different. Based on a series of FEA results, it is observed that the current density on the top surface of the top layer generally follows a reciprocal function of r, with an offset of the inner rim radius r_{in}, and the coefficient of the function can be found according to the total winding current. A detailed derivation is included in Appendix B.

The effectiveness of the approximate model in combination with the proposed superposition strategy is validated by an exhaustive sweep within the inductor parameter ranges defined in Section II and a wide frequency range between 6 and 3 MHz. The R_{ac} values are computed, respectively, using 2-D FEA simulation, the proposed approximate model, and the 1-D model using the conventional MLT-based scaling approach. The FEA-based $R_{ac,FEA}$ is considered as the baseline, which took more than 50 to generate the entire dataset, whereas the datasets of the equation-based $R_{ac,EQN}$ were generated in less than 10 min. The accuracy is then evaluated by the term $R_{ac,EQN}/R_{ac,FEA}$ on a log scale, which displays the modeling errors in order of magnitude. The data points for frequencies between 100 and 500 kHz (covering the range of the first harmonic based on the intended converter switching frequencies) are plotted in Fig. 5(a)–(c), respectively, for the 2-D planar model, the axisymmetric model and the complete inductor. The term c_w/z_w is swept across the x-axis, and according to 1-D modeling error shown in Fig. 5(a), it is critically and positively correlated to the fringing effect. In comparison, the approximate model achieves significant improvement in accuracy in both of the 2-D models. Although the error could be more than 10% for the approximate model, it will be shown in Section V that the error is acceptable in an optimization-oriented analysis as the model is able to accurately predict the trend of the loss as a function of multiple variables.

Note that the approximate model clearly has a limited validity with respect to frequency because the approximate current distribution only applies under the assumption that the frequency is relatively high. To be more specific, as the skin effect is also related to the copper thickness t_{cu}, the validity of the model is related to the factor φ, which is defined as

$$\varphi = \frac{t_{cu}}{\delta} = \frac{t_{cu}}{\sqrt{\rho/(\pi\mu f)}} \tag{4}$$

where δ is the skin depth, μ is the permeability of copper, and ρ is the copper resistivity. In Fig. 6, the error of $R_{ac,EQN}$ generated by the approximate and the 1-D models are compared as functions of φ. Based on the data points presented in Fig. 6(a), the root mean squared logarithmic error (RMLSE) is computed as shown in Fig. 6(b), indicating that the approximate model is able to achieve good and consistent accuracy when $\varphi > 0.5$. Note that in practical designs of planar inductors, φ is commonly selected around one to minimize ac winding loss when considering the proximity effect, and the approximate model is able to accurately predict R_{ac} values at both the first and the higher harmonics in such cases.

IV. Modeling and Enhancement of Thermal Management

The objectives in this section are to present enhanced thermal management solutions for high-power planar magnetics, and to develop a computationally efficient thermal model suitable for inductor optimization.

To further improve the power density metric, a comprehensive liquid cooling-based thermal management solution with a series of enhancement strategies is proposed, as illustrated in Fig. 7, which is an extension of the work reported in [23]. The key strategies are as follows.

1) Custom Aluminum Plate: The planar inductor is mounted on a custom liquid-cooled aluminum cold plate with a slot fitting the core so that the aluminum block is able to absorb heat from the core and the winding PCB simultaneously.

2) Ceramic Shim: A 0.5-mm thick shim made of thermally conductive aluminum oxide (Al_2O_3) is sandwiched between the winding PCB and the cold plate for insulation. With the insulation layer, the solder mask on the bottom side of the PCB is removed to further improve the heat conduction. The ceramic shim also touches the planar E core, providing an alternative

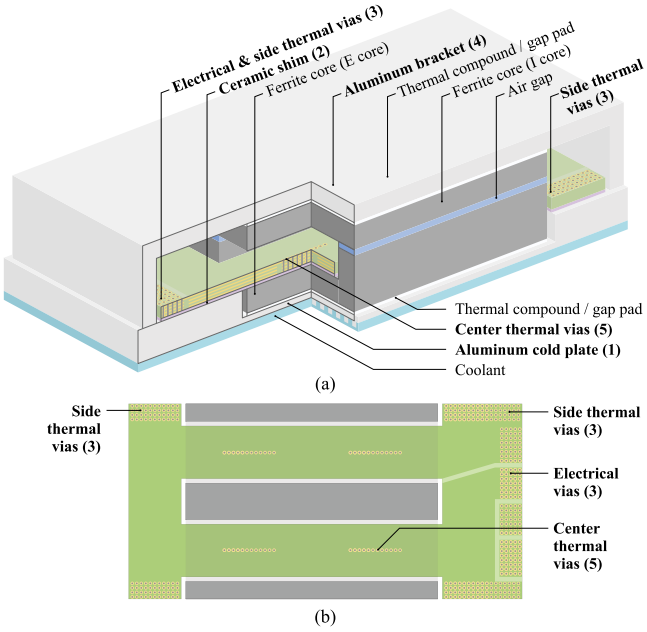


Fig. 7. Thermal management enhancements for planar inductors. (a) 3-D overview. (b) Top view of the winding PCB.

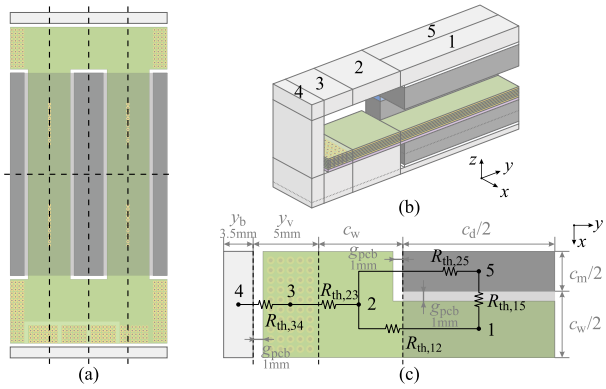


Fig. 8. One-eighth simplification of the 3-D planar inductor geometry. (a) Top view of the slices that create the one-eighth thermal model. (b) 3-D view of the one-eighth model with five-region meshing (without center thermal vias). (c) Lateral thermal resistance network and dimensions.

TABLE II
THERMAL CONDUCTIVITY OF THE MATERIALS AND THE CONVECTION HEAT TRANSFER FACTOR OF THE COLD PLATE

Material	Specs	Material	Specs
PCB copper	385 W/m K	Ceramic shim	17 W/m K
PCB FR4	0.3 W/m K	Gap pad	5 W/m K
Aluminum	160 W/m K	Air-gap shim	0.2 W/m K
Ferrite	5 W/m K	Cold plate h factor	3 kW/m^2 K

heat transfer path to bring the heat out of the winding vertically. To ensure a solid contact, a thermally conductive gap pad is added under the core to compensate for dimensional errors and tolerances in the core height.

3) Aluminum Bracket: The entire inductor structure is covered by another piece of aluminum bracket to manage the I core temperature. The bracket is kept away from the air gap fringing field to avoid eddy current loss in the bracket.

4) Side Thermal Vias: A number of thermal vias are placed around all sides of the PCB to transfer heat from the winding to the cold plate more effectively. For inductors, the thermal vias are all connected to the top layer, which has the highest winding loss due to the proximity and the fringing effects.

5) Center Thermal Vias: A number of thermal vias are introduced at the center of the PCB winding, adding an additional vertical thermal conduction path from the top winding to the E-core through the ceramic shim. While the vias slightly increase the dc winding resistance by obstructing the current flow in the other winding layers, the impact on the ac winding resistance is, in fact, very small, because the current in all the layers is crowded on the two edges due to the end effect, and the ac current density at the center of the winding is relatively small.

A. Thermal Management Enhancements

It is worth noting that compared with a conventional liquid-cooled inductor, the proposed enhancements require only an additional standard Al_2O_3 ceramic shim and some custom aluminum parts. The approach does not require any advanced PCB substrate materials, nor insulation materials with very high thermal conductivity, such as aluminum nitride, which may substantially add to the cost. Nevertheless, the proposed solution may also be combined with the use of advanced materials to pursue even better thermal performance.

B. Modeling of the Thermal System

The thermal analysis of planar inductors can be done using 3-D FEA simulation, which is computationally intensive and not well suited for parameter sweeping in an electrothermal optimization process. Instead, simpler lumped thermal resistance models may be considered [24]–[26]. For the considered planar inductor structure, to further reduce complexity, a complete system model can be sliced into eight similar pieces as shown in Fig. 8(a). In this "one-eighth" (1/8) model, the area for the vias is averaged across all the pieces, and the vias are only connected to the top layer for simplicity.

The lumped thermal resistance model with the proposed thermal management solution is developed based on the 1/8 model. For demonstration, modeling of the inductor without the center thermal vias is explained first. As illustrated in Fig. 8(b) and (c), the entire solution domain is divided into ive regions in the x-y plane labeled as 1 to 5, and then divided in z direction according to the interfaces between segments of different materials. Then, for each element, the equivalent thermal resistances in x, y, and z directions can be analytically calculated according to the thermal properties summarized in Table II. Note that the z-direction thermal resistance of the vias is computed based on the cross-sectional area of via plating, which is set to 8% of the total area based on an the actual PCB winding prototype. Further simplification is made by neglecting the lateral thermal resistances of FR4, ceramic shim, and thermal pads, which are

TABLE III
COMPUTED MAXIMUM TEMPERATURE RISE AND COMPUTATION TIMES FOR THE FEA MODELS AND THE PROPOSED LUMPED RESISTANCE MODEL

Model	Max ΔT_{pcb}	Max ΔT_{core}	Comput. time
Full model FEA (Icepak)	55.0 °C	28.1 °C	5 min
1/8 model FEA (Icepak)	59.9 °C	27.3 °C	1 min
Lumped model (Matlab script)	57.9 °C	28.9 °C	0.25 ms

much larger than the resistances of the metal layers. Additionally, the cold plate-to-coolant thermal resistance is found based on the heat transfer coefficient, and the radiation effect and the heat convection of air are neglected.

Since all of the thermal resistances can be computed analytically, a MATLAB script is developed to automatically generate the lumped thermal resistance network matrix when provided with the system specifications as inputs, which is then used in the optimization process discussed in Section V.

The lumped model is validated in a case study based on a 4-turn, 5-oz planar inductor using two sets of ELP 43 cores in a stack, where the power loss values for the winding layers (from bottom to top) are, respectively, set as 16, 16, 16, and 24, and 36 W for the core. The temperatures are computed using FEA for the complete system (implemented in Ansys Icepak), FEA for the 1/8 model, and the proposed lumped thermal resistance model. The computed maximum temperature rise and the running time using the same workstation for each approach are summarized in Table III. Observe that both the 1/8 simplification and the lumped modeling approach are able to maintain accuracy while reducing the computational effort. In particular, the lumped resistance model can be solved in a small fraction of the time compared to the Icepak-based full FEA model, thus enabling much more practical parameter sweeping in the optimization process.

Another important benefit of having a lumped model is to intuitively visualize the thermal system in a circuit diagram, as presented in Fig. 9 for the example case. The nodes are arranged from top to bottom according to their position in the z-direction, and from left to right by the region. The equivalent thermal resistance values, along with the computed temperature rise of the core and the winding elements, are all shown in the diagram. Furthermore, the magnitude of heat flow is visually demonstrated by the width of the pink arrows aligned with the circuit branches.

Various observations can be made based on the circuit model and the computed temperature rise results. First, due to the large lateral thermal resistance of the winding, the heat from the winding travels mostly along the vertical direction in both region 1 and 2, revealing the importance of both the winding-shim-cold plate and the winding-shim-core heat transfer paths. Second, the side thermal vias make a very small vertical thermal resistance in region 3, but can only effectively take the heat out of the top layer in region 2 and not the more remote region 1. Third, the vertical thermal resistance of the ceramic shim is already sufficiently small comparing to that of the FR4 layers, suggesting that the effect of upgrading the ceramic shim would be very limited. And as for the I core, the thermal management heavily relies on the

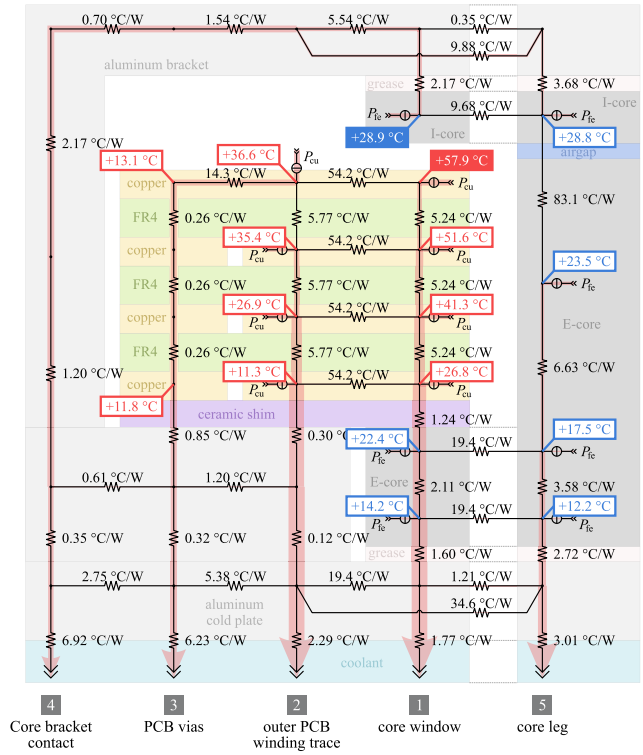


Fig. 9. Lumped thermal resistance model for the example planar inductor with the proposed thermal management enhancements.

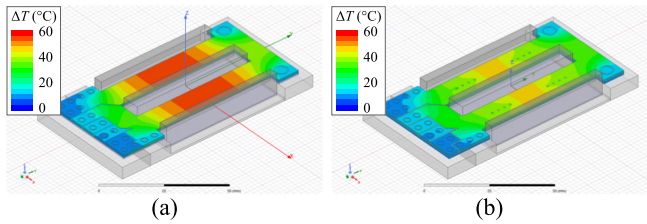


Fig. 10. FEA simulation results for the winding PCB temperature rise (a) without and (b) with the center thermal vias.

aluminum bracket rather than the underneath airgap and the core legs, which contribute very large thermal resistances.

The hot spot of the top layer winding in region 1 is also clearly depicted by the FEA simulation results shown in Fig. 10(a), an advantage of such models, further justifying the strategy of adding center thermal vias to enhance the vertical heat transfer path in the core window region. The immediate impact of the center thermal vias is illustrated by the FEA result in Fig. 10(b): For the example case, the strategy reduces the peak temperature rise by around 20%, from 55.0 °C to 45.6 °C, and makes the temperature gradient in the winding more uniform. In addition to the FEA analysis, the lumped thermal resistance model can also be extended to the case with the thermal vias, as discussed in detail in Appendix C.

A comparison study is conducted to evaluate the impact of the proposed thermal management enhancements by finding the temperature rise under the condition of removing specific thermal management strategies in the thermal model. As shown in Table IV, the winding temperature rise is approximately doubled

TABLE IV
COMPUTED WINDING AND CORE TEMPERATURE RISE FOR VARIOUS COMBINATIONS OF THERMAL MANAGEMENT STRATEGIES

Case	ΔT_{pcb}	ΔT_{core}
With everything	46.3 °C	28.1 °C
Without center vias	57.9 °C	28.9 °C
Without center vias & shim-core contact	109.9 °C	31.3 °C
Without center vias & shim-cold plate contact	161.9 °C	45.5 °C
Without center vias & side thermal vias	66.1 °C	28.3 °C
Without center vias & I-core bracket	58.8 °C	195.2 °C

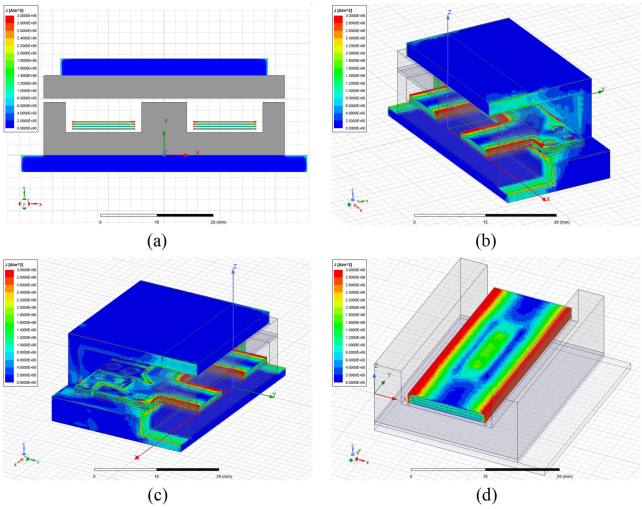


Fig. 11. FEA simulation results for high-frequency current distribution. (a)–(c) Eddy current in aluminum parts, respectively, for 2-D planar model, far side, and terminal side of the inductor, and (d) current distribution in the winding PCB with the center thermal vias.

when the shim-core contact is removed, and tripled without the shim-cold plate contact, demonstrating the importance of both strategies. Also shown is the importance of the I-core bracket, without which the peak core temperature is seven times higher. Additionally, the side thermal vias reduce the temperature rise on the winding by ∼20%.

C. Impact on AC Ohmic Loss

While the proposed strategies substantially improve the thermal management, they also introduce additional ac ohmic loss compared to a standard design. The additional loss is primarily due to eddy current loss in the aluminum parts around the planar inductor, and the increased winding loss due to addition of the thermal vias in the center of the winding.

The eddy current in the aluminum heat sink and the bracket is mainly due to the fringing field of the air gap and the proximity of the winding, which can be modeled in part starting from the 2-D planar model introduced in Section III, by adding aluminum structures in the 2-D FEA model, as shown in Fig. 11(a). Regarding the end portions of the inductor, 3-D FEA simulation is the only viable solution approach. To achieve the best possible meshing quality, separated eddy current FEA models are made for each end portion in Ansys Maxwell, as shown in Fig. 11(b) and (c). The accurate modeling of ac winding loss

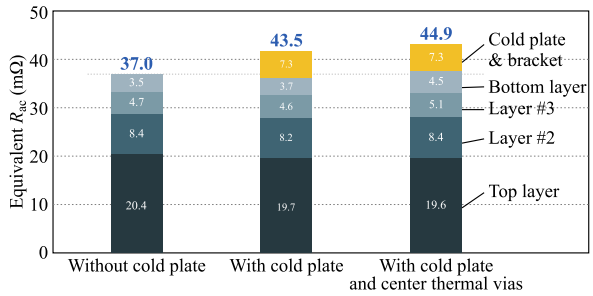


Fig. 12. Breakdown of the equivalent ac resistance without and with the cold plate and the center thermal vias.

with the thermal vias also relies on 3-D FEA simulation, which is illustrated in Fig. 11(d).

The ac ohmic loss breakdown of the inductor with and without the thermal management strategies is shown in Fig. 12. The cold plate leads to an approximate 15% increase in R_{ac}. However, it is worth noting that the extra power loss occurs in the aluminum parts, where the heat conduction to the coolant is sufficiently large. As the loss in the winding and the core generally remains the same, the additional losses do not invalidate the aforementioned thermal management analysis and model. One may also note that the center thermal vias increase R_{ac} by only 4%, and the loss in the top layer is not increased, which validates the assumptions made in the development of the thermal model and the results obtained.

D. Validation of Thermal Management Enhancements

The primary motivation for thermal management enhancements is to improve the system power density by allowing more compact inductor designs while meeting all material temperature rise limits. To demonstrate the benefit of the proposed strategies, the inductor design incorporating the proposed enhancements is compared with passive cooling, fan cooling, and conventional liquid cooling solutions. Specifically, the following cases are analyzed.

1) *Passive Cooling:* The component is cooled by free air convection through the exposed surfaces of the core and the winding. In this analysis, the heat transfer coefficient h is set as 30 W/m^2 K, which is near the upper limit of passive air cooling [27].
2) *Off-the-Shelf Cold Plate:* The E core of the inductor is attached to a liquid-cooled cold plate with $h = 3\,\text{kW}/\text{m}^2\,\text{K}$, which is same as the proposed solution and close to the limit of the off-the-shelf options. The rest of the parts are cooled through free air convection.
3) *Fan Cooling:* With forced air convection, the heat transfer coefficient of the exposed surfaces is substantially upgraded, which is set to 200 W/m^2 K in this case study, according to the common range for forced air cooling [27].
4) The proposed solution without the center thermal vias.
5) The proposed solution with the center thermal vias, the number of which is proportionally scaled according to the dimensions of the baseline design.

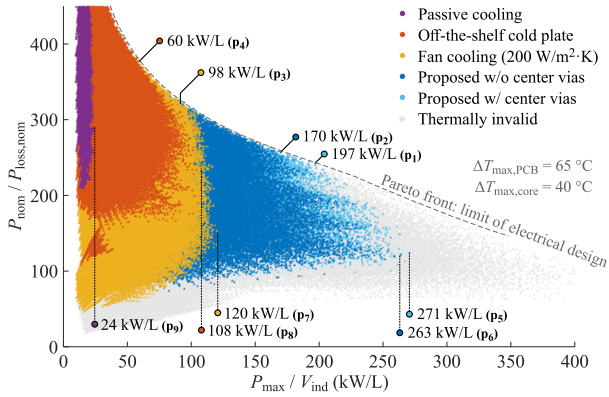


Fig. 13. Design data points in the loss and volume metrics plane. Designs that are thermally feasible under the conventional and proposed thermal management strategies are marked in different colors.

To find the generalized design limits under the respective cooling solutions, a comprehensive parameter sweep over the range defined in Section II is performed based on the proposed lumped thermal resistance model, which takes approximately 200 s to generate 800 000 data points, as opposed to an estimate of 2800 d needed by the full FEA models. The proposed approximate model is used to compute the winding loss, and as for the core loss, the basic Steinmetz's equation is used, and the worst case loss that occurs at the lowest ambient temperature is considered for simplicity. The data points with respect to their volume and loss metrics are plotted in Fig. 13, with colors marking the feasibility under different cooling strategies. Note that the eddy current loss in the cold plate is ignored for simplicity. Furthermore, since the planar inductors considered in this work are utilizing a double-sided cold plate presented in [28], where the cold-plate size is determined mainly by the thermal management requirements of the power devices, the volume of the cold plate is excluded in the size comparison focused on the inductor designs. With the proposed strategies, a maximum $P_{\text{max}}/V_{\text{ind}}$ of 271 kW/L (point p_5) is achieved, which is about 11 times higher power density compared to the passive cooling case (p_9), 2.3 times higher than the fan cooling solution (p_7), and 2.5 times higher than the case of the conventional liquid-cooled cold plate (p_8). Another observation is that the smallest possible size can only be achieved at the cost of significantly larger loss. Among the designs at the top-right Pareto front, which signifies the best tradeoff between loss and volume, a reasonable choice for $P_{\text{max}}/V_{\text{ind}}$ is at 197 kW/L (p_1), which is around 3.3 times better than the case with off-the-shelf cold plate (p_4).

V. Inductor Design Optimization

With the loss and thermal models introduced in the previous sections, it is now possible to show how these tools can be used in the inductor design optimization for the case study defined in Section II. The optimization objectives are efficiency and power density, which are, respectively, evaluated by the metrics $P_{\text{nom}}/P_{\text{loss,nom}}$ and $P_{\text{max}}/V_{\text{ind}}$ defined in Section II. As illustrated in Fig. 14, the optimization is implemented as a hierarchical two-step process as follows.

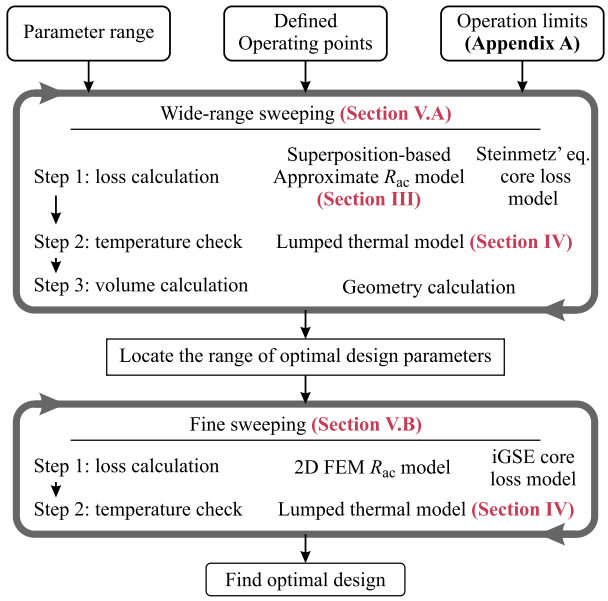


Fig. 14. Diagram of the proposed inductor design strategy utilizing the proposed winding loss and thermal models.

1) A wide-range parameter sweep using the proposed simplified models, in order to identify design insights and drive the key design parameters towards a narrower range.
2) A fine-tuning step focused on the much narrower range generated in the first step, based on more accurate, more time-consuming models.

A. Wide-Range Parameter Sweep

Among all the data points shown in Fig. 13, the points located at the top-right Pareto front are the designs representing the optimal loss versus volume tradeoff. It is of interest to find common characteristics among these optimal designs, in order to identify the desired range of the parameter for the fine-tuning step. In the following analysis, the data points representing the designs for various sets of parameter values are divided into three categories according to the volume-related metric $P_{\text{max}}/V_{\text{ind}}$, so that the relationship between the parameters and the potentials to reduce loss can be clearly identified under the same volume constraint.

1) Spacing to Air Gap: The spacing between the winding and the air gap is evaluated by the term $c_{\text{w}}/z_{\text{w}}$. As discussed in Section III, this is the critical factor that determines the fringing effect. However, while smaller $c_{\text{w}}/z_{\text{w}}$ generally leads to less prominent fringing effect, a too small value may either compromise the width of the window c_{w} resulting in larger dc resistance R_{dc}, or require a large z_{w}, which increases the height of the component reducing the power density. According to Fig. 15(b), where the Pareto-front data points for the loss metric are plotted as functions of $c_{\text{w}}/z_{\text{w}}$ for three different volume constraints, the optimal ratio generally lies in the range between 2 and 4. Note that, this conclusion may only hold for high-ripple inductors, and the optimal ratio is expected to be much larger

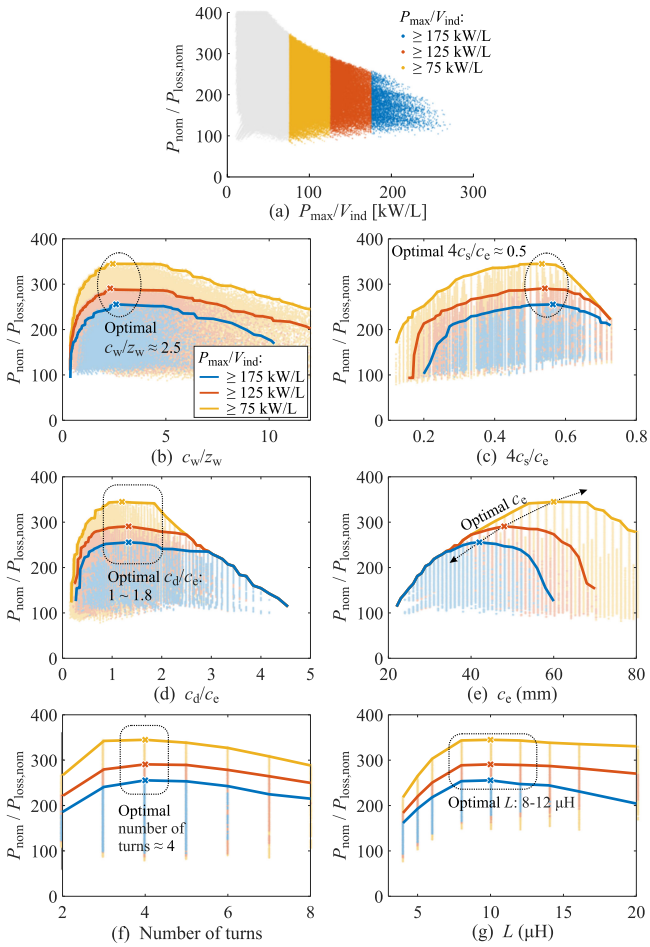


Fig. 15. (a) Design points are divided into three categories based on volume constraints. For each category, the maximum possible $P_{nom}/P_{loss,nom}$ (Pareto-front designs) is plotted as a function of various design parameters: (b) c_w/z_w; (c) $4c_s/c_e$; (d) c_d/c_e; (e) c_e; (f) number of turns; and (g) inductance.

for gapless transformers and for low-ripple dc inductors, where the fringing effect is much less significant.

2) Width of Core Legs: To find a more general conclusion, the width of the core leg is normalized and evaluated by the ratio of the total core leg width $4c_s$ to the total core width c_e. Inductors with higher $4c_s/c_e$ have wider core legs under a compromised window width. Wider core legs effectively increase the core cross-sectional area, which helps reduce core loss by reducing the ac flux density ΔB, but the winding loss increases as the width of the winding is sacrificed. According to Fig. 15(c), the optimal ratio generally lies in the range between 0.2 and 0.3, irrespective of the volume constraint.

One interesting finding is that the optimal range of $4c_s/c_e$ is higher than the ratio found in commercially available large-size ELP planar cores. This can be explained by the fringing effect, which causes the current to be more crowded on the edges. As a result, beyond a certain point, increasing the winding width does not help in reducing the current density and bringing the ac winding loss down. In contrast, when the fringing effect becomes very weak, the winding loss can be further decreased always by increasing the winding width, and the optimal width of the core legs in such cases is smaller. The common ELP 43 and ELP 64 cores having $4c_s/c_e < 0.4$ are generally suitable for the cases when fringing effect is small, but their $4c_s/c_e$ is somewhat too small for the design of high-ripple inductors, where the fringing effect is significant.

3) Core Depth: The depth of the core c_d is also normalized and evaluated by the term c_d/c_e. The result presented in Fig. 15(d) suggests that the optimal ratio generally lies in the range between 1.0 and 1.8, irrespective of the volume constraint. This is another departure from the off-the-shelf cores, where $c_d/c_e < 1$. The reason is as follows: When comparing two inductors with the same volume but different c_d/c_e values, the one with a smaller c_d and a larger c_e generally comes with a larger winding width as well, making the area taken by the PCB out of the core relatively larger. Consequently, the volume effectively taken by the core is smaller, leading to a larger core loss due to the increased ΔB. Certainly, excessively long core depth should also be avoided, because it leads to narrow and long traces resulting in large winding loss. The optimal ratio c_d/c_e represents a balance between core loss and winding loss.

4) Core Width: The results for the optimal core width c_e are shown in Fig. 15(e). As the power density constraint decreases, the optimal c_e increases and the efficiency potential is improved. It is important to note that this numerical solution is less general, and holds only for the case-study system defined in Section II.

5) Number of Turns: According to Fig. 15(f), the optimal number of turns is approximately 4, and leaning to 5 at higher power density constraint. This result represents a well-known tradeoff between the core loss, which generally goes up when the number of turns is reduced, and the winding loss, which is higher when the number of turns is increased. The optimal range for the number of turns is specific for the case-study system defined in Section II.

6) Inductance: As shown in Fig. 15(g), the optimal inductance lies between 8 and 12 μH, which is again specific for the considered case study. With lower inductance, power loss increases significantly because of the 350-kHz frequency limit, which forces the converter to operate in CCM resulting in higher current ripple and therefore higher winding loss. With inductance higher than optimal, however, the inductor will either require more turns which leads to higher winding loss, or larger core which compromises power density.

Since the optimal ranges for all the parameters except c_e remain the same irrespective of the volume constraint, the designs within the aforementioned ranges of the five parameters are highlighted in the $P_{nom}/P_{loss,nom}$ versus P_{max}/V_{ind} plot shown in Fig. 16, with a colormap indicating the respective c_e values. All the highlighted points are positioned near the top-right Pareto front, suggesting that the featured parameter ranges are very effective in screening out the optimal designs.

An important point to note is that the validity of the numerical optimization critically depends on modeling accuracy. To validate the effectiveness of the approximate ac resistance model described in Section III, the parameter sweep is also performed with the 2-D FEA superposition-based model, and the 1-D MLT-based model, and correspondingly two more sets of data points are generated. The ranges of optimal parameters generated using

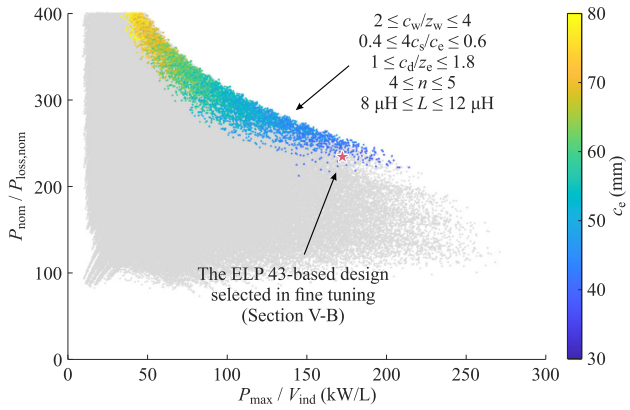


Fig. 16. $P_{nom}/P_{loss,nom}$ versus P_{max}/V_{ind} metrics for the designs based on the sets of parameters in the ranges identified for fine tuning. The final design selected in the fine tuning stage (see Section V-B) is marked by a star.

TABLE V
OPTIMAL PARAMETERS GENERATED BY THE SIMPLIFIED AND THE FEA MODELS FOR TWO VOLUME CONSTRAINT CATEGORIES

Item	$P_{max}/V_{ind} \ge 175$ kW/L			$P_{max}/V_{ind} \ge 75$ kW/L		
	2D FEA model	Approx. model	1D model	2D FEA model	Approx. model	1D model
c_e	42 mm	42 mm	44 mm	60 mm	60 mm	70 mm
c_w/z_w	2.4	2.4	6.2	2.4	2.4	16.5
$4c_s/c_e$	0.52	0.56	0.42	0.52	0.56	0.42
c_d/c_e	1.3	1.3	1.5	1.0	1.1	1.0
n	4	4	4	4	4	6
L	10 µH	10 µH	10 µH	10 µH	10 µH	20 µH

different ac winding loss models are compared in Table V. For all the parameters shown in the table, the proposed approximate ac resistance model leads to almost the same result as the FEA model. In contrast, the 1-D model predicts a much larger c_w/z_w as it underestimates the fringing effect. The optimum values for c_e, n and L predicted by the 1-D model match well with the FEA model only for $P_{max}/V_{ind} \ge 175$ kW/L, while the errors become very significant for the $P_{max}/V_{ind} \ge 75$ kW/L volume constraint category.

B. Fine-Tuning

Based on the optimal parameter ranges identified in the previous section, fine-tuning is performed next to find the more accurate solution of optimization. In the specific case study, the volume metric is prioritized, and consequently the design space is narrowed to the $P_{max}/V_{ind} \ge 175$ kW/L category.

The optimal geometrical parameters obtained in the previous analysis can be used to design a custom core. Alternatively, off-the-shelf cores can be selected according to the optimal parameter ranges. For the prototype inductor, two off-the-shelf core options can be found that are close to the optimal core size $c_e = 42$ mm: ELP 43 ($c_e = 43.2$ mm) and ELP 38 ($c_e = 38.1$ mm). The parameters for the two options are provided in Table VI. Both options have acceptable c_w/z_w and $4c_s/c_e$ values. However, the c_d/c_e ratio of both options is only around 0.65, which is well below the optimal range. A better solution can be achieved by stacking multiple cores, and two ELP 43 and three ELP 38 core stacking configurations are selected as the

TABLE VI
PARAMETERS OF ELP 43 AND ELP 38 CORES

Item	ELP 43	ELP 38
c_e	43.2 mm	38.1 mm
c_w/z_w	3–4	3–4
$4c_s/c_e$	0.38	0.40
c_d/c_e	0.64	0.67
c_d/c_e with stacking cores	2 pieces: 1.28	3 pieces: 2.00
P_{max}/V_{ind} (kW/L)	175–185	180–190

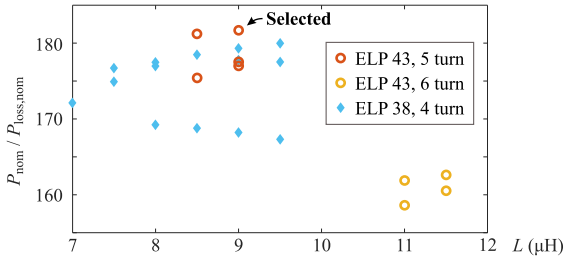


Fig. 17. All of the valid design data points generated in the fine-tuning step, including the selected 9-μH, five-turn ELP 43 design and the other design candidates.

candidates. The remaining parameters to be swept include: n ranging from 3 to 6, copper thickness ranging from 4 to 6 oz, and L ranging from 8 to 12 μH.

In the fine-tuning step, R_{ac} is based on accurate FEA simulations: 2-D FEA for the planar inside-the-core part, and 3-D FEA for the terminal outside-the-core sides, including considerations of the eddy current loss in the cold plates, as discussed in Section IV. Furthermore, the R_{ac} values at up to seventh harmonic frequencies are computed to improve the accuracy. Core losses are modeled using the iGSE method [29], taking into account the triangular flux waveform. For simplicity, the increase of R_{ac} due to the center thermal vias is ignored, and the temperature variation is not considered. Instead, the worst-case temperature (highest for the winding loss, and lowest for the core loss) is used in loss calculations. The lumped thermal resistance model is used for the temperature calculations. Additionally, in consideration of PCB manufacturing practicality and reliability, for design configurations having an odd number of turns, the number of layers is rounded up to an even number, and the bottom layer copper is made open circuit to avoid substantial impact on proximity or fringing effects.

Since the two stacked core options have very similar volume, the power loss metric becomes the key concern, and the $P_{nom}/P_{loss,nom}$ data for all the feasible designs in the fine-tuning step are plotted in Fig. 17. The 9-μH, five-turn, and 5-oz ELP 43 configuration achieves the lowest power loss among all the designs. It is worth noting that since the core option is only suboptimal due to the lower-than-ideal c_d/c_e values, the design has a feasibility cutoff beyond 9 μH because of the flux density limit addressed in Appendix A. While it is possible to achieve a higher peak current by adding more turns, as a consequence the winding loss also increases substantially, leading to lower $P_{nom}/P_{loss,nom}$, as shown by the data points with more turns located in the bottom-right corner in Fig. 17.

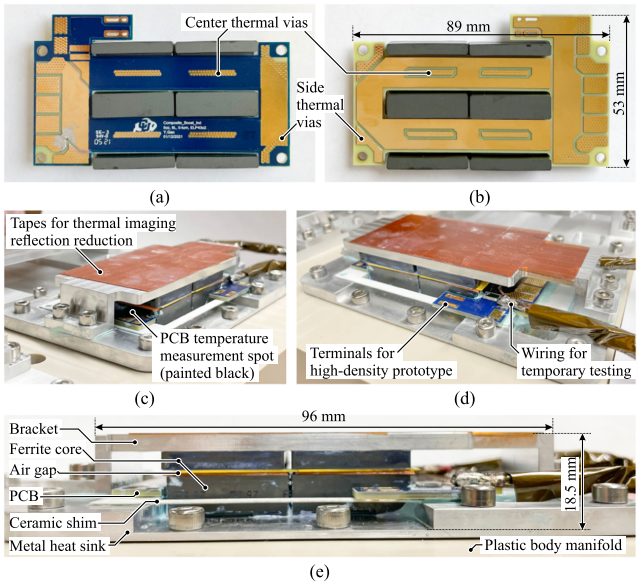


Fig. 18. Inductor prototype. (a) PCB top view. (b) PCB bottom view. (c) View of thermal imaging. (d) View of terminal side. (e) Side view of the assembled inductor.

Finally, the 9-μH, 5-turn, and 5-oz, ELP 43 configuration is selected, which has the best $P_{\text{nom}}/P_{\text{loss,nom}} = 182$. Compared with the ELP 38 options, the selected design has a lower length–width ratio, which is favored in the overall system layout. This design also comes with a wider winding trace so that R_{ac} is less affected by the addition of the center thermal vias. Furthermore, the data point of the selected design in the wide-range sweeping, which is close to the predicted optimal designs, is also highlighted in Fig. 16.

VI. Experimental Validation

The experimental inductor prototype for the 5-turn, 5-oz, and ELP 43 configuration is shown in Fig. 18. To achieve 9-μH inductance, the air gap made from plastic shim stock is set as 1.35 mm. The test results reported in this article are obtained using a large benchtop cold plate. In a future high-density prototype, a more compact double-sided cold plate will be used for both the inductors and the power modules. The prototype inductor achieves $P_{\text{max}}/V_{\text{ind}} = 175.7$ kW/L, where the cold plate manifold and the mounting bolts are excluded in the volume calculation. Additionally, the temperature is measured using a FLIR E6 thermal camera with ± 2 °C accuracy, and the planar PCB as well as the bracket are painted dark to reduce effects of reflections.

A. Converter Operation

The prototype inductor is used in a boost converter having two Cree CPM3-0900-0010 A SiC-MOSFETs (900 V, 10 mΩ) per switch position. The converter is, respectively, tested at the typical and the peak operating points defined in Section II, with the coolant temperature maintained at 25.0 °C. As shown by the measured switch node voltage and inductor current waveforms in Fig. 19, the converter operates in ZVS-QSW mode at the typical point, and falls into hard-switched CCM at the peak point. The steady-state thermal images of the inductor are shown in Fig. 20. Since the PCB inside the core window is not accessible to the thermal camera, the temperature rise of the PCB outside the core window, i.e., region 2 defined in Fig. 8, is taken as a substitute, denoted as $\Delta T_{\text{PCB, region 2}}$. The experimental results are presented in Table VII, showing that the converter achieves 98.8% efficiency at the typical point, and is thermally capable of operation at the peak point. The measured temperature rise values are closely matching the analytical results based on the lumped thermal model developed in Section IV.

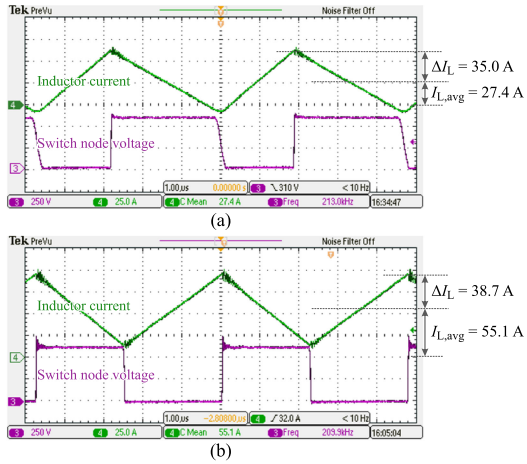


Fig. 19. Inductor current and switch node waveforms in the boost converter operating at (a) typical 9.45-kW point and (b) peak 16.5-kW point.

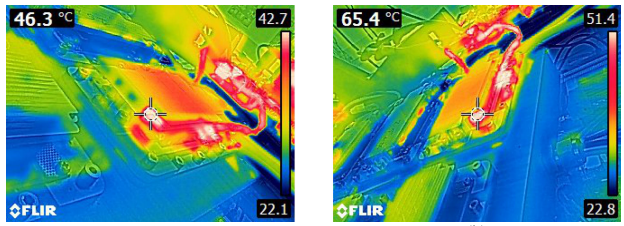


Fig. 20. Steady-state thermal images of the inductor prototype operating at (a) typical 9.45-kW point and (b) peak 16.5-kW point.

TABLE VII
Efficiency and Temperature Measurements of the Boost Converter Using the Inductor Prototype

Items	Typical point	Peak point
Measured V_{in} and V_{out}	351 V / 582 V	301 V / 630 V
Measured power	9.5 kW	16.7 kW
Measured efficiency	98.81%	97.19%
Computed efficiency	98.90%	97.55%
Computed winding loss	32.0 W	68.0 W
Computed maximum ΔT_{PCB}	26.5 °C	56.5 °C
Computed $\Delta T_{\text{PCB, region 2}}$	20.7 °C	43.1 °C
Measured $\Delta T_{\text{PCB, region 2}}$	21.3 °C	40.4 °C
Computed maximum ΔT_{core}	12.2 °C	18.9 °C
Measured ΔT_{core}	14.4 °C	18.6 °C

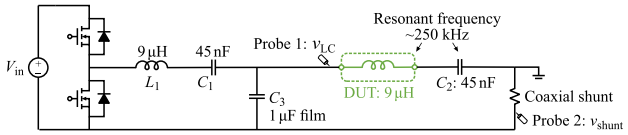


Fig. 21. *LC* resonance setup for ac resistance calibration.

TABLE VIII
EXPERIMENTALLY MEASURED AC RESISTANCE AT 25 °C

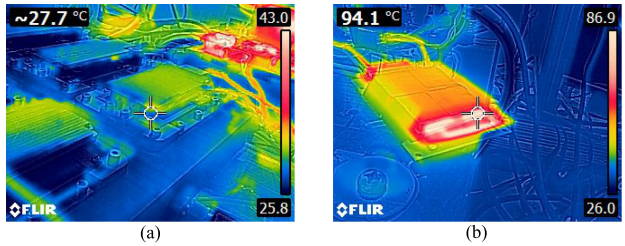
Item	With the cold plate	Passively cooled
Frequency	248.2 kHz	255.7 kHz
First harmonic current	8.25 A	8.20 A
Measured loss in LC tank	4.99 W	4.17 W
Computed core & ESR losses	1.76 W	1.79 W
AC ohmic loss	3.23 W	2.37 W
AC resistance (measured)	47.5 mΩ	35.4 mΩ
AC resistance (FEA)	46.2 mΩ	38.9 mΩ
AC resistance (analytical)	-	34.1 mΩ

B. AC Resistance Calibration

To calibrate the ac resistance at a certain frequency, a testing setup is constructed based on the *LC* resonance concept [30], [31], as shown in Fig. 21, where L_1 is identical to device under test (DUT), and C_1 and C_2 are the resonant capacitors. When the half bridge is switched at the resonant frequency f_r, a sinusoidal current with very little harmonics is obtained, and the ac resistance at f_r can be found according to the inductor power loss computed based on voltage and current measurements. The current is measured by a voltage probe across a coaxial shunt connected in series, which generally offers better precision than current probes. The voltage across the *LC* tank is dominated by the active power component so that the power loss can be measured accurately. Finally, the equivalent ac resistance is found by subtracting the core loss computed using the Steinmetz equation, and the loss due to the equivalent series resistance (ESR) of C_2 .

The inductors with and without the cold plate are, respectively, deployed as the DUT. For fair comparison, the operation time is minimized to keep the inductor temperature rise under 5 °C in both cases. The measurement results, as detailed in Table VIII, generally match well with the FEA results, with errors being less than 10%. The prototype with the cold plate turns out to have higher equivalent ac resistance, which validates the arguments presented in Section IV.

To further compare the proposed inductor prototype with the passive cooling solution, the two inductors along with the resonant capacitors are all connected in series, and a 12-A rms, 250-kHz current excitation is applied to both inductors by powering up the half bridge. According to the thermal images shown in Fig. 22, the passively cooled inductor has more than 65 °C of temperature rise on both the PCB and the core, which exceeds the design limit, whereas with the proposed cooling solution, the temperature rise is less than 3 °C, even though the loss is expected to be slightly higher. The thermal results demonstrate the necessity of the proposed thermal management solutions for planar inductors in high power applications.



(a) (b)

Fig. 22. Steady-state thermal images of the inductors carrying 12-A, 250-kHz current with (a) proposed cooling solution and (b) passive cooling.

C. Limitations and Future Directions

This work is focused on the design optimization of high-power high-current-ripple planar inductors based on advances in approximate winding loss modeling, thermal design strategies, and sweeps over wide ranges of design parameters. Limitations of the approach and potential future directions can be summarized as follows.

1) The proposed approximate model overcomes limitations of conventional 2-D models, and successfully captures the impact of a number of design parameters, including the z_w/c_w, on the winding loss. However, the model performance with respect to other factors, such as the air-gap length and the number of turns, warrants further analysis and verification.
2) The proposed modeling approach is focused on the winding losses and the impact of the core geometrical parameters. As noted in Section II, only the N87 core material is considered as a representative. The optimization approach can be easily extended to treat the choice of the core material as a sweeping parameter.
3) While the impact of the cold plate and the center vias to the ac resistance is examined in one case study, which shows that this impact is negligible in the wide-range sweeping step, a more exhaustive 3-D FEA analysis would be required to validate this more generally.
4) The optimization process presented in this work is focused on the electrical design. Thermal management strategies are taken into account, but the thermal design variables are not swept in the design optimization process. Using the models proposed in Section IV, the approach can be extended to a more general optimization that would also sweep over the thermal design variables, such as the thickness of the FR4 layers, and the number of center vias.

VII. CONCLUSION

This article is focused on enhanced modeling, thermal management, and electro-thermal design optimization techniques aimed at scaling planar magnetics to switched-mode power converter applications at relatively high power levels in the tens of kilowatt range. A case study considered is the design of a high-current-ripple planar inductor for an SiC-based boost converter intended for electric-vehicle drivetrain applications with liquid cooling. Electrothermal design optimization based on power density and efficiency metrics, which is performed by

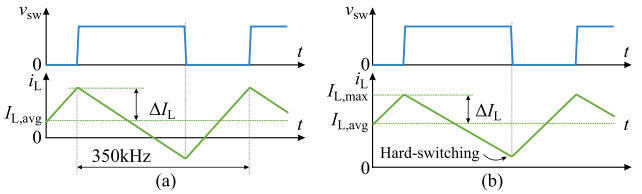


Fig. 23. Two exceptions when the converter operates in CCM instead of ZVS-QSW. (a) Switching frequency exceeding the limit. (b) Peak flux density exceeding the limit.

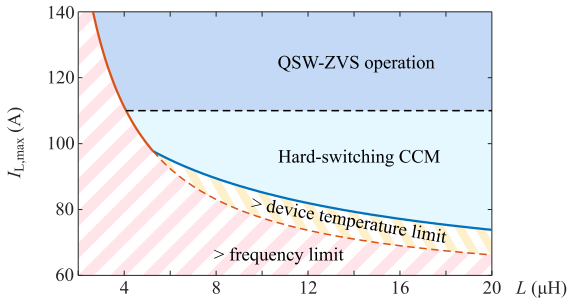


Fig. 24. Feasibility at the worst-case operating point considering frequency and power device temperature limits, with respect to inductance and maximum inductor current specifications.

sweeps over wide ranges of design parameters, requires accurate yet computationally viable models for ac winding losses and for thermal management.

The accuracy of ac winding loss modeling is notably improved by the introduction of a 2-D axisymmetric model, which correctly takes into account current distribution and ac winding losses in the portion of the planar PCB windings outside the core. Furthermore, an approximate ac winding loss model is developed, which achieves substantially better accuracy compared to the conventional 1-D model by including the fringing effect, while being substantially faster to compute compared with finite-element based models. In pursuit of high power density, a series of thermal management enhancement strategies are proposed, improving the power density of the inductor by 2.5–3 times compared to standard-practice solutions. A lumped thermal resistance model is also developed to enable computationally efficient thermal analysis in the design optimization process.

With the proposed modeling and thermal management strategies, comprehensive optimization is conducted for the inductors in a 66-kW four-phase SiC boost converter, and general guidelines are developed regarding the optimal core dimensions for high-power, high-current-ripple planar inductors. In the case study considered, the optimized solution is a 9 μH, five-turn, and ELP 43-based inductor. Featuring $P_{\max}/V_{\text{ind}} = 175.7$ kW/L power density, the design is experimentally verified on a 98.8% efficient converter prototype, which exhibits less than 60 °C of worst-case temperature rise with a winding loss of 68 W in full power operation.

Appendix A

Operating Modes

While the case-study converter is primarily designed for ZVS-QSW operation, CCM operation is occasionally required, as explained in the following.

1) Frequency Limit: The converter is forced to operate in high-current-ripple CCM when the switching frequency necessary for ZVS-QSW operation exceeds a limit, as illustrated in Fig. 23(a). This limit is imposed by the gate driver temperature limit, which is directly caused by the gate-driver power loss that is proportional to the switching frequency. In the experimental prototype converter, the limit is set to 350 kHz.

2) Flux Density Limit: The converter is forced to operate in hard-switched CCM when the peak current in ZVS-QSW operation exceeds a maximum inductor current limit $I_{\text{L,max}}$, which is set by the saturation flux density. Although the system efficiency drops substantially under hard-switching conditions, this CCM operation is still acceptable over short periods of time, and only at the worst-case operating point. In automotive drivetrain applications, efficiency at light to medium load conditions is of the greatest concern. However, with the large amount of power loss, the hard-switching operation should also meet the thermal limit of the power devices. To evaluate the design limit of $I_{\text{L,max}}$ versus inductance, a curvefitted model for hard switching energy loss $E_{\text{loss,sw}}$ is developed based on experimental measurements on a double-pulse setup

$$E_{\text{loss,sw}}(\mu\text{J}) \approx 55(\mu\text{J}) + 0.79V_{\text{ds}}(\text{V}) - 5.6I_{\text{d}}(\text{A}) + 0.043[V_{\text{ds}}(\text{V})][I_{\text{d}}(\text{A})] + 0.044[I_{\text{d}}(\text{A})]^2 \quad \text{(A1)}$$

and the junction temperature rise ΔT_{j} of the specific bottom device follows:

$$\Delta T_{\text{j}} \approx 0.45^{\circ}\text{C/W} \times \left(E_{\text{loss,sw}} f_{\text{s}} + (I_{\text{L,avg}}^2 + \Delta I_{\text{L}}^2/3) D R_{\text{on}}\right) \quad \text{(A2)}$$

where D, R_{on} are, respectively, the bottom switch duty cycle, and the on-resistance of the SiC-MOSFET, which is 5 mΩ in the prototype system.

By using the above device models, feasibility at the the 16.5-kW worst-case operation with respect to inductance and maximum inductor current specifications can be developed, as shown in Fig. 24. The feasible design range, which is shown as the blue area in Fig. 24 is considered in the parameter sweeps during optimization.

Appendix B

Approximate Model for the AC Resistance

Following the modeling approach discussed in Section III, approximate analytical expressions are derived here for the ac resistances associated with the portion of the winding inside the core (2-D planar model), and outside the core (2-D axisymmetric model).

A. 2-D Planar Model: Starting with the 1-D model with only proximity effects taken into account, on the top layer, the per-unit power loss in the x-direction is [8]

$$P_{\text{ac}}(x) = P_{\text{dc}}\varphi\left((F_1^2(x) + F_2^2)G_1(\varphi) - 4F_1(x)F_2G_2(\varphi)\right) \quad \text{(B1)}$$

where

$$P_0 = I^2 R_{\text{dc}}/x_{\text{w}}, \quad \varphi = t_{\text{cu}}/\delta, \quad \delta = \sqrt{\rho/\pi\mu_0 f}$$
$$F_1(x) = n, \quad F_2 = (n-1)$$
$$G_1(\varphi) = \frac{\sinh(2\varphi)+\sin(2\varphi)}{\cosh(2\varphi)-\cos(2\varphi)}$$
$$G_2(\varphi) = \frac{\sinh\varphi\cos\varphi+\cosh\varphi\sin\varphi}{\cosh(2\varphi)-\cos(2\varphi)} \tag{B2}$$

and t_{cu}, ρ, and f, respectively, denote the copper layer thickness, copper resistivity, and frequency.

Considering the approximate current distribution discussed in Section III and plotted in Fig. 4(a), a modification of the 1-D model can be developed, which is to convert $F_1(x)$ into a segmental linear function. For simplicity, the lateral gap between the winding and the core is ignored, i.e., $c_{\text{w}} = x_{\text{w}}$. Depending on the relationship between x_{w} and z_{w}, three cases are considered as follows. If $x_{\text{w}} \geq 4z_{\text{w}}$

$$F_1(x) = \begin{cases} -\dfrac{x_{\text{w}}n}{4z_{\text{w}}^2}x + \dfrac{x_{\text{w}}n}{2z_{\text{w}}}, & 0 \leq x \leq 2z_{\text{w}} \\ 0, & 2z_{\text{w}} \leq x \leq x_{\text{w}} - 2z_{\text{w}} \\ -\dfrac{x_{\text{w}}n}{4z_{\text{w}}^2}(x_{\text{w}}-x) + \dfrac{x_{\text{w}}n}{2z_{\text{w}}}, & x_{\text{w}} - 2z_{\text{w}} \leq x \leq x_{\text{w}}. \end{cases} \tag{B3}$$

On the other hand, if $4z_{\text{w}} < x_{\text{w}} < 4z_{\text{w}}$

$$F_1(x) = \begin{cases} -\dfrac{x_{\text{w}}n}{4z_{\text{w}}^2}x + \dfrac{x_{\text{w}}n}{2z_{\text{w}}}, & 0 \leq x \leq x_{\text{w}} - 2z_{\text{w}} \\ -\dfrac{x_{\text{w}}^2 n}{4z_{\text{w}}^2} + \dfrac{x_{\text{w}}n}{z_{\text{w}}}, & x_{\text{w}} - 2z_{\text{w}} \leq x \leq 2z_{\text{w}} \\ -\dfrac{x_{\text{w}}n}{4z_{\text{w}}^2}(x_{\text{w}}-x) + \dfrac{x_{\text{w}}n}{2z_{\text{w}}}, & 2z_{\text{w}} \leq x \leq 4x_{\text{w}}. \end{cases} \tag{B4}$$

Finally, if $x_{\text{w}} \leq 2z_{\text{w}}$, the fringing effect becomes relatively small as the field produced by the left and the right gaps cancel each other out, leading to

$$F_1(x) = n. \tag{B5}$$

By combining (9)–(11) with (7), the equivalent ac resistance $R_{\text{ac,in}}$ of the top layer is derived as

$$R_{\text{ac,in}} = \frac{1}{I^2}\int_0^{x_{\text{w}}} P_{\text{ac}}(x)\text{d}x$$
$$= R_{\text{dc,in}}\varphi\left[\left(kn^2+(n-1)^2\right)G_1(\varphi) - 4n(n-1)G_2(\varphi)\right] \tag{B6}$$

where

$$k = \begin{cases} \dfrac{x_{\text{w}}}{3z_{\text{w}}}, & x_{\text{w}} \geq 4z_{\text{w}} \\ \dfrac{5x_{\text{w}}^3}{96z_{\text{w}}^3} - \dfrac{x_{\text{w}}^2}{2z_{\text{w}}^2} + \dfrac{11x_{\text{w}}}{8z_{\text{w}}} - \dfrac{1}{3}, & 2z_{\text{w}} < x_{\text{w}} < 4z_{\text{w}} \\ 1, & x_{\text{w}} \leq 2z_{\text{w}}. \end{cases} \tag{B7}$$

B. 2-D Axisymmetric Model: In the curved planar winding outside the core in the 2-D axisymmetric model, the normalized dc current density in the r direction is

$$\tilde{J}_{\text{dc}}(r) = \frac{1}{r}\log^{-1}\frac{r_{\text{in}}+x_{\text{w}}}{r_{\text{in}}}. \tag{B8}$$

In the high-frequency ac scenario, as the winding is affected by a perpendicular field produced by the current flowing through the winding itself, it is observed that the current distribution on the top surface of the top layer becomes

$$\tilde{J}_{\text{ac}}(r) = \frac{1}{r-r_0}\log^{-1}\frac{r_{\text{in}}+x_{\text{w}}-r_0}{r_{\text{in}}-r_0} \tag{B9}$$

where r_0 is very close to r_{in}, and is empirically set as

$$r_0 = 0.975 r_{\text{in}}. \tag{B10}$$

The same applies to the bottom surface of the bottom layer.

Starting with the 1-D model, when considering the ac effect, the power loss density in the top layer along the r-axis is modified as

$$P_{\text{ac,out}}(r) = P_{\text{dc}}(r)\varphi \cdot \left((F_1^2(r)+F_2^2)G_1(\varphi) - 4F_1(r)F_2G_2(\varphi)\right) \tag{B11}$$

where

$$P_{\text{dc}}(r) = \frac{2\pi\rho}{k_1^2 t_{\text{cu}}}\frac{I^2}{r}, \quad F_1(r) = nk_{\text{j}}(r), \quad F_2 = n/2-1$$
$$k_{\text{j}}(r) = \tilde{J}_{\text{ac}}(r)/\tilde{J}_{\text{dc}}(r) = k_1 r/\left(k_2(r-r_0)\right)$$
$$k_1 = \log\frac{r_{\text{in}}+x_{\text{w}}}{r_{\text{in}}}, \quad k_2 = \log\frac{r_{\text{in}}+x_{\text{w}}-r_0}{r_{\text{in}}-r_0}. \tag{B12}$$

The equivalent ac resistance $R_{\text{ac,out}}$ for the very top and the very bottom layers is found by integration of (17)

$$R_{\text{ac,out}} = \frac{1}{I^2}\int_{r_{\text{in}}}^{r_{\text{in}}+x_{\text{w}}} P_{\text{ac,out}}(r)\text{d}r$$
$$= \left[\left(\frac{n}{2}-1\right)^2 + \frac{k_1k_3n^2}{4k_2^2}\right]\frac{2\pi\rho}{k_1t_{\text{cu}}}\varphi G_1(\varphi) - k_2n(n-2)\frac{2\pi\rho}{k_1t_{\text{cu}}}\varphi G_2(\varphi) \tag{B13}$$

where

$$k_3 = \left(\frac{r_0}{r_{\text{in}}+x_{\text{w}}-r_0} - \frac{r_0}{r_{\text{in}}-r_0}\right) + \log\frac{r_{\text{in}}+x_{\text{w}}-r_0}{r_{\text{in}}-r_0}. \tag{B14}$$

Alternatively, as

$$R_{\text{dc,out}} = \frac{2\pi\rho}{k_1 t_{\text{cu}}} \tag{B15}$$

the solution can be rewritten as

$$R_{\text{ac,out}} = R_{\text{dc,out}}\varphi\left\{\left[\left(\frac{n}{2}-1\right)^2 + \frac{k_1k_3n^2}{4k_2^2}\right]G_1(\varphi) - k_2n(n-2)G_2(\varphi)\right\}. \tag{B16}$$

C. Lumped Thermal Model With Center Thermal Vias

To account for the the center thermal vias, a new region 6 is added to represent the area of the vias. This region is

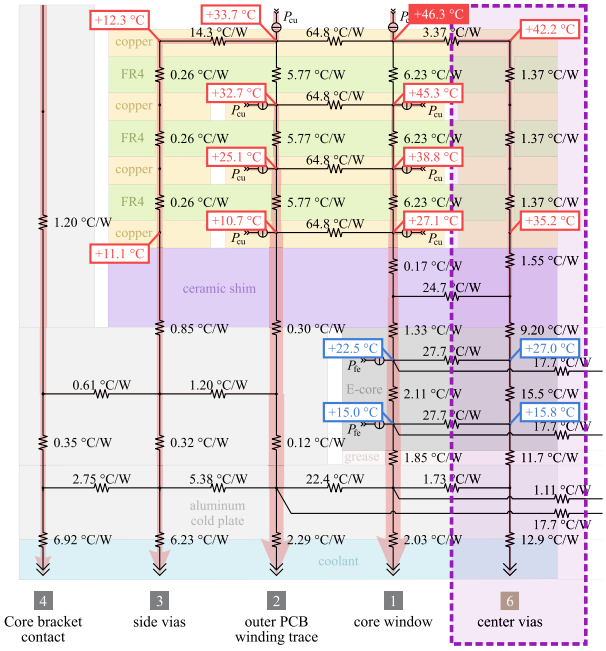


Fig. 25. Modified lumped thermal model with center thermal vias. The portion of the I core is omitted, which is the same, as shown in Fig. 9.

only connected to region 1 in the x-direction. Note that for this connection, the equivalent x-direction thermal resistance is calculated according to the y-direction length of region 6, rather than the length of region 1. With the new region 6, the lumped thermal resistance model can be updated following the same principles as discussed in Section IV, as shown in Fig. 25. One modification is that the x-direction thermal resistance of the ceramic shim is included between regions 1 and 6, which is comparable to that of the ferrite core.

In Fig. 25, the heat transfer paths are also labeled. The center thermal vias can effectively bring the heat out of the top winding layer, substantially dropping the peak temperature of the PCB. An unfavorable effect of the center thermal vias is that the temperature rise of the E core is increased by about 5 °C, which is still acceptable for the considered case. Nevertheless, while this effect may become a problem for designs with high core loss, the center thermal vias strategy is still generally beneficial, as it enables designs with high winding loss, which is clearly shown in Fig. 13 of Section IV.

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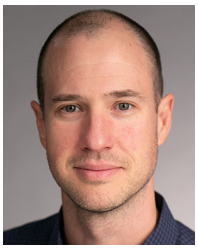

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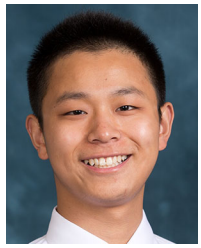

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