Implementing Symmetrical Structure in MOV-RCD Snubber-Based DC Solid-State Circuit Breakers

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***Abstract*—This article deals with metal-oxide varistor (MOV) and resistor–capacitor–diode (RCD) snubber-based solid-state circuit breakers (SSCBs). There are two main contributions. First, a design methodology of MOV-RCD snubber parameters is proposed by considering thermal dissipation and snubber charging time for the first time. The thermal profile of the main conduction switches determines nominal current under passive cooling. Based on the nominal current, the fault current magnitude is derived, and a design method of key parameters of an MOV-RCD snubber is proposed. Four snubbers are designed with different fault currents and dc voltages. Second, symmetrical layouts with distributed parallel cells are proposed for high current capability, which enables scalability. Q3D simulations facilitate the evenly distributed stray inductances among paralleled branches. Both low- and medium-voltage SSCBs are implemented, ranging from 500 V/300 A to 2 kV/1 kA. The power density achieves 37.8 kW/L at 500 V/1 kA. Experiments demonstrate that the reverse voltage reaches 4.88 kV with an ultrafast interruption speed of 24 μs for 2 kV/1.144 kA fault current including the MOV conduction time interval.**

***Index Terms*—DC power system, metal-oxide varistor (MOV), resistor–capacitor–diode (RCD) snubber, solid-state circuit breaker (SSCB).**

I. Introduction

DC POWER grids have been adopted in various applications, such as electric ship and aircraft propulsion systems [1]–[3]. Other than the traditional ac power systems, dc systems lack natural current zero-crossings, and dc circuit breakers (DCCBs) are important to clear faults. Solid-state circuit breaker (SSCB) is a promising solution, which enables a high interrupting current with high efficiency at fast response speed within microseconds [4]–[6].

However, a high *di*/*dt* is usually generated during turn-OFF [4]. Due to the transmission line inductance and current limiting line inductors, huge inductive energy is applied across main switches and generates serious *dv*/*dt* and overvoltage. It might exceed device rating and cause failure [7]. Also, a high *dv*/*dt* can induce gate oscillation, gate-oxide degradation, and false turn-ON, causing reliability and lifetime issues [8], [9].

Zaman *et al.* [10] propose to reduce gate oscillation by adding gate resistances or ferrite beads. Liu *et al.* [11] propose to use a gate capacitance to reduce oscillation. These measures have limitations, such as slowing down device speed [12]. Recently, negative voltage turn-OFF [13] and active Miller clamping [14] have been applied to suppress oscillations. However, extremely high *dv*/*dt* still presents a risk of failure even with those designs. To cut the problem at its root, a well-designed voltage clamping circuit, also known as a snubber, should be adopted in SSCBs to avoid high *dv*/*dt* during turn-OFF [4]. The snubber utilizes energy-absorbing components to reduce *dv*/*dt* and energy-dissipating components to clamp overvoltage across devices [4]. For an SSCB, attention should be paid to the *dv*/*dt* suppression capability and fast speed during current interruption.

Various snubber configurations have been reported in SSCBs [4], [15]–[23]. In [15], metal-oxide varistor (MOV) and pure capacitor (C) snubbers are applied to suppress the turn-OFF overvoltage, and the effects of capacitance values on the voltage suppression capability are analyzed. But the major concern in a pure C-type snubber is the generated high discharge current during reclosing process [4]. A snubber resistor in series with the capacitor can reduce the discharge current [16], and an MOV in parallel with an RC snubber considerably reduces the required capacitance [17], [18].

However, in an RC snubber, the voltage across the resistor during turn-OFF is also applied on main switches, which leads to an extra voltage stress and power shock [4], [19]. Alternatively, a resistor-capacitor-diode (RCD) snubber can separate charging and discharging paths [4], [19]–[26]. Wu *et al.* [19] compare turn-OFF transients of IGCT based on RC and RCD snubbers in terms of transient power shock and overvoltage suppression. Berg *et al.* [20] analyze an MOV-RCD snubber using analytical investigations, where the short circuit current capability, clearance time, and transient power shock are considered. A 10-kV press-pack IGBT-based SSCB is used in [21], and RCD snubbers can reduce the overvoltage. Liu *et al.* [22] introduce three RCD configurations in a low-voltage dc (LVdc) microgrid. Giannakis and Peftitsis [23] propose the performance evaluation of three different overvoltage suppression circuits, including an RCD circuit employed in a SSCB for low- and medium-voltage dc grids. In [24], an RCD snubber is adopted with an

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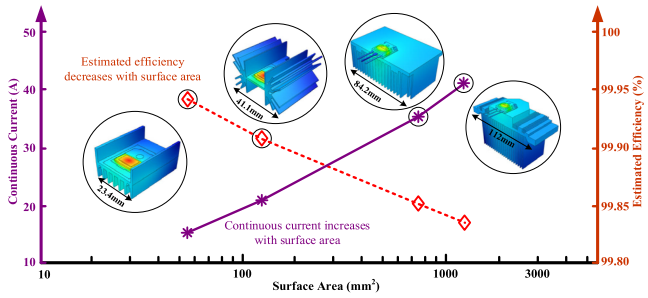

Fig. 1. FEA simulated SSCB continuous current and efficiency versus heatsink area.

MOV to provide a voltage clamping function in an IGBT-based SSCB.

In a dc system, short-circuit fault current magnitude ranges typically 2–10 times of rated current [27], [28]. Recent research on snubbers focuses on short-term fault current protection with high magnitude but ignores long-term thermal capability of main conduction devices under nominal current, which should be considered in a practical SSCB. This article proposes a design methodology of MOV-RCD snubber considering both nominal and fault current magnitudes. There are two major contributions. First, the thermal dissipation capability under nominal current and the reaction speed under fault current are identified as critical design criteria. Second, symmetrical main conduction layouts with distributed snubbers/conduction cells are proposed for high current capability, which also enables scalability and efficiency enhancement.

II. Thermal Capability Oriented Rated Conditions

A. Conflicts Between Thermal Capability and Efficiency

The efficiency of an SCCB [5] at a continuous dc current I_{dc} and a dc voltage V_{dc} is shown in (1). In this article, one thing to note is that (1) is valid specifically for MOSFET-based SSCBs

$$\eta = \left(1 - \frac{P_{cond}}{V_{dc} I_{dc}}\right) \times 100\%, P_{cond} = I_{dc}^2 R_{ds,on}. \quad (1)$$

The conduction loss should be dissipated by a proper cooling system. I_{dc} is limited by the thermal dissipation capability of its cooling approach. To increase I_{dc} for high power density [29], [30], recent research studies cooling systems with high thermal conductivity and heat transfer coefficient, such as forced air and liquid cooling [31]. Although these state-of-art cooling approaches are effective, there is a critical conflict with efficiency.

Fig. 1 provides an example to explain the conflict. Various heatsinks with different surface areas are adopted for natural passive cooling. Finite-element analysis (FEA) is performed to derive heat dissipation when rendering the same steady-state junction temperature below 100 °C ($R_{ds,on}$ = 20.8 mΩ). With an increasing of heatsink area, I_{dc} increases from 15.3 to 40.3 A, which reduces SSCB efficiency from 99.94% to 99.83% based on (1). The same trend can be applied to parallel switch-based SSCBs. This conflict reveals that using cooling approaches to improve current conduction capability is not always good solution since it negatively impacts the efficiency of an SSCB, which is not desired. Therefore, this article aims to propose a new design methodology for SSCBs based on predetermined thermal dissipation capability.

B. Continuous Current Based on Heat Dissipation Capability

Table I provides four examples to show the design process of continuous rated current based on heat dissipation capability. This design procedure and thermal analysis are suitable for both discrete device- and module-based SSCBs.

1) SSCB #1 Based on Single Discrete MOSFET: A single 1.2 kV SiC MOSFET (C3M0016120D) is used in a 500-V dc bus. When the generated heat is 25 W, Fig. 2(a) shows the FEA-simulated heatsink surface temperature.

Fig. 3(a) shows the cross-sectional temperature distribution of the MOSFET, including the internal multilayer materials. The maximum steady-state temperature is limited to 92 °C, implying the heat dissipation capability of the heatsink is sufficient for 25-W internal heat. Given a safety margin and $R_{ds,on}$ = 20.8 mΩ, the rated current is selected as 30 A. The estimated efficiency of the SSCB achieves 99.88%.

2) SSCB #2 Based on Four Paralleled Discrete MOSFETS: Four MOSFETS are parallel in a 500-V dc system. Each one generates 6.25-W heat, resulting in a total of 25 W. Fig. 2(b) shows the simulated heatsink surface temperature.

Fig. 3(b) shows that the internal temperature is limited within 80 °C in the steady state, implying the four distributed heatsinks are capable to handle 25 W. Given a safety margin and $R_{ds,on}$ = 20.8 mΩ, the rated current is selected as 15 A for each switch, resulting in a total current of 60 A and efficiency of 99.94%.

3) SSCB #3 Based on Ten Paralleled Discrete MOSFETS: Ten MOSFETS are parallel in a 500-V dc system. Each one generates 2.5-W heat, resulting in a total of 25 W. Fig. 2(c) shows the simulated heatsink surface temperature.

Fig. 3(c) shows that the internal temperature is limited within 65 °C in the steady state, validating a heat dissipation capability of 25 W. Given a safety margin and $R_{ds,on}$ = 17.6 mΩ at 65 °C, the rated current selected as 10 A for each switching, resulting in a total current of 100 A and efficiency of 99.96%.

4) SSCB #4 Based on 3×3 Series-Parallel SiC Modules: In a 2-kV dc bus, 3×3 series-parallel 1.2-kV SiC modules (CAB450M12XM3), instead of discrete devices, are adopted. When the generated heat of each module is 25 W, Fig. 2(d) shows the simulated heatsink surface temperature.

Fig. 3(d) shows the cross-sectional temperature distribution of the module. The maximum steady-state temperature is limited to 55 °C, implying the heat dissipation capability of the heatsink is sufficient for 25 W. Given a safety margin and $R_{ds,on}$ = 4.07 mΩ at 60 °C, the rated current of each module is selected as 33.3 A. For a 3×3 series-parallel SSCB, the continuous rated current is 100 A, and the estimated efficiency is 99.96%.

As summarized in Table I, the rated current values provide important basis for snubber design in Section III.

TABLE I
SPECIFICATIONS OF SSCBS AT CONTINUOUS RATED CONDITIONS

No.	Series-Parallel Configuration	DC Bus Voltage (V)	Total Heat Dissipation (W)	Distributed Heat Dissipation (W)	Total Rated Current (A)	Distributed Rated Current (A)	Efficiency (%)
#1	1×1	500	25	25	30	30	99.88
#2	1×4	500	25	6.25	60	15	99.94
#3	1×10	500	25	2.5	100	10	99.96
#4	3×3	2000	225	25	100	33.3	99.96

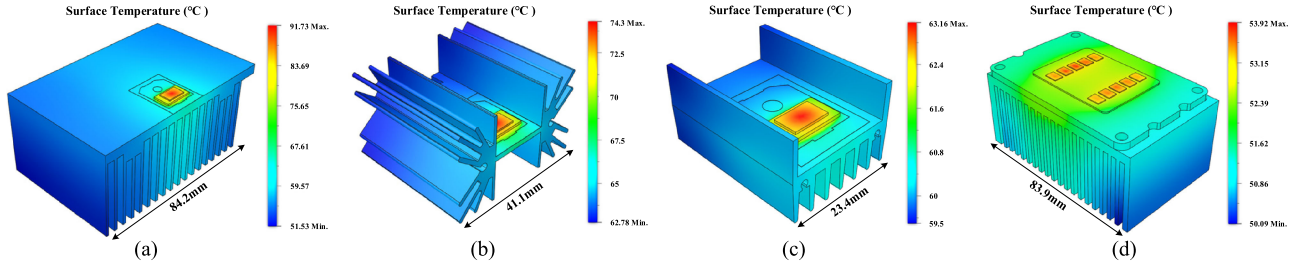

Fig. 2. Simulated surface temperature profile. (a) Discrete MOSFET 25 W. (b) Discrete MOSFET 6.25 W. (c) Discrete MOSFET 2.5 W. (d) Module 25 W.

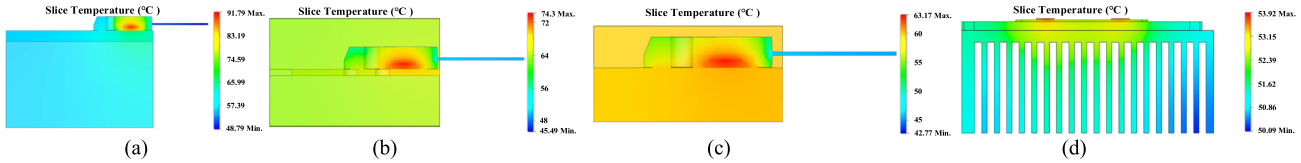

Fig. 3. Simulated slice temperature profile. (a) Discrete MOSFET 25 W. (b) Discrete MOSFET 6.25 W. (c) Discrete MOSFET 2.5 W. (d) Module 25 W.

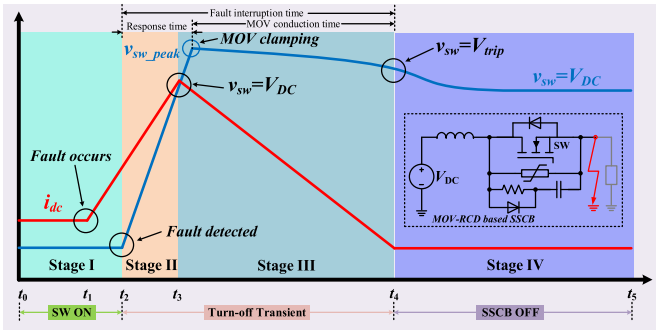

Fig. 4. Working stages of an MOV-RCD snubber-based main conduction path.

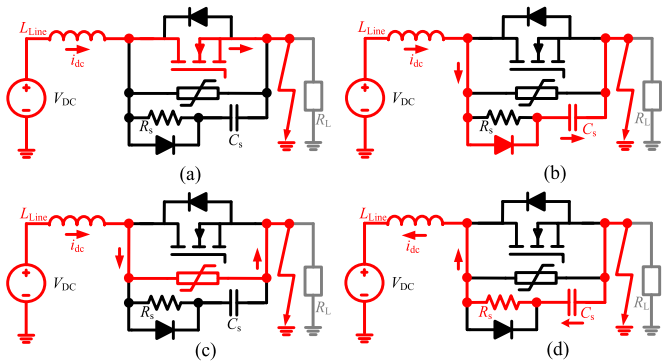

Fig. 5. Equivalent circuit of an MOV-RCD snubber during turn-OFF transient. (a) Stage I. (b) Stage II. (c) Stage III. (d) Stage IV.

III. MOV-RCD SNUBBER ENABLED FAULT PROTECTION

A. Circuit Description

In this design, an MOV-RCD snubber is adopted to absorb the fault energy. The circuit topology and working principle are shown in Figs. 4 and 5, explained as follows [25], [26].

Stage I (t_0-t_2): From t_0 to t_1, the SSCB works in a normal mode. At t_1, a fault occurs, and the current i_{ft} increases rapidly.

Stage II (t_2-t_3): At t_2, the main switch turns OFF, and current i_{ft} commutates to charge C_s. At t_3, $v_{sw}= V_{dc}$, i_{ft} reaches the peak.

Stage III (t_3-t_4): MOV conducts, i_{ft} commutates to the MOV branch, and the voltage is clamped. The inductive energy in L_{Line} dissipates in MOV and i_{ft} decreases to zero at t_4.

Stage IV (t_4-t_5): The snubber capacitor C_s discharges through the resistor and L_{Line} to the dc bus. v_{sw} gradually decreases from the MOV tripping voltage V_{trip} as shown in Fig. 4.

In this article, the snubber charging time (response time) Δt is defined as the increasing time of v_{sw} from zero to its peak, which is the MOV clamping voltage. On one hand, Δt should be small to achieve a fast response speed. On the other hand, Δt should be large enough to reduce dv/dt during the turn-OFF transient [19]. Therefore, a good snubber design should realize a reasonable Δt for both considerations.

TABLE II
SPECIFICATIONS OF MOV-RCD SNUBBERS AT FAULT CONDITIONS

No.	Series-Parallel Configuration	DC Bus Voltage (V)	Distributed Fault Current (A)	Total Fault Current (A)	Distributed Cs (nF)	Total Cs (nF)	Distributed Rs (Ω)	MOV DC/Clamping Voltage (V)
#1	1×1	500	300	300	300	300	50	560/1060 (V420LT40BP)
#2	1×4	500	150	600	200	800	75	560/1060 (V420LT40BP)
#3	1×10	500	100	1000	100	1000	180	560/1060 (V420LT40BP)
#4	3×3	2000	333	1000	200	200	50	850/1720 (V661HA40)

B. Components Selection of MOV-RCD Snubber

1) MOV Selection: MOV selection depends on both the dc bus voltage and the rating of main switch, as shown in the following:

$$V_c \leq 0.9 \times V_{ds,rating}, V_{M(DC)} \geq 1.1 \times V_{DC}. \quad (2)$$

The clamping voltage V_c should be 10% lower than the switch rating voltage $V_{ds,rating}$ to provide a reliable protection. The MOV continuous dc voltage $V_{M(dc)}$ should be 10% higher than the dc bus voltage to avoid leakage currents [4].

2) Snubber Capacitor Selection: The snubber capacitance can be selected as follows [21], [32]:

$$C_s \approx I_{peak}\Delta t/V_c. \quad (3)$$

It shows that C_s depends on the fault current magnitude, the snubber charging time Δt, and the MOV clamping voltage. In this article, the snubber charging time Δt is selected between 0.5 μs and 2 μs to ensure both a fast speed and a smooth *dv/dt*. With the maximum fault current I_{peak}, clamping voltage V_c, C_s can be derived in (3).

3) Snubber Resistance Selection: In Fig. 5(d), R_s should be slightly larger than the critical damping resistance [20], [23].

$$R_s \geq 2\sqrt{\frac{L_{Line}}{C_s}}, R_s \rightarrow 2\sqrt{\frac{L_{Line}}{C_s}}. \quad (4)$$

With a proper R_s, the voltage oscillation can be prevented and it attenuates exponentially from V_{trip} to V_{dc} with a time constant $2\times L_{Line}/R_s$. R_s cannot be too large to avoid slow discharging that delays the SSCB reclosing. Besides, the reclosing current must be below the pulse current rating of the main switch ($I_{D,\ pulse}$) as in (5). The larger one of (4) and (5) determines the final R_s.

$$R_s \geq V_{DC}/I_{D,pulse}. \quad (5)$$

C. Specifications of MOV-RCD Snubbers

The existing research [19]–[23] mainly focuses on the RCD snubber design in fault conditions, where the magnitude is 10 times of a nominal value [27], [28]. However, an SSCB should have both thermal dissipation capability at a nominal current and interruption capability at a fault current. This article provides a design methodology of SSCBs to interrupt different currents with high speed and efficiency, as summarized in Fig. 6.

Based on Fig. 6, MOV-RCD snubbers can be developed for SSCBs in Table I. The snubber parameters are shown in Table II. To demonstrate these examples, the main conduction layout design and experimental validations are provided as follows.

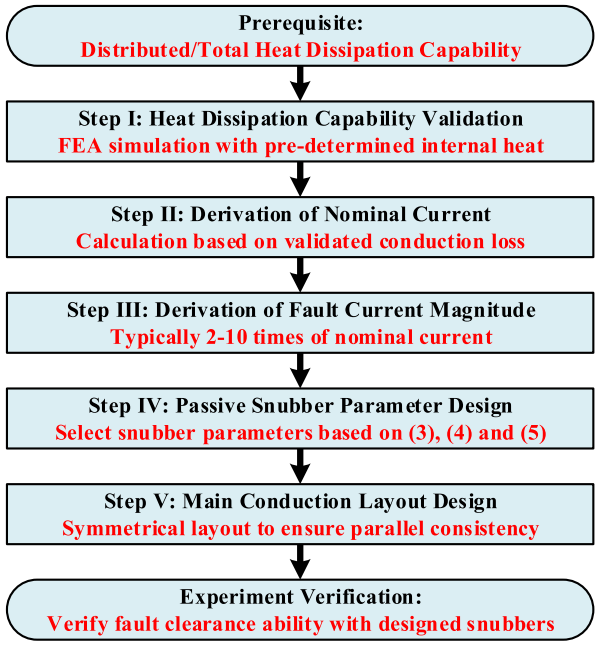

Fig. 6. Flowchart of the proposed MOV-RCD snubber design methodology.

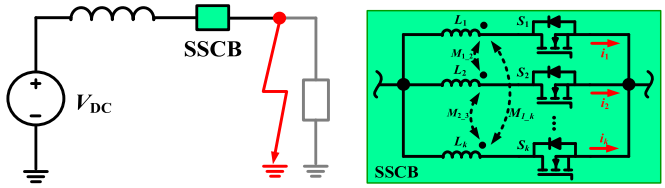

Fig. 7. SSCB based on parallel devices considering stray inductances.

IV. SYMMETRICAL DESIGN OF THE MAIN CONDUCTION LAYOUT

The proposed SSCBs adopt parallel configuration of multiple switches, it is necessary to address the conduction layout issue to ensure good consistency. Therefore, symmetrical layout justification and design procedures are presented. This design process and stray inductance analysis are suitable for both discrete device- and module-based SSCBs.

A. Stray Inductance Analysis

Fig. 7 shows the equivalent circuit of main conduction strings considering stray inductances, which affect current distribution and overvoltage due to *di/dt* [5]. The circuit can be modeled by

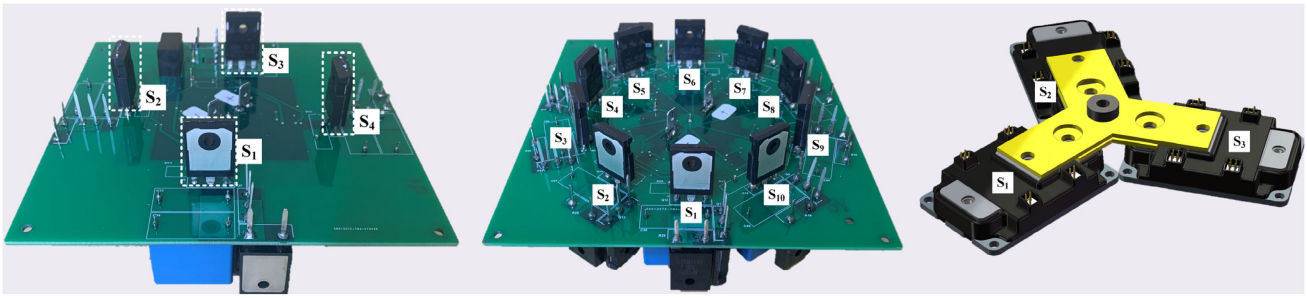

Fig. 8. Main conduction layouts. (a) Four paralleled discrete MOSFETS. (b) Ten paralleled discrete MOSFETS. (c) Three paralleled MOSFET modules.

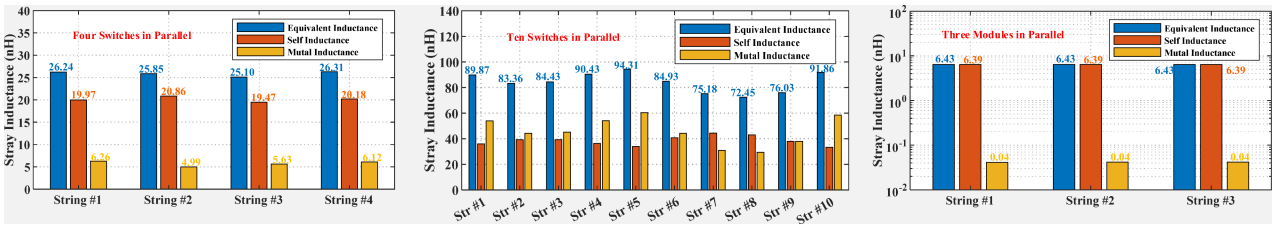

Fig. 9. Q3D simulated stray inductances. (a) Four paralleled discrete MOSFETS. (b) Ten paralleled discrete MOSFETS. (c) Three paralleled MOSFET modules.

the self and mutual inductances as follows:

$$v_{sw} = \begin{bmatrix} L_1 & M_{12} & \cdots & M_{1\_k} \\ M_{21} & L_2 & \cdots & M_{2\_k} \\ \vdots & \vdots & \ddots & \vdots \\ M_{k\_1} & M_{1\_2} & \cdots & L_k \end{bmatrix} \times \begin{bmatrix} di_1/dt \\ di_2/dt \\ \vdots \\ di_k/dt \end{bmatrix} \tag{6}$$

where i_k is the current flowing through the kth string. In a symmetrical layout, there is the following approximation

$$di_1/dt = di_2/dt = \cdots = di_k/dt. \tag{7}$$

Substituting (7) into (6), the decoupled stray inductance of each string is described in the following:

$$L_{eq\_j} = L_j + \sum_{i=1, i\neq j}^{k} M_{i\_j} \tag{8}$$

where L_{eq_j} represents the equivalent stray inductances in the jth string. It provides a significant revelation that both self and mutual inductances contribute to the total stray inductance. Then, the current in the jth string is calculated as follows:

$$\begin{aligned} V_{DC} &= L_{Line} \cdot di_{ft}/dt + L_{eq\_j} \cdot di_j/dt \\ i_j(t) &= \frac{V_{DC} - L_{Line} \cdot di_{ft}/dt}{L_{eq\_j}} \cdot t + i_j(0) \end{aligned} \tag{9}$$

where $i_j(0)$ represents the kth string nominal current before the fault. Equations (8) and (9) reveal that the symmetrical layout is a promising solution for a good current sharing because it can realize consistency of the stray inductances.

In this article, three different layouts are studied as in Fig. 8: four-parallel and ten-parallel of discrete MOSFETS, and three-parallel power modules. All designs adopt a symmetrical layout to ensure an evenly distributed stray inductance in each string.

1) Four Paralleled Discrete MOSFETS: Fig. 8(a) shows the layout of four parallel switches (S_1–S_4) that are symmetrically distributed. L_1–L_4 are regarded as stray self-inductances of main conduction strings. Fig. 9(a) shows the equivalent inductance L_{eq_k}, self-inductance L_k, and the sum of mutual inductances in four strings, which are extracted by ANSYS Q3D at 1 MHz. The average equivalent inductance is 25.87 nH with a maximum deviation of 3%. It validates that the symmetrical layout achieves good consistency among four conduction paths with low stray inductances.

2) Ten Paralleled Discrete MOSFETS: Fig. 8(b) shows the layout of ten parallel strings (S_1–S_{10}) that are symmetrically distributed. L_1–L_{10} are considered as the stray self-inductances. Fig. 9(b) shows equivalent inductances acquired by Q3D. The average equivalent inductance is 84.28 nH with a maximum deviation of 14%, validating an acceptable consistency. Compared with the four-parallel case, it shows that with more strings in parallel, the equivalent inductance of each string increases due to the mutual inductances.

3) Three Paralleled SiC Modules: Fig. 8(c) shows a symmetrical layout of three parallel power modules (S_1–S_3), and L_1–L_3 stand for the stray self-inductances. Fig. 9(c) shows simulated inductances from Q3D, indicating good consistency among various strings. It is because this design is a strictly coaxial symmetrical layout, which makes the difference between multiple paths extremely slight. One thing to emphasize is that this layout is based on SiC modules instead of discrete devices.

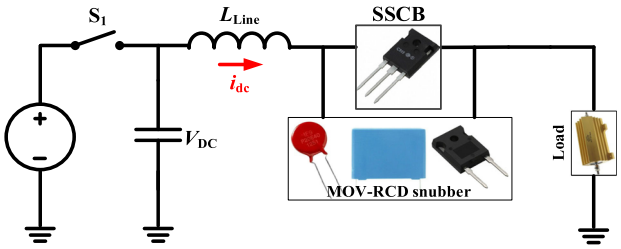

Fig. 10. Circuit topology of implemented dc current interruption testing platform.

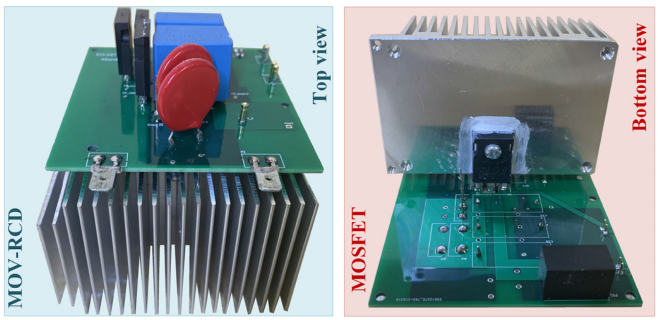

Fig. 11. 500 V/300 A SSCB prototype based on a single MOSFET switch.

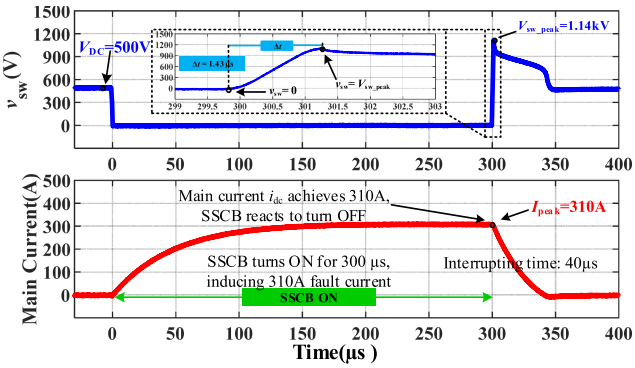

Fig. 12. Experimental waveform of a single-MOSFET SSCB to interrupt 310-A current with 500-V dc bus voltage, 63 μH line inductor, and 1.6-Ω load resistor.

V. Experiments: Fault Current Interruption Test

A. 500 V/300 A Single-Switch SSCB Interruption Test

Based on Tables I and II, a single-switch SSCB is developed using C3M0016120D. The targeted nominal current is 30 A, and the fault current capability is 300 A in a 500-V dc system.

Fig. 10 shows the dc current interruption testing circuit, and Fig. 11 shows the implemented 500 V/300 A prototype. Snubber parameters follow Table II. A dc source is used to charge a capacitor bank (750 μF); load resistor (1.6 Ω) is used to emulate a fault impedance; and the line inductor L_{Line} is 63 μH.

Fig. 12 shows the measured waveforms to interrupt 310 A with 500-V dc bus voltage. It validates a fast interruption speed. During turn-OFF, the snubber charging time Δt is 1.4 μs. The peak voltage across the switch is clamped by MOV to 1.14 kV, and the current decreases to zero within 40 μs.

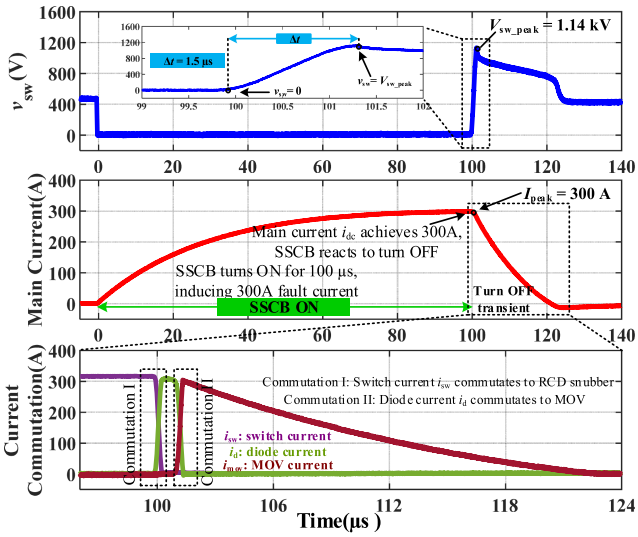

Fig. 13. Experimental waveform of a single-MOSFET SSCB to interrupt 300-A fault current with 36.8-μH line inductor and 1.6-Ω resistor, showing commutation.

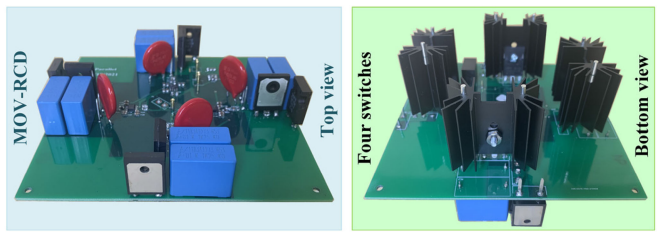

Fig. 14. 500 V/600 A SSCB prototype based on four-parallel MOSFET switches.

Fig. 13 shows the experimental results to emulate a fault current scenario. The line inductance L_{Line} is reduced to 36.8 μH to achieve a fast current ramping rate. The fault current reaches 300 A in 100 μs, and SSCB successfully interrupts the current to zero within 20 μs.

Fig. 13 also provides details of current commutation inside the snubber. In the turn-OFF transient, there are two commutation processes within the MOV-RCD-based SSCB. First, the main switch current i_{sw} rapidly decreases and commutates to charge the snubber capacitor. When i_{sw} reaches zero, commutation I completes. A constant current continues charging the snubber capacitor, and v_{sw} increases rapidly to MOV tripping voltage. Second, the current in capacitor decreases and commutates to MOV, which is defined as commutation II. The residual energy dissipates in MOV. The commutation waveforms in Fig. 13 are also consistent with turn-OFF stages in Figs. 4 and 5.

B. 500 V/600 A Four-Switch Parallel SSCB Interruption Test

Based on Tables I and II, four MOSFETS are connected in parallel to form an SSCB. The targeted nominal current is 60 A and the fault current capability is 600 A.

Fig. 14 shows the implemented 500 V/600 A SSCB prototype. Four distributed MOV-RCD snubbers are placed close to the switches. Fig. 15 shows experimental results to interrupt 600 A

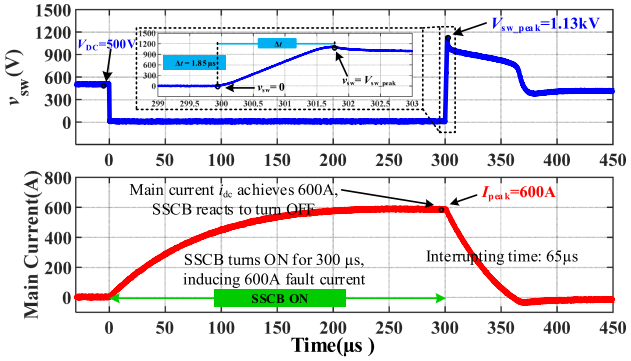

Fig. 15. Experimental waveform of a four-switch SSCB to interrupt 600-A current with 500-V dc bus voltage, 63-μH line inductor, and 0.83-Ω load resistor.

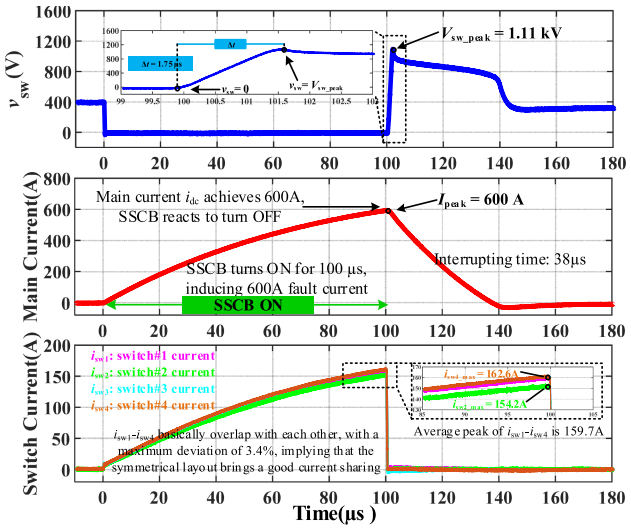

Fig. 16. Experimental waveform of a four-switch SSCB to interrupt 600-A fault current with 36.8-μH line inductor and 0.25-Ω resistor, showing current sharing.

in a 500-V dc system. The line inductor L_{Line} is 63 μH, and the load resistance is 0.83 Ω. The snubber charging time Δt is 1.9 μs. The peak voltage across the switch is clamped by MOV to 1.13 kV, and the current decreases to zero within 65 μs.

Fig. 16 further tests the fast response speed in a fault current scenario. The line inductor L_{Line} is reduced to 36.8 μH, and the load resistance is 0.25 Ω. The fault current increases to 600 A in 100 μs, and the SSCB interrupts it within 38 μs. The currents in four switches (i_{sw1}–i_{sw4}) are also measured, which validates a good consistency, and the current deviation is only 3.4%. It implies that the proposed symmetrical layout realizes current sharing among four parallel switches.

C. 500 V/1000 A Ten-Switch Parallel SSCB Interruption Test

Then, ten MOSFETS are connected in parallel. The nominal and fault current capabilities are 100 A and 1 kA, respectively.

Fig. 17 shows the implemented 500 V/1 kA prototype. The MOV-RCD snubbers are also symmetrically distributed. Fig. 18 shows the experimental results to interrupt 1 kA in a 500-V dc system. The line inductor 63 μH, and the external connected

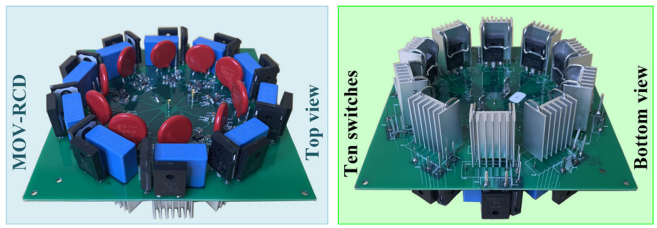

Fig. 17. 500 V/1 kA SSCB prototype based on ten-parallel MOSFET switches.

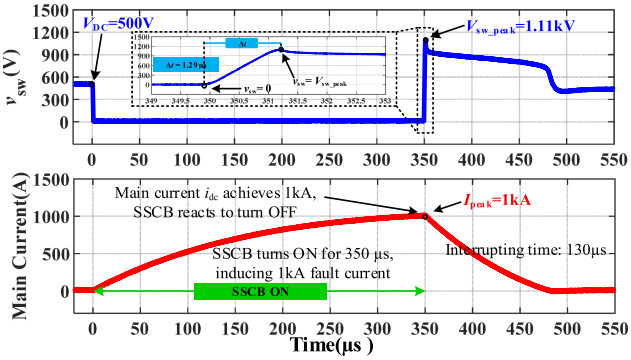

Fig. 18. Experimental waveform of a ten-switch SSCB to interrupt 1-kA current with 500-V dc bus voltage, 63-μH line inductor, and 0.5-Ω load resistor.

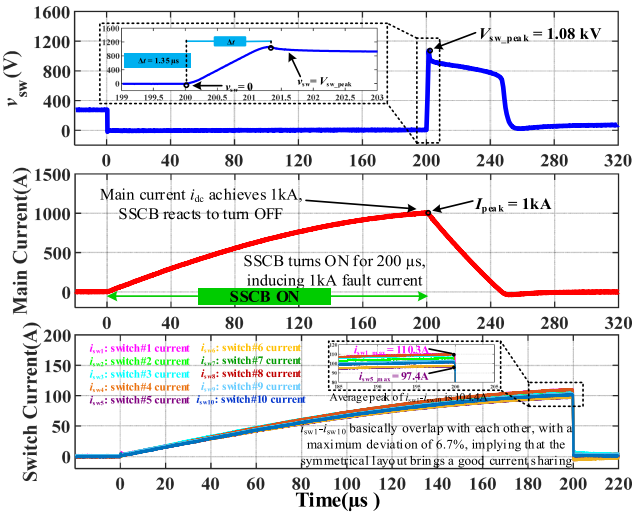

Fig. 19. Experimental waveform of a ten-switch SSCB to interrupt 1-kA short-circuit fault current with 36.8-μH line inductor, showing current sharing.

load resistance is only 0.15 Ω. The snubber charging time Δt is 1.3 μs, which meets the snubber design requirement. The 1-kA fault current is cleared in 130 μs, implying a fast fault clearance speed for this high current magnitude.

Fig. 19 further tests a short-circuit fault interruption process. The line inductor L_{Line} is 36.8 μH, and the load terminals are just shorted. The initial capacitor bank voltage is 300 V, and the fault current increases to 1 kA within 200 μs. The distributed currents in ten switches (i_{sw1}–i_{sw10}) are also measured, showing a good consistency with a deviation within 6.7% and good current sharing performance of ten parallel switches.

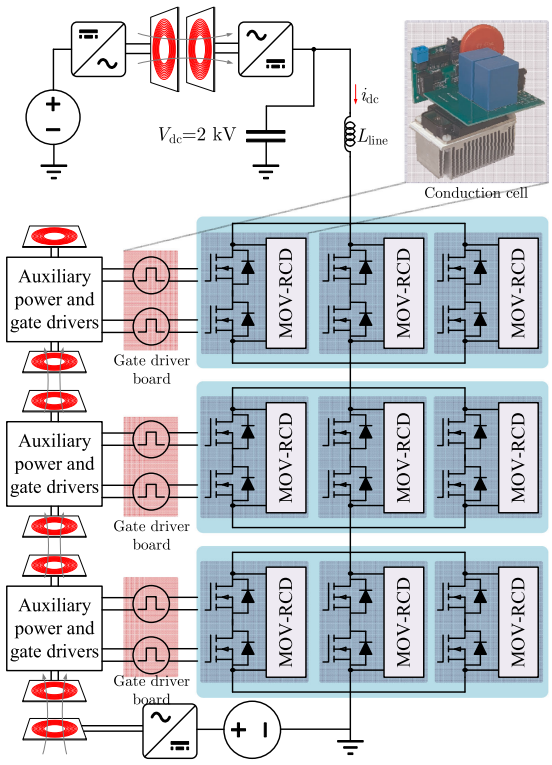

Fig. 20. Circuit topology of the implemented dc current interruption testing platform for 2 kV/1 kA SSCB based on a 3×3 power module structure.

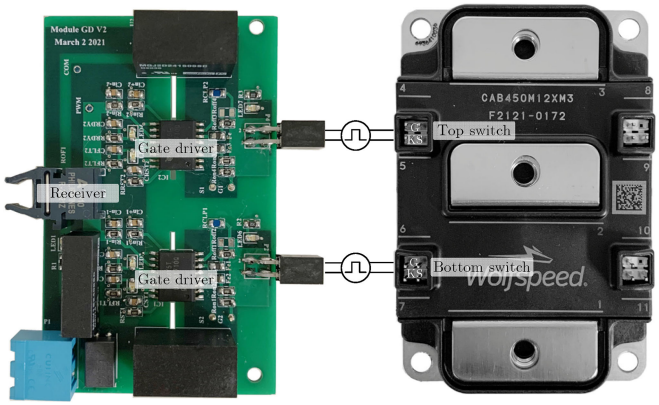

Fig. 21. Implemented gate driver board for each module.

D. 2 kV/1000 A 3×3 Power Module SSCB Interruption Test

1) Hardware Description: Furthermore, based on Tables I and II, a 3×3 power module-based SSCB is developed as shown in Fig. 20. The rated current is 100 A, and fault current is 1 kA in a 2-kV dc system. In this design, a domino wireless power transfer (WPT) system is used to supply power to multiple gate drivers [5]. Another WPT system is used to charge the capacitor bank to 2 kV [33].

Fig. 21 shows the gate driver design of each module. The gate driver UCC21710Q1 from Texas Instruments is adopted. Two gate driving loops are designed strictly identical to ensure the control signal synchronization.

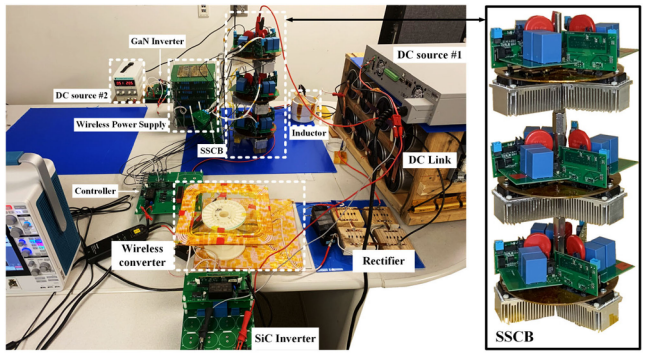

Fig. 22. Experimental setup of 2 kV/1 kA SSCB with 3×3 power modules.

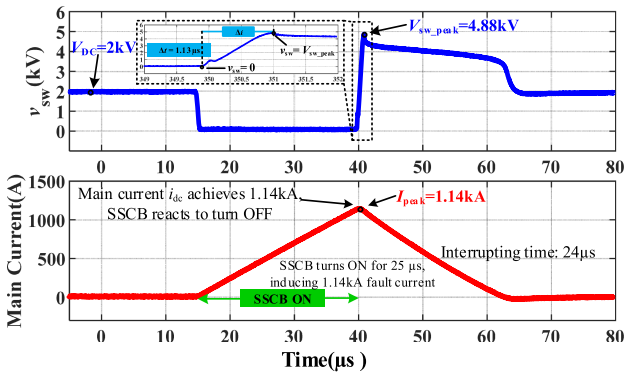

Fig. 23. Experimental waveform of a 3×3 power module SSCB to interrupt 1-kA short-circuit current in a 2-kV dc system with 36.8-μH line inductor.

Fig. 22 shows a testing bench of a 2 kV/1 kA SSCB prototype. The SSCB is in a three-layer tower structure, and each layer contains three parallel modules with MOV-RCD snubbers.

2) 2 kV/1000 A Interruption Test: Fig. 23 shows a short-circuit fault testing with a fault current magnitude of 1.14 kA in a 2-kV dc system. The line inductor L_{Line} is 36.8 μH, and the load terminals are directly shorted. The snubber charging time Δt is 1.13 μs. The peak voltage across the SSCB is clamped to 4.88 kV. It validates a fast response speed, and the current decreases to zero within 24 μs.

Another short-circuit testing is conducted at 300 V dc voltage to investigate the voltage and current distribution. A relatively low dc voltage helps to slow down the transient and provide more details on voltage and current sharing. During test, the line inductance L_{Line} is 36.8 μH, and the load terminals are shorted. The experimental results are provided in Fig. 24.

Fig. 24 shows that voltage is evenly distributed among series-connected layers: 1.55, 1.59, and 1.58 kV, respectively. Moreover, the transient voltage sharing among series-connected MOSFETS inside module is also acceptable: switch voltage deviation is below 10%. Meanwhile, the current is also evenly distributed. Inside one layer, measured currents in three parallel modules are 343.8, 339.3, and 330.9 A, with a deviation of 2.1% from the average value. Therefore, the symmetrical busbar design is effective to realize evenly distributed voltage and current sharing.

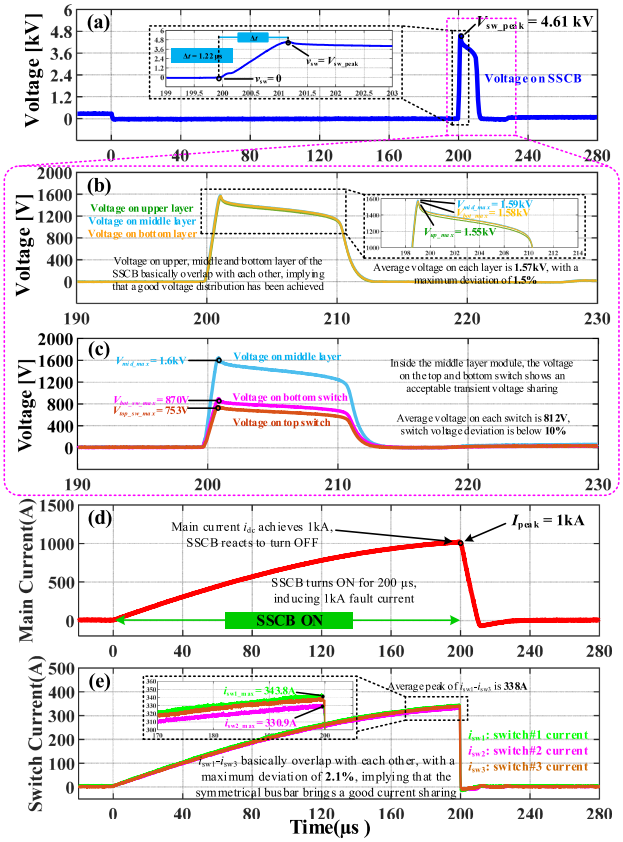

Fig. 24. Experimental waveform of a 3×3 power module SSCB to interrupt 1-kA short-circuit current with 300-V dc voltage and 36.8-μH line inductor. (a) SSCB voltage. (b) Layer voltage balancing. (c) Switch voltage balancing. (d) Main current. (e) Switch current balancing.

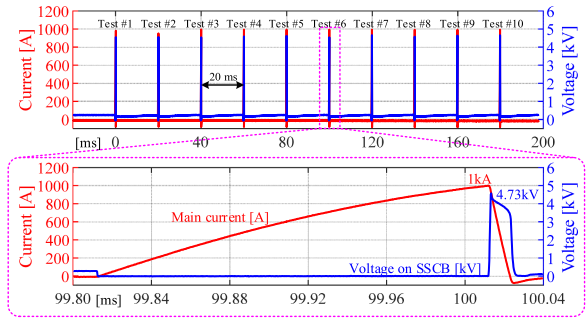

Fig. 25. Ten consecutive 1-kA interruption test events with 20-ms gap.

3) SSCB Endurance: Consecutive 1 kA Interruption Test Events: Then, consecutive short-circuit interruption test events are conducted to investigate the endurance of SSCB in the cases that a series of short circuits happen [34]. The dc capacitor bank is 1000 μF and line inductor L_{Line} is 36.8 μH. The load terminals are shorted. Tests are conducted at 1-kA fault current condition.

Fig. 25 shows ten consecutive interruption events with 20-ms time gap. During the tests, the fault current reaches 1 kA and the peak voltage of the SSCB is clamped to 4.73 kV. When the main current reaches zero, a test event completes. The same test pattern is repeated for ten times. Each test event takes around 240 μs. However, it takes about 19 ms to recharge the dc capacitor bank for next test event. Therefore, the events gap is selected as 20 ms.

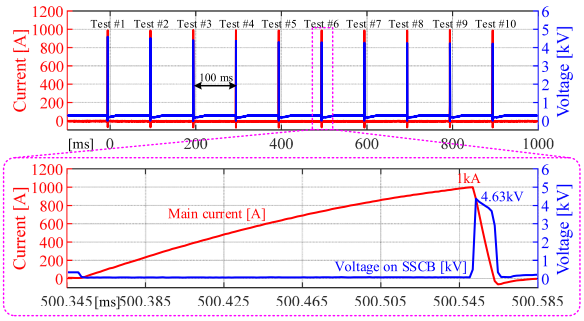

Fig. 26. Ten consecutive 1-kA interruption test events with 100-ms gap.

Another consecutive interruption test is conducted with 100-ms time gap to investigate the SSCB endurance in a different test frequency. Fig. 26 clearly shows that the dc capacitor bank is recharged in 100-ms gap between consecutive test events. During each test, the fault current still reaches 1 kA and the peak voltage is clamped to 4.63 kV. It validates good endurance in situations that a series of short circuits happen.

E. Summary and Comparison of Designed SSCBs

Table III summarizes the comparison of the proposed SSCBs with key parameters. With the increasing of parallel switches, the nominal and fault current magnitudes increases nonlinearly. It is limited by thermal dissipation capability of semiconductor devices and the SSCB structure. For example, ten parallel switches can bring a fault current capability of 1 kA and a high efficiency of 99.96%, but the power density is not significantly improved compared with the single- and four-switch SSCBs. In addition, the fault current clearance time is increased (130 μs) due to the residual energy in the line inductor L_{Line}.

For the 3×3 power module-based SSCB, it is flexible to adjust series and parallel number of switches through the busbar design. It has the benefit to achieve high efficiency with a good scalability. Due to the high voltage across switches, interrupting time is only 24 μs for 1-kA fault current. Table III also validates that, with the proposed snubber design methodology, all the implemented SSCBs have achieved the desired charging time Δt, which is between 0.5 to 2 μs.

F. Comparative Study

Table IV provides a comparative study, where ten design parameters are considered. Wu *et al.* [19] present the RC and RCD snubber design for IGCT-based MV DCCBs. dv/dt and power shock are also considered, which ensures the turn-OFF safety. Berg *et al.* [20] focus on the design of an MOV-RCD snubber by considering power shock of the main switch and damping resistance in the discharging process. It also incorporates series scalability by adopting distributed snubbers. Feng *et al.* [21] show an HV DCCB design with distributed IGBTs and snubbers for scalability. The charging time and dv/dt are both considered in the snubber capacitor design. Liu *et al.* [22] and Giannakis

TABLE III
COMPARISON BETWEEN DIFFERENT SSCB PROTOTYPES

No.	Series-Parallel Configuration	DC Bus Voltage (V)	Nominal Current (A)	Fault Current (A)	Estimated Efficiency (%)	Power Density (kW/L)	Δt (μs)	Interrupting Time (μs)
#1	1×1	500	30	300	99.88	36.8	1.4	40
#2	1×4	500	60	600	99.94	27.4	1.9	65
#3	1×10	500	100	1000	99.96	37.8	1.3	130
#4	3×3	2000	100	1000	99.96	15.4	1.1	24

TABLE IV
COMPARATIVE STUDY

Parameters(1)	Thermal analysis	Symmetrical structure	Charging time(2)	dv/dt	Power shock	Discharging process	scalability	Efficiency	Power density	Voltage range
Proposed	✓	✓	✓	✓	×	✓	✓	✓	✓	LV-MV(3)
[19]	×	×	×	✓	✓	×	×	×	×	MV
[20]	×	×	✓	✓	✓	✓	✓	×	×	MV
[21]	×	×	✓	✓	×	✓	✓	✓	×	HV(4)
[22]	×	×	×	✓	×	✓	×	×	×	LV
[23]	×	×	✓	✓	✓	✓	✓	×	×	LV-MV

(1) Key parameters considered in designing MOV-RCD-based SSCBs; (2) It is related to response speed by considering current magnitude, snubber capacitor, and MOV clamping voltage; (3) Low voltage and medium voltage; and (4) High voltage.

and Peftitsis [23] design the snubber capacitance by considering energy conservation law with the line inductance. For the snubber resistor design, discharging process is also considered, in terms of power dissipation and critical damping. To summarize, the existing references provide comprehensive design factors which should be considered for passive snubber-based SSCB design.

As noted in Table IV, the proposed methodology in this article is unique from three aspects: conduction loss-based thermal analysis, symmetrical implementation, and power density. With respect to other factors, the presented design procedure systematically incorporates them, and provides more complete design guidelines compared with the existing pieces of literature.

VI. CONCLUSION

This article investigates MOV-RCD snubber-based SSCBs. The thermal dissipation capability is identified as an important constraint in determining the nominal current of an SSCB. Then, the fault current capability can be further derived from the nominal current to guide the MOV-RCD snubber design. The selection of key component, that is snubber capacitance, depends on the fault current magnitude, the dv/dt related snubber charging time, and the MOV-related clamping voltage. Moreover, parasitic inductances extraction results by Q3D are given to validate the evenly distributed stray inductances in the proposed symmetrical layout. 500 V/300 A, 500 V/600 A, 500 V/1 kA, and 2 kV/1 kA SSCBs prototypes are implemented with good scalability. The maximum efficiency can achieve 99.96%. Experimental results validate that the proposed SSCBs can successfully interrupt 1 kA with a fast speed of 24 μs. Meanwhile, in the proposed symmetrical series and parallel structures, the currents and voltages are evenly distributed with low deviation. This article aims to provide a point of reference in designing MOV-RCD snubber for SSCBs.

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