Ground Fault Analysis and Grounding Method of Static Power Converters in Flexible AC Traction Power Supply Systems

Ziming Li, Xiaoqian Li, *Senior Member, IEEE*, Yingdong Wei, *Member, IEEE*, Chao Lu, *Senior Member, IEEE*, Yunzhi Lin, and Zengqin Li

***Abstract*—Flexible traction power supply system (FTPSS) can eliminate neutral sections of all catenaries and improve the poor power quality of railway substations. The static power converter (SPC) is the key equipment of FTPSS and its internal faults must be quickly identified and cleared with minimal impact on catenaries to ensure the safety and reliability. This article investigates the two-stage fault characteristics in FTPSS. Before blocking, overcurrent and voltage distortion may result in a wide range of abnormal power supply. After blocking, capacitor overvoltage becomes the primary problem threatening the safety of faulty SPC because of the energy feeding from other SPCs. Equivalent circuits are established and applied to various fault conditions. The most serious fault case can be found through the comparison, so the complicated large-scale simulation scanning can be avoided. A T-shaped grounding method is proposed to solve the problem of fault current and capacitor overvoltage. Based on the calculation and simulation results of several typical fault cases, the dimensioning criterion of grounding circuit is provided for reference. Moreover, a comprehensive scheme of grounding protection is designed to detect and isolate serious faults. The theoretical fault analysis and the proposed grounding method are verified by simulations and experiments.**

***Index Terms*—Fault analysis, flexible traction power supply system (FTPSS), grounding method, static power converter (SPC).**

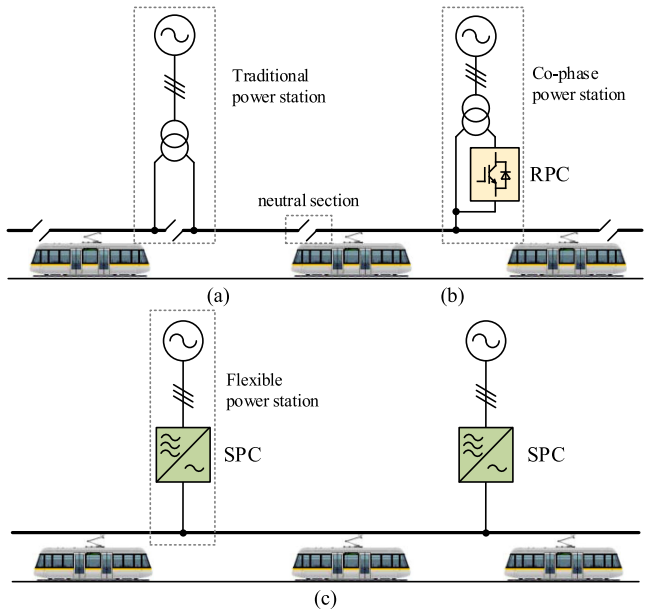

Fig. 1. Diagram of a TPSS. (a) Traditional system. (b) Cophase system. (c) Flexible system.

I. Introduction

THE 25-kV ac single-phase traction power supply system (TPSS) is widely used in many countries. The problems of passing neutral sections, power quality, and power supply capability have restricted the development of electrified railways for a long time [1]. Cophase TPSS can mitigate the effects of current imbalance with a railway power conditioner (RPC) [2]–[4]. However, this compensation method can only eliminate neutral sections in traction substations [5]. The reserved neutral sections between substations still cause locomotive speed loss. With the development of large-capacity power electronics technology [6]–[9], flexible traction power supply system (FTPSS) can achieve complete cancelation of neutral sections, as shown in Fig. 1. The poor power quality problem, which includes large negative sequence current, low power factor, and serious harmonic pollution, can be solved. Therefore, FTPSS envisions a promising future of rail transit power supply [10]. It is widely used in German railway systems. In China, this technology is also applied to Beijing Daxing International Airport Express.

The static power converter (SPC) is the core device of FTPSS. Safe, reliable operation of SPC is the prerequisite for improving system reliability. The line-to-ground fault is a common kind of

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fault that should be paid attention to when transmitting electric power [11]–[13]. Ground faults inside SPC can produce serious consequences. For converters, ground faults threaten equipment safety, which means that power devices require increased safety margins and costs. For systems, if ground faults inside converters exert a great impact on the voltage of the catenary side, the impact will spread to other traction stations and locomotives through the catenary. A single faulty converter may cause the entire power supply system to stop operating. This situation is detrimental to system reliability and availability.

The grounding method directly affects the characteristics of internal ground faults, which are closely related to protection strategy, device parameters, redundant design, and system control [13]. Grounding is thus the foundation of SPC main circuit design and deserves further research. The grounding methods can be divided into four types, which are ungrounded neutral, solidly grounding, resistance grounding, and reactance grounding [14]. Resistance grounding is the preferred choice in voltage-source converters (VSC) [15]. When the insulation is broken somewhere, a short circuit is formed between the grounding point and the fault point. The conventional resistance grounding method aims at limiting the transient short-circuit current within the safety range when ground faults occur [16], [17]. Considering the short-circuit energy feeding from other nonfaulty converters, power modules and external ac sources are coupled through the fault path. Except for the rapidly rising fault current before blocking, the capacitor overvoltage after blocking becomes another serious problem [12], [18]. One solution is to place thyristor bypass branches in parallel with upper arms of modular multilevel converters (MMCs) [12]. Although the overvoltage can be effectively eliminated, an equivalent dc-side short-circuit is created by the trigger thyristors. In [18], an inductor and resistor parallel grounding circuit is employed to create current zero crossings. Increasing resistance can reduce the magnitude of the fault current, but the overvoltage of the upper arm increases. The grid-side ac circuit breakers (CBs) must trip before the upper arms are charged to the maximum value.

In addition, existing research on transient characteristics of internal ground faults is insufficient. Most studies have focused on the analysis of ground faults in two-level ac/dc or dc/dc converters [20], [21]. Compared with small-capacity converters in dc distribution systems, multilevel ac/dc/ac converters in FTPSS behave differently during faults [22]–[24]. Moreover, only the fault point of input port was considered. The fault points located in submodules and output port were disregarded. Insufficient analysis of fault points is not conducive to identifying the most serious fault condition, thus causing difficulties to the design of the main circuit parameters and protection strategy.

This article bridges the aforementioned research gap by comprehensively analyzing the fault characteristics in two stages and proposing a T-shaped grounding method. First, several typical ground fault points are selected as research objects in order to find the most serious fault case. Immediate blocking in some fault cases may lead to capacitor overvoltage because of mesh feeding. The fault points are classified into two types according to whether the fault path is changed before and after blocking. Equivalent circuits with expansibility in various cases are established to avoid complicated large-scale offline simulation scanning. Then, a T-shaped grounding method is proposed to solve the problem of device overcurrent and capacitor overvoltage. Three protection strategies are designed to detect fault currents in the grounding components. Finally, the dimensioning criterion of grounding circuit is provided for reference based on the calculation or simulation results of several typical fault cases. The device safety is consequently guaranteed, and the power supply reliability of the whole system is improved.

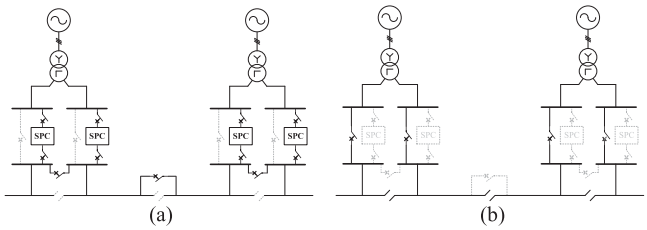

Fig. 2. System configuration diagrams. (a) Flexible mode. (b) Traditional mode.

When the catenary fault occurs, SPCs detect a rapid rise in the output current. Then, SPCs will switch from voltage control mode to current control mode. Each SPC provides a stable current to the fault point. Therefore, the fault section can be located through differential relay or other schemes, and the CBs will trip to clear the catenary fault. The catenary voltage then restores and SPCs switch back to voltage control mode. The future research will pay attention to the clearance process of catenary faults.

The rest of this article is organized as follows. Section II presents the SPC topology and the selected typical fault points. Section III analyzes the fault characteristics of the first type. Section IV presents equivalent circuits and dynamic equations to investigate fault characteristics in two stages by taking one fault point of the second type as an example, and then extends to other cases. Section V proposes three protection strategies to detect fault currents. Section VI presents the simulation results and component dimensioning criterion for reference. The experimental results are discussed in Section VII. Finally, Section VIII concludes this article.

II. Configuration and Grounding Method

The Beijing Daxing International Airport Express Project is an upgrade project that needs to operate in either flexible mode or traditional mode, as shown in Fig. 2(a) and (b). The Scott transformers must be reserved. The voltages of two secondary windings of the Scott transformer are in different phases, and they are converted into voltages in the same phase by two SPCs. When one or two SPCs stop operating, the flexible mode can still supply sufficient power. When three or four SPCs stop operating, the power supply system can switch to the traditional operation mode. Thus, the reliability of the whole system is improved. Three main solutions are currently adopted

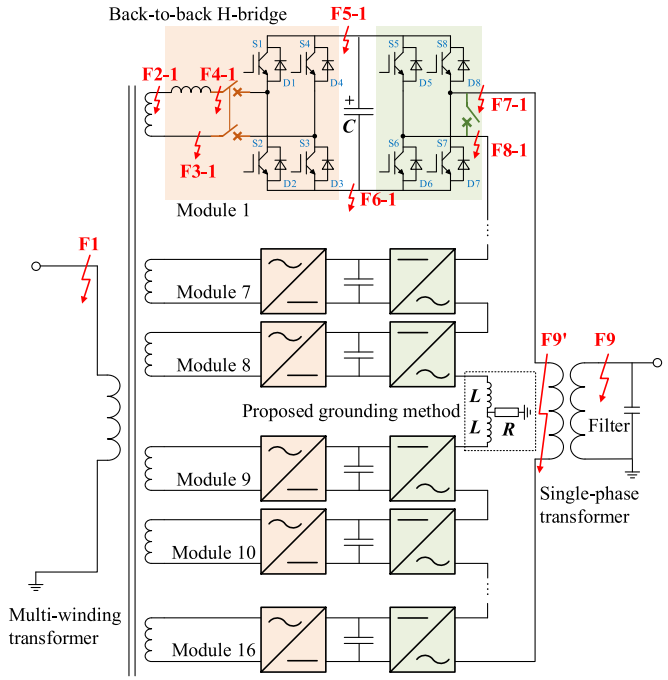

Fig. 3. SPC topology and ground fault locations.

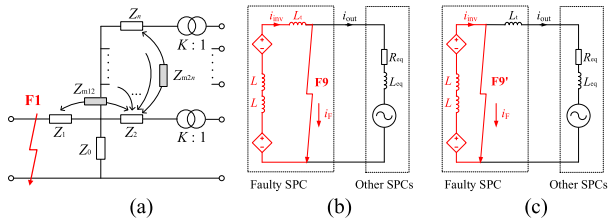

Fig. 4. Equivalent fault circuit before SPC blocking. (a) F1. (b) F9. (c) F9′.

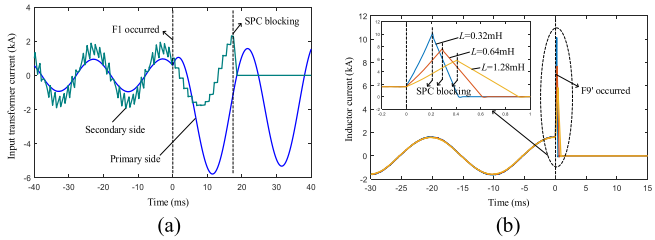

Fig. 5. Fault current waveforms in the case of (a) F1 and (b) F9′.

for the SPC topology: direct MMC [25], indirect MMC [26], and cascaded H-bridge converters [27]. Siemens has applied the direct MMC topology to the 16.7-Hz TPSS, but it is difficult to realize equal frequency conversion. The cascaded neutral point clamped converters have a high practical value because it can realize arbitrary frequency conversion, and they have been used in ABB PCS 6000 Rail series products. However, solutions based on three-phase system are not applicable to the Beijing Daxing International Airport Express Project. A single-phase to single-phase topology based on parallel cascaded H-bridge converter with a multiwinding transformer is proposed [28]. Compared with indirect MMC, this topology has fewer switching devices and is entirely free of circulation and capacitor voltage equalization problems. Therefore, this study focuses on the cascaded H-bridge converter topology.

Fig. 3 presents an overview of the SPC topology studied in this work. A single-phase ac/dc/ac SPC can be divided into three parts: input transformer, power modules, and output transformer [29]. The primary winding of the input transformer connects the Scott transformer, and the N split secondary windings connect N power modules. Each module consists of two back-to-back H-bridges and dc-link capacitors. The output transformer connects cascaded H-bridges with the catenary. The transformer achieves electrical insulation, which can reduce the mutual influence between SPC and catenary when a fault occurs. Moreover, leakage reactance can be used as part of the filter to block the harmonic current of the locomotive. The rectifier-side H-bridges are independently controlled to stabilize the dc voltage. The inverter-side H-bridges are controlled in a unified manner to output N+1 level ac voltage.

The dashed box in Fig. 3 shows the proposed grounding method. Two inductors and one resistor form a T shape. The current flowing through the grounding branch is theoretically zero during steady-state operation. In a power system based on VSCs, there are two main grounding locations: grid-connection transformer grounding on the ac side, and mid-point grounding on the dc side [15], [19]. The transformer grounding is widely used in three-phase system, but it is unsuitable for single-phase system. Thus, the grounding location of SPC is at the neutral point, also the mid-point of cascaded H-bridges.

Several possible locations of ground faults inside SPC are shown in Fig. 3. The main reason of ground faults is insulation breakage. This work focuses on metallic ground faults. When SPC protection system detects a fault, it blocks all switching devices within tens of microseconds, and then trips the input and output CBs after tens to hundreds of milliseconds.

III. Fault Analysis of F1 and F9

F1 and F9 do not change the current path in N modules. Blocking SPC can quickly clear F1 or F9, and the fault current in switching devices can be cut off to zero. However, F2-n to F8-n cannot be totally cleared until the CBs trip. n is the module number. Blocking SPC changes the fault current path in the modules. Thus, the fault characteristics of F2-n to F8-n behave differently before and after blocking.

F1 and F9 occur on the input transformer and the output transformer, respectively. Given that the transformer has the function of electrical isolation, neither will form a fault path with the grounding point of modules.

F1 has little effect on switching devices. The split reactance between the primary and secondary windings is relatively large because of the special structure of the multiwinding transformer. The equivalent circuit of the input transformer is shown in Fig. 4(a). We take winding 2 as an example. The mutual inductance Z_{m12} is designed to be large. F1 causes a large fault current on the primary side of the input transformer and a small fault current on the secondary side, as shown in Fig. 5(a). The SPC

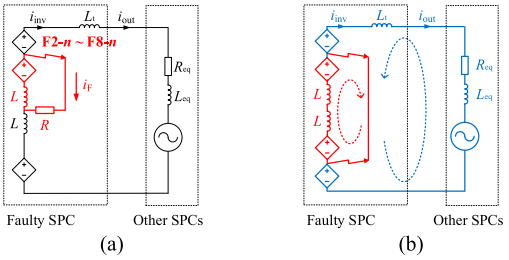

Fig. 6. Equivalent fault circuit of F2-n to F8-n before SPC blocking. (a) One ground fault. (b) Two ground faults.

simulation parameters are listed in Table I in the Appendix. The load condition shown in Fig. 5 is 20 MW resistive load, equal to the rated capacity of SPC.

F9 causes an extremely large fault current in switching devices. From the perspective of other nonfaulty SPCs, it is similar to a catenary fault [30]. Without transformer leakage inductance L_t, F9′ is more serious than F9, as shown in Fig. 4(b) and (c). F9′ should be given priority when designing fault current limiting inductors. Fig. 5(b) illustrates the current-limiting effect of different inductance values on fault F9′.

IV. Fault Analysis of F2–F8

Mesh feeding is a significant difference between flexible system and traditional system. The blocking behavior of converters in FTPSS changes the current paths of F2-n to F8-n, so the fault characteristics behave differently in two stages. The fault characteristics after blocking are analyzed in detail in Part B. The subsequent analysis is based on the upper arm under the premise of symmetry.

A. Fault Characteristics Before Blocking

The overcurrent in the switching devices deserves careful attention before SPC blocking. As shown in Fig. 6(a), an extra current path is formed because the fault point and the grounding point are connected by the earth. Some modules are in the fault path. The inserted capacitors in these modules are discharged through the upper inductor and the grounding resistor. If the fault current i_F is too large, the capacitor voltage drop will result in output voltage distortion. Increasing R can enhance the damping effects, thereby reducing the impact of ground faults.

The inductors are installed next to neutral point so that they can function in the case of various fault locations, as shown in Fig. 6(a) and (b). Compared with increasing the leakage inductance of the output transformer, additional inductors can limit the fault current not only in the case of secondary faults, but primary faults as well. When more than one ground fault occurs in power modules, a line-to-line fault forms. Capacitor discharge leads to fault current in the inner fault path and mesh feeding causes fault current in the outer fault path. The fault currents can be limited by additional inductors and leakage inductance of the output transformer, respectively.

Fig. 7 illustrates the fault waveforms with different ground resistance values. The damping in the fault circuit is too small, and causes severe voltage drop of dc capacitors in the path. When the value of R is small, the fault current on the ground resistance is large. i_F interferes with the output voltage and an obvious voltage sag occurs at the fault moment. Increasing the ground resistance can effectively improve the ground fault characteristics before SPC blocking. Therefore, the neutral point of SPC needs to be grounded with suitable resistance.

B. Fault Characteristics After Blocking

Tens to hundreds of milliseconds are consumed from SPC blocking to input and output CBs tripping. During this period, the catenary voltage manipulated by other nonfaulty SPCs influences the faulty SPC through the output transformer. The output characteristics of faulty and nonfaulty SPCs are coupled through feeders. The grounding method that only includes current limiting inductance is not effective enough in a system where multiple SPCs are in cooperative operation. High ground resistance can weaken the coupling effect.

When faults F2-n to F8-n occur in module n ($0 \leq n \leq N/2$) of the upper arm, all power modules exhibit diode characteristics. According to diodes circuits, modules can be divided into three types. The first type only includes the faulty module n, whose fault current path maybe affected by ac sources on both sides. The second type includes module $N/2+1$ to module N in the lower arm and module 1 to module $n-1$ in the upper arm (if $n = 1$, only includes modules in the lower arm). These modules are only affected by the inverter-side ac source. The third type includes module $n+1$ to module $N/2$ (if $n = N/2$, the third type does not exist). These modules are bypassed by the fault path. There is no fault current flow through the third type of modules, and the capacitor voltages remain the same after SPC blocking.

1) Example Analysis of F6-n After Blocking: We take fault F6-n as an example for analysis. The fault current path is shown in Fig. 8 when $n = 1$, $N = 16$. The fault point and grounding point are equivalently connected. C is the module dc capacitor. The fault location decides the number of capacitors inserted in the path. C_1 to C_n in the upper arm and $C_{N/2+1}$ to C_N in the lower arm are charged when inverter current i_{inv} flows into SPC. C_1 to C_{n-1} in the upper arm and $C_{N/2+1}$ to C_N in the lower arm are charged when inverter current i_{inv} flows out of SPC.

If ground resistance $R = 0$, the fault path only has inductors and capacitors without any energy-consuming components. A total of N capacitors are connected in series before SPC blocking, and no more than $N/2+n$ capacitors are connected in series after SPC blocking. Capacitor voltages increase faster when less capacitors are inserted.

The equivalent circuit of F6 is shown in Fig. 9. The nonfaulty SPC can be simplified into an ac voltage source, which can be expressed as

$$u_s(t) = K_t U_m \sin \omega t \tag{1}$$

where U_m is the peak voltage of the catenary and K_t is the output transformer ratio.

Here, R_e and L_e correspond to

$$R_e = R + R_{eq}, L_e = L + L_t + L_{eq} \tag{2}$$

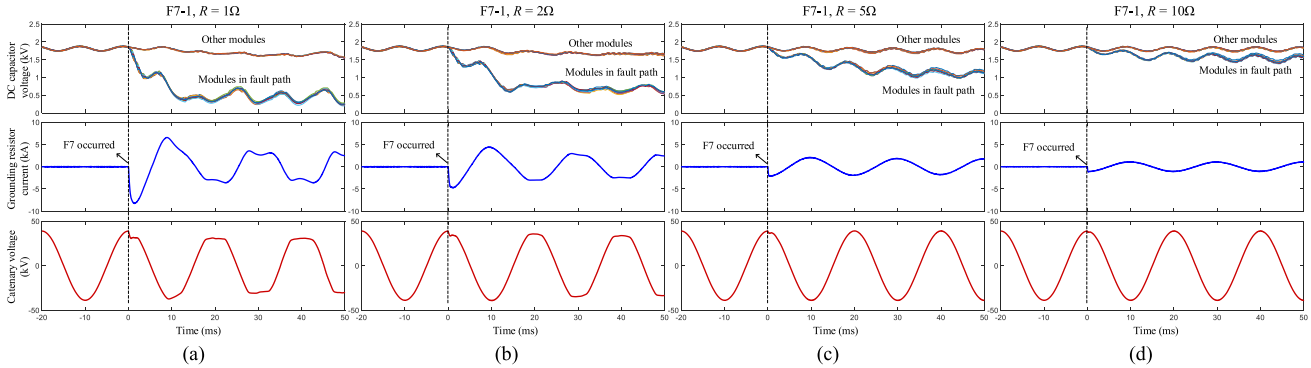

Fig. 7. Fault characteristics before SPC blocking in the case of F7-1 with different ground resistances. (a) R = 1 Ω. (b) R = 2 Ω. (c) R = 5 Ω. (d) R = 10 Ω.

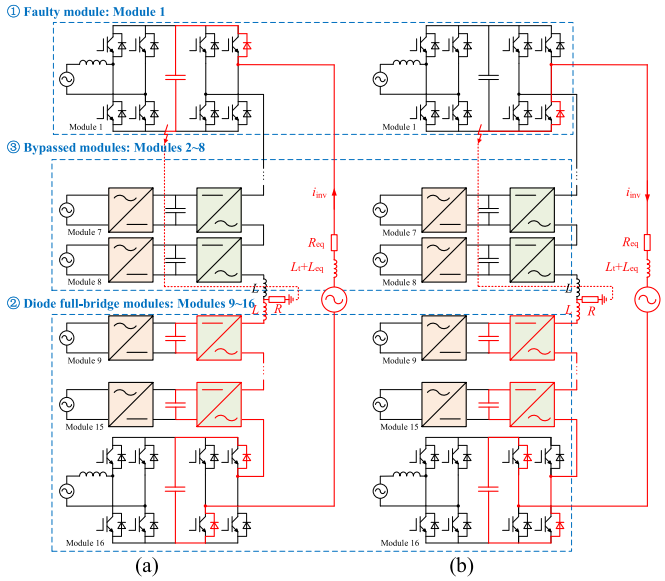

Fig. 8. Fault current path of F6-1 after SPC blocking. (a) $i_{\mathrm{inv}} < 0$. (b) $i_{\mathrm{inv}} > 0$.

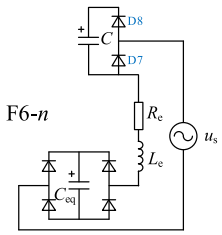

Fig. 9. Equivalent circuit of F6 after SPC blocking.

where R indicates the ground resistance, L indicates the single-arm inductance, L_t indicates the leakage inductance of output transformer, and R_{eq} and L_{eq} represent the equivalent impedance of other nonfaulty SPCs.

The faulty SPC can be simplified into an *RLC* load with diodes. These diodes include the first type and the second type in Fig. 8. The structure of the first type is a diode half-bridge and the module capacitor C. The second type is equivalent to a diode full-bridge and the capacitor C_{eq}, which can be expressed as

$$C_{\mathrm{eq}} = \frac{C}{\frac{N}{2} + n - 1}. \tag{3}$$

Assuming that all capacitor voltages are balanced, the initial voltages of C and C_{eq} can be defined as

$$\begin{cases} u_{\mathrm{C}}(0) = (1+\varepsilon) U_{\mathrm{CN}} \\ u_{\mathrm{Ceq}}(0) = \left(\frac{N}{2} + n - 1\right)(1+\varepsilon) U_{\mathrm{CN}} \end{cases} \tag{4}$$

where U_{CN} is the rated capacitor voltage and ε is the voltage ripple percentage.

The total voltage of the capacitors inserted in fault path is

$$u_{\mathrm{Csum}}(t) = u_{\mathrm{C}}(t) + u_{\mathrm{Ceq}}(t). \tag{5}$$

If $u_{\mathrm{Csum}}(t) < K_{\mathrm{t}} U_{\mathrm{m}}$, mesh feeding will cause overvoltage through diodes. The capacitor voltage rise will not stop until $u_{\mathrm{Csum}}(t) \geq K_{\mathrm{t}} U_{\mathrm{m}}$.

Diodes are OFF in every half-cycle when $u_{\mathrm{Csum}}(t) > u_{\mathrm{s}}(t)$. A second-order *RLC* circuit with sinusoidal excitation is formed when $u_{\mathrm{Csum}}(t) < u_{\mathrm{s}}(t)$. C is inserted in one half-cycle and bypassed in another half-cycle according to the inverter current direction. The equivalent C_{eq} is inserted in the entire cycle. When diodes are ON, the circuit dynamic equations can be described as

$$C\frac{du_{\mathrm{C}}(t)}{dt} = i_{\mathrm{inv}}(t) \tag{6}$$

$$u_{\mathrm{s}}(t) = \begin{cases} R_{\mathrm{e}} i_{\mathrm{inv}}(t) + L_{\mathrm{e}} \frac{di_{\mathrm{inv}}(t)}{dt} + \left(\frac{N}{2} + n\right) u_{\mathrm{C}}(t) & , i_{\mathrm{inv}} < 0 \\ R_{\mathrm{e}} i_{\mathrm{inv}}(t) + L_{\mathrm{e}} \frac{di_{\mathrm{inv}}(t)}{dt} + \left(\frac{N}{2} + n - 1\right) u_{\mathrm{C}}(t) & , i_{\mathrm{inv}} > 0. \end{cases} \tag{7}$$

At the beginning of each half-cycle, the initial value of inverter current is zero. At the end of each half-cycle, the capacitor voltages increase or remain constant.

Fig. 10(a)–(d) illustrates the simulation waveforms when F6-n occurs in modules 1, 2, 3, and 4, respectively. SPC is blocked immediately when fault current is detected by differential protection. For F6-1 in Fig. 10(a), U_{C2} to U_{C8} remain constant after SPC blocking (the third type). U_{C9} to U_{C16} grow in the same trend and are charged every half-cycle (the second type). U_{C1} rises slowly and is charged every other half-cycle (the first

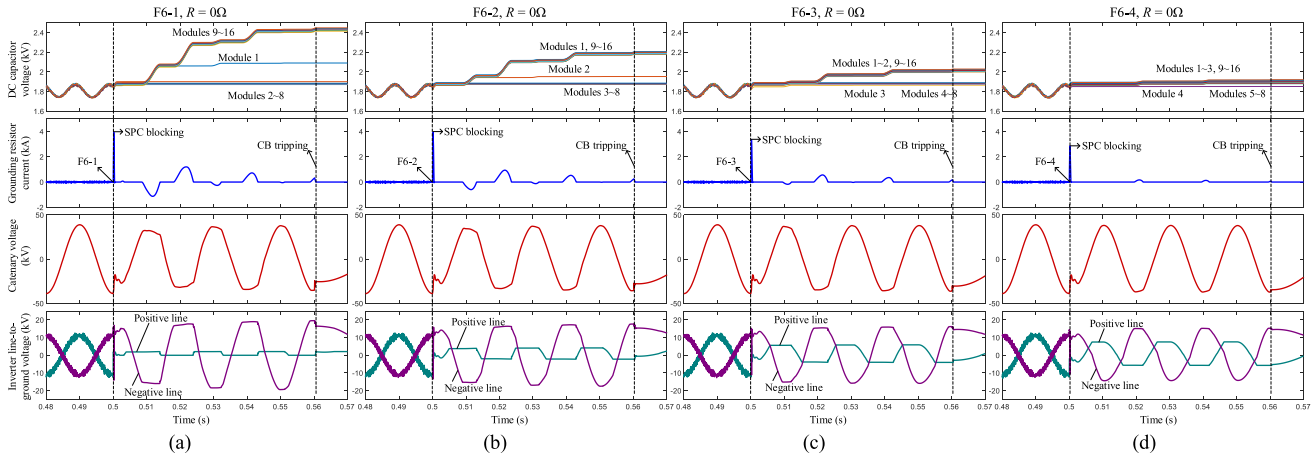

Fig. 10. Fault characteristics after SPC blocking in the case of F6-*n* with different fault modules. (a) F6-1. (b) F6-2. (c) F6-3. (d) F6-4.

type). For F6-2 in Fig. 10(b), U_{C3} to U_{C8} remain constant, U_{C1} and U_{C9} to U_{C16} are charged every half-cycle, U_{C2} is charged every other half-cycle. For F6-3 in Fig. 10(c), the rise of U_{C3} is unobvious and is similar to U_{C4} to U_{C8} in bypassed modules. In Fig. 10(d), the voltages of all capacitors are almost unchanged.

When the faulty module gets closer to the grounding point, more capacitors are in the path and the overvoltage is less serious. Therefore, the most serious case of capacitor voltage rise is the ground fault in module 1 or 16.

2) Extension of Equivalent Circuits After Blocking: The equivalent circuits for F2-*n* to F8-*n* are slightly different, as shown in Fig. 11. All the equivalent circuits are essentially second-order *RLC* circuits. Excitation is the sinusoidal voltage source, and the initial capacitor voltages are nonzero. Fault location affects the inductance and capacitance parameters. The direction of i_{inv} may affect the capacitance parameter as well. Similar to F6-*n*, F5-*n*, F7-*n*, and F8-*n* are located on the inverter side, and only the catenary voltage affects the characteristics. F2-*n*, F3-*n*, and F4-*n* are located on the rectifier side, so the fault characteristics are affected by the catenary voltage and the public grid voltage. The rectifier side is involved, which can be simplified into voltage source u_{rec}, input transformer leakage inductance L_r, and series inductor L_k.

The conduction of D1–D4 is related to the double-side power supply, namely, u_s and u_{rec}.

According to the equivalent circuit and simulation results in Fig. 11, the most serious fault case can be found. The voltages rise higher when less capacitors are inserted in the fault path. When CB trip time is constant, both the faulty module number and the specific fault location in the module affect the maximum capacitor voltage. The previous analysis has indicated that the overvoltage is more serious in the case of $n = 1$ or 16 than other cases. The waveforms are also shown in Fig. 11 when $n = 1$. When F7-1 occurs, the faulty module is bypassed and there are only eight capacitors charged by other SPCs. In the other cases shown in Fig. 11, nine capacitors are charged. Therefore, F7-1 is the most serious fault case.

F5-1 and F6-1 are similar. The capacitor in module 1 is inserted every other half-cycle, so U_{C1} does not rise as high as U_{C9} to U_{C16}. In the cases of F2-1, F3-1, F4-1, and F8-1, the capacitor in module 1 is inserted every half-cycle, like modules 9–16. The rectifier-side ac source has little effect, so the maximum capacitor voltages are about the same in these four cases.

The equivalent circuits are established to find the most serious fault case, and the simulation results verify the analysis. The simulation condition $R = 0$ is to make the fault characteristics evident. Increasing ground resistance is an effective solution to decrease the maximum capacitor voltage.

C. Discussions

The performance of F2-*n* to F8-*n* can be divided into two stages. Before blocking, the fault current in the switching devices increases rapidly, and the dc capacitor voltage continues to drop, causing output voltage distortion. The ground resistance and arm inductance can limit the fault current. After blocking, the fault current is at a low level, but the dc capacitors maybe charged by other nonfaulty SPCs before output CB tripping. Fig. 10 shows fault characteristics of different module numbers. Fig. 11 shows fault characteristics of different locations in one module. Through the comparison of two dimensions, the most serious fault case after blocking, F7-1, is found. The ground resistance plays an important role in preventing overvoltage. The minimum resistance should ensure that the capacitor voltage does not exceed the safe range. The maximum resistance should ensure that the fault current can be detected by current sensors. This will be analyzed in detail in Section VI.

The proposed method can be applied to other cascaded multilevel converters. The fault current before SPC blocking can be significantly limited by enlarging ground resistance. Capacitor overvoltage after blocking becomes the primary problem in actual design. The faulty submodule string is coupled with nonfaulty converters, and the equivalent circuits can be obtained in the case of various fault locations. After comparison and analysis, the most serious overvoltage case and the lowest fault current case can be found. The relationship between overvoltage and ground resistance, and the relationship between fault

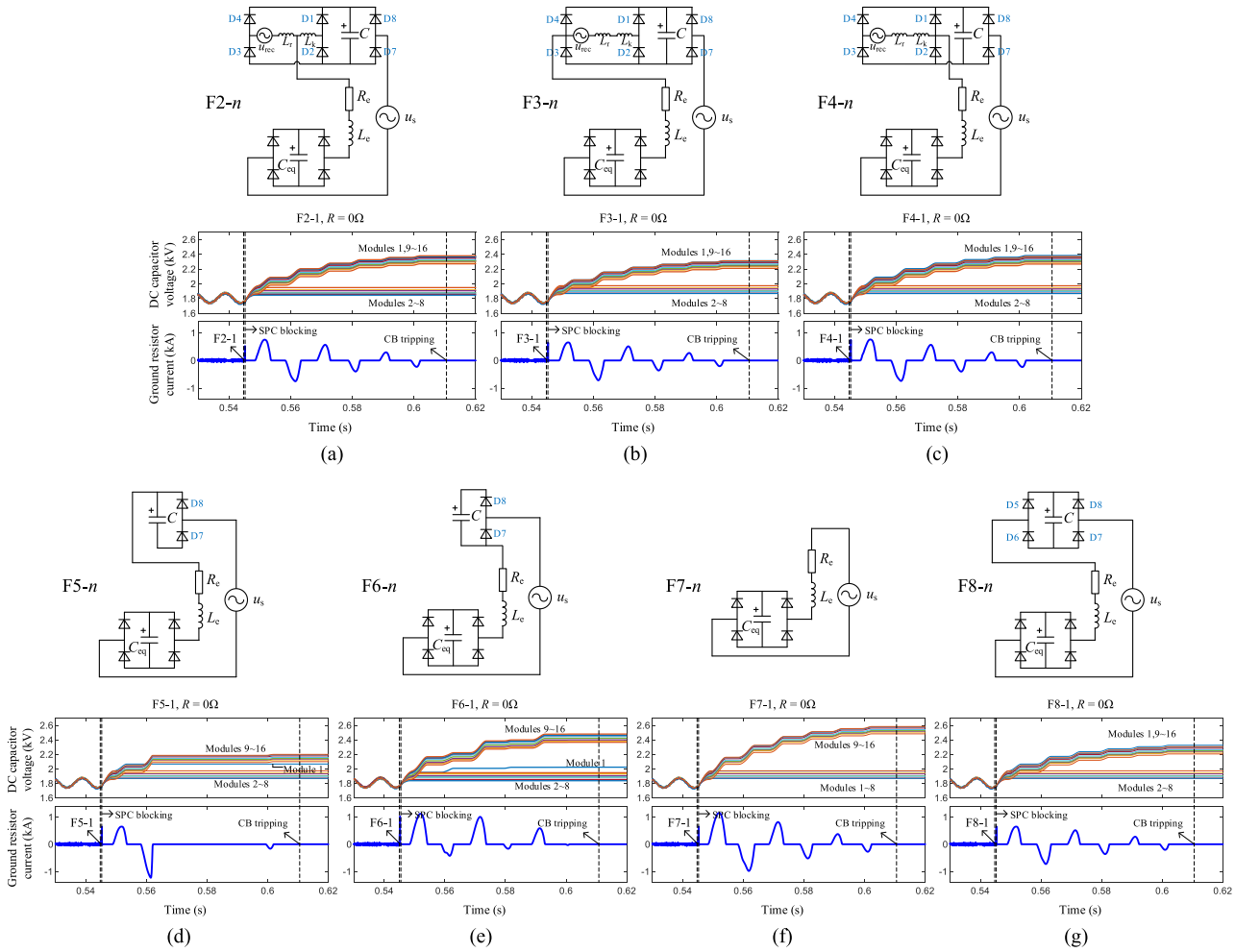

Fig. 11. Fault characteristics after SPC blocking with different fault locations in one module. (a) F2-1. (b) F3-1. (c) F4-1. (d) F5-1. (e) F6-1. (f) F7-1. (g) F8-1.

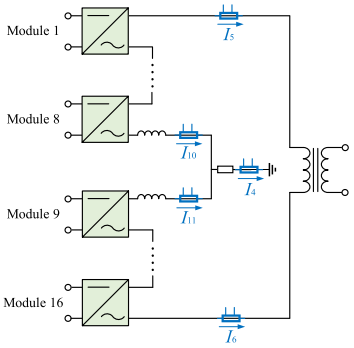

Fig. 12. Current sensor positions at the SPC inverter side.

current and ground resistance, can be obtained by simulation or numerical calculation.

V. Protection Strategies

The current sensors are configured as shown in Fig. 12. Differential protection and overcurrent protection are used to detect ground faults in module zone. The differential current and the restraint current for the differential scheme can be expressed as follows:

$$I_{\mathrm{d}} = |I_5 + I_6 + I_{10} + I_{11}| \tag{8}$$

$$I_{\mathrm{r}} = 0.5 \times |I_5 - I_6| . \tag{9}$$

The percentage differential relay operates when

$$\begin{cases} I_{\mathrm{d}} \geq K_{\mathrm{d}} I_{\mathrm{N}} \\ I_{\mathrm{d}} \geq K_{\mathrm{r}} I_{\mathrm{r}} \end{cases} \tag{10}$$

where I_{N} is the rated inverter current, K_{d} is the differential coefficient ($0 < K_{\mathrm{d}} < 1$), and K_{r} is the restraint coefficient ($0 < K_{\mathrm{r}} < 1$).

When ground faults occur in low-potential modules, such as module 8 or module 9, the fault current is at a very low level. The measurement accuracy of I_5, I_6, I_{10}, and I_{11} may not be satisfied. Therefore, a high-accuracy current sensor I_4 is applied in series with the grounding resistor. The ground overcurrent scheme can be expressed as follows:

$$I_{4\_\mathrm{rms}} > I_{\mathrm{th}} \tag{11}$$

where I_{4_rms} is the root mean square (rms) of I_4, and I_{th} is the threshold current. In order to avoid disturbance, protection

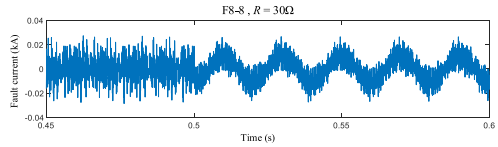

Fig. 13. Fault current in the case of F8-8.

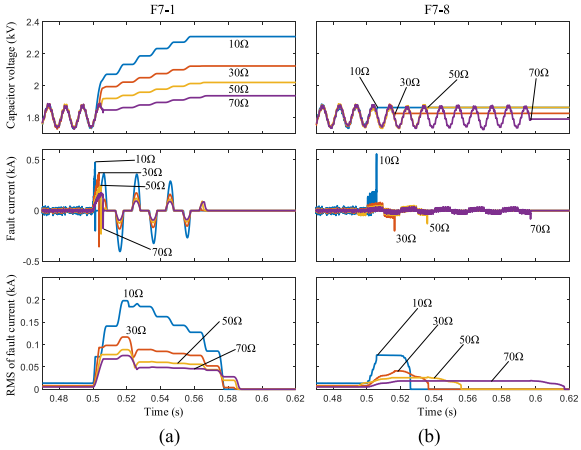

Fig. 14. Simulation results of 27.5 kV system with different ground resistances. (a) F7-1. (b) F7-8.

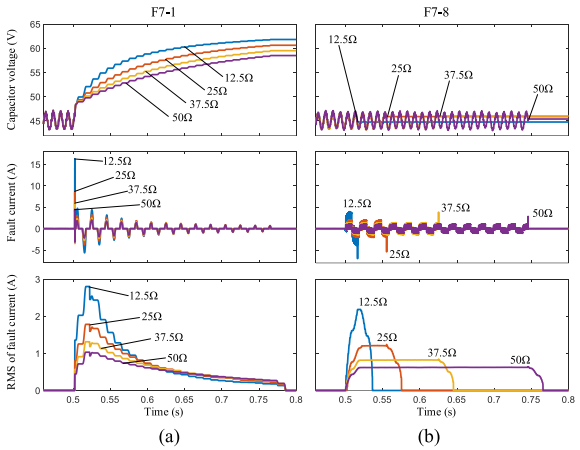

Fig. 15. Simulation results of 380 V system with different ground resistances. (a) F7-1. (b) F7-8.

delay is not a fixed value. The delay time increases as I_{4_rms} decreases.

Another overcurrent protection is designed to detect line-to-ground faults on the secondary side of the output transformer and line-to-line faults on the primary side. The inductor overcurrent relay operates when

$$|I_{10}| > K\sqrt{2}I_{\mathrm{N}} \text{ or } |I_{11}| > K\sqrt{2}I_{\mathrm{N}} \tag{12}$$

where K is the overcurrent coefficient ($K > 1$).

VI. Dimensioning Criterion

The previous analysis has obtained the fault characteristics of two stages, and has designed the corresponding protection strategy. The selection of current-limiting inductance and ground resistance is introduced in this section.

A. Current-Limiting Inductance

For the selection of inductance, not only line-to-ground faults but also line-to-line faults should be considered as well. In the case of F9′, all 16 capacitors discharge through the fault path, and the short-circuit current rises extremely fast. The minimum current-limiting inductance should ensure that the power electronics devices can tolerate the fault current before blocking.

To calculate the most severe fault current, the initial conditions are assumed to be most unfavorable. The load current is 1.2 times rated, and the capacitor voltage ripple ε reaches the upper limit. The value of inductance should satisfy

$$2L > \frac{NU_{\mathrm{C}}\left(1+\varepsilon\right)T_{\mathrm{blk}}}{I_{\max} - 1.2\sqrt{2}I_{\mathrm{inv}}} \tag{13}$$

where I_{inv} is the rated inverter current, $I_{\max}$ is the maximum current of switching devices, U_{C} is the rated capacitor voltage, and T_{blk} is the time from fault occurrence to SPC blocking.

Each inductor limits the discharge current caused by $N/2$ capacitors in time T_{blk}. The inductance value should satisfy (13). Enlarging inductance is beneficial to suppress the output current harmonics. However, it will also increase reactive power loss and affect the dynamic performance of current control, and the equipment cost will increase. In this article, the sum of current-limiting inductance and output transformer leakage inductance is designed to be no more than 0.10 p.u.

B. Ground Resistance

Low ground resistance leads to insulated gate bipolar transistor (IGBT) overcurrent and capacitor overvoltage. The fault current before SPC blocking can be effectively limited by enlarging ground resistance. Considering the mesh feeding, the only way to protect capacitors from overvoltage after SPC blocking is tripping CBs. Thus, capacitor overvoltage after SPC blocking becomes the primary problem when designing ground resistance.

According to the equivalent circuit in Fig. 11, the minimum resistance should ensure that the capacitor voltage does not exceed the safe range. In the case of F7-1 or F7-16, only eight capacitors are charged by other nonfaulty SPCs, and the overvoltage phenomenon is the most serious.

The maximum resistance should ensure that the fault current can be detected by current transformers (CT). In the case of F8-8 or F8-9, all 16 modules are in the fault circuit, and the fault current is the lowest. The sum of 16 capacitor voltages is greater than the peak of catenary voltage, so the overvoltage will not occur. However, there is little difference between fault current and steady-state operating current, as shown in Fig. 13 when ground resistance is 30 Ω in 27.5 kV system. If it is a nonmetallic fault, the fault current will be even smaller. Under

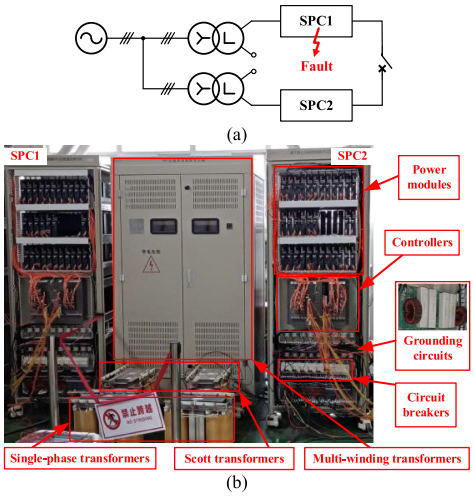

Fig. 16. Experimental system diagram. (a) Wiring diagram. (b) Photograph of the main components.

the condition of normal measurement accuracy, the ground fault is hard to be detected until another fault occurs. In contrast, case F7-8 or F7-9 is more practical in actual design.

Capacitor overvoltage and fault current may cause damage to power modules. Besides, rms of fault current is another important factor for the selection of ground resistance. It is related to the setting of protection strategy parameters, and it represents the heating power. When a nonmetallic ground fault occurs in low-potential modules, such as module 8 or 9, the fault current is at a very low level and maybe just below the threshold current of overcurrent protection. The fault will not be detected, and the fault current will flow through the grounding resistor continuously. The grounding resistor must be able to withstand the heating power for a long time.

In the 27.5 kV simulation system whose parameters are listed in Table I in the Appendix, the maximum capacitor voltage is 2.2 kV. Through the simulation results shown in Fig. 14, the ground resistance should be greater than 10 Ω. If the CT used is 100 A rated current, 1% accuracy, the resistance is selected as 50 Ω. If the grounding resistance is higher than 70 Ω, other methods should be used to detect the presence of ground faults.

VII. Experimental Verification

Ground fault experiments are performed on an SPC scaled-down prototype to verify the fault characteristics mentioned above. The parameters of the prototype are listed in Table II in the Appendix. Two SPCs run in parallel, one in voltage mode and the other in current mode. Ground faults occur in the current-mode SPC. The fault impedance is about 0.1 Ω. In the 380 V experimental system, the maximum capacitor voltage is designed to be 60 V. Through the simulation results as shown in Fig. 15, the ground resistance should be greater than 25 Ω. If the CT used is 10 A rated current, 0.2% accuracy, the resistance is selected as 37.5 Ω. The wiring diagram and photograph of the prototype are shown in Fig. 16, and the experimental results are shown in Fig. 17.

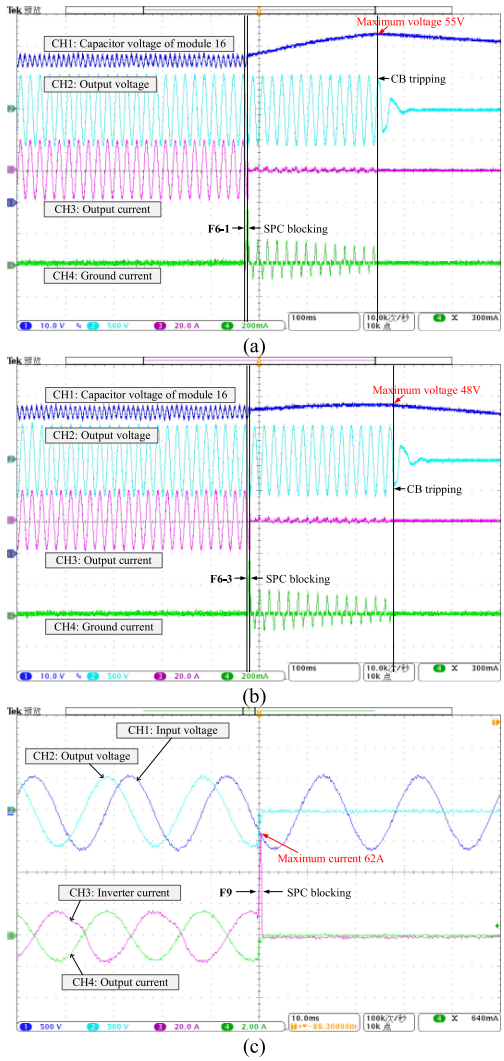

Fig. 17. Experimental waveforms of (a) F6-1, (b) F6-3, and (c) F9.

F6-1 and F6-3 cause capacitor overvoltage after blocking. For comparison, capacitor voltage of module 16, output voltage, output current, and ground current are presented in Fig. 17(a) and (b). When F6-*n* occurs, module 16 is the second type whose capacitor voltage rises the highest among the three types. The maximum capacitor voltage of F6-1 and F6-3 reaches 55 and 48 V, respectively. Compared with F6-1, two more capacitors are inserted in the fault path of F6-3. The total voltage of capacitors coupled with the catenary is higher, so the charging time in every half-cycle gets shorter. Because the potential of module 1 and module 3 is high enough, the fault current can be detected by differential protection. SPC blocks very quickly. The CB trip time in 380 V system is rather long, about 200 to 300 ms. Therefore, the ground resistance is designed high enough to protect capacitors from overvoltage.

In Fig. 17(c), F9 causes a rapid rise in inverter current before blocking. The two current-limiting inductors are inserted in the fault path. The inductor overcurrent relay operates very soon, no more than 200 μs. The instantaneous IGBT peak current of the prototype is 100 A. The inverter current reaches 62 A, still in the safe range.

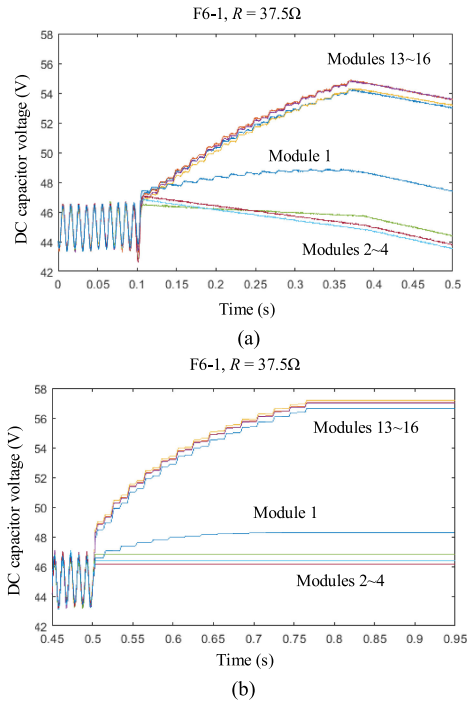

Fig. 18. DC capacitor voltages of different modules. (a) Experimental results. (b) Simulation results.

Eight capacitor voltage waveforms are recorded by AD sampling of the prototype in Fig. 18(a) and (b) is the corresponding simulation results. The maximum capacitor voltage reaches 55 and 57 V, respectively. Module 1 is the first type, modules 13–16 are the second type, and modules 2–4 are the third type. The voltage change of each capacitor is consistent with that in the previous analysis. In the experimental results in Fig. 18(a), the capacitors start to discharge after blocking because of the 18-V auxiliary power circuit inside the modules. In the simulation results in Fig. 18(b), the capacitor voltages remain the same after CBs trip.

The theoretical analysis of fault characteristics and the proposed grounding method are verified by simulation and experimental results.

VIII. Conclusion

This article analyzes the ground fault characteristics of SPCs in two stages. Before blocking, overcurrent and the voltage distortion may result in a wide range of abnormal power supply. After blocking, capacitor overvoltage becomes the primary problem threatening the safety of the faulty SPC because of the energy feeding from other nonfaulty SPCs.

A general fault analysis method based on equivalent circuits is proposed to reflect the influence of module number, fault location, and impedance of fault path. The most serious fault case is obtained through the comparison in various cases to avoid large-scale simulation scanning. F9′ causes the most serious overcurrent before blocking and F7-1 or F7-16 causes the most serious capacitor overvoltage after blocking.

The proposed grounding method can solve the problems of fault current and capacitor overvoltage at the same time. Based on the calculation and simulation results of several typical fault cases, the dimensioning criterion of grounding circuit is provided for reference. Protection strategies are designed to detect and isolate serious faults. Simulation and experimental results verify that the proposed grounding method is beneficial for device safety and system reliability.

Appendix

TABLE I
Parameters of the Simulation System

Parameters	Values
Rated power	20 MW
System frequency	50 Hz
Input transformer ratio	27.5 kV/1.05 kV *16
Output transformer ratio	15.75 kV /27.5 kV
Input transformer leakage reactance	0.07 p.u.
Output transformer leakage reactance	0.06 p.u.
Rated DC capacitor voltage	1.8 kV
Maximum DC capacitor voltage	2.2 kV
Modular number	16
Circuit breaker trip time	50–70 ms
Series inductance	0.4 mH
IGBT repetitive peak collector current	3kA *2
Current-limiting inductor	0.64 mH
Grounding resistor	50 Ω

TABLE II
Parameters of the Scaled-Down Prototype

Parameters	Values
Rated power	7.6 kW
System frequency	50 Hz
Input transformer ratio	380 V/24 V*16
Output transformer ratio	380 V/380 V
Input transformer leakage reactance	0.07 p.u.
Output transformer leakage reactance	0.06 p.u.
Rated capacitor DC voltage	45 V
Maximum DC capacitor voltage	60 V
Modular number	16
Circuit breaker trip time	200–300 ms
Series inductance	0.6 mH
IGBT repetitive peak collector current	50 A
Current-limiting inductor	1 mH
Grounding resistor	37.5 Ω

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