Finite Control Set–Model Predictive Control of H8 Inverter Considering Dead-Time Effect for PMSM Drive Systems With Reduced Conducted Common-Mode EMI and Current Distortions

Won-Sang Jeong, *Student Member, IEEE*, Sung-Hun Kim, *Student Member, IEEE*, Junsin Yi, *Member, IEEE*, and Chung-Yuen Won, *Senior Member, IEEE*

***Abstract*—To reduce the conducted common-mode (CM) electromagnetic interference (EMI) and current total harmonic distortion (THD) in permanent magnet synchronous motor drive systems, this article proposes a finite control set–model predictive control (FCS–MPC) method for an H8 inverter considering the dead-time (DT) effect. In a real system, the DT causes unexpected peak common-mode voltages (CMVs) and distortion of the inverter output voltage, which deteriorates both the CM EMI and current THD. The conventional double active voltage vector (VV) based MPC methods with an H6 inverter may not be a good solution because of the numerous CMV variations and the limit of the VV transitions. In contrast, the proposed FCS–MPC method allows all VV transitions possible without the peak CMVs by instantly operating the series-connected switch of the H8 inverter based on the previous VV, predicted current sector, and next optimal VV. Furthermore, the nonlinearity of the inverter output voltage due to the DT is compensated in a discrete-time model used for the current prediction, considering the calculation delay of the digital controller. Consequently, the current THD as well as the CM EMI can be improved. The simulation and experimental results are presented to verify the effectiveness of the proposed method.**

***Index Terms*—Common-mode electromagnetic interference (EMI), model predictive control (MPC), total harmonic distortion (THD), two-level voltage source inverters (2l-VSIs).**

I. Introduction

RECENTLY, three-phase two-level voltage source inverters (2L-VSIs) have been widely used in various industrial areas, such as photovoltaic grid-connected power systems and motor drives [1]–[3]. In addition, 2L-VSIs have become more efficient and compact with fast switching operations. However, as the switching frequency increases, the common-mode voltage (CMV) issues become critical [4]. In motor drive systems, such as permanent magnet synchronous motor (PMSM) drive systems, the common-mode currents (CMCs) caused by the CMV variations may lead to bearing failures and the common-mode (CM) electromagnetic interference (EMI), thereby affecting the system reliability [5], [6]. Thus, the CMV reduction methods in motor drives have received considerable attention. When compared with 2L-VSIs, multilevel inverters, such as cascaded H-bridge inverters [7] and neutral-point-clamped inverters [8], can reduce the CMVs partially or completely; however, they require a number of power devices and gate drivers, which make the system costly and complicated. This article focuses on 2L-VSIs mainly used in the low- and medium-power drive systems whose the dc-link voltage and power are lower than several hundred volts and several kilowatts, respectively.

One of the widely applied methods for CMV attenuation is the use of a passive [9] or an active [10] CM filter. Passive filters can reduce the *dv/dt* of the CMVs at motor input terminals. However, as the operating switching frequency increases, the passive filters become larger and heavier [11]. Also, an active filter typically adopts a CM transformer of significant size, which increases the system size and weight. To reduce CMVs without additional passive components, various pulsewidth modulation (PWM) based CMV reduction methods have been proposed and are summarized in [12]. Although these methods can reduce the CMVs to a certain extent, they not only require PWM blocks but also degrade the performance of the inverter, such as the linearity of the modulation range.

In recent years, a finite control set–model predictive control (FCS–MPC) has generated significant interest in PMSM drives owing to its simple control concept and rapid dynamic response. Considering all possible switching states of a 2L-VSI, eight voltage vectors (VVs) can be extracted: six active VVs (AVVs) and two zero VVs (ZVVs). The CMV reduction in FCS–MPC could be easily achieved by excluding the use of ZVVs that generate a peak CMV of zero or V_{dc} [13]–[21]. In [13], the optimal VV was selected among only six AVVs to restrict the CMV from $V_{\mathrm{dc}}/3$ to $2V_{\mathrm{dc}}/3$. Furthermore, in [14], the optimal

Manuscript received July 19, 2021; revised October 27, 2021; accepted December 1, 2021. Date of publication December 13, 2021; date of current version January 19, 2022. This work was supported by the Korea Agency for Infrastructure Technology Advancement grant funded by the Ministry of Land, Infrastructure, and Transport under Grant 21RSCD-C160566-01. Recommended for publication by Associate Editor R. Kennel. *(Corresponding author: Chung-Yuen Won.)*

The authors are with the Department of Electronic and Electrical Engineering, School of Information and Communication Engineering, Sungkyunkwan University, Suwon 440-746, South Korea (e-mail: ho92po@skku.edu; regar14@skku.edu; junsin@skku.edu; woncy@skku.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3134255.

Digital Object Identifier 10.1109/TPEL.2021.3134255

VV was selected among four preselected AVVs to reduce the switching loss and computational effort. However, the methods in [13] and [14] do not consider the dead-time (DT) effect. In actual 2L-VSIs, the DT should be inserted between the gate signals of two switches in a leg to prevent a short circuit. Unfortunately, the DT can cause unexpected peak CMV of zero or $V_{\rm dc}$, as well as the distortion of the output voltage.

To completely eliminate the peak CMVs even at the DT, the MPC method was modified in [15]–[21]. In [15], the two-leg-changed AVV transitions, which can cause the peak CMVs during the DT, were excluded. However, the reduced number of available VVs leads to an increase in the current total harmonic distortion (THD). To reduce the increased current THD with the restricted CMVs, a hybrid-AVV preselection-based MPC was proposed in [18], which can add one more available AVV depending on the current sector (CS). In [19], a hybrid-synthesized AVV preselection-based MPC, which utilizes two adjacent AVVs during one sampling period, was proposed to further improve the current THD, compared with that reported in [18]. Unfortunately, the methods in [18] and [19] require complicated VV preselection algorithms. Similar to [19], a double AVV (DAVV) based MPC with the optimal distributed time was proposed in [20] and [21] to improve the current THD without using ZVVs. However, the computational burden is rapidly increased to calculate the optimal distributed time. Particularly, the CMCs and CM EMI significantly increase in the DAVV-based MPC methods in [19]–[21] because of the large number of CMV variations.

In summary, the conventional modified MPC methods have the following disadvantages.

1) Increased current THD due to the absence of ZVVs with reduced number of available AVVs [15].
2) Increased control complexity because of the complicated VV preselection algorithms [18], [19].
3) High CMCs and CM EMI due to the large number of CMV variations [19]–[21].
4) Huge computational burden [20], [21].

From another perspective, CMVs can be inherently reduced by modifying inverter topologies [22]–[29]. In [22] and [23], a four-leg inverter, for which a fourth leg is added to the traditional H6 inverter, was used to reduce the CMVs. In [24], an H10 inverter comprising ten power devices was proposed to achieve constant or zero CMV. However, the four-leg inverter again requires an additional *LC* filter, and the H10 inverter requires many power devices with multiple dc sources.

Recently, studies have focused on H8 inverter topologies considering the tradeoff between the CMV reduction capability, power density, and economic efficiency [25]–[29]. As shown in Fig. 1(a), an H8 inverter has only two additional switches between the dc-link and the traditional H6 inverter. The peak CMVs at the ZVVs can be reduced by appropriately turning OFF the series-connected switches. Traditionally, NAND- [26], [27] and OR- [28], [29] gate-based logics have been used to control the series-connected switches. However, a NAND-gate-based logic cannot reduce the peak CMVs during the DT when entering and leaving the ZVV. Although an OR-gate-based logic reduces the peak CMVs at the ZVVs, it was considered only for the operations entering and leaving the ZVVs; the peak CMVs are still generated at the two-leg-changed AVV transitions.

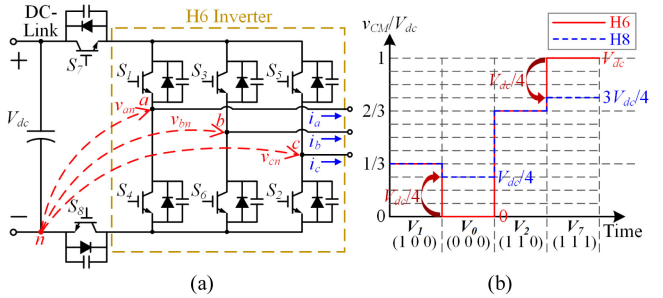

Fig. 1. (a) Circuit configuration of H8 inverter. (b) Comparison of CMV waveforms between H6 and H8 inverters.

This article proposes an FCS–MPC method for an H8 inverter with the optimal operation of the series-connected switch, which can reduce the peak CMVs without a complex control algorithm and a large computational burden. Unlike the traditional FCS–MPC, the proposed method instantly operates the series-connected switches based on three factors: the previous VV; predicted CS; and next optimal VV, and thus, eliminates the peak CMVs even at all VV transitions. In addition, the nonlinearity of the inverter output voltage due to DT is compensated in a discrete-time model of the current prediction while considering the calculation delay of the digital controller. As a result, along with accurate current prediction, the current THD can be considerably improved over the entire operating condition. The effectiveness of the proposed method was verified using numerous simulation and experimental results.

The rest of this article is organized as follows. Section II reviews the conventional gate logics for an H8 inverter. Section III presents the proposed FCS–MPC method in detail. The simulation and experimental results are given in Sections IV and V, respectively. Finally, Section VI concludes this article.

II. Review of Conventional Control Methods for H8 Inverter

A CMV $v_{\rm CM}$ can be calculated using the inverter output voltages v_{an}, v_{bn}, and v_{cn} as follows:

$$v_{\rm CM} = (v_{an} + v_{bn} + v_{cn})/3. \tag{1}$$

Both the magnitude of and variation in $v_{\rm CM}$ should be reduced to suppress the CMCs and the CM EMI. A peak CMV of zero or $V_{\rm dc}$ is inevitably generated at the ZVV in the traditional H6 inverter, whereas the H8 inverter in Fig. 1(a) can reduce the peak CMVs using the series-connected switches S_7 and S_8. At $\boldsymbol{V_0}$, the switches S_1, S_3, and S_5 are turned OFF, whereas the switches S_4, S_6, and S_2 are turned ON. Thus, the inverter output terminals are tied to the lower side of the inverter. At that time, to float the output terminals from the negative side of the dc-link, S_8 is turend OFF. In this case, the output voltages and $v_{\rm CM}$ can be calculated based on the complex frequency-domain model [28]. If the inherent junction capacitors of all switches (S_1–S_8) are the

TABLE I
COMPARISON OF CMV BETWEEN H6 AND H8 INVERTERS

Voltage Vector		(F_a, F_b, F_c)[1)]	CMV	
			H6 Inverter	H8 Inverter
ZVV	V_0	(0, 0, 0)	0	$V_{dc}/4$
AVV	V_1	(1, 0, 0)	$V_{dc}/3$	$V_{dc}/3$
	V_2	(1, 1, 0)	$2V_{dc}/3$	$2V_{dc}/3$
	V_3	(0, 1, 0)	$V_{dc}/3$	$V_{dc}/3$
	V_4	(0, 1, 1)	$2V_{dc}/3$	$2V_{dc}/3$
	V_5	(0, 0, 1)	$V_{dc}/3$	$V_{dc}/3$
	V_6	(1, 0, 1)	$2V_{dc}/3$	$2V_{dc}/3$
ZVV	V_7	(1, 1, 1)	V_{dc}	$3V_{dc}/4$

[1)] $F_{x\ (x=a,\ b,\ c)}$ is switching function at each leg: "1" is case where upper switch is in ON-state and lower switch is in OFF-state, and "0" is opposite case.

TABLE II
CMV VARIATIONS BETWEEN TWO VVS FOR H6 AND H8 INVERTERS

Voltage Vector Transition	Magnitude of CMV Variation	
	H6 Inverter	H8 Inverter
AVV to AVV	0 or $V_{dc}/3$	0 or $V_{dc}/3$
AVV to ZVV[1)]	$V_{dc}/3$	$V_{dc}/12$
ZVV to AVV[2)]	$V_{dc}/3$ or $2V_{dc}/3$	$V_{dc}/12$ or $5V_{dc}/12$

[1)] Assume that odd number AVV (V_1, V_3, and V_5) is always changed to V_0, whereas even number AVV (V_2, V_4, and V_6) is changed to V_7 in order to reduce redundant switching operations.
[2)] Assume that any ZVV can be changed to any AVV.

same, $v_{\rm CM}$ becomes $V_{\rm dc}/4$ at V_0. Similarly, S_7 is turned OFF at V_7 to float the inverter output terminals from the positive side of the dc-link, and $v_{\rm CM}$ becomes $3V_{\rm dc}/4$. Table I gives a comparison of $v_{\rm CM}$ between the H6 and H8 inverters, and Fig. 1(b) depicts an example of their waveforms. The magnitude of CMV at the ZVV can be reduced in the H8 inverter. In addition, Table II gives the CMV variations between two VVs for H6 and H8 inverters. As given in Table II, the H8 inverter can also reduce the CMV variations between the AVV and ZVV in an ideal case. However, in an actual system, the DT bewteen two VVs may cause unexpected peak CMVs with additional CMV variations.

To completely eliminate the peak CMVs, the timing of turning ON/OFF of S_7 and S_8 is important in the H8 inverter. As a conventional control method for S_7 and S_8, a NAND-gate-based logic ($G_7 = \overline{G_1 \cdot G_3 \cdot G_5}$ and $G_8 = \overline{G_2 \cdot G_4 \cdot G_6}$ is proposed, as shown in Fig. 2(a), where $G_{i\ (i\ =\ 1,\ 2,\ ..,\ 8)}$ is the gate signal of the switch S_i. Unfortunately, the NAND logic can cause the peak CMVs when entering and leaving the ZVV depending on the CS. For example, a VV transition is assumed from V_1 to V_0 when the polarities of the three-phase current are $i_a > 0$, $i_b < 0$, and $i_c > 0$. The equivalent circuit at V_1 is shown in Fig. 2(c). In this circuit configuration, S_1 is turned OFF during the DT to change the a-phase switching state, and then i_a starts to discharge the junction capacitor of S_4, as shown in Fig. 2(d). As G_4 is at a low level during the DT, S_8 maintains the ON-state via the NAND logic in Fig. 2(a), thus decreasing $v_{\rm CM}$ to the peak value of zero.

As another conventional control method for S_7 and S_8, an OR-gate-based logic ($G_7 = G_2 + G_4 + G_6$ and $G_8 = G_1 + G_3 + G_5$) is proposed, as shown in Fig. 2(b). For the same VV transition, S_8 is turned OFF at the start of the DT because the gate signals of G_1, G_3, and G_5 become low. Thus, $v_{\rm CM}$ does not decrease to zero because of the charged voltage of S_8, as shown in Fig. 2(e). However, the operation was considered only when entering and leaving the ZVVs. The two-leg-changed AVV transitions can still cause unexpected peak CMVs. An example of a vector transition between V_1 and V_5 is shown in Fig. 2(f), where a peak CMV of zero is generated during the DT. To optimally control S_7/S_8 not only when entering and leaving the ZVV but also at the transition between two AVVs, instant CS information is required, which is difficult in the traditional FCS–MPC algorithm because of sensing and calculation delays. Even the exclusion of the two-leg-changed AVV transitions to avoid the peak CMVs deteriorates the current THD in FCS–MPC.

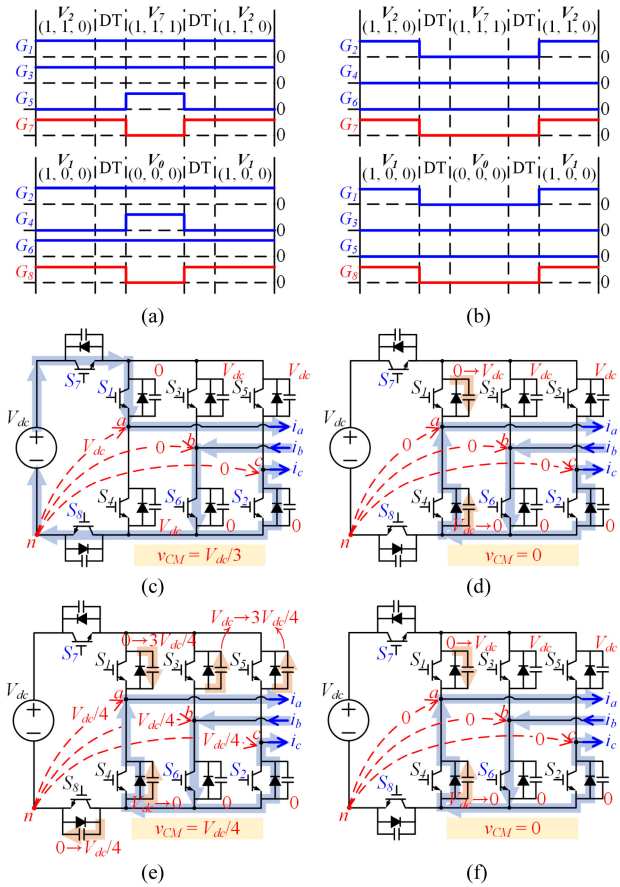

Fig. 2. (a) NAND-gate-based logic [26], [27]. (b) OR-gate-based logic [28], [29]. (c)–(f) Equivalent circuits of H8 inverter when $i_a > 0$, $i_b < 0$, and $i_c > 0$. (c) At V_1. (d) At DT between V_1 and V_0 with NAND-gate-based logic. (e) At DT between V_1 and V_0 with OR-gate-based logic. (f) At DT between V_1 and V_5.

III. PROPOSED FINITE CONTROL SET–MODEL PREDICTIVE CONTROL OF H8 INVERTER

The proposed FCS–MPC method optimally controls the series-connected switches based on the previous VV, predicted CS, and next optimal VV. First, the conditions generating peak

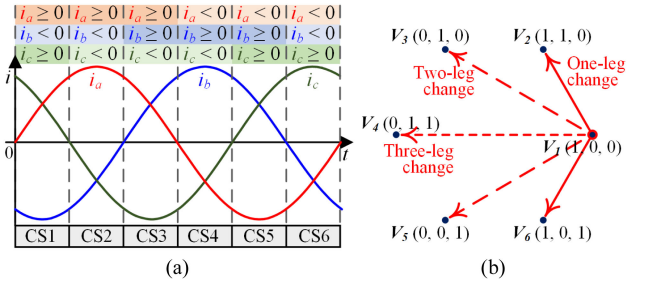

Fig. 3. (a) Definition of CS. (b) Example of vector transition between AVVs.

CMVs during the DT are investigated based on the CS and VV transition cases. Subsequently, the operation of the series-connected switches eliminating peak CMVs is established. Second, a compensation method for the nonlinearity of the inverter output voltage due to the DT is proposed considering the calculation delay of the digital controller.

A. Common–Mode Voltage During Dead–Time

As given in Table I, the CMV at a particular VV is simply determined by the switching state of the VV, whereas that generated during the DT depends on both the CS and the switching state at the instant. Even the switching state during the DT differs according to the previous and next VVs. Therefore, the CMV-generated pattern during the DT should be investigated, particularly between the AVVs, to determine when the peak CMVs is generated.

The definition of the CS depending on the current polarity and an example of a vector transition between AVVs are shown in Fig. 3(a) and (b), respectively. In the case of the one-leg-changed vector transition, a peak CMV of zero or $V_{\rm dc}$ is not generated regardless of the CS because one switch always turns ON at each upper and lower side among the three legs. For example, for the transition from $\boldsymbol{V_1}$ to $\boldsymbol{V_2}$ in Fig. 3(b), the upper switch of the a-phase and the lower switch of the c-phase maintain the ON-state during the DT. In addition, a vector transition changing all three legs, such as from $\boldsymbol{V_1}$ to $\boldsymbol{V_4}$, does not generate a peak CMV because the inverter operates as a three-phase diode rectifier during the DT. On the other hand, the peak CMVs can be generated in the case of a two-leg-changed transition, such as $\boldsymbol{V_1}$ to $\boldsymbol{V_3}$. Fig. 4 shows the three cases of the transition between $\boldsymbol{V_1}$ and $\boldsymbol{V_3}$ depending on the CS.

1) *Transition between Powering and Regenerating VVs [see Fig. 4(a)–(c)]:* In CS1, AVV $\boldsymbol{V_1}$ transfers the power from the dc-link to the ac load [see Fig. 4(a)]; hence, $\boldsymbol{V_1}$ becomes the powering VV in this CS. In contrast, AVV $\boldsymbol{V_3}$ transfers the power in the reverse direction, i.e., from the ac load to the dc-link [see Fig. 4(c)]; hence, $\boldsymbol{V_3}$ becomes the regenerating VV. When the transition occurs from $\boldsymbol{V_1}$ to $\boldsymbol{V_3}$, all switches in the a- and b-phases turn OFF during the DT, as shown in Fig. 4(b). Accordingly, currents i_a and i_b flow through the anti-parallel diode at each leg, which inverts both output voltages in the a- and b-phases, respectively. The current path during the DT is the same as that of the regenerating VV $\boldsymbol{V_3}$, thus generating the CMV of $V_{dc}/3$. This is similar to the other two-leg-changed transitions between the powering and regenerating VVs, i.e., the CMV at the DT is always the same as that of the regenerating VV.

2) *Transition between Powering VVs [see Fig. 4(d)–(f)]:* In CS3, both $\boldsymbol{V_1}$ and $\boldsymbol{V_3}$ become the powering VVs, as shown in Fig. 4(d) and (f), respectively. During the transition from $\boldsymbol{V_1}$ to $\boldsymbol{V_3}$, the output voltage in the a-phase leg, which is the one between the two changed legs, is inverted in the direction of generating a peak CMV of zero during the DT [see Fig. 4(e)]. Similarly, whenever a two-leg-changed transition occurs between the powering VVs, a peak CMV is generated during the DT because the output voltage in one leg between the two changed legs becomes the same as that of the remaining two legs.

3) *Transition between Regenerating VVs [see Fig. 4(g)–(i)]:* Both $\boldsymbol{V_1}$ and $\boldsymbol{V_3}$ become the regenerating VVs in CS6, as shown in Fig. 4(g) and (i), respectively. In this case, the output voltage in one leg between the two changed legs is inverted during the DT, similar to the transition between the powering VVs. However, a peak CMV is not generated because the output voltage is changed opposite to that of the unchanged leg. For example, in Fig. 4(h), the b-phase output voltage becomes $V_{\rm dc}$ during the DT, opposite to the c-phase output voltage, and a peak CMV is not generated.

TABLE III
CMV-GENERATED PATTERN DURING DT BETWEEN AVVS

Vector Transition between AVVs		CMV Generated during DT
One-Leg Change		$V_{dc}/3$ or $2V_{dc}/3$
Two-Leg Change[1)]	$\boldsymbol{V_P} \leftrightarrow \boldsymbol{V_R}$	$V_{dc}/3$ or $2V_{dc}/3$
	$\boldsymbol{V_P} \leftrightarrow \boldsymbol{V_P}$	0 or V_{dc}
	$\boldsymbol{V_R} \leftrightarrow \boldsymbol{V_R}$	$V_{dc}/3$ or $2V_{dc}/3$
Three-Leg Change		$V_{dc}/3$ or $2V_{dc}/3$

[1)] $\boldsymbol{V_P}$ **and** $\boldsymbol{V_R}$ denote powering and regenerating VVs, respectively.

Table III gives the CMV-generated patterns during the DT between the AVVs. In all AVV transition cases, a peak CMV of zero or $V_{\rm dc}$ is generated only at the two-leg-changed transition between the powering VVs, where appropriate control of the series-connected switches is required to allow all AVV transitions without peak CMVs. As indicated in Fig. 4, the powering and regenerating VVs are changed depending on the CS. Table IV gives the powering and regenerating VVs based on the CS with the operation of S_7/S_8 to eliminate the peak CMVs.

B. Compensation Method for Accurate Current Prediction

As previously mentioned, because the powering and regenerating VVs are determined depending on the CS, and this is related to the generation of the peak CMVs at the DT, accurate CS detection at that moment is required. However, in the traditional FCS–MPC algorithm, the instantaneous CS detection and operation of S_7/S_8 are difficult because of the delay in the sensing and calculation processes of a digital controller. The

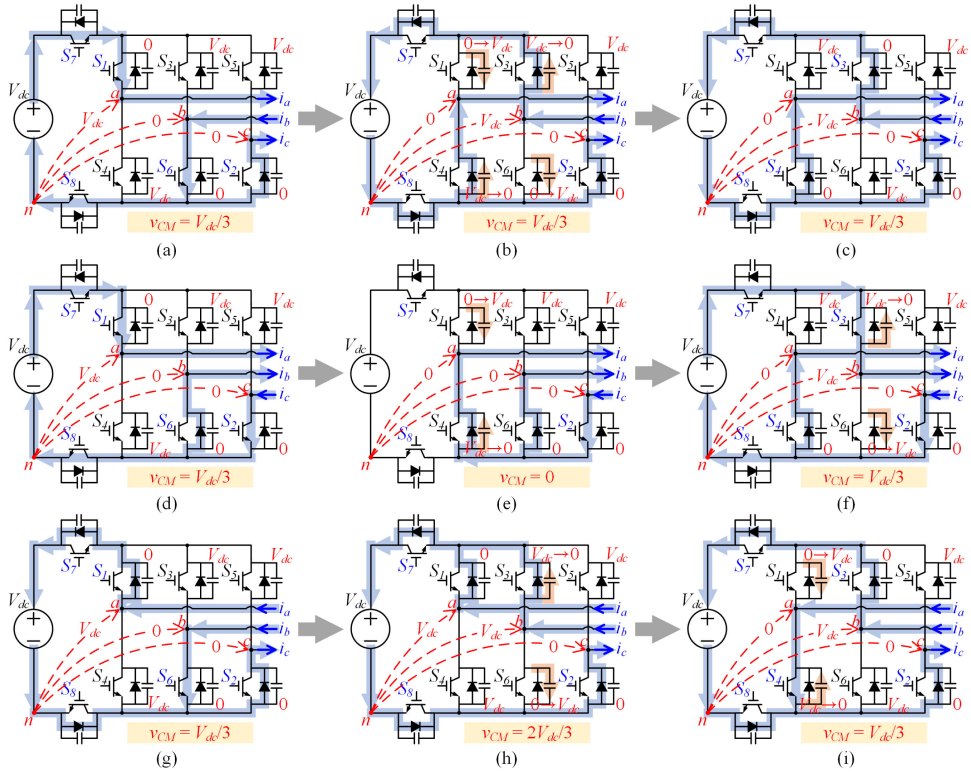

Fig. 4. Three cases of transition between V_1 and V_3 depending on CS. (a)–(c) CS1. (d)–(f) CS3. (g)–(i) CS6.

TABLE IV
POWERING AND REGENERATING AVVS DEPENDING ON CS

	Powering VV	Regenerating VV	Generated Peak CMV	S_7/S_8 Operation
CS1	V_1, V_5, V_6	V_2, V_3, V_4	0 at $V_1 \leftrightarrow V_5$	S_7 ON/S_8 OFF
CS2	V_1, V_2, V_6	V_3, V_4, V_5	V_{dc} at $V_2 \leftrightarrow V_6$	S_7 OFF/S_8 ON
CS3	V_1, V_2, V_3	V_4, V_5, V_6	0 at $V_1 \leftrightarrow V_3$	S_7 ON/S_8 OFF
CS4	V_2, V_3, V_4	V_1, V_5, V_6	V_{dc} at $V_2 \leftrightarrow V_4$	S_7 OFF/S_8 ON
CS5	V_3, V_4, V_5	V_1, V_2, V_6	0 at $V_3 \leftrightarrow V_5$	S_7 ON/S_8 OFF
CS6	V_4, V_5, V_6	V_1, V_2, V_3	V_{dc} at $V_4 \leftrightarrow V_6$	S_7 OFF/S_8 ON

delayed operation of S_7/S_8 may cause peak CMVs. To solve the above problems, the proposed method detects the CS based on the predicted currents in FCS–MPC algorithm and instantly operates S_7/S_8 at the CS instant. Besides, the nonlinearity of the inverter output voltage during the DT is compensated to detect the CS accurately and further improve the current THD.

The sampling sequence of the proposed FCS–MPC is illustrated in Fig. 5. For simplicity, only the α-axis current i_α in the stationary reference frame is considered. The β-axis current i_β is controlled similarly. The red solid line represents the reference current, and the blue solid and dashed lines represent the actual and predicted currents, respectively. At the start of the $[k]$th sequence, the current $i_\alpha[k]$ is measured, and the optimal VV $V_{\alpha\_\mathrm{opt}}[k]$ previously selected in the $[k-1]$th sequence is applied. Based on $i_\alpha[k]$ and $V_{\alpha\_\mathrm{opt}}[k]$, the current $i^p_{\alpha d}[k]$ at the $[k]$-th DT can be predicted using a discrete-time model. When $\boldsymbol{i}_{\alpha\beta}[k] = [i_\alpha[k]\ i_\beta[k]]^\mathrm{T}$, $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k] = [V_{\alpha\_\mathrm{opt}}[k]\ V_{\beta\_\mathrm{opt}}[k]]^\mathrm{T}$, and the back electromotive force (EMF) $\boldsymbol{e}_{\alpha\beta}[k] = [e_\alpha[k]\ e_\beta[k]]^\mathrm{T}$, the predicted current $\boldsymbol{i}^{\boldsymbol{p}}_{\boldsymbol{\alpha\beta d}}[k] = [i^p_{\alpha d}[k]\ i^p_{\beta d}[k]]^T$ is

$$i^p_{\alpha\beta d}[k] = \left(1 - \frac{R_s\,(1-d)\,T_s}{L_s}\right)\cdot i_{\alpha\beta}[k] + \frac{(1-d)\,T_s}{L_s}\cdot\left(V_{\alpha\beta\_opt}[k] + e_{\alpha\beta}[k]\right), \quad (2)$$

where R_s, L_s, T_s, and d are the stator resistance, stator inductance, sampling period, and DT ratio within T_s, respectively. In (2), since $\boldsymbol{i}_{\alpha\beta}[k]$ is measured after the $[k-1]$-th DT and the applied time (AT) of $\boldsymbol{V}_{\alpha\beta\_\boldsymbol{opt}}[k]$ is considered as $(1\text{-}d)T_s$ excluding the DT interval, the DT effect can be eliminated in the current prediction of $\boldsymbol{i}^{\boldsymbol{p}}_{\boldsymbol{\alpha\beta d}}[k]$. Based on $\boldsymbol{i}^{\boldsymbol{p}}_{\boldsymbol{\alpha\beta d}}[k]$, the CS at the $[k]$-th DT is predicted in advance, and S_7/S_8 can be instantly operated at that time according to the CS.

Based on Fig. 5, $i^p_{\alpha d}[k]$ is also used in the prediction of current $i^p_{\alpha d}[k+1]$ at the $[k+1]$th DT, considering all possible $V_\alpha[k+1]$. However, $V_{\alpha d}[k]$ during the $[k]$th DT causes the nonlinearity of inverter output voltage, affecting the trajectory of i_α. This nonlinearity should be considered for accurate prediction of $\boldsymbol{i}^{\boldsymbol{p}}_{\boldsymbol{\alpha\beta d}}[k+1]$. The current $\boldsymbol{i}^{\boldsymbol{p}}_{\boldsymbol{\alpha\beta}}[k+1] = [i^p_\alpha[k+1]\ i^p_\beta[k+1]]^\mathrm{T}$ after the $[k]$th DT can be calculated as follows:

$$i^p_{\alpha\beta}[k+1] = \left(1 - \frac{R_s dT_s}{L_s}\right)\cdot i^p_{\alpha\beta d}[k] + \frac{dT_s}{L_s}\cdot\left(V_{\alpha\beta d}[k] + e_{\alpha\beta}[k]\right) \quad (3)$$

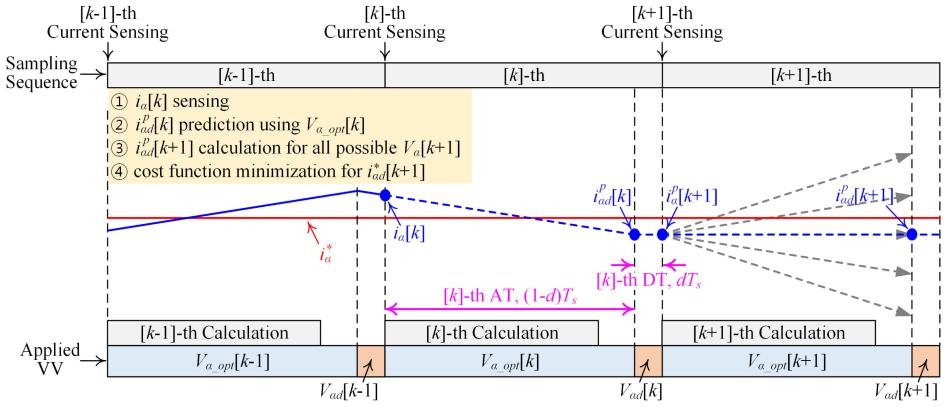

Fig. 5. Sampling sequence of proposed FCS–MPC considering calculation delay and nonlinearity of inverter output voltage due to DT.

where $\boldsymbol{V}_{\alpha\beta d}[k]$ is the equivalent VV during the $[k]$th DT, which is determined by $\boldsymbol{V}_{\alpha\beta\_opt}[k]$, CS, and $\boldsymbol{V}_{\alpha\beta}[k+1]$. Then, $\boldsymbol{i^p_{\alpha\beta d}}[k+1]$ can be estimated using $\boldsymbol{i^p_{\alpha\beta}}[k+1]$ for all possible $\boldsymbol{V}_{\alpha\beta}[k+1]$ as follows:

$$i^p_{\alpha\beta d}[k+1] = \left(1 - \frac{R_s\,(1-d)\,T_s}{L_s}\right) \cdot i^p_{\alpha\beta}[k+1] + \frac{(1-d)\,T_s}{L_s} \cdot \left(V_{\alpha\beta}[k+1] + e_{\alpha\beta}[k+1]\right). \tag{4}$$

By substituting (3) into (4) and neglecting the term multiplied by the square of T_s, $\boldsymbol{i^p_{\alpha\beta d}}[k+1]$ expressed by $\boldsymbol{i^p_{\alpha\beta d}}[k]$ can be calculated as follows:

$$i^p_{\alpha\beta d}[k+1] = \left(1 - \frac{R_s T_s}{L_s}\right) \cdot i^p_{\alpha\beta d}[k] + \frac{T_s}{L_s} \cdot \left(dV_{\alpha\beta d}[k] + (1-d)\,V_{\alpha\beta}[k+1] + e_{\alpha\beta}[k+1]\right). \tag{5}$$

The back EMF $\boldsymbol{e}_{\alpha\beta}[k+1]$ can be simply assumed to be equal to $\boldsymbol{e}_{\alpha\beta}[k]$ when the sampling frequency f_s is much higher than the back EMF frequency [30]. In PMSM drives, $\boldsymbol{e}_{\alpha\beta}[k]$ can be expressed as

$$e_{\alpha\beta}[k+1] \simeq e_{\alpha\beta}[k] = \begin{bmatrix} e_\alpha[k] \\ e_\beta[k] \end{bmatrix} = \psi_m \omega_r \begin{bmatrix} \sin\left(\theta_r\,[k]\right) \\ -\cos\left(\theta_r\,[k]\right) \end{bmatrix} \tag{6}$$

where ψ_m, ω_r, and θ_r are the flux magnitude, electric angular speed, and electric angular position of the rotor, respectively.

For comparison, the predicted currents at the $[k]$th sequence in the traditional FCS–MPC are expressed as follows:

$$i^p_{\alpha\beta}[k+1] = \left(1 - \frac{R_s T_s}{L_s}\right) \cdot i_{\alpha\beta}[k] + \frac{T_s}{L_s} \cdot \left(V_{\alpha\beta\_opt}[k] + e_{\alpha\beta}[k]\right) \tag{7}$$

$$i^p_{\alpha\beta}[k+2] = \left(1 - \frac{R_s T_s}{L_s}\right) \cdot i^p_{\alpha\beta}[k+1] + \frac{T_s}{L_s} \cdot \left(V_{\alpha\beta}[k+1] + e_{\alpha\beta}[k+1]\right). \tag{8}$$

As can be inferred from Fig. 5, $\boldsymbol{i^p_{\alpha\beta}}[k+1]$ and $\boldsymbol{i^p_{\alpha\beta}}[k+2]$ in the traditional FCS–MPC correspond to $\boldsymbol{i^p_{\alpha\beta d}}[k]$ and $\boldsymbol{i^p_{\alpha\beta d}}[k+1]$ in the proposed method, respectively. It is worth mentioning that only one term of $d\boldsymbol{V}_{\alpha\beta d}[k]$ is added in (5) compared with (8), which barely increases the additional calculation load, whereas the nonlinearity of the inverter output voltage due to the DT is simply compensated. The value of $\boldsymbol{V}_{\alpha\beta d}[k]$ can be obtained using the lookup table in a digital controller, as given in Appendix A.

The cost function g, which is defined as the error between the reference and predicted currents, is expressed in the proposed method as follows:

$$g = \left(i^*_{\alpha d}\,[k+1] - i^p_{\alpha d}\,[k+1]\right)^2 + \left(i^*_{\beta d}\,[k+1] - i^p_{\beta d}\,[k+1]\right)^2. \tag{9}$$

As indicated in (9), the proposed method uses the reference current $\boldsymbol{i^*_{\alpha\beta d}}[k+1]$ and predicted current $\boldsymbol{i^p_{\alpha\beta d}}[k+1]$, whereas $\boldsymbol{i^*_{\alpha\beta}}[k+2]$ and $\boldsymbol{i^p_{\alpha\beta}}[k+2]$ are used in the cost function of the traditional FCS–MPC method. By evaluating g for all possible $\boldsymbol{V}_{\alpha\beta}[k+1]$, the optimal VV $\boldsymbol{V}_{\alpha\beta\_opt}[k+1]$ minimizing the current error can be selected and applied in the $[k+1]$th sequence.

C. Implementation of Proposed FCS–MPC Method

Based on the $[k]$th sequence, the control block diagram and flowchart of the proposed FCS–MPC method are shown in Figs. 6 and 7, respectively. Although the proposed method is implemented based on a PMSM drive system in this article, it can also be implemented with an *R–L* load by neglecting the back EMF. In Fig. 6, the control block diagram is divided into two parts: a current prediction and cost function minimization part, and a switching signal generation part. In the former, $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k+1]$ is selected based on predicted currents $\boldsymbol{i^p_{\alpha\beta d}}[k]$ and $\boldsymbol{i^p_{\alpha\beta d}}[k+1]$. In the latter, the switching signals of the H8 inverter at the $[k]$th DT and the $[k+1]$th AT are determined. Because the CS is detected based on $\boldsymbol{i^p_{\alpha\beta d}}[k]$, the switching state at the $[k]$th DT, which should consider $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k]$, the CS, and $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k+1]$, can be predetermined. At the start of the DT or AT, the digital controller applies the corresponding switching state to the H8 inverter. Consequently, the instant operation of

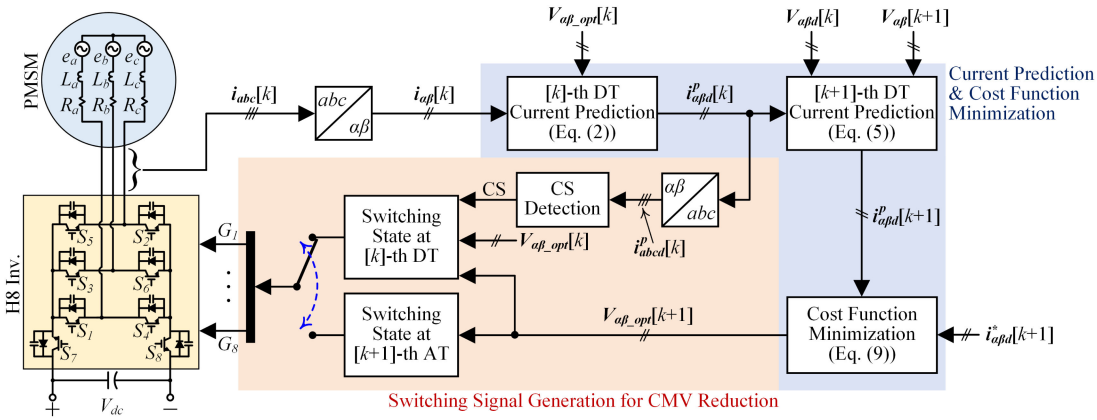

Fig. 6. Control block diagram of proposed FCS–MPC method.

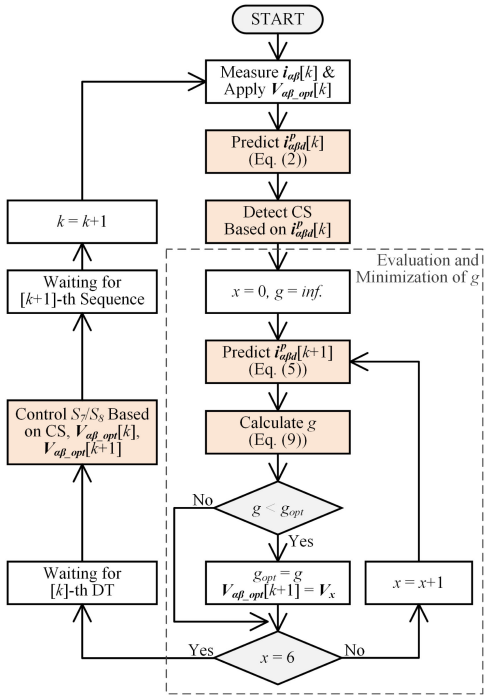

Fig. 7. Flowchart of proposed FCS–MPC method.

S_7/S_8 becomes possible, which can eliminate the peak CMVs even at all VV transitions.

In Fig. 7, g is evaluated as defined in (9) for seven VVs ($\boldsymbol{V_0}$–$\boldsymbol{V_6}$) to obtain $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k+1]$. If g is minimized when $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k+1] = \boldsymbol{V_0}$, $\boldsymbol{V_0}$ or $\boldsymbol{V_7}$ is selected as $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k+1]$ based on $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k]$: $\boldsymbol{V_0}$ is selected when $\boldsymbol{V}_{\alpha\beta\_\mathbf{opt}}[k] = \boldsymbol{V_0}$ or an odd number AVVs, or $\boldsymbol{V_7}$ is selected otherwise. When $\boldsymbol{V_0}$ ($\boldsymbol{V_7}$) is applied at the $[k+1]$th AT, the digital controller turns OFF S_8 (S_7) from the start of the $[k]$th DT to the end of the $[k+1]$th DT, as shown in Fig. 2(b). This ensures reduction of the peak CMVs, regardless of their occurrence during the DT.

Because the proposed FCS–MPC allows all VV transitions, the current THD can be improved without a complex control algorithm, unlike the DAVV MPC method. In particular, the CM EMI caused by CMV variations can be significantly reduced because only one VV is applied in each sampling sequence.

TABLE V
PARAMETERS OF H8 INVERTER AND SPMSM

Parameter		Description	Value	Unit
H8 Inverter	V_{dc}	DC-Link Voltage	70	V
	f_s	Sampling Frequency	20	kHz
	T_s	Sampling Period	50	μs
	d	DT Ratio	0.12	-
	S_i	RGTH40TK65D	-	-
SPMSM	P_{rated}	Rated Power	750	W
	I_{rated}	Rated RMS Current	4.4	A
	T_{rated}	Rated Torque	2.39	N·m
	p	The Number of Poles	10	-
	R_s	Stator Resistance	0.633	Ω
	L_s	Stator Inductance	2.08	mH
	V_{pk}/kr/min	Peak Line-to-Line Back EMF Constant	45	V/kr/min

IV. SIMULATION RESULTS

To verify the performance of the proposed FCS–MPC method, simulation was conducted using Powersim software. The parameters of the H8 inverter and the surface mounted PMSM (SPMSM) are given in Table V. As the series-connected switches in the proposed method should be turned OFF and ON during a particular DT interval, d was sufficiently set as 0.12 (6 μs at $T_s = 50$ μs). Although DT interval in the proposed method is set relatively larger than the traditional one (2–5 μs), it does not affect current prediction error and current THD because the DT effect is compensated. The parasitic components, such as parasitic inductance and capacitance, were also considered in the simulation circuit. For comparison, the DAVV MPC method [19] as well as the traditional FCS–MPC method in the H8 inverter with NAND- [26], [27] and OR- [28], [29] gate-based logics were also simulated.

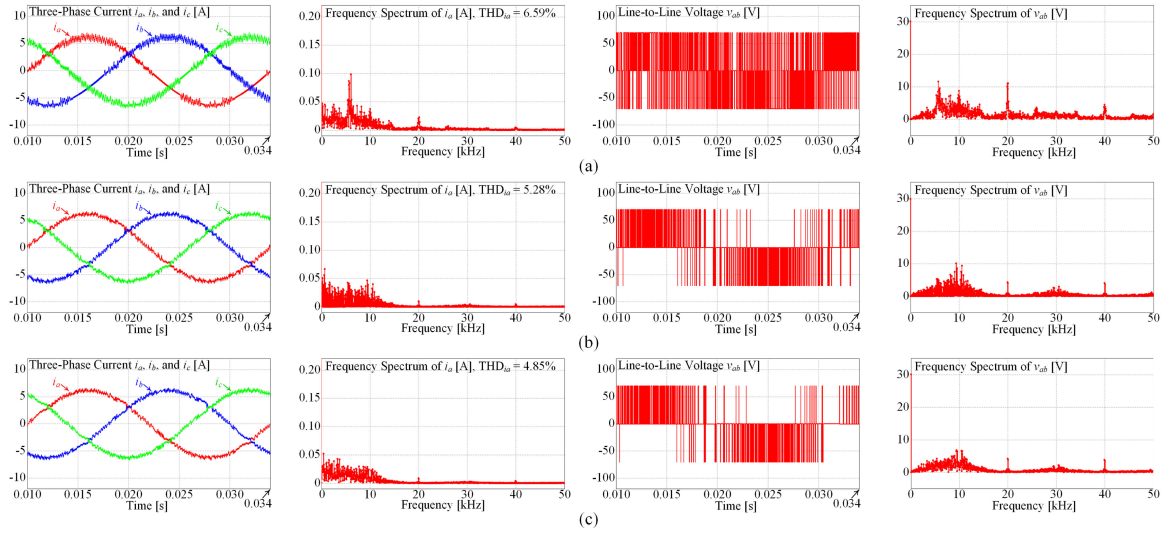

Fig. 8. Simulation results of three-phase current and line-to-line voltage at rated current (6.22 A_{peak}) and rotor speed of 500 r/min. (a) DAVV MPC method. (b) Traditional FCS–MPC method. (d) Proposed FCS–MPC method.

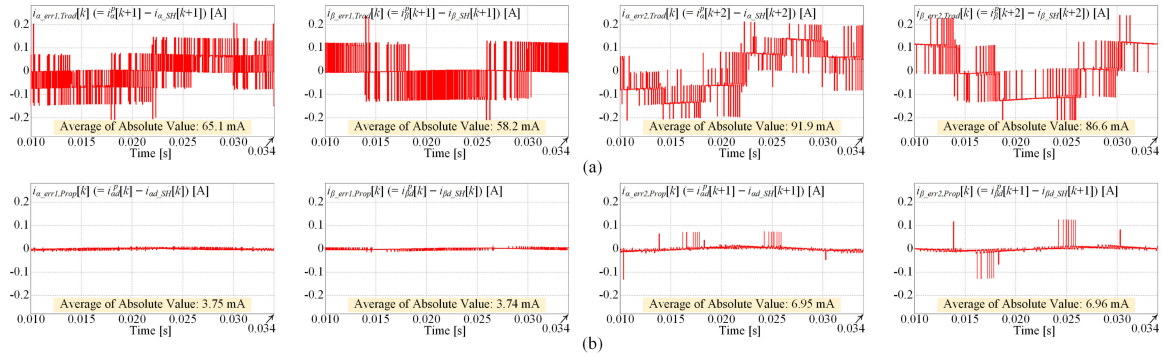

Fig. 9. Simulation results of predicted current errors at rated current and rotor speed of 500 r/min. (a) Traditional FCS–MPC method. (b) Proposed FCS–MPC method.

A. Current THD and Predicted Current Error

The simulation results of the three-phase current and line-to-line voltage with their frequency spectra are shown in Fig. 8. The current THD of i_a was calculated as follows:

$$\%\mathrm{THD}_{ia} = \sqrt{\left(\sum_{n>1}^{\infty} i_{an,\mathrm{rms}}^2\right) / i_{a1,\mathrm{rms}}^2} \cdot 100 \qquad (10)$$

where $i_{a1,\mathrm{rms}}$ and $i_{an,\mathrm{rms}}$ are the root-mean-square (RMS) values of the fundamental and $[n]$th harmonic components of i_a, respectively. As shown in Fig. 8(a), the DAVV MPC method exhibits the highest current THD compared with the other methods while generating an undesirable bipolar line-to-line voltage. This is because a ZVV was replaced by a VV synthesized using one or two AVVs. Even a synthesized VV should be preselected depending on the CS to avoid the peak CMVs during the DT, which indicates that the optimal one minimizing the current error may not be selected.

On the other hand, the traditional and proposed FCS–MPC methods mostly generate unipolar line-to-line voltages owing to the use of ZVVs. In this case, the proposed method further reduces the harmonic components in both the line-to-line voltage and current compared with that of the traditional FCS–MPC.

The compensation of the proposed method also reduces the prediction current errors. Fig. 9 shows a comparison of the predicted current errors between the traditional and proposed FCS–MPC methods. In each case, for reasonable comparison, two current errors $\boldsymbol{i}_{\alpha\beta\_\mathbf{err1}}[k]$ and $\boldsymbol{i}_{\alpha\beta\_\mathbf{err2}}[k]$ are defined differently as follows (referring to (7), (8) for the traditional FCS–MPC and (2), (5) for the proposed FCS–MPC)

$$\begin{cases} i_{\alpha\beta\_\mathrm{err1,Trad}}[k] = i_{\alpha\beta}^{p}[k+1] - i_{\alpha\beta\_SH}[k+1] \\ i_{\alpha\beta\_\mathrm{err2,Trad}}[k] = i_{\alpha\beta}^{p}[k+2] - i_{\alpha\beta\_SH}[k+2] \end{cases} \qquad (11)$$
$$\text{for Traditional FCS} - \text{MPC Method}$$

$$\begin{cases} i_{\alpha\beta\_\mathrm{err1,Prop}}[k] = i_{\alpha\beta d}^{p}[k] - i_{\alpha\beta d\_SH}[k] \\ i_{\alpha\beta\_\mathrm{err2,Prop}}[k] = i_{\alpha\beta d}^{p}[k+1] - i_{\alpha\beta d\_SH}[k+1] \end{cases} \qquad (12)$$
$$\text{for Proposed FCS} - \text{MPC Method}$$

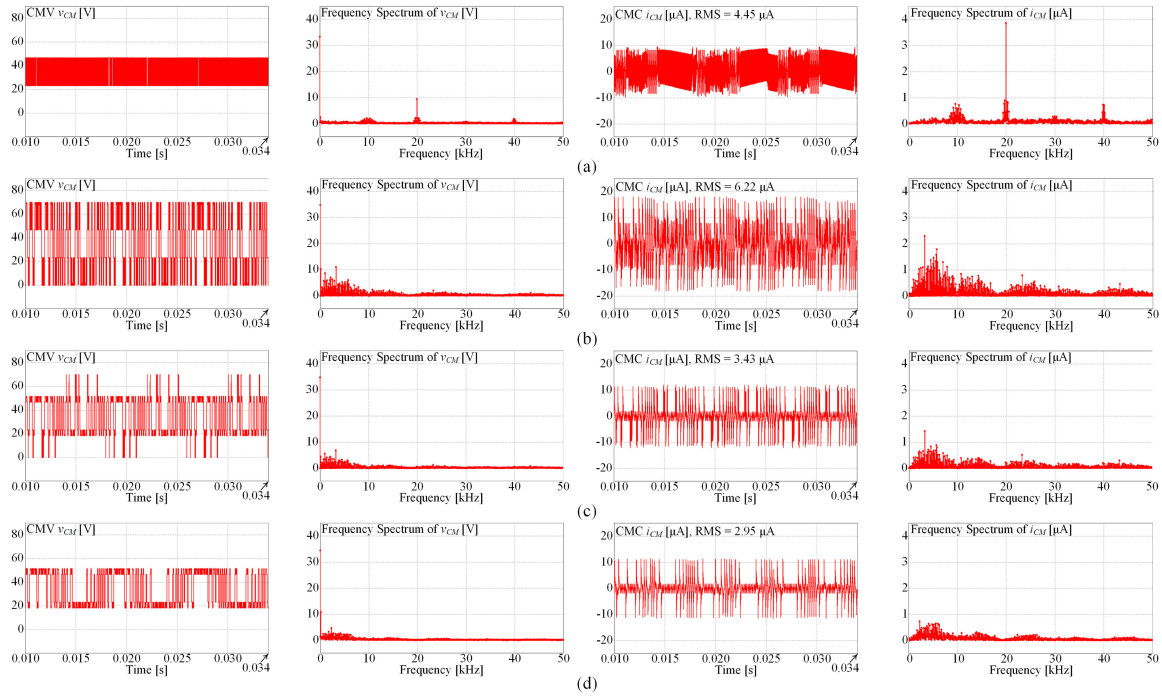

Fig. 10. Simulation results of CMV and CMC at rated current and rotor speed of 500 r/min. (a) DAVV MPC method. (b) Traditional FCS–MPC method with NAND-gate-based logic. (c) Traditional FCS–MPC method with OR-gate-based logic. (d) Proposed FCS–MPC method.

where $\boldsymbol{i}_{\alpha\beta\_SH}[k+1]$, $\boldsymbol{i}_{\alpha\beta\_SH}[k+2]$, $\boldsymbol{i}_{\alpha\beta d\_SH}[k]$, and $\boldsymbol{i}_{\alpha\beta d\_SH}[k+1]$ are the sample-and-hold values of $\boldsymbol{i}_{\alpha\beta}$ at the start of the $[k+1]$th AT, $[k+2]$th AT, $[k]$th DT, and $[k+1]$th DT, respectively. As indicated in both (11) and (12), the subscripts err1 and err2 represent the current errors for the first and second predicted currents at the $[k]$th sequence in the two methods, respectively. As shown in Fig. 9, $\boldsymbol{i}_{\alpha\beta\_\mathbf{err1,Prop}}[k]$ and $\boldsymbol{i}_{\alpha\beta\_\mathbf{err2,Prop}}[k]$ are significantly reduced compared with $\boldsymbol{i}_{\alpha\beta\_\mathbf{err1,Trad}}[k]$ and $\boldsymbol{i}_{\alpha\beta\_\mathbf{err2,Trad}}[k]$, respectively. As $\boldsymbol{i}_{\alpha\beta\_\mathbf{err1,Prop}}[k]$ decreases, accurate CS detection is possible, and as $\boldsymbol{i}_{\alpha\beta\_\mathbf{err2,Prop}}[k]$ decreases, accurate current prediction for cost function minimization is possible.

B. CMV and CMC

The simulation results of the CMV and CMC with their frequency spectra are shown in Fig. 10. In Fig. 10(a), the DAVV MPC method eliminates the peak CMV of zero or V_{dc}, but the RMS value of the CMC is increased because of a large number of CMV variations. In Fig. 10(b), the traditional FCS–MPC with the NAND-gate-based logic generates many peak CMVs because it cannot reduce the peak CMVs at the DT, as described in Section II. In Fig. 10(c), although the OR-gate-based logic can reduce the peak CMVs to a certain extent, several peak CMVs are still generated at the transition between the two-leg-changed powering VVs. In contrast, the proposed method completely eliminates the peak CMVs by instantly operating the series-connected switches, as shown in Fig. 10(d). Accordingly, the RMS value of the CMCs is the lowest compared with the other methods.

In addition, in the DAVV MPC method, it is observed that the highest harmonic component of the CMC occurs at the sampling frequency ($= 20$ kHz). In contrast, the harmonic components of the CMV and CMC are more spread over the frequency range in the traditional and proposed FCS–MPC methods. Herein, it is noticeable that the proposed method reduces most of the harmonic components in both the CMV and CMC, compared with the traditional FCS–MPC methods.

C. Parameter Mismatch

An FCS–MPC method is sensitive to the model parameter mismatches because it implements a model-based control strategy [31]. The proposed method was also evaluated under the parameter mismatches. Fig. 11 shows the average values of $|i_{\alpha\_\mathrm{err1,Prop}}|$ and $|i_{\alpha\_\mathrm{err2,Prop}}|$ during a fundamental period of current when L_s or R_s in the controller is changed between 50% and 200% of its nominal value. As can be seen, the average current errors increase as the parameter mismatch becomes larger. The proposed method could completely reduce the peak CMVs even at the parameter mismatches, except when the inductance mismatch ratio is 2.0 in Fig. 11(a). Only when L_s was twice its nominal value, a few peak CMVs were generated due to the detection error of the CS.

D. Average Switching Frequency

As a synthesized VV is applied in the DAVV MPC method, the average switching frequency rapidly increases. Fig. 12 shows the average switching frequencies for the DAVV MPC and the

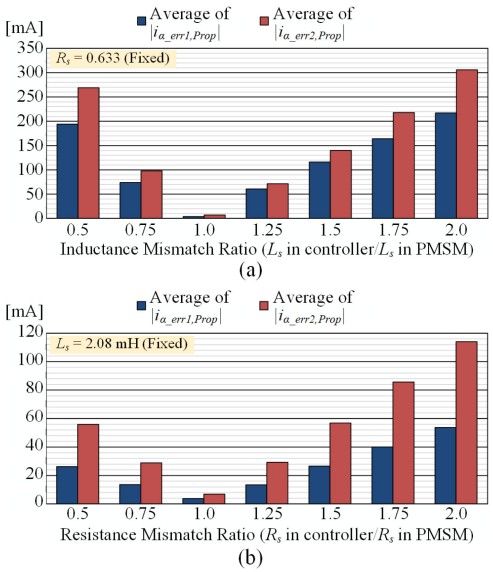

Fig. 11. Predicted current errors of proposed method under parameter mismatches. (a) Varying L_s with fixed R_s. (b) Varying R_s with fixed L_s.

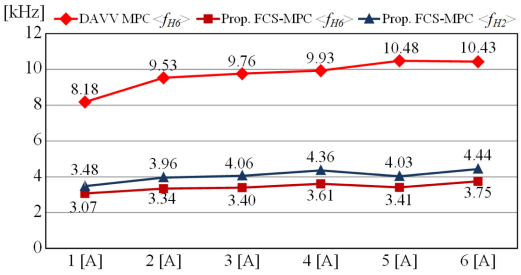

Fig. 12. Average switching frequencies in DAVV MPC and proposed methods depending on peak current.

proposed methods. <f_{H6}> and <f_{H2}> denote that the average switching frequencies in the H6 inverter and the series-connected switches, respectively. The calculations of <f_{H6}> and <f_{H2}> are presented in Appendix B. As shown in Fig. 12, although the proposed method requires two additional switches whose <f_{H2}> is approximately 4 kHz, <f_{H6}> related to the six switches can be significantly reduced, compared with that of the DAVV MPC method. This is because the proposed method uses only one VV during a sampling period. The difference in the average switching frequencies between the two methods may also affect the system efficiency.

E. Loss and Efficiency

Fig. 13(a) shows a comparison of the inverter and SPMSM losses between the DAVV MPC, traditional FCS–MPC, and proposed FCS–MPC methods. $P_{\rm swit}$ and $P_{\rm cond}$ denote switching loss and conduction loss of power device in the inverter, whereas $P_{\rm cu}$, $P_{\rm fe}$, and $P_{\rm str}$ denote copper loss, iron loss, and stray loss in the SPMSM, respectively. Mechanical and windage losses in the SPMSM were neglected. $P_{\rm swit}$ and $P_{\rm cond}$ were calculated using the thermal module where electrical characteristics

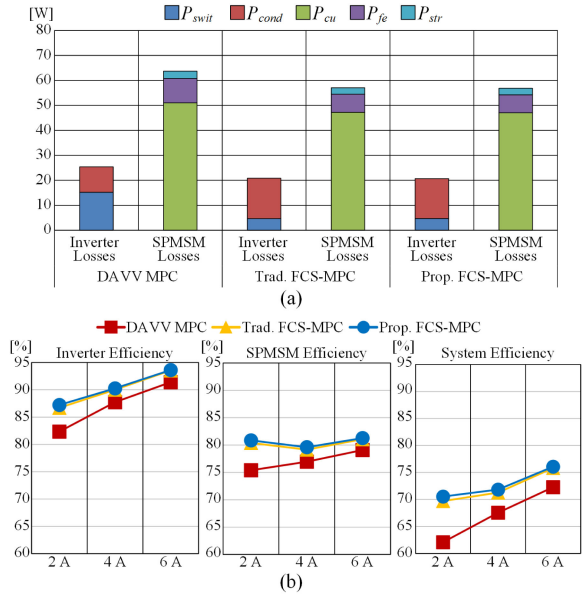

Fig. 13. Comparisons of losses and efficiencies between DAVV MPC, traditional FCS–MPC, and proposed FCS–MPC methods. (a) Inverter losses and SPMSM losses. (b) Efficiencies.

of power device (ROHM RGTH40TK65D) are entered based on manufacturer's datasheet, whereas $P_{\rm cu}$, $P_{\rm fe}$, and $P_{\rm str}$ were calculated based on the measured current/voltage [32] and data from manufacturers. As shown in Fig. 13(a), $P_{\rm cu}$ is much more dominant than $P_{\rm fe}$ and $P_{\rm str}$ in the SPMSM losses at the rated current and a rotor speed of 1000 r/min. In the DAVV MPC method, $P_{\rm cu}$ and $P_{\rm fe}$ are increased due to the high frequency current ripples (skin and proximity losses [33]) and bipolar line-to-line voltage (hysteresis loss [34]), respectively. In addition, as expected, $P_{\rm swit}$ is significantly increased due to high <f_{H6}> in the inverter. On the other hand, $P_{\rm cu}$, $P_{\rm fe}$, and $P_{\rm swit}$ can be reduced in both the traditional and proposed FCS–MPC methods, whereas $P_{\rm cond}$ is increased due to the series-connected switches on the dc-link.

Fig. 13(b) shows comparison of the inverter, SPMSM and overall system efficiencies for varying current. The DAVV MPC method shows relatively lower efficiencies in both the inverter and SPMSM, compared with the other methods. The difference in the overall system efficiencies between the DAVV MPC and proposed FCS–MPC is increased as the current is decreased because high $P_{\rm fe}$ and $P_{\rm swit}$ persist in the DAVV MPC. Meanwhile, there are no noticeable differences in the efficiencies between the traditional and proposed FCS–MPC methods.

V. Experimental Results

The performance of the proposed method was experimentally verified using an SPMSM test bench, which is shown in Fig. 14. The conducted CM EMI was extracted and measured using a pair of line impedance stabilization networks (LISNs, LN2-100T: 150 kHz–30 MHz) and an EMI test receiver (FFT 3010: 9 kHz–30 MHz), respectively. The midpoint of the LISNs and the motor frame were connected to a grounded aluminum

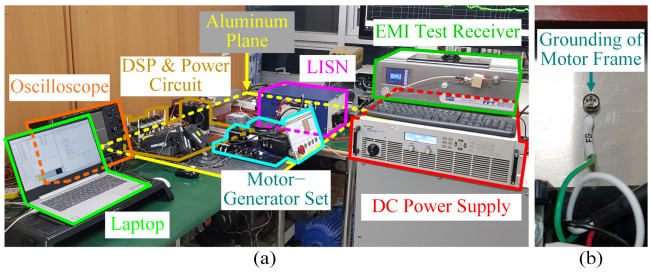

Fig. 14. Test bench for proposed method. (a) Overview. (b) Grounding of motor frame.

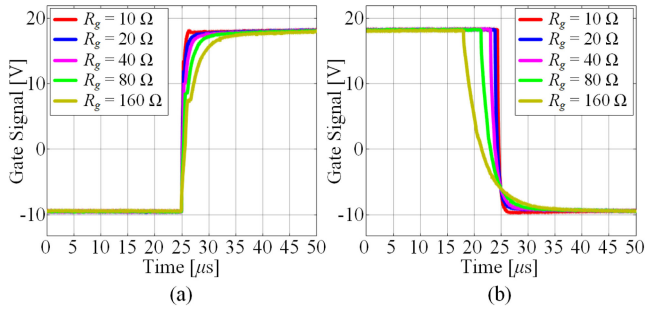

Fig. 15. Turn-ON and turn-OFF characteristics of power device depending on gate resistor. (a) Turn-ON characteristics. (b) Turn-OFF characteristics.

plane. The control algorithms were implemented using a DSP board (Texas Instrument TMS320F28335). The experimental parameters were the same as the simulation parameters given in Table V, except for T_s and d. T_s was reduced from 20 to 15 kHz considering the calculation time. Accordingly, in the proposed method, d was adjusted to 0.09. Fig. 15 shows the turn-ON/OFF characteristics of the used power device. In this experiment, the gate resistor (R_g) was selected as 80 Ω; however, the proposed method can be also operated with low R_g, such as 10 Ω.

A. CMV and Current THD

Fig. 16 shows the experimental results of the a-phase current (i_a), three-phase output voltage (v_{an}, v_{bn}, and v_{cn}), and CMV at the rated current and a rotor speed of 500 r/min for the traditional and proposed FCS–MPC methods. The CMV was calculated using the three-phase output voltage with reference to (1). As shown in Fig. 16(a), the traditional FCS–MPC with NAND-gate-based logic causes many peak CMVs because the gate logic does not operate the series-connected switches during the DT. In Fig. 16(b), the OR-gate-based logic reduces the peak CMVs when entering and leaving the ZVVs; however, several peak CMVs are still generated during the transition between the two-leg-changed powering AVVs. Unlike the traditional methods, the proposed FCS–MPC can completely eliminate the peak CMVs, as shown in Fig. 16(c). In addition, the current THDs of the traditional FCS–MPC methods are similar (11.3% and 10.9%, respectively), whereas that of the proposed method is further improved to 8.9%.

Similarly, the experimental results when the rotor speed is increased to 1000 r/min are shown in Fig. 17. Compared with the traditional methods in Fig. 17(a) and (b), the proposed method not only completely eliminates the peak CMVs, but also considerably improves the current THD, as shown in Fig. 17(c).

A comparison of the current THDs depending on the current and rotor speed between the traditional and proposed FCS–MPC methods is shown in Fig. 18. Although the calculation delay is also compensated in the traditional method, the difference in the current THD between the two methods is large: the proposed method improves the current THD by up to 2.9% compared with that of the traditional method at the current of 2 A and a rotor speed of 500 r/min.

B. Operation of Series–Connected Switches

Detailed operation of the series-connected switches S_7 and S_8 in the proposed method is shown in Figs. 19 and 20, respectively. Fig. 19 shows the experimental waveforms of the gate signal of S_7 (G_7), three-phase output voltage, and CMV. As an example of the operation of S_7, Fig. 19(a) shows the waveforms at the VV transitions from $\boldsymbol{V_2}$ to $\boldsymbol{V_7}$ and from $\boldsymbol{V_7}$ to $\boldsymbol{V_5}$: $v_{an} = v_{bn} = V_{dc}$, $v_{cn} = 0$ during $\boldsymbol{V_2}$, and $v_{an} = v_{bn} = 0$, $v_{cn} = V_{dc}$ during $\boldsymbol{V_5}$. In this case, S_7 turns OFF at the start of the DT before $\boldsymbol{V_7}$ and turns ON at the end of the DT after $\boldsymbol{V_7}$, thus completely reducing the peak CMV of $V_{\rm dc}$. As another example of the operation of S_7, Fig. 19(b) shows the VV transition from $\boldsymbol{V_6}$ to $\boldsymbol{V_4}$ at CS6. As described in Section III-A, both $\boldsymbol{V_6}$ and $\boldsymbol{V_4}$ are the powering VVs at CS6, and the peak CMV of $V_{\rm dc}$ is generated during the DT between $\boldsymbol{V_6}$ and $\boldsymbol{V_4}$ if S_7 does not operate. In the proposed method, as shown in Fig. 19(b), S_7 turns OFF during the DT by G_7, and the peak CMV is reduced.

Similar to Fig. 19, Fig. 20 shows the experimental results of the gate signal of S_8 (G_8), three-phase voltage, and CMV to verify the operation of S_8. Fig. 20(a) shows the experimental waveforms when entering and leaving $\boldsymbol{V_0}$. As shown in this figure, S_8 turns OFF at the start of the DT before $\boldsymbol{V_0}$ and maintains the OFF-state until the end of the DT after $\boldsymbol{V_0}$; therefore, the peak CMV of zero can be completely reduced. In addition, when the VV is changed from $\boldsymbol{V_1}$ to $\boldsymbol{V_3}$ at CS3 in Fig. 20(b), S_8 is instantly operated during the DT by G_8, and the peak CMV of zero can be reduced.

C. Dynamic Performance

To compare the dynamic performance of the traditional and proposed FCS–MPC methods, the experimental results of the three-phase current when the current changes in steps from 1 to 6 A and vice versa are shown in Fig. 21. As can be seen, the response times of the two methods are similar at 0.4 ms in both cases of current change from 1 to 6 A and vice versa.

D. Calculation Time

Table VI gives a comparison of the calculation times between the DAVV MPC, traditional FCS–MPC, and proposed FCS–MPC methods. The DAVV MPC method requires the long

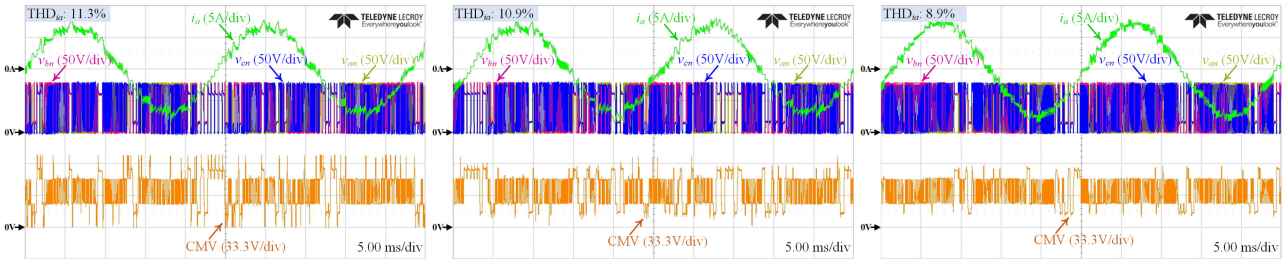

Fig. 16. Comparison of experimental results between conventional and proposed methods at rated current and rotor speed of 500 r/min. (a) Traditional FCS–MPC method with NAND-gate-based logic. (b) Traditional FCS–MPC method with OR-gate-based logic. (c) Proposed FCS–MPC method.

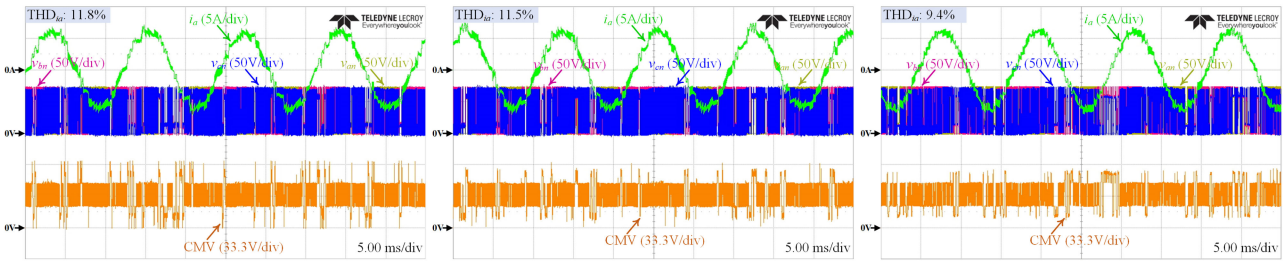

Fig. 17. Comparison of experimental results between conventional and proposed methods at rated current and rotor speed of 1000 r/min.
(a) Traditional FCS–MPC method with NAND-gate-based logic. (b) Traditional FCS–MPC method with OR-gate-based logic. (c) Proposed FCS–MPC method.

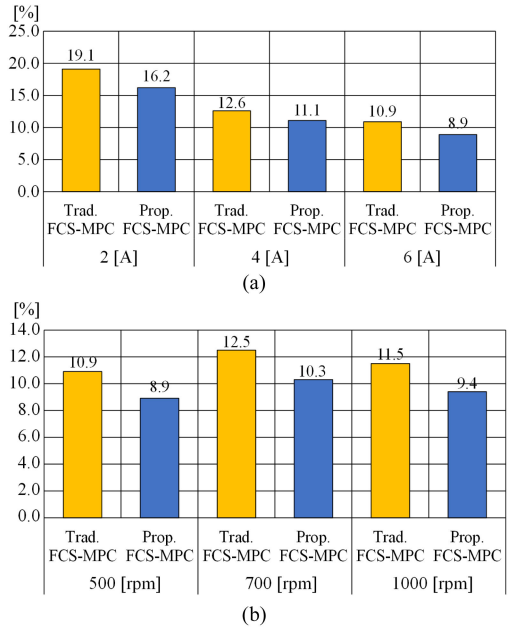

Fig. 18. Comparison of current THDs between traditional and proposed FCS–MPC methods. Calculation delay of digital controller is compensated in both methods. (a) At fixed rotor speed of 500 r/min and varying current. (b) At fixed current of 6.22 A_{peak} and varying rotor speed.

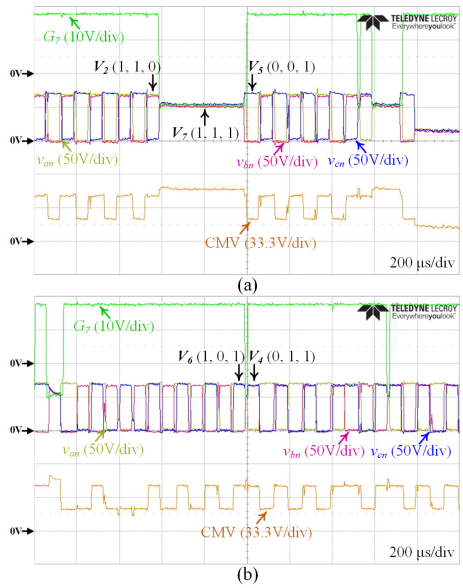

Fig. 19. Experimental results of switching operation of S_7 in proposed method. (a) When entering and leaving V_7. (b) When VV transition occurs between V_6 and V_4 at CS6.

calculation time of 47 μs due to its complicated control algorithm, whereas the traditional and proposed FCS–MPC methods require relatively shorter calculation times of 30 and 34 μs, respectively. The calculation time of the proposed method is slightly longer than that of the traditional method due to the additional calculation of DT VV term in the current prediction model.

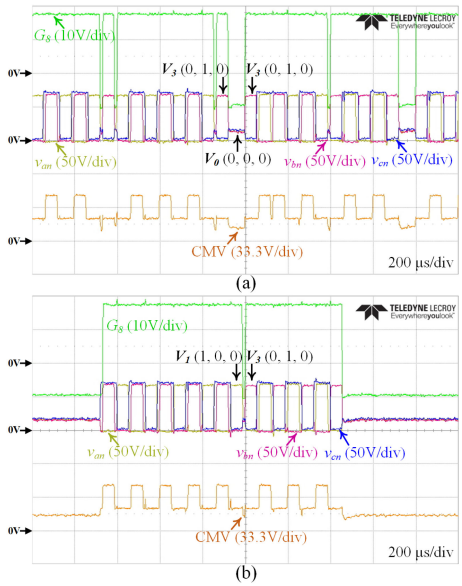

Fig. 20. Experimental results of switching operation of S_8 in proposed method. (a) When entering and leaving V_0. (b) When VV transition occurs between V_1 and V_3 at CS3.

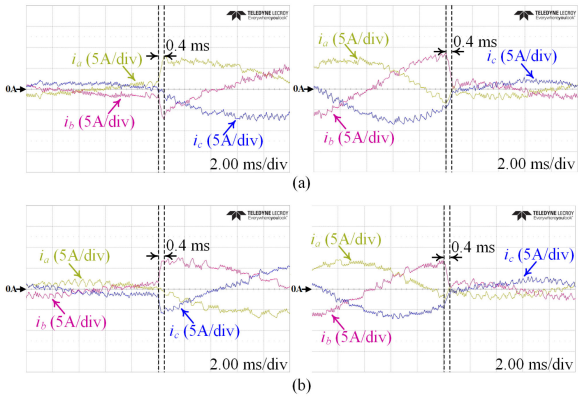

Fig. 21. Comparison of experimental results when three-phase current changes in steps from 1 to 6 A and vice versa. (a) Traditional FCS–MPC method. (b) Proposed FCS–MPC method.

TABLE VI
COMPARISON OF CALCULATION TIMES BETWEEN DAVV MPC, TRADITIONAL FCS–MPC, AND PROPOSED FCS–MPC METHODS

	DAVV MPC	Traditional FCS–MPC	Proposed FCS–MPC
Calculation Time	47 μs	30 μs	34 μs

E. Efficiency

Table VII gives the experimentally measured efficiencies of the inverter, SPMSM, and overall system at the rated current and a rotor speed of 1000 r/min. The input and output powers of the inverter were measured using a power analyzer (Yokokawa WT3000), whereas the shaft power of the SPMSM was calculated by multiplying the load torque and rotor speed. The inverter efficiency was calculated by dividing the inverter input power into its output power, and the SPMSM efficiency was calculated by dividing the inverter output power into the SPMSM shaft power. Multiplying the inverter efficiency by the SPMSM efficiency, the system efficiency was obtained. The efficiency results in Table VII coincide with these in the simulation results. That is, the inverter and SPMSM efficiencies of the DAVV MPC method are lower than these of the traditional and proposed FCS–MPC methods. On the other hand, there are no noticeable efficiency differences between the traditional and proposed FCS–MPC methods.

TABLE VII
COMPARISON OF EFFICIENCIES BETWEEN DAVV MPC, TRADITIONAL FCS–MPC, AND PROPOSED FCS–MPC METHODS

	DAVV MPC	Traditional FCS–MPC	Proposed FCS–MPC
Inverter Efficiency	89.5%	92.2%	92.6%
SPMSM Efficiency	78.4%	79.5%	79.6%
System Efficiency	70.2%	73.3%	73.7%

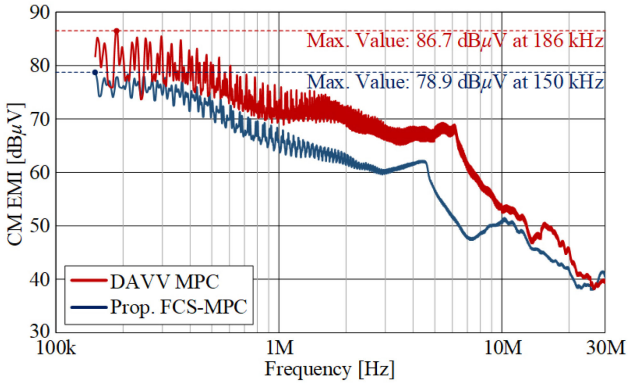

Fig. 22. Comparison of conducted CM EMI between DAVV MPC and proposed FCS–MPC methods.

F. Conducted CM EMI

A comparison of the conducted CM EMI between the DAVV MPC and proposed FCS–MPC methods is shown in Fig. 22. As can be seen, the DAVV MPC method significantly increases the conducted CM EMI because of a large number of CMV variations. The result indicates that the conventional DAVV-based MPC methods may be unsuitable solutions for suppressing the CM EMI in PMSM drive systems. On the other hand, the proposed method can suppress the CM EMI in a wide frequency range. The proposed method can approximately achieve 5 dBμV of attenuation in the range of 150 kHz–1 MHz and 9 dBμV of attenuation in the range of 1–10 MHz.

VI. CONCLUSION

This article proposed an FCS–MPC method for an H8 inverter considering the DT effect to reduce the CM EMI and current THD in PMSM drive systems. First, the CMV-generated pattern

TABLE VIII
VV GENERATED DURING DT[1)]

$V_{\alpha\beta}[k]$	$V_{\alpha\beta}[k+1]$	$V_{\alpha\beta d}[k]$					
		CS1	CS2	CS3	CS4	CS5	CS6
V_0	V_1	V_0	V_0	V_0	V_1	V_1	V_1
	V_2	V_3	V_3	V_0	V_1	V_1	V_2
	V_3	V_3	V_3	V_0	V_0	V_0	V_3
	V_4	V_3	V_4	V_5	V_5	V_0	V_3
	V_5	V_0	V_5	V_5	V_5	V_0	V_0
	V_6	V_0	V_5	V_5	V_6	V_1	V_1
V_1	V_2	V_2	V_2	V_1	V_1	V_1	V_2
	V_3	V_3	V_3	V_0	V_1	V_1	V_2
	V_4	V_3	V_4	V_5	V_6	V_1	V_2
	V_5	V_0	V_5	V_5	V_6	V_1	V_1
	V_6	V_1	V_6	V_6	V_6	V_1	V_1
V_2	V_3	V_3	V_3	V_3	V_2	V_2	V_2
	V_4	V_3	V_4	V_4	V_7	V_2	V_2
	V_5	V_3	V_4	V_5	V_6	V_1	V_2
	V_6	V_2	V_7	V_6	V_6	V_1	V_2
V_3	V_4	V_3	V_4	V_4	V_4	V_3	V_3
	V_5	V_3	V_4	V_5	V_5	V_0	V_3
	V_6	V_3	V_4	V_5	V_6	V_1	V_2
V_4	V_5	V_4	V_4	V_5	V_5	V_5	V_4
	V_6	V_4	V_4	V_5	V_6	V_6	V_7
V_5	V_6	V_5	V_5	V_5	V_6	V_6	V_6
V_7	V_1	V_2	V_7	V_6	V_6	V_1	V_2
	V_2	V_2	V_7	V_7	V_7	V_2	V_2
	V_3	V_3	V_4	V_4	V_7	V_2	V_2
	V_4	V_4	V_4	V_4	V_7	V_7	V_7
	V_5	V_4	V_4	V_5	V_6	V_6	V_7
	V_6	V_7	V_7	V_6	V_6	V_6	V_7

[1)] Following cases are omitted: self-VV transitions, such as $V_{\alpha\beta\_\mathbf{opt}}[k] = V_{\alpha\beta\_\mathbf{opt}}[k+1]$, because there is no change in switching state, and same $V_{\alpha\beta d}[k]$ occurs; and opposite VV transitions, such as $V_{\alpha\beta\_\mathbf{opt}}[k] = V_2$ and $V_{\alpha\beta\_\mathbf{opt}}[k+1] = V_1$, because $V_{\alpha\beta d}[k]$ is same in case of $V_{\alpha\beta\_\mathbf{opt}}[k] = V_1$ and $V_{\alpha\beta\_\mathbf{opt}}[k+1] = V_2$.

during the DT between two AVVs was investigated. Based on the analysis, the proposed method instantly operated the H8 inverter to reduce the peak CMVs even at the DT. Furthermore, the nonlinearity of the inverter output voltage due to the DT was compensated considering the calculation delay. As a result, the proposed method not only allowed all VV transitions without the peak CMVs but also significantly improved the current THD over the entire operating condition. The proposed method would be an appropriate solution for suppressing both the CM EMI and current THD in PMSM drive systems along with a simple control concept and a rapid dynamic response.

APPENDIX A

The DT VV $V_{\alpha\beta d}[k]$ depending on the previous VV, CS, and next VV is given in Table VIII.

APPENDIX B

The equivalent switching frequency $f_{\mathrm{eq\_}si}$ during a fundamental period T_0 of the output current is calculated as

$$f_{\mathrm{eq\_}si} = N_{si}/2T_0 \tag{13}$$

where N_{si} is the number of switching transitions in the switch S_i during T_0. Then, the average switching frequencies in the H6 inverter and the series-connected switches, $\langle f_{H6} \rangle$ and $\langle f_{H2} \rangle$ respectively, can be calculated as

$$\langle f_{H6} \rangle = \sum_{n=1}^{m} \left\{ \sum_{i=1}^{6} f_{\mathrm{eq\_}si,n} \right\} / 6m \tag{14}$$

$$\langle f_{H2} \rangle = \sum_{n=1}^{m} \left\{ \sum_{i=7}^{8} f_{\mathrm{eq\_}si,n} \right\} / 2m \tag{15}$$

where $f_{\mathrm{eq\_}si,n}$ is $f_{\mathrm{eq\_}si}$ at the $[n]$th the fundamental period, and m is the total number of the fundamental periods. In this article, m is set as 5.

REFERENCES

[1] M. C. Cavalcanti, K. C. de Oliveira, A. M. de Farias, F. A. S. Neves, G. M. S. Azevedo, and F. C. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1360–1368, Apr. 2010, doi: 10.1109/TIE.2009.2029511.

[2] J. Liu, W. Zhang, F. Xiao, C. Lian, and S. Gao, "Six-step mode control of IPMSM for railway vehicle traction eliminating the DC offset in input current," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8981–8993, Sep. 2019, doi: 10.1109/TPEL.2018.2888877.

[3] S. Wang and P. W. Lehn, "A 3-phase electric vehicle charger integrated with dual inverter drive," *IEEE Trans. Transp. Electrific.*, to be published, doi: 10.1109/TTE.2021.3102192.

[4] D. Han, S. Li, Y. Wu, W. Choi, and B. Sarlioglu, "Comparative analysis on conducted CM EMI emission of motor drives: WBG versus si devices," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8353–8363, Oct. 2017, doi: 10.1109/TIE.2017.2681968.

[5] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 469–476, Mar./Apr. 1999, doi: 10.1109/28.753643.

[6] A. M. Hava and E. Ün, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 241–252, Jan. 2009, doi: 10.1109/TPEL.2008.2005719.

[7] H. Yao, Y. Yan, T. Shi, G. Zhang, Z. Wang, and C. Xia, "A novel SVPWM scheme for field-oriented vector-controlled PMSM drive system fed by cascaded H-bridge inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8988–9000, Aug. 2021, doi: 10.1109/TPEL.2021.3054642.

[8] H. Zhang, A. V. Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, Nov./Dec. 2000, doi: 10.1109/28.887217.

[9] X. Chen, D. Xu, F. Liu, and J. Zhang, "A novel inverter-output passive filter for reducing both differential- and common-mode dv/dt at the motor terminals in PWM drive systems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 419–426, Feb. 2007, doi: 10.1109/TIE.2006.885517.

[10] S. Takahashi, S. Ogasawara, M. Takemoto, K. Orikawa, and M. Tamate, "Common-mode voltage attenuation of an active common-mode filter in a motor drive system fed by a PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2721–2730, May/Jun. 2019, doi: 10.1109/TIA.2019.2892364.

[11] D. Han, C. T. Morris, W. Lee, and B. Sarlioglu, "Comparison between output CM chokes for SiC drive operating at 20- and 200-kHz switching frequencies," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2178–2188, May/Jun. 2017, doi: 10.1109/TIA.2017.2672919.

[12] H. Chen and H. Zhao, "Review on pulse-width modulation strategies for common-mode voltage reduction in three-phase voltage-source inverters," *IET Power Electron.*, vol. 9, no. 14, pp. 2611–2620, 2016.
[13] S. K. Hoseini, J. Adabi, and A. Sheikholeslami, "Predictive modulation schemes to reduce common-mode voltage in three-phase inverters-fed AC drive systems," *IET Power Electron.*, vol. 7, no. 4, pp. 840–849, 2014.
[14] L. Guo, X. Zhang, S. Yang, Z. Xie, and R. Cao, "A model predictive control-based common-mode voltage suppression strategy for voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6115–6125, Oct. 2016, doi: 10.1109/TIE.2016.2574980.
[15] S. Kwak and S. Mun, "Common-mode voltage mitigation with a predictive control method considering dead time effects of three-phase voltage source inverters," *IET Power Electron.*, vol. 8, no. 9, pp. 1690–1700, 2015.
[16] L. Guo *et al.*, "Hybrid voltage vector preselection based model predictive control to reduce the common-mode voltage for 2-level voltage source inverters," *IET Power Electron.*, vol. 12, no. 3, pp. 541–549, 2019.
[17] L. Guo *et al.*, "Hybrid single and double-voltage vector-based model predictive common-mode voltage reduction method for 2-level voltage source inverters," *IET Power Electron.*, vol. 12, no. 8, pp. 2086–2094, 2019.
[18] L. Guo, N. Jin, C. Gan, L. Xu, and Q. Wang, "An improved model predictive control strategy to reduce common-mode voltage for two-level voltage source inverters considering dead-time effects," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3561–3572, May 2019, doi: 10.1109/TIE.2018.2856194.
[19] L. Guo, N. Jin, C. Gan, and K. Luo, "Hybrid voltage vector preselection-based model predictive control for two-level voltage source inverters to reduce the common-mode voltage," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 4680–4691, Jun. 2020, doi: 10.1109/TIE.2019.2931257.
[20] S. Kwak and S. Mun, "Model predictive control methods to reduce common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5019–5035, Sep. 2015, doi: 10.1109/TPEL.2014.2362762.
[21] T. Jin, J. Guo, M. A. Mohamed, and M. Wang, "A novel model predictive control via optimized vector selection method for common-mode voltage reduction of three-phase inverters," *IEEE Access*, vol. 7, pp. 95351–95363, 2019, doi: 10.1109/ACCESS.2019.2928440.
[22] A. L. Julian, G. Oriti, and T. A. Lipo, "Elimination of common-mode voltage in three-phase sinusoidal power converters," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 982–989, Sep. 1999, doi: 10.1109/63.788504.
[23] X. Guo, R. He, J. Jian, Z. Lu, X. Sun, and J. M. Guerrero, "Leakage current elimination of four-leg inverter for transformerless three-phase PV systems," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1841–1846, Mar. 2016, doi: 10.1109/TPEL.2015.2477539.
[24] A. Hota and V. Agarwal, "Novel three-phase H10 inverter topology with zero common mode voltage for three-phase induction motor drive applications," *IEEE Trans. Ind. Electron.*, to be published, doi: 10.1109/TIE.2021.3097656.
[25] L. Concari, D. Barater, G. Buticchi, C. Concari, and M. Liserre, "H8 inverter for common-mode voltage reduction in electric drives," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4010–4019, Sep./Oct. 2016, doi: 10.1109/TIA.2016.2581763.
[26] C. T. Morris, D. Han, and B. Sarlioglu, "Reduction of common mode voltage and conducted EMI through three-phase inverter topology," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1720–1724, Mar. 2017, doi: 10.1109/TPEL.2016.2608388.
[27] R. Rahimi, S. Farhangi, B. Farhangi, G. R. Moradi, E. Afshari, and F. Blaabjerg, "H8 inverter to reduce leakage current in transformerless three-phase grid-connected photovoltaic systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 910–918, Jun. 2018, doi: 10.1109/JESTPE.2017.2743527.
[28] Y. Xiang, X. Pei, M. Wang, P. Shi, and Y. Kang, "An improved H8 topology for common-mode voltage reduction," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5352–5361, Jun. 2019, doi: 10.1109/TPEL.2018.2870039.
[29] W.-S. Jeong, K.-M. Choo, J.-H. Lee, and C.-Y. Won, "A common-mode voltage reduction method of FCS-MPC in H8 inverter for SPMSM drive system considering dead-time effect," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 1–8, doi: 10.23919/ICPE2019-ECCEAsia42246.2019.8796923.
[30] J. Rodriguez *et al.*, "Predictive current control of a voltage source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 495–503, Feb. 2007, doi: 10.1109/TIE.2006.888802.
[31] H. A. Young, M. A. Perez, and J. Rodriguez, "Analysis of finite-control-set model predictive current control with model parameter mismatch in a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 3100–3107, May 2016, doi: 10.1109/TIE.2016.2515072.
[32] R. E. Neapolitan and K. H. Nam. *AC Motor Control and Electrical Vehicle Applications*. Boca Raton, FL, USA: CRC Press, 2018.
[33] S. Iwasaki, R. P. Deodhar, Y. Liu, A. Pride, Z. Q. Zhu, and J. J. Bremner, "Influence of PWM on the proximity loss in permanent-magnet brushless AC machines," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1359–1367, Jul./Aug. 2009, doi: 10.1109/TIA.2009.2023488.
[34] S. Zhu and B. Shi, "Modeling of PWM-Induced iron losses with frequency-domain methods and low-frequency parameters," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2402–2413, Mar. 2022, doi: 10.1109/TIE.2021.3065626.

Won-Sang Jeong (Student Member, IEEE) received the B.S. degree in electrical and electronic engineering from Anyang University, Anyang, South Korea, in 2017. He is currently working toward the Ph.D. degree in electrical and computer engineering with Sungkyunkwan University, Suwon, South Korea.

His current research interests include power electronic of electric machines.

Sung-Hun Kim (Student Member, IEEE) received the B.S. degree in electronics engineering from Kwangwoon University. Seoul, South Korea, in 2017. He is currently working toward the Ph.D. degree in electrical and computer engineering with Sungkyunkwan University, Suwon, South Korea.

His current research interests include power converters for renewable energy systems and dc microgrid.

Junsin Yi (Member, IEEE) was born in Seoul, South Korea, in 1962. He received the B.S. degree in electronic and electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 1989, and the M.S and Ph.D. degrees in electronic and electrical engineering from The State University of New York, University at Buffalo, Buffalo, NY, USA, in 1991 and 1994, respectively.

He is currently a Professor with Sungkyunkwan University, Suwon, South Korea. His current research interests include solar cells, and thin film transistor and their applications.

Chung-Yuen Won (Senior Member, IEEE) was born in South Korea in 1955. He received the B.S. degrees from Sungkyunkwan University, Suwon, South Korea, in 1978, and the M.S. and Ph.D. degrees from Seoul National University, Seoul, South Korea, in 1980 and 1987, respectively, all in electrical engineering.

From 1990 to 1991, he was with the Department of Electrical Engineering, University of Tennessee, Knoxville, TN, USA, as a Visiting Professor. Since 1988, he has been a member of the Faculty of Sungkyunkwan University, where he is currently a Professor with the College of Information and Communication Engineering. Also, from 2008 to 2013, he was the Director of Samsung Energy Power Research Center. He was the President of the Korean Institute of Power Electronics in 2010. Since 2016, he has been the Director of the DC Distribution Research Center. His current research interests include power electronic of electric machines, electric/hybrid vehicle drives, and power converters for dc distribution system.