Energy Diverting Converter Topology Using Unidirectional Current H-Bridge Submodules for VSC-HVDC Transmission System

Zhengxuan Li, *Student Member, IEEE*, Yuebin Zhou, *Senior Member, IEEE*, Nan Zhang, Qiang Song, *Senior Member, IEEE*, Rong Zeng, *Senior Member, IEEE*, Biao Zhao, *Senior Member, IEEE*, and Zhanqing Yu, *Member, IEEE*

***Abstract*—The voltage source converter-based high-voltage direct current transmission has been the preferred choice for integrating long-distance, bulky offshore wind farms. The fault ride-through capability during onshore ac network faults is one of the greatest challenges, and the dynamic braking resistor (DBR) circuit for diverting the excess energy is essential. In this article, a novel modular multilevel converter (MMC) DBR circuit based on unidirectional current H-bridge submodules (UCH-SMs) and a two-state transition control strategy are proposed. The UCH-SM-based MMC-DBR (UCH-MMC-DBR) has advantages, such as a simple lumped cooling system and a modular design. The semiconductor usage is very low compared with the existing topologies. The two-state transition control strategy can maintain the charging–discharging balance on the SM capacitors while enabling the braking power to track the reference. The feasibility of the proposed UCH-MMC-DBR and the two-state transition control strategy is verified using the simulation and experimental results.**

***Index Terms*—Dynamic braking resistor (DBR), modular multilevel converter (MMC), offshore wind power, voltage source converter-based high-voltage dc (VSC-HVdc).**

I. Introduction

OFFSHORE wind power has been researched in recent years [1] and it now accounts for an increasing proportion of renewable energy sources. The voltage source converter-based high-voltage direct current (VSC-HVdc) transmission has been the preferred choice for connecting long-distance offshore wind farms in numerous existing projects [2].

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Zhengxuan Li, Qiang Song, Rong Zeng, Biao Zhao, and Zhanqing Yu are with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: zx-li18@mails.tsinghua.edu.cn; songqiang@tsinghua.edu.cn; zengrong@tsinghua.edu.cn; zhao-biao@tsinghua.edu.cn; yzq@tsinghua.edu.cn).

Yuebin Zhou is with the Electric Power Research Institute of China Southern Power Grid, Guangzhou 510663, China (e-mail: zhouyb@csg.cn).

Nan Zhang is with Maintenance and Test Center, Extra High Voltage Power Transmission Co., China Southern Power Grid Co., Ltd., Guangzhou 510620, China (e-mail: zhangnan@ehv.csg.cn).

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TABLE I
Comparison of the FRTs Based on Between Control Strategies and DBRs

FRT methods	FRTs based on control strategies	FRTs based on DBRs
Principle	dynamically reducing the power generation of turbines	dynamically dissipating the excess power by DBRs locally
Cost	low	medium
Response speed	sluggish for the HVDC system	fast
Ride-through failure risk	high	low
Stress on WTG	high	low
Applicable to all WTG types	the response of different types of turbines are not same	suitable for a wide range of turbines

However, the fault ride-through (FRT) capability of the VSC-HVdc system connecting offshore wind farms remains one of the greatest challenges during onshore ac grid faults. The ac power output capability of the grid-side converter decreases during the fault [3] while the offshore wind farms cannot reduce their output power quickly. Therefore, excess power between the sending-end and receiving-end converters leads to the overvoltage of dc lines or even shutdown of the VSC-HVdc system. The existing FRT methods can be classified into two groups: fast power reduction from wind farms using control strategies [4]–[9] and energy dissipation using a dynamic braking resistor (DBR) circuit [10]–[17].

The basic characteristics of the FRTs based on control strategies and based on DBRs are given in Table I [8]. The FRT methods based on control strategies reduce the power of the wind farm during FRT and do not need to add any hardware. However, they are characterized as sluggish for VSC-HVdc since the voltage increase of the dc system may be very fast [4], [7], [8]. The responses of different types of wind turbine generators (WTGs) are also different, and thus, it is difficult to implement a control strategy-based FRTs that are suitable for a certain wind farm that consists of different types of turbines [8]. By contrast, the DBR-based FRTs are adequately fast to fit the VSC-HVdc since they can handle the excess power locally onshore. Moreover, the DBR-based FRTs are suitable

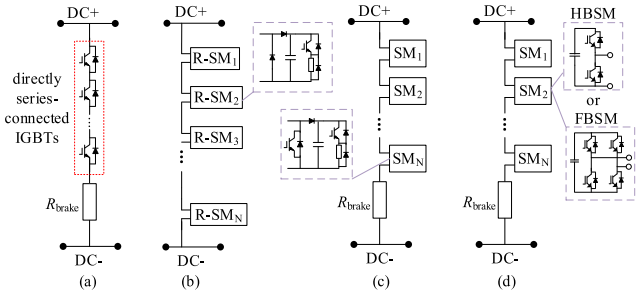

Fig. 1. Existing DBR topologies. (a) Braking chopper. (b) Modular DBR. (c) Modified modular DBR. (d) MMC DBR.

for different types of turbines since there is no disturbance of turbines [7], [8]. Hitherto, the DBRs have already been applied to a variety of projects, including Borwin2 and Helwin1 [13]. The DBRs are also essential components in VSC-HVdc projects in Rudong, China, which will be commissioned in the future.

Fig. 1 illustrates four existing DBR solutions. In Fig. 1(a), the braking chopper consists of numerous series-connected insulate gate bipolar transistors (IGBTs) and a lumped resistor [10], [11], [17]. The cooling system for the lumped resistor is simple, with relatively low cost [11]. However, the dynamic voltage sharing of the IGBTs is a great challenge in real implementation due to the nonsimultaneous commutation of a large number of series-connected IGBTs. The high *dv*/*dt* values due to the high-voltage two-level modulation is another drawback of the braking chopper solution.

The modular DBR, as shown in Fig. 1(b), has a modular structure and distributes the braking resistors inside each cell [13], [17]. Direct series connection does not exist in the modular DBR and it can regulate power smoothly. However, the distributed resistors should be installed in each module, which adds the investment and the complexity for cooling system design, compared with the lumped resistor.

Fig. 1(c) shows the modified modular DBR with both lumped and distributed resistors [12]. Although this topology adopts a lumped braking resistor design, there is still a discharge resistor designed within each module. When the current flows through the submodules (SMs), the capacitors are charged and the voltages increase. The distributed resistors are used to dissipate the power to keep the capacitors and semiconductors from overvoltage. The distributed cooling system is also required in this kind of topology.

The modular multilevel converter (MMC) DBR, as shown in Fig. 1(d), consists of an MMC arm and a lumped resistor [14]–[16]. The MMC arm is composed of either half-bridge SMs (HBSMs) or full-bridge SMs (FBSMs). In the MMC DBR, the voltage applied to the lumped braking resistor is the difference between the dc-line voltage and the MMC arm voltage. Therefore, the dissipation power can be controlled by varying the arm voltage. Meanwhile, the charging balance of the floating SM capacitors in the MMC arm must be ensured. Either the current or the voltage across the arm needs to be reversed to achieve zero mean power of the MMC arm (when ignoring the losses). A sinusoidal voltage modulation is used in the HBSM-based MMC DBR (HB-MMC-DBR), and the maximum arm voltage should reach 1.37 times as high as the dc-line voltage to generate negative current for charging balance because the HB-MMC arm cannot generate negative voltages [14]. This adds 37% extra semiconductor usage compared with a conventional HB-MMC arm. The arm using FBSMs can easily reverse its voltage and does not need to generate a higher voltage for generating negative current. However, the semiconductor usage of the FBSM-based MMC-DBR (FB-MMC-DBR) is even higher than that of the HB-MMC-DBR because the number of semiconductors in an FBSM is twice as much as that in an HBSM.

The MMC DBR combines the advantages of the braking chopper and the modular DBR, such as the simple cooling system for the lumped resistor, the modular design, and avoidance of series connection of IGBTs. The main drawback of the existing MMC DBR solutions is the high semiconductor usage. A unidirectional current H-bridge SM (UCH-SM) was proposed in [18] and [19] as a cell of MMC based on the fact that an FBSM can be simplified to a UCH-SM if the current that flows through the SM is unidirectional. The semiconductor usage in a UCH-SM is half that in an FBSM. However, the arm current that is involved in [18] and [19] is discontinuous, and thus, there is high harmonic distortion. In [20], an MMC based on the UCH-SM and the active circulating current were proposed to force the arm current to be unidirectional under lower ac voltages.

The arm current of FB-MMC-DBR is naturally unidirectional, from the positive dc bus to the negative one. This enables the UCH-SM to be also utilized in the DBR. Based on this fact, a new UCH-SM-based MMC DBR (UCH-MMC-DBR) is proposed in this article. The semiconductor usage in the UCH-MMC-DBR can be similar to that of a conventional HB-MMC arm, which is 37% lower than that in the HB-MMC-DBR and 50% lower than that in the FB-MMC-DBR. However, different from the ac/dc converters based on UCH-SM, the charging and discharging of the SM capacitors are not naturally balanced in a UCH-MMC-DBR when the arm simply outputs a dc voltage. The arm output voltage must alternate between the positive and negative voltages to ensure the charging balance. Therefore, a two-state transition control strategy is proposed in this article, which creates a positive–negative waveform to keep the charging balance of the SM capacitors and, meanwhile, enables the braking power to follow its reference. The equations for solving the required output voltages and duty cycles for a given dissipation power reference are also found. Analysis shows that meaningful solutions of voltages and duty cycles, which can fulfill the charging-balance constraint, can be found for all the dissipation power references. The feasibility of the proposed UCH-MMC-DBR and two-state control strategy has been verified using the simulation and experimental results.

II. Topology and Control of UCH-MMC-DBR

A. Principle of UCH-MMC-DBR

In a braking branch, if the braking current is kept positive, the FBSM-based arm voltage can be alternately positive and negative to keep the charging balance. When the current flowing through the FBSM is unidirectional, as Fig. 2(a) shows, the

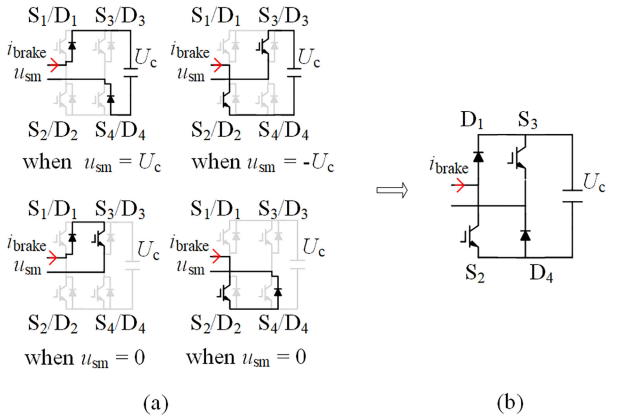

Fig. 2. Principle of simplification from FBSM to UCH-SM. (a) Current paths of the FBSM. (b) Topology of UCH-SM.

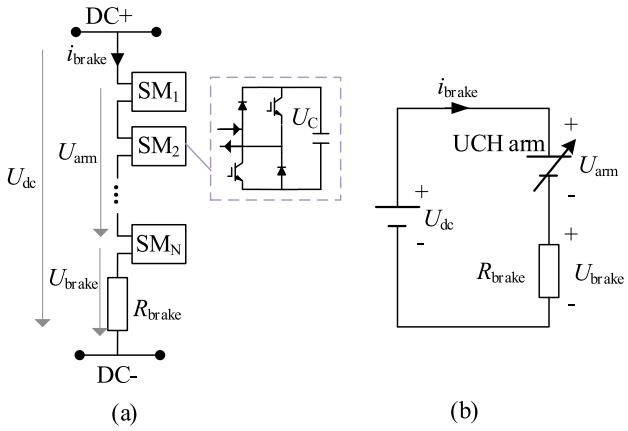

Fig. 3. Proposed UCH-MMC-DBR circuit. (a) Topology of UCH-MMC-DBR. (b) Equivalent circuit.

current never flows through S_1, S_4, D_2, and D_3. Therefore, two IGBTs and two diodes can be eliminated, and an FBSM is simplified into a UCH-SM topology, as shown in Fig. 2(b). The UCH-SM is a simplified variant of FBSM under the condition of unidirectional current, and it maintains the inheritability of outputting "0," "1," and "−1" voltages. Thus, the UCH-SM can maintain zero mean power into the arm circuit while the semiconductor usage can be reduced by half compared with FBSM.

Based on the UCH-SM, a UCH-MMC-DBR is proposed in this study, as illustrated in Fig. 3(a). The DBR circuit consists of a UCH-MMC arm and a lumped braking resistor. The MMC arm consists of N series-connected UCH-SMs. When the rated dc-line voltage is $U_{\rm dc}$, the rated capacitor voltage of the UCH-SM can be expressed as follows:

$$U_{\rm CN} = \frac{U_{\rm dc}}{N}. \tag{1}$$

Compared with the FB-MMC-DBR, the UCH-MMC-DBR can reduce the installed switching devices by half while maintaining the maximum value of the braking current. According

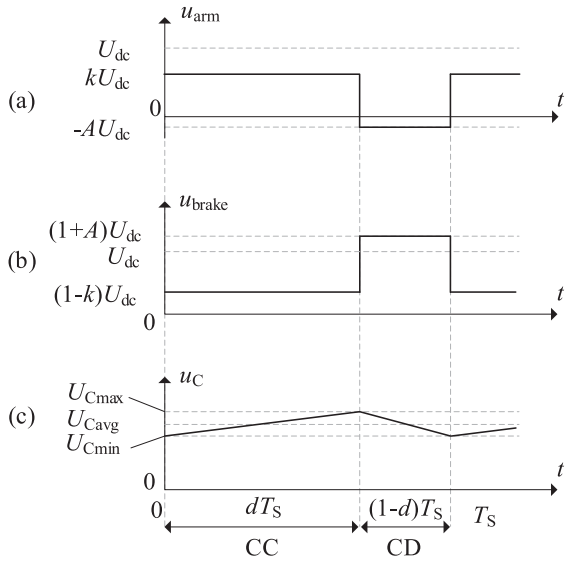

Fig. 4. Diagram of the two-state transition control strategy. (a) UCH arm output voltage. (b) Voltage added on the braking resistor. (c) Capacitor voltage.

to the comparison standard provided in [14], the UCH-MMC-DBR has very high braking performance among various DBR topologies, which will be analyzed in Section IV.

Assuming that the capacitor voltages are always maintained around $U_{\rm CN}$, the output voltage across the UCH arm can be expressed as follows:

$$u_{\rm arm} = n_{\rm arm} U_{\rm CN} \tag{2}$$

where $n_{\rm arm}$ is the number of the inserted UCH-SMs and its variation range is from $-N$ to N. Therefore, the UCH arm can be a controllable voltage source, as illustrated in the equivalent circuit in Fig. 3(b). By varying the voltage of the UCH arm, the voltage across the braking resistor can be varied as follows:

$$u_{\rm brake} = U_{\rm dc} - u_{\rm arm}. \tag{3}$$

The braking current and the instantaneous dissipation power can be controlled by the arm voltage and are expressed as

$$i_{\rm brake} = \frac{u_{\rm brake}}{R_{\rm brake}} = \frac{U_{\rm dc} - u_{\rm arm}}{R_{\rm brake}} \tag{4}$$

$$p_{\rm brake} = u_{\rm brake} i_{\rm brake} = \frac{(U_{\rm dc} - u_{\rm arm})^2}{R_{\rm brake}}. \tag{5}$$

The instantaneous power of the UCH arm is expressed as

$$p_{\rm arm} = u_{\rm arm} i_{\rm brake}. \tag{6}$$

B. Two-State Transition Control Strategy

The charging balance of the SM capacitors should be kept. Given that the arm current is unidirectional, the arm voltage should be alternately positive and negative to maintain the charging balance of the SM capacitors. A two-state transition control strategy for the UCH-MMC-DBR is proposed.

Fig. 4 illustrates that the arm voltage is switched between two states, the capacitor charging (CC) state and the capacitor discharging (CD) state. In the CC state, the arm outputs a

voltage of $kU_{\rm dc}$, where k is the positive amplitude coefficient that varies from 0 to 1.0. The duration time of the CC state is $dT_{\rm S}$, where $T_{\rm S}$ is the wave period, and d is the duty cycle that varies between 0 and 1.0. The capacitors are charged and the voltage [denoted as $u_{\rm C}$ in Fig. 4(c)] increases. The values of k and d are dynamically adjusted by the controller. In the CD state, the arm outputs a voltage of $-AU_{\rm dc}$ to discharge the SM capacitors to maintain charging–discharging balance and the capacitor voltage decreases. During the CD state, the voltage stress on the resistor becomes $(1+A)U_{\rm dc}$. Considering the permitted voltage stress across the resistor and the peak current flowing through the semiconductors, coefficient A can be designed as a fixed small value. For example, the range of 0.1–0.25 is recommended. The duration time of the CD state is $(1-d)T_{\rm S}$. The slope of the arm voltage when transiting the state can be controlled to improve the electromagnetic compatibility performance. The fast calculation of the number of inserted SMs during the slopes can be implemented by the field-programmable gate array (FPGA). The two-state control strategy ensures the capacitor voltage to be around the average voltage.

In the two-state transition control strategy, the arm voltage $u_{\rm arm}$, braking resistor voltage $u_{\rm brake}$, and braking current $i_{\rm brake}$ can be expressed as

$$u_{\rm arm}(t)=\begin{cases} kU_{\rm dc}, 0\le t<dT_{\rm S} \\ -AU_{\rm dc}, dT_{\rm S}\le t<T_{\rm S}\end{cases} \tag{7}$$

$$u_{\rm brake}(t)=\begin{cases} (1-k)U_{\rm dc}, 0\le t<dT_{\rm S} \\ (1+A)U_{\rm dc}, dT_{\rm S}\le t<T_{\rm S}\end{cases} \tag{8}$$

$$i_{\rm brake}(t)=\begin{cases} \frac{(1-k)U_{\rm dc}}{R_{\rm brake}}, 0\le t<dT_{\rm S} \\ \frac{(1+A)U_{\rm dc}}{R_{\rm brake}}, dT_{\rm S}\le t<T_{\rm S}.\end{cases} \tag{9}$$

Fig. 4 illustrates that the UCH arm voltage is switched between the CC and CD states during a wave cycle. According to (7)–(9), the average power dissipation during a wave cycle can be calculated as

$$\begin{aligned}\overline{P}_{\rm brake}&=\frac{1}{T_{\rm S}}\int_0^{T_{\rm S}} u_{\rm brake}(t)i_{\rm brake}(t)dt \\ &=\frac{\left[(1-k)\,U_{\rm dc}\right]^2}{R_{\rm brake}}d+\frac{\left[(1+A)\,U_{\rm dc}\right]^2}{R_{\rm brake}}\,(1-d)\,.\end{aligned} \tag{10}$$

The average absorbed power of the UCH arm during a wave cycle can be calculated as

$$\begin{aligned}\overline{P}_{\rm arm}&=\frac{1}{T_{\rm S}}\int_0^{T_{\rm S}} u_{\rm arm}(t)i_{\rm brake}(t)dt \\ &=k\,(1-k)\,\frac{U_{\rm dc}^2}{R_{\rm brake}}d-A\,(1+A)\,\frac{U_{\rm dc}^2}{R_{\rm brake}}\,(1-d)\,.\end{aligned} \tag{11}$$

Here, $\bar{P}_{\rm arm}$ is the average net power flowing into the UCH arm, which can be used to control the time average of the capacitor voltages to alleviate overvoltage or undervoltage. Defining the time average of energy storage within the arm is $E_{\rm arm}$, then the following equation is gained:

$$E_{\rm arm}=N\times\frac{1}{2}C_{\rm SM}U_{\rm C}^2 \tag{12}$$

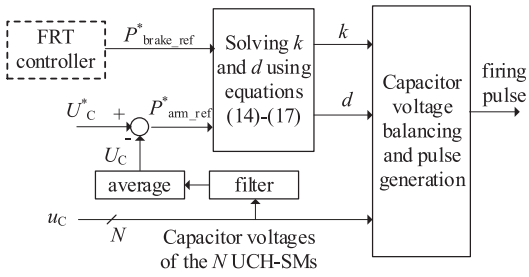

Fig. 5. Diagram of the two-state transition control strategy for UCH-MMC-DBR.

where $C_{\rm SM}$ is the SM capacitance, and $U_{\rm C}$ is the time average of the capacitor voltage, assuming that the capacitor voltages are the same. Then, the mathematical model of the capacitor in the energy–power form is

$$\frac{dE_{\rm arm}}{dt}=NC_{\rm SM}U_{\rm C}\frac{dU_{\rm C}}{dt}=\overline{P}_{\rm arm}. \tag{13}$$

Based on (13), the reference average arm power $\bar{P}_{\rm arm\_ref}$ can be generated by a capacitor voltage controller, as shown in Fig. 5.

According to (10) and (11), the following equations can be obtained:

$$P^*_{\rm brake\_ref}=\frac{P_{\rm brake\_ref}}{P_{\rm base}}=(1-k)^2d+(1+A)^2\,(1-d) \tag{14}$$

$$P^*_{\rm arm\_ref}=\frac{P_{\rm arm\_ref}}{P_{\rm base}}=k\,(1-k)\,d-A\,(1+A)\,(1-d) \tag{15}$$

where $P_{\rm base}=U^2{}_{\rm dc}/R_{\rm brake}$ is the base value of the active power and is also the rated braking power; $P_{\rm brake\_ref}$ and $P^*{}_{\rm brake\_ref}$ are the nominal and per-unit values of the reference dissipation power generated by the FRT controller, respectively; and $P_{\rm arm\_ref}$ and $P^*{}_{\rm arm\_ref}$ are the nominal and per-unit values of the referenced average arm power, respectively.

The diagram of the two-state transition controller for the UCH-MMC-DBR is shown in Fig. 5. The key control variables are the positive amplitude coefficient k and the duty cycle d. First, the average dissipation power during a wave cycle should be equal to the reference value. Once the reference values of the average braking power and the arm power are determined, the amplitude coefficient k and the duty cycle d can be solved. According to (15), the duty cycle can be expressed as

$$d=\frac{A\,(1+A)+P^*_{\rm arm\_ref}}{k\,(1-k)+A\,(1+A)}. \tag{16}$$

Then, substituting (16) into (14) comes a quadratic equation in terms of k as follows:

$$ak^2+bk+c=0 \tag{17}$$

where

$$\begin{cases} a=-\,(1+A)+P^*_{\rm arm\_ref}+P^*_{\rm brake\_ref} \\ b=1-A^2-2P^*_{\rm arm\_ref}-P^*_{\rm brake\_ref} \\ c=-A\,(A+2)\,P^*_{\rm arm\_ref}+A\,(1+A)\left(1-P^*_{\rm brake\_ref}\right).\end{cases} \tag{18}$$

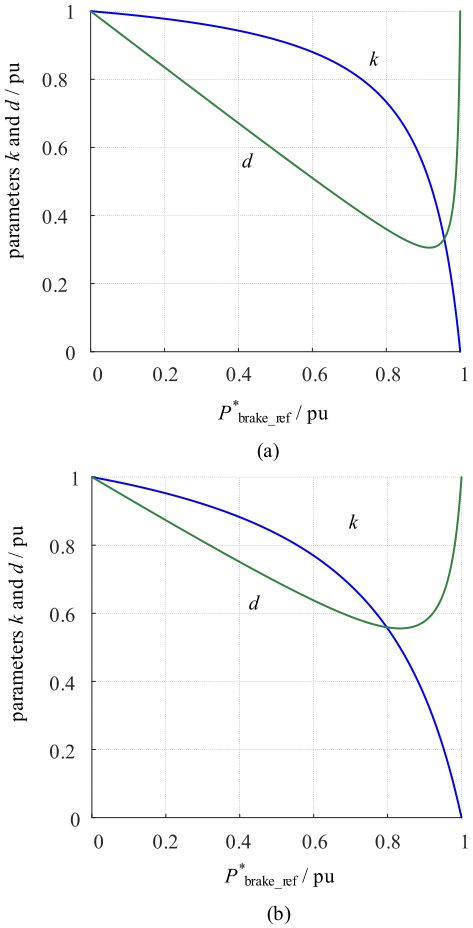

Fig. 6. Relationship between the average braking power and parameters k and d. (a) $A = 0.1$. (b) $A = 0.25$.

Considering that k is meaningful only between 0 and 1, the solution of k can be obtained as follows:

$$k = \frac{-b - \sqrt{b^2 - 4ac}}{2a}. \tag{19}$$

After k and d are determined, the arm voltage can be switched between the two states by varying the number of inserted SMs. During the steady state, the average voltage on capacitors is controlled very close to the reference, so $P^*_{\text{arm\_ref}}$ is close to zero. Based on this assumption, Fig. 6 shows the varying pattern of k and d following the braking power reference. Occasions of $A = 0.1$ and 0.25 are drawn for clarity. Based on Fig. 6, meaningful solutions of k and d can be found for all the dissipation power references.

III. Energy Storage Requirement of UCH-MMC-DBR

The energy storage requirement of the UCH-MMC-DBR is demonstrated in this section. First, the rated voltage of the SM is decided according to the voltage ratings of the semiconductors and the capacitors on the market, which is denoted as U_{CN}. Then, the number of SMs is decided by

$$N = \text{round}\left(\frac{U_{\text{dc}}}{U_{\text{CN}}}\right). \tag{20}$$

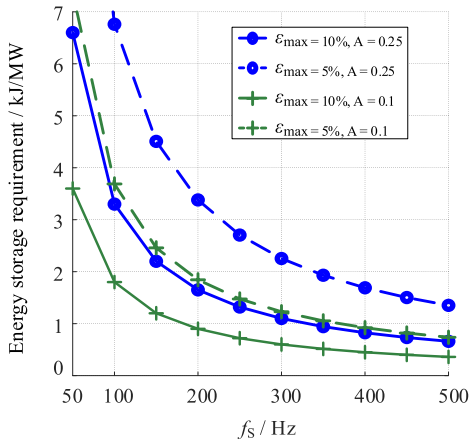

Fig. 7. Relationship between the wave frequency and the energy storage requirement.

Correspondingly, the rated energy storage in the whole arm is

$$E_{\text{armN}} = \frac{1}{2} N C_{\text{SM}} U_{\text{CN}}^2. \tag{21}$$

The energy ripples exist around the arm. According to (11), the peak ripple energy in the arm is expressed as

$$e_{\text{arm}} = \frac{U_{\text{dc}}^2}{2R_{\text{brake}}} \times k\,(1-k)\,dT_{\text{S}}. \tag{22}$$

The energy ripples generate the voltage ripples. Denoting the peak voltage as U_{Cpeak}, it can be expressed as

$$U_{\text{Cpeak}} = (1 + \varepsilon_{\max})\, U_{\text{CN}} \tag{23}$$

where $\varepsilon_{\max}$ denotes the maximum permissible ripple rate of the capacitor voltage. The relationship between the stored energy and the SM voltage is

$$E_{\text{armN}} + e_{\text{arm}} \le \frac{1}{2} N C_{\text{SM}} U_{\text{Cpeak}}^2 = (1+\varepsilon_{\max})^2 E_{\text{armN}}. \tag{24}$$

Substituting (22) into (24), the energy storage should meet

$$E^*_{\text{armN}} = \frac{E_{\text{armN}}}{P_{\text{base}}} \ge \max_{k,d}\{k \times (1-k) \times d\} \times \frac{1}{(1+\varepsilon_{\max})^2 - 1} \times \frac{1}{2f_{\text{S}}} \tag{25}$$

where E^*_{armN} defines the energy storage requirement within the arm in a unit of kJ/MW, and f_{S} denotes the wave frequency, defined as

$$f_{\text{S}} = \frac{1}{T_{\text{S}}}. \tag{26}$$

Since the energy ripples and the capacitor voltage ripples vary according to different k and d, the energy storage requirement would be the peak value by scanning all the possible k–d pairs. The energy storage requirements for different operation frequencies are shown in Fig. 7, based on different negative coefficients A and different maximum permissible ripple rates. A higher operation frequency, a smaller coefficient A, and a larger maximum permissible ripple rate would result in a lower energy storage requirement.

TABLE II
COMPARISON AMONG DIFFERENT DBRS

terms	braking chopper	modular DBR	modified modular DBR	HB-MMC-DBR	FB-MMC-DBR	UCH-MMC-DBR
require series IGBTs	***yes***	no	no	no	no	no
multilevel capability	no	yes	yes	yes	yes	yes
require water cooling	no	***yes***	***yes***	no	no	no
min. number of SMs	-	400	400	548	400	400
total IGBT/diode	400/400	400/1600	800/1600	1096/1096	***1600/1600***	800/800
total CAU	600	1200	1600	1644	***2400***	1200
max. IGBT/diode peak current / A	1562.5	1562.5	1562.5	1562.5	1718.7	1718.7
brake performance / MW/CAU	1.67	0.83	0.63	0.61	0.42	0.83
control complexity	requires simultaneous switching of IGBTs	do not require alternating voltage or current		require alternating voltage or current to keep charging balance		

Bold entities in Table II were aimed to emphasize the fatal defects of the braking chopper, the modular DBR, the modified modular DBR, and the FB-MMC-DBR.

IV. COMPARISON AMONG THE EXISTING DBRS AND THE PROPOSED UCH-MMC-DBR

The comparison among various existing DBR solutions and the proposed UCH-MMC-DBR is conducted. The rated power and the dc voltage are chosen as 1000 MW/±320 kV. The rated SM voltages in the existing DBR topologies [see Fig. 1(b)–(d)] and the proposed UCH-MMC-DBR are chosen as 1.6 kV. Therefore, the prevailing 3.3 kV IGBTs and diodes are chosen as the semiconductor devices in the DBRs. The chip area unit (CAU) and the braking performance that was defined in [14] are used to evaluate the semiconductor usage in various DBR topologies. A single IGBT is approximated as 1.0 CAU and a single diode is 0.5 CAU. Furthermore, braking performance is defined as the braking power capability per CAU. Higher braking performance means a higher utilization of the semiconductors.

The comparison results are given in Table II. The braking chopper has the simplest topology, where tens or hundreds of IGBTs are connected in series, and then they are connected with the braking resistor. The least IGBTs and diodes are used in the braking chopper circuit, and thus, the highest braking performance is achieved. However, dynamic voltage sharing is a great challenge in this solution because hundreds of IGBTs are connected in series. All the IGBTs must be switched ON or OFF simultaneously in real applications.

As for the modular DBR and the modified modular DBR, the braking resistors are distributed in each SM. This inevitably requires the distributed water-cooling system. The cost of this kind of cooling system is very high. This increases the project investment.

The HB- and FB-MMC-DBRs alleviate the series connection of the IGBTs and the centralized braking resistor enables the air cooling of the resistor. However, as for the HB-MMC-DBR, 37% extra semiconductor usage is required to generate the reverse discharging current, compared with a conventional HB-MMC arm. The FB-MMC-DBR uses even more IGBTs than the HB-MMC-DBR. The braking performance of these two types of DBRs is low.

Since each UCH-SM contains only two IGBTs and two diodes, the total CAU of UCH-MMC-DBR is much lower than that of HB-MMC-DBR and FB-MMC-DBR. As given in Table II, among the modular-structured topologies, the UCH-MMC-DBR and modular DBR have the lowest CAU and the highest braking performance. Compared with the modular DBR, the employment of the lumped resistor in the UCH-MMC-DBR alleviates the distributed water-cooling system, which lowers the cost and facilitates the cooling system design. Therefore, considering the cost of the braking resistor and cooling system, the cost of the UCH-MMC-DBR will be lower than that of the modular DBR. From the aspect of the controllers, the modular DBR and the modified modular DBR have the simplest controllers since there is no need for the alternation of either the arm current or the arm voltage. Although the HB-, FB-, and UCH-MMC-DBR need to calculate the time points where the current or the voltage changes the direction, the technique can be easily realized by the digital signal processors (DSPs) or FPGAs. Although the maximum peak current of IGBTs/diodes in the UCH-MMC-DBR is a little higher, the peak current of 1718.7 A is still acceptable for the IGBTs with 1500 A rated current (the repetitive peak collective collector current of which can reach 3000 A).

In conclusion, the UCH-MMC-DBR has many advantages in cost and design difficulties over modular DBR, modified modular DBR, HB-MMC-DBR, and FB-MMC-DBR, and the modular design and multilevel characteristics make it more accessible than the braking chopper. The controller of the UCH-MMC-DBR can be easily realized in the DSPs or FPGAs.

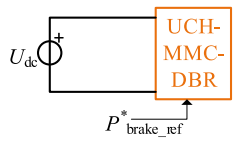

Fig. 8. Diagram of the simulation model of the UCH-MMC-DBR connected with a voltage source.

V. SIMULATION RESULTS

First, a 640 kV/1000 MW simulation model consisting of a dc voltage source and a UCH-MMC-DBR was built within MATLAB/Simulink, as shown in Fig. 8, to verify the power

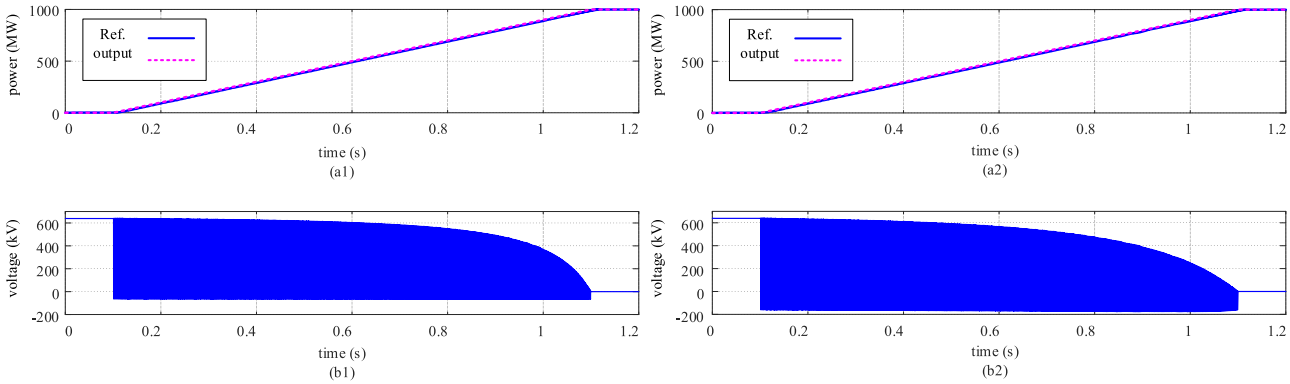

Fig. 9. Power rising simulation. (a1) Braking power and its reference when $A = 0.1$. (b1) UCH-MMC arm output voltage when $A = 0.1$. (a2) Braking power and its reference when $A = 0.25$. (b2) UCH-MMC arm output voltage when $A = 0.25$.

TABLE III
MAIN PARAMETERS OF THE SIMULATION MODEL OF THE UCH-MMC-DBR CONNECTED WITH A VOLTAGE SOURCE

Terms	Values
dc voltage	640 kV
rated dissipation power	1000 MW
braking resistance	410 Ω
wave frequency	500 Hz
SM voltage	1600 V
number of UCH-SMs	400
SM capacitance	700 μF

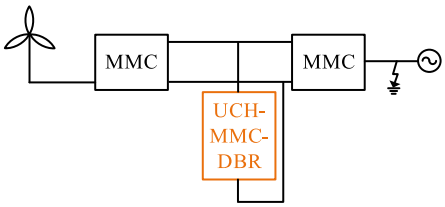

Fig. 10. Diagram of the simulation model of the UCH-MMC-DBR in a VSC-HVdc system.

braking performance of the UCH-MMC-DBR under different braking power references. The UCH-MMC-DBR was connected with a constant dc voltage source. The detailed parameters of the simulation model are listed in Table III. The cases of the negative voltage level $A = 0.1$ and $A = 0.25$ were simulated, respectively. Since the dc voltage was constant, the braking power reference was given from an outer control port. The power reference rose from 0 to 1.0 p.u. (1000 MW) in a sloped wave.

The simulation results when $A = 0.1$ and $A = 0.25$ are shown in Fig. 9. Using the proposed two-state transition control strategy, the UCH-MMC arm output voltage varied based on the braking power reference and the power followed its reference well from 0 to 1000 MW.

Then, a 1000 MW simulation model was built within MATLAB/Simulink, as shown in Fig. 10, to show the overvoltage suppression effects of the UCH-MMC-DBR in a VSC-HVdc system. The model was composed of an onshore MMC connected with an ac grid and an offshore MMC connected with a wind farm. The UCH-MMC-DBR was installed close to the dc port of the onshore MMC. The simulation parameters are listed

TABLE IV
MAIN PARAMETERS OF THE SIMULATION

Terms	Values
dc voltage	640 kV
rated power	1000 MW
braking resistance	410 Ω
wave frequency	500 Hz
parameter A	0.1
energy storage requirement	360 kJ
SM voltage	1600 V
number of UCH-SMs	400
SM capacitance	700 μF
max. ripple rate	10%

in Table IV. The wave frequency is designed as 500 Hz, and the maximum permissible ripple rate of the capacitor voltage is designed as 10%. Based on the results, as shown in Fig. 7, the energy storage requirement is 0.36 kJ/MW and the SM capacitance is 700 μF. The dc voltage trigger of the UCH-MMC-DBR was set as 1.2 p.u., namely, 768 kV. The braking power reference was generated by a closed-loop proportional–integral (PI) controller of dc voltage. The dc voltage reference of the UCH-MMC-DBR was set as 1.0 p.u. (640 kV).

At the beginning of the simulation, the system was in the steady state, transmitting the power of 1000 MW. At $t = 1.8$ s, a three-phase fault was simulated at the onshore grid and the ac voltage drops to 0.2 p.u.

The simulation results when UCH-MMC-DBR operated were shown in Fig. 11. At $t = 1.8$ s, the ac voltage decreased to 0.2 p.u. because of the fault, as shown in Fig. 11(a). In Fig. 11(b), the ac power transmission capability of onshore MMC was reduced to 200 MW. Fig. 11(c) shows the dc voltage. The dc voltage began to increase because the power was stuck in the dc system. When the dc voltage reached 1.2 p.u., the UCH-MMC-DBR was triggered and started to operate.

At the beginning of the operation of the UCH-MMC-DBR, the UCH arm output zero voltage and the dc voltage were added on the braking resistor, as shown in Fig. 11(d). This is because the dc voltage was high, and the braking power reference, as shown in the dashed line in Fig. 11(b), reached the rated power 1000 MW and the power that was absorbed by the resistor followed its reference. The dc voltage decreased very quickly at

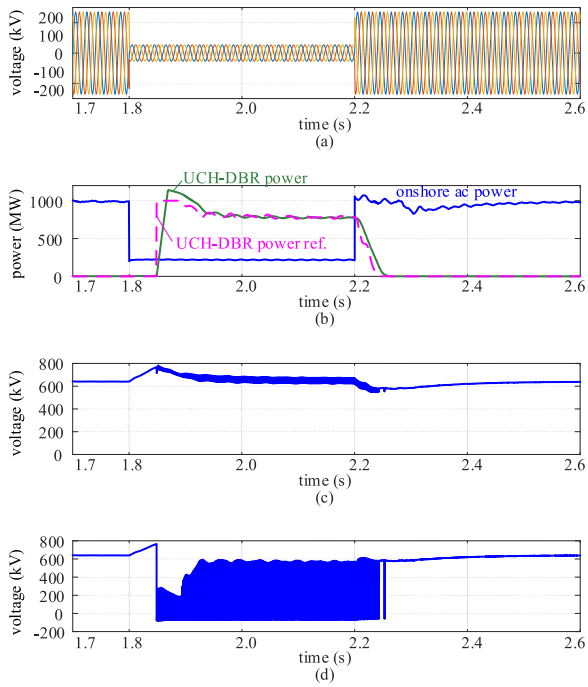

Fig. 11. Simulation results of the system when the UCH-MMC-DBR operates. (a) AC voltage. (b) Power. (c) DC voltage. (d) Arm output voltage.

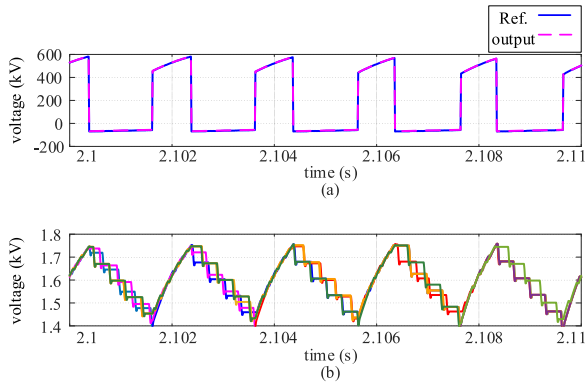

Fig. 12. Simulation result of detailed waveforms. (a) UCH-MMC-DBR arm output waves. (b) Capacitor voltages of SMs.

this stage. Then, the UCH-MMC-DBR operated with variable voltage levels, as shown in Fig. 11(d), and the dc voltage was kept as 640 kV. At $t = 2.0$ s, the fault was cleared, and the power transmission capability of the onshore ac grid resumed to 1000 MW. The braking power of UCH-MMC-DBR returned to zero and then it was blocked. The whole system returned to normal operation.

Fig. 12 shows the detailed waveforms in operation. Fig. 12(a) shows the arm output voltage. The simulated real output wave followed its reference using the two-state transition control strategy, as shown in Fig. 12(a). Fig. 12(b) shows some of the SM capacitor voltages. The wave frequency, as given in Table IV, was 500 Hz, so the capacitors were charged–discharged with a time period of 0.002 s. The voltage sorting method ensured the voltage balance of SMs. The voltage ripple of the capacitors in the steady-state braking stage did not exceed the limitation, which is 10% of the average voltage.

TABLE V
MAIN PARAMETERS OF THE EXPERIMENT

Terms	Values
dc voltage	800 V
rated power	3.2 kW
braking resistance	200 Ω
wave frequency	250 Hz
parameter A	0.25
energy storage requirement	7.8 J
SM voltage	100 V
number of UCH-SMs	8
SM capacitance	195 μF
max. ripple rate	5.5%

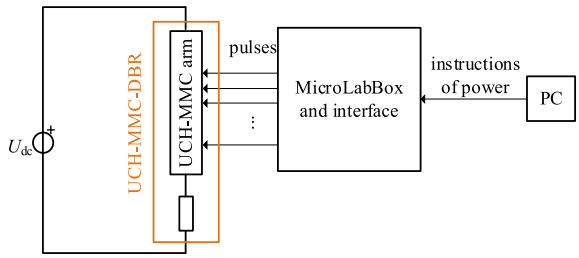

Fig. 13. Diagram of the experimental platform.

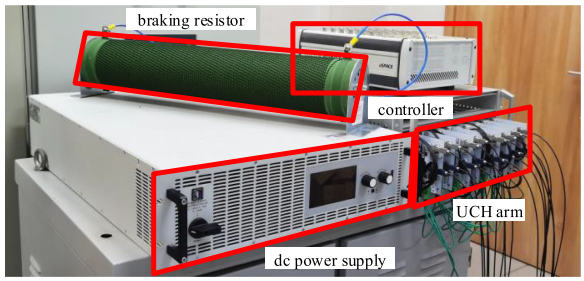

Fig. 14. Photograph of the experimental platform.

VI. EXPERIMENTAL RESULTS

An experimental prototype was built to verify the proposed UCH-MMC-DBR. The rated dc voltage was 800 V, and the rated dissipation power was 3.2 kW. The main parameters of the prototype are listed in Table V. The wave frequency was designed as 250 Hz. The maximum permissible ripple rate of the SM capacitor voltages was designed as 5.5%. Based on the energy storage requirement analysis, the energy storage requirement was 2.44 kJ/MW, and the SM capacitance was 195 μF. The diagram and the photograph of the experimental platform are shown in Figs. 13 and 14, respectively. A programmable dc power supply was used to simulate the dc voltage. The dSPACE MicroLabBox was used as the controller. The proposed two-state transition control strategy was used.

Fig. 15(a)–(c) shows the experimental results at $P^*_{\text{brake}} =$ 0.1 p.u., 0.5 p.u., and 0.8 p.u., respectively. The arm output voltage changed between the positive and the negative voltages. The positive output voltage of the arm varied according to the different braking powers. Higher power references resulted in lower positive voltage levels. The resistor voltage and current changed corresponding to the arm output voltages. The current was always unidirectional during the operation. The capacitor

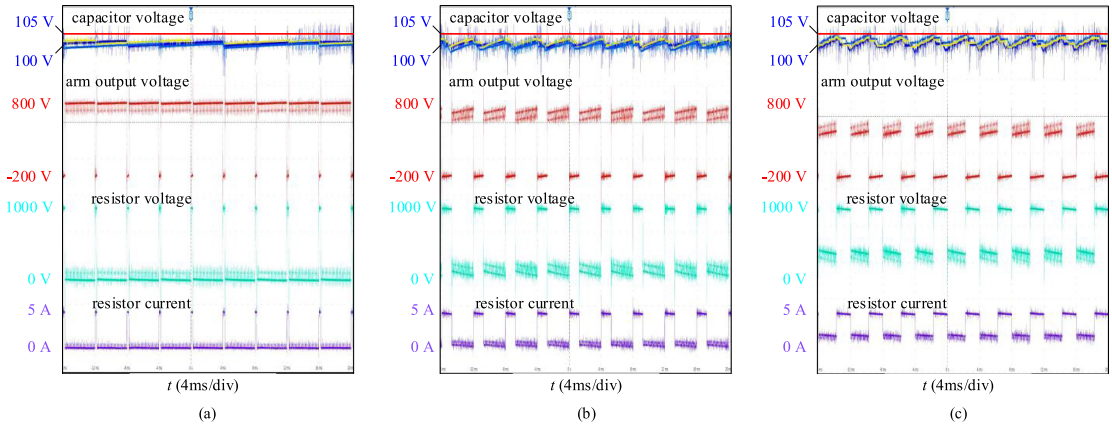

Fig. 15. Experimental results when $P_{\mathrm{brake}} = 0.1$ p.u., 0.5 p.u., and 0.8 p.u. (a) $P_{\mathrm{brake}} = 0.1$ p.u., 320 W. (b) $P_{\mathrm{brake}} = 0.5$ p.u., 1600 W. (c) $P_{\mathrm{brake}} = 0.8$ p.u., 2560 W.

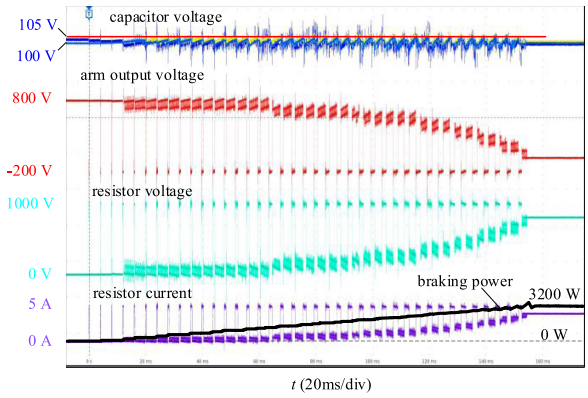

Fig. 16. Experimental results when power dissipation increases from 0 to 1.0 p.u.

voltages were overlaid to see the effects of the sorting algorithm. The time averages of the capacitor voltages were around 100 V. The instantaneous capacitor voltages fluctuated as the arm output voltage alternated between the positive and negative voltage levels.

Fig. 16 shows the waveforms when the reference dissipation power was gradually increased from 0 to 1.0 p.u. The average braking power was also calculated using recorded data. With the braking power increasing, the positive output voltage of the arm decreased, allowing more current to flow through the braking resistor. The capacitor voltages were well balanced. The capacitor voltage ripples varied at different braking powers. The maximum voltage was 105 V, which was below the maximum permissible voltage.

The scaled prototype was designed and constructed under the similarity theory as a real megawatt-level project. Therefore, the charging balance, the energy storage requirement and the dynamic process, and other physical characteristics can be truly reflected using the experiments on the scaled prototype. Using the characteristic of the capacitor voltage ripple as an example, the ripple rate of the capacitor voltage is related to the per-unit energy storage requirement (E^*_{armN} in kJ/MW), the negative voltage coefficient (A), and the wave frequency (f_{S}). As long as E^*_{armN}, A, and f_{S} are the same, the maximum ripple rate of the capacitor voltage would be exactly the same in systems with different power levels.

VII. Conclusion

The DBRs in the HVdc systems are essential equipment to limit the dc voltage during ac faults. The existing HB- and FB-MMC-based DBRs require relatively large semiconductor usage and are not cost efficient. Based on the fact that an FBSM can be simplified to a UCH-SM, a new UCH-MMC-DBR circuit with a two-state transition control strategy is proposed. The UCH-MMC-DBR can avoid series connection of IGBTs and has advantages, such as the simple lumped resistor and the modular design. The semiconductor usage in UCH-MMC-DBR is 37% lower than that in the HB-MMC-DBR and 50% lower than that in the FB-MMC-DBR. The evaluation result shows that the UCH-MMC-DBR has advantages in cost and design difficulties over other existing DBR topologies. The proposed two-state transition control strategy can enable the braking power to track the reference while maintaining the charging balance of the SM capacitors in a UCH-MMC-DBR. The simulation and experimental results verified the feasibility of the proposed UCH-MMC-DBR and the two-state transition control strategy.

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Zhengxuan Li (Student Member, IEEE) was born in Beijing, China, in 1995. He received the B.S. degree from North China Electric Power University, Beijing, China, in 2018. He is currently working toward the Ph.D. degree with Tsinghua University, Beijing, China.

His current research interests include modular multilevel converter, wind power, and VSC-HVdc transmission system.

Yuebin Zhou (Senior Member, IEEE) was born in Shaanxi, China, in 1987. He received the B.E.E. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2009 and 2014, respectively.

He is currently a Researcher with Electric Power Research Institute, China Southern Power Grid, Guangzhou, China. His main research interests include flexible alternating-current transmission systems and voltage-sourced converter-based high-voltage direct current systems.

Nan Zhang was born in 1978. He received the B.S. degree in 2001 from the Hefei University of Technology, Hefei, China.

He is currently working with the DC Technology Department of Maintenance and Test Center of Extra High Voltage Power Transmission Co., China Southern Power Grid Co., Ltd., Guangzhou, China. His main research interests include control and protection strategies in HVDC transmission systems and VSC-HVDC.

Qiang Song (Senior Member, IEEE) was born in Changchun, China, in 1975. He received the B.E.E. and Ph.D. degrees both in electrical engineering from Tsinghua University, Beijing, China, in 1998 and 2003, respectively.

From 2003 to 2008, he was a Lecturer with the Department of Electrical Engineering, Tsinghua University, where he has been an Associate Professor since 2008. His main research interests include high-power electronic interfaces for utility system, flexible ac transmission system, VSC-HVdc system, and custom power quality.

Rong Zeng (Senior Member, IEEE) was born in Shaanxi, China, in 1971. He received the B.Eng., M.Eng., and Ph.D. degrees from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 1995, 1997, and 1999, respectively.

He was a Lecturer with the Department of Electrical Engineering, Tsinghua University, in 1999, an Associate Professor and a Professor with the same department in 2002 and 2007, respectively. He is currently working in the fields of air gap discharge, lightning protection, electromagnetic compatibility in power systems, electric and magnetic field measurement by integrated electro-optical sensors, power semiconductor, HVdc system, and direct current circuit breaker.

Biao Zhao (Senior Member, IEEE) was born in Hubei, China, in 1987. He received the B.S. degree from the Department of Electrical Engineering, Dalian University of Technology, Dalian, China, in 2009, and the Ph.D. degree from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2014.

He is currently an Associate Professor with the Department of Electrical Engineering, Tsinghua University. His research interests include high-power converters, high-power semiconductor devices, and flexible dc transmission and distribution systems.

Dr. Zhao is a Senior Member of the Chinese Society for Electrical Engineering and the Chinese Electrotechnical Society.

Zhanqing Yu (Member, IEEE) was born in Inner Mongolia, China, in 1981. He received the B.Sc. and Ph.D. degrees from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in July 2003 and July 2008, respectively.

After graduation, he became a Postdoctor and a Lecturer with the Department of Electrical Engineering, Tsinghua University, in July 2008 and July 2010, respectively, and an Associate Professor with the same department in December 2012. He has participated in several projects sponsored by High-Tech R&D Program (863 Program), National Basic Research Program of China (973 Program), and National Natural Science Foundation of China. His research interests include dc grid, dc breaker, electromagnetic environment and electromagnetic compatibility, and lightning protection.