Direct Integration of Optimized Phase-Change Heat Spreaders Into SiC Power Module for Thermal Performance Improvements Under High Heat Flux

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***Abstract*—Silicon carbide (SiC) power modules are attractive in many applications due to the superiority of their semiconductor characteristics. However, power modules are subjected to repetitive thermo-mechanical stress caused by the mismatch of the coefficient of thermal expansion between different layers of materials. Moreover, the relatively smaller die size of SiC chips makes the heat flux increase significantly, which brings new challenges to the thermal management and reliability of SiC power modules. To tackle these challenges, this article proposes a new thermal enhanced packaging method based on vapor chamber (VC) phase change heat spreader (PCHS) for SiC power modules, achieving the advantages of high thermal conductivity, low weight, low cost, and low thermal stress. In this new design, SiC MOSFET bare dies are directly soldered on the top of VC-PCHS, which not only act as heat spreaders but also conduct the drain current of MOSFETs. The integrated VC-PCHS is optimized based on thermal and thermomechanical performance. An SiC power module prototype directly integrated with VC-PCHS is built using a new fabrication process. Both the simulations and experiments demonstrate significant improvements in thermal and thermomechanical performance. The modules integrated with VC-PCHS can operate under 200 W of power dissipation per die (632 W/cm^2) without exceeding the maximum rated junction temperature. This article reveals the potential of directly integrating phase change cooling components inside power modules, providing a new solution to improve the thermal performance and reliability of SiC power modules without adding complexity and energy consumptions to external cooling systems.**

***Index Terms*—High heat flux, phase-change heat spreader (PCHS), reliability, SiC power module packaging, thermal management, thermal stress, vapor chamber (VC).**

I. Introduction

COMPARED with silicon-based semiconductors, wide-bandgap (WBG) semiconductors such as silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) have benefits including high blocking voltage, low ON-resistance and the capability to work at a higher frequency [1]–[3]. After years of development in manufacturing techniques, commercialized SiC MOSFET can replace Si IGBT at the medium voltage range [4], pushing the power converters toward higher efficiency and higher power density. In 20 kVA solid-state transformer applications, a 10 kV SiC MOSFET can work at 7–10 times higher switching frequency than a 6.5 kV Si IGBT [5]. A three-port dc/dc converter based on the dual active bridge (DAB) using SiC MOSFETs is reported to have 2.74 kW/L power density and 98.2% efficiency [6]. An SiC-based *LLC* on-board charger (OBC) reaches the power density of 3.42 kW/L with the peak efficiency of 96% at 6.6 kW output power [7]. Compared with the Si-based reference design, the SiC-based OBC can increase the power density by 55.6% and the efficiency by more than 2%.

For the same voltage and current ratings, SiC devices usually have much smaller sizes than their Si counterparts. This is because the per area-specific ON-resistance of SiC MOSFETs is 5 times smaller than that of Si IGBT [10]. Fig. 1 compares the die size between the commercially available Si IGBT and SiC MOSFET bare dies at the same voltage and current ratings of 1200 V, 150 A. In this case, the SiC MOSFET is 4.4 times smaller than Si IGBT. On the one hand, this reduction in die area opens the opportunity to increase the power density of modules; on the other hand, under the same power losses per die, the heat flux goes through the chip's bottom increases dramatically, up from

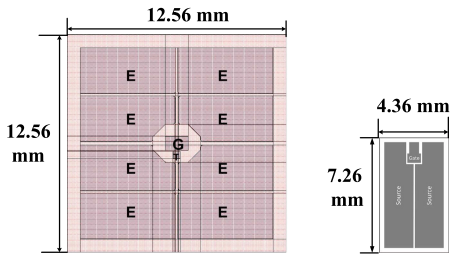

Fig. 1. Comparison of die size between (a) 1200 V, 150 A, Si IGBT (Infineon SIGC158T120R3E) [8], and (b) 1200 V, 149 A SiC MOSFET (CREE CPM3-1200-0013A) [9].

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100–250 W/cm^2 to 1 kW/cm^2 [11]. Furthermore, the thermal capacitance of the SiC die is also smaller due to its small size, which limits the short-circuit and over current capability and leads to more significant junction temperature swings [10]. The high heat flux and small thermal capacitance bring challenges to the packaging and thermal management system for SiC power modules.

A. Advancements in Thermal Management Systems

More advanced cooling solutions have been extensively researched in recent years. Some of them were initially designed for integrated circuits (ICs) in computers or high-power LEDs, but they can be modified and applied to power modules. Generally, micro- and mini-channel liquid cooling can provide better cooling performance than the conventional cold plates [12]. However, the nonuniform temperature distribution caused by flow redistribution, clogging and pressure drop are the main drawbacks of micro- and mini-channel heatsinks. A genetic algorithm is employed in [13] to optimize the temperature uniformity and reduce the pressure drop of liquid-cooled heatsink according to the layout of thermal loadings and structure of the substrate. Near junction cooling and embedded cooling were proposed and implemented in power devices recently. The concept of three types of embedded cooling for vertical current WBG semiconductor devices are proposed in [14]. Zhou *et al.* [11] introduce a 20 mm $\times$ 10 mm cooling chip based on microchannel plus jet impingement array architecture. The cooling chip achieved a heat transfer coefficient of 120.2 kW/(m^2·K), enabling a five-to ten-fold reduction in package size. As a high risk and high reward cooling strategy, embedded cooling requires building channels for fluid flow inside power devices, electrodes or cooling chips, which is relatively complex.

Thermoelectric cooling (TEC) has advantages including high reliability, low weight, small size, and precise control of temperature [15]. However, the maximum power dissipation of TEC is limited and it generates heat during operation. Jet impingement is becoming attractive in high heat flux applications. More than 2 kW/cm^2 heat removal capability is reported in [16]. Gould *et al*. utilize a custom-designed heat sink with an array of liquid jet impingement orifices directly embedded at the base plate of the 938-W SiC JFET power electronics module. Under 100 °C coolant temperature, jet impingement cooling can reduce the junction temperature by 121 °C compared with the commercial cold plate and by 46 °C compared with the commercial micro-channel cold plate [20]. Two-phase forced cooling using a compressor is reported to have a 39 °C temperature reduction compared with single-phase cooling for automotive IGBT power module applications [17]. Combined with micro-channel structures, two-phase cooling can reach a heat transfer coefficient up to 50 k W/(m^2·K) [18], [19]. There are two major drawbacks for jet impingement and forced two-phase cooling using a compressor. First, both cooling systems are complex and costly. Second, for jet impingement cooling, a more powerful pump is required to cope with the significant pressure drop in impingement orifices and for forced two-phase cooling, a power-consuming compressor is often used, increasing the weight and energy consumption of the thermal management system.

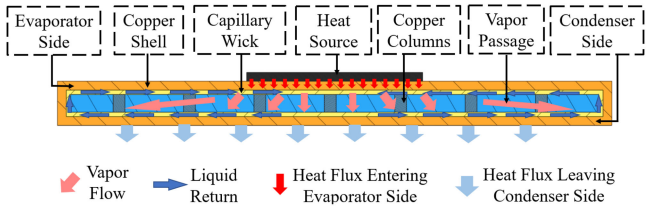

Fig. 2. Cross-section of a VC-PCHS.

B. Advancements in Packaging Elements and Structures

With the downsizing of power semiconductor devices, a lot of researches have been done to design novel packaging structures and new types of materials have been adopted to deal with the increasing heat flux density generated by power semiconductor devices.

Aluminum oxide is the most commonly used insulator in direct bonded copper (DBC). However, Al_2O_3 has a low thermal conductivity of 24 W/(m·K), making the thermal resistance of Al_2O_3 based DBC relatively high. Aluminum nitride (AlN) is a high-performance dielectric material with high breakdown voltage and high thermal conductivity (170 W/ (m·K)). However, AlN is a brittle material and not mechanically strong enough. So, the dielectric layer in AlN-based DBC is commonly 630 μm or 1 mm thick. Although the thermal conductivity of silicon nitride (Si_3N_4) is not as high as AlN, Si_3N_4 is mechanically stronger than AlN. Therefore, Si_3N_4 can be made thinner to match the thermal performance of AlN substrates [21]. Both AlN and Si_3N_4 based DBC is more expensive to manufacture.

New packaging structures have been proposed to promote the heat spreading inside power modules and reduce thermal resistance. Gurpinar *et al.* [21] design an insulated metal substrate (IMS) to replace DBC for high-power WBG modules. Because the dielectric layer HT-07006 in this article has poor thermal conductivity (2.2 W/(m·K)), the thickness of the top layer copper core is 1.6 mm to promote heat spreading and reduce overall thermal resistance. Later, they integrate graphite in the copper core which utilizes the high in-plane thermal conductivity of graphite to further increase the heat spreading ability and heat capacity [22]. The designed thermally-annealed-pyrolytic-graphite-embedded insulated metal substrate (IMSwTPG) can reduce the thermal resistance up to 17%. A thick lead frame substrate made of copper is proposed in [23]. This structure can spread heat effectively before it passes the insulation layers. Shao *et al.* [24] directly embed copper frame containing phase change material on DBC to improve the over current capability of power modules [24]. However, the thermal stress introduced by the thicker copper frame is not mentioned in [23] and. For double-sided packaging, copper posts are often used as the spacer between chips and the top substrate for their good heat spreading and current-conducting performance [25]. Nevertheless, large thermomechanical stress is introduced by a double-sided structure both at the joint and chip [26]. To reduce the thermal stress, trenched copper plates are introduced in [27]

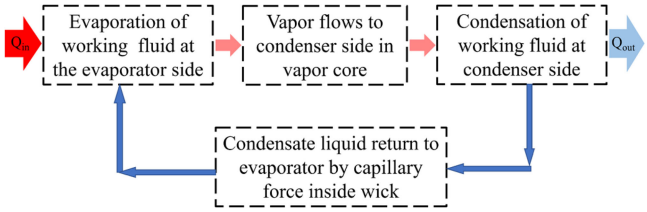

Fig. 3. Phase change loop and working principles in VC-PCHS.

and the molybdenum buffer layer is adopted in [28], whereas the thermal performance is slightly degraded in these structures. A novel bridge buffering spacer is presented in [29]. Generally speaking, the design of the spacer needs a tradeoff between thermal performance and thermal stress. Vapor chamber (VC), which is a phase-change heat spreader (PCHS), is adopted in power module packaging in [30]–[32]. However, in these designs, the VC-PCHS is far from the die of power devices, which restrains VC-PCHS's heat spreading ability.

This article presents for the first time, the optimization, simulation, fabrication process, and experimental validation of directly integrating VC phase-change heat spreaders into SiC power modules. In this article, the VC-PCHSs not only act as heat spreaders but also conduct the drain current of MOSFETs. Because of the hollow structure and the excellent thermal conductivity of the VC-PCHS, the thermal resistance of the packaging is significantly reduced while the thermal stress is kept low. Besides, VC-PCHS can be made into flexible shapes [33] according to the layout of DBC substrate and power devices, which is compatible with current packaging structures. Adding VC-PCHSs does not add energy consumptions to the cooling system and the cost is modest.

The rest of this article is organized as follows. Section II introduces the working principle of VC-PCHSs, the optimization based on the thermal and thermomechanical performance and their integration with SiC power modules. Section III presents the finite-element analysis (FEA) model and the thermal and mechanical simulation results. Section IV presents the experimental setup and analysis. Finally, Section V concludes this article.

II. Direct Integration of VC-PCHS Into SiC Power Module

A. Working Principles and Thermal Model of VC-PCHS

The cross-section of VC-PCHS is shown in Fig. 2. It is a metallic shell with capillary wick at the inside wall. The inside of the shell is a vacuum vapor core containing working fluid. Copper and water are the most often used material of the shell and the working fluid. The shell is mainly composed of evaporator and condenser sides. Copper studs form the joint between the two sides to strengthen the shell against vapor pressure change. The closed-looped phase change cycle is illustrated in Fig. 3. In this article, as the concentrated heat flux dissipated by SiC MOSFETs enters the evaporation side, the working fluid will instantly absorb latent heat and vaporize to fill in the vacuum vapor core. When the vapor comes into contact with a cooler surface, it condenses and releases the latent heat. In this way, the concentrated heat source is spread to a much larger domain. The condensed working fluid flows back to the heat source by capillary force, which is capable of overcoming gravity and allow the VC-PCHS to work in any direction [34]. Because of the high heat transfer coefficient of the phase change process, a VC-PCHS's effective thermal conductivity reaches 20 kW/(m·K) [35], which is 50 times higher than copper.

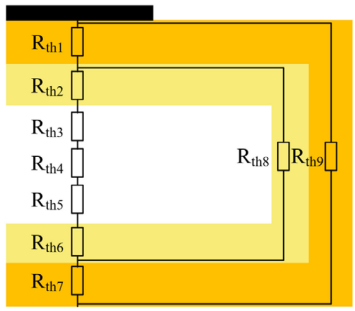

Fig. 4. Equivalent thermal resistance network inside VC-PCHS.

TABLE I
Thermal Resistance Notations

Notation	Thermal Resistance
R_{th1}, R_{th7}	Thermal resistance of metallic shell
R_{th2}, R_{th6}	Thermal resistance of polyporous wick
R_{th3}, R_{th5}	Thermal resistance of liquid-gas interface
R_{th4}	Thermal resistance of vapor propagation
R_{th8}	Thermal resistance of transverse thermal conduction in the polyporous wick
R_{th9}	Thermal resistance of transverse thermal conduction in the metallic shell

In order to calculate the temperature distribution of the VC-PCHS and the power devices attached to it, a thermal model of the VC-PCHS needs to be built and the thermal conductivity and capacitance of each layer should be known. The equivalent thermal resistance network is shown in Fig. 4 and the meaning of each thermal resistance is shown in Table I. The thermal resistance of liquid–gas interface R_{th3} and R_{th5} varies with the level of phase-change. The thermal resistance of transverse thermal conduction in polyporous wick R_{th8} is large compared with the others.

In this article, the shell of VC-PCHS is made of copper with thermal conductivity of 401 W/(m·K). Copper powder with a porosity ratio of 70% is sintered at the inside of the shell. The effective thermal conductivity $k_{\text{eff-wick}}$ and the volumetric heat capacity $(\rho C_p)_{\text{eff-wick}}$ of the wick can be calculated using the equation proposed by Faghri [36]

$$k_{\text{eff}-\text{wick}} = k_p \left(\frac{2 + \frac{k_f}{k_s} - 2\varphi\left(1 - \frac{k_f}{k_s}\right)}{2 + \frac{k_f}{k_s} + \varphi\left(1 - \frac{k_f}{k_s}\right)} \right) \tag{1}$$

$$(\rho C_P)_{\text{eff}-\text{wick}} = \varphi(\rho C_P)_f + (1-\varphi)(\rho C_P)_s \tag{2}$$

where φ is the porosity ratio, k_f and k_s are the thermal conductivity of working fluid and solid, which are water and copper

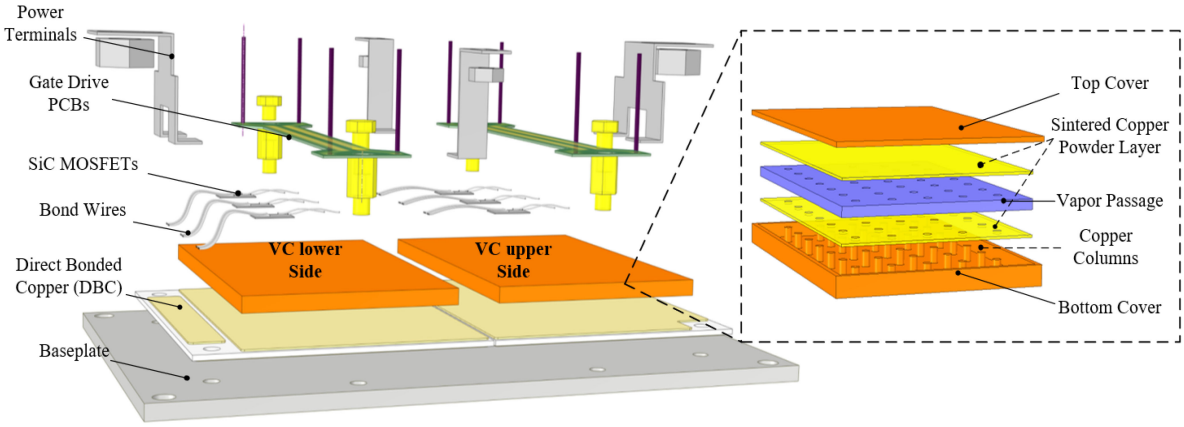

Fig. 5. Exploded view of a half-bridge module integrated with VC-PCHSs under SiC dies.

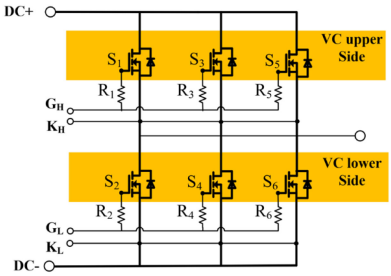

Fig. 6. Schematic diagram of the SiC power module integrated with VC-PCHSs.

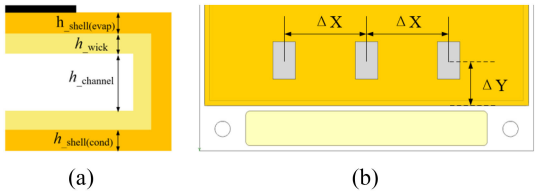

Fig. 7. Parameters of (a) interior structure of VC-PCHS and (b) layout of SiC MOSFETs.

powder in this case. Generally, in VC-PCHS made of copper, k_{eff} of the wick is about 50 W/(m·K) and the k_{eff} of the vapor core ranges from 50 to 200 kW/(m·K) [37].

B. Design and Optimization

The power device selected in this study is SiC MOSFET (CREE CPM3-0900-0010A) rated at 900 V, 194 A, and 10 mΩ. This SiC die's footprint is only 0.32 cm2 (4.36 mm×7.26 mm), making the thermal capacitance relatively low and the heat flux density very high. As a result, the thermal issue is the bottleneck limiting the current carrying capability and reliability of this device.

Fig. 5 illustrates the exploded view of the half-bridge module in this article as an example to demonstrate the thermal performance improvements of directly integrating, and Fig. 6 illustrates its schematic diagram integrated with VC-PCHSs. On each side of the half-bridge, there are three aforementioned SiC MOSFETs connected in parallel and a customized VC-PCHS soldered under these MOSFETs. Gate drive PCB with drive resistors is mounted on the VC-PCHS. Bond wires make the electrical linkages between power terminals and the Kelvin-source connection for the gate and source terminals.

The main parameters considered in this article are demonstrated in Fig. 7. $h_{\text{-shell(evap)}}$ is the thickness of the shell at the evaporator side. The heat flux dissipated by the MOSFET dies should first go through the solder and the copper shell of VC-PCHS and then enters the wick structure where the phase change of working fluid happens. Because the transverse thermal conductivity of the wick is relatively low, the copper shell acts as a first-stage heat spreader. A thicker shell can spread the heat flux more sufficiently before it reaches the wick, avoiding the local dry out of the wick. $h_{\text{-shell(evap)}}$ also influences the thermal stress inside the solder layer between SiC die and the shell due to the mismatch of coefficient of thermal expansion (CTE). Solder is a ductile material in which ductile rupture occurs when accumulative plastic deformation results in a progressive reduction in the local cross-sectional area [27]. In von Mises' maximum distortion energy theory, failure occurs when the distortion energy u_{d} reaches a critical level $u_{\text{d,y}}$

$$u_d = \frac{1+\nu}{6E}\left[(\sigma_1-\sigma_2)^2+(\sigma_2-\sigma_3)^2+(\sigma_3-\sigma_1)^2\right] \quad (3)$$

$$u_{d,y} = \frac{1+\nu}{3E}\sigma_y^2 \quad (4)$$

where σ_1, σ_2, and σ_3 are the principal stress. σ_y is the yield stress. E is Young's modulus and ν is Poisson's ratio. By combining (3) and (4), the material fails when

$$\sqrt{\frac{1}{2}\left[(\sigma_1-\sigma_2)^2+(\sigma_2-\sigma_3)^2+(\sigma_3-\sigma_1)^2\right]} = \sigma_y. \quad (5)$$

The left part of the (5) is defined as the equivalent von Mises stress σ_{eq}. For ductile material, σ_{eq} should be kept below σ_y to prevent failure. The distribution and the value of von Mises stress can be used to predict a ductile rupture in the power module [38].

Assuming the power loss of 60 W per die, the results of the thermal and stress-strain analysis are shown in Fig. 8. When $h_{\text{-shell(evap)}} \leq 1.2$ mm, the temperature decreases as

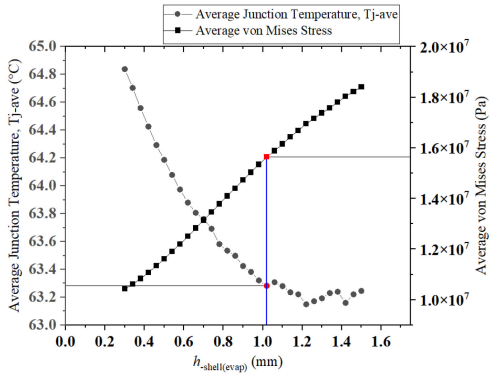

Fig. 8. Thickness of the copper shell at the evaporator side $h_{\text{-shell(evap)}}$ and its influence on junction temperature and von Mises stress in the die solder layer.

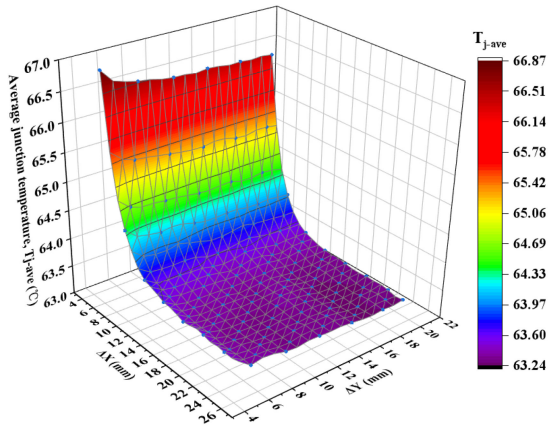

Fig. 9. Layout of SiC bare dies on the VC-PCHS and its relation with the average junction temperature.

the thickness of the wall increases. σ_{eq} increases linearly with $h_{\text{-shell(evap)}}$. Because the VC-PCHS is vacuumed and injected with the working fluid, it is subjected to the pressure difference between the atmosphere outside and the vaporization of the working fluid inside VC-PCHS under different temperatures. A thicker copper shell can reinforce the structure allowing the VC-PCHS to withstand the high temperature inside the SiC module. So, a 1 mm shell on the evaporator side is chosen by considering the thermal performance, thermal stress and working temperature. The thickness of the copper shell at the condenser side $h_{\text{-shell(cond)}}$ is 0.8 mm. There are two reasons for a thinner copper shell at the condenser side. First, the condenser side of the VC-PCHS is soldered on the top of DBC substrate, so the overall structure is reinforced by the DBC attached to it and a thinner shell can satisfy the demand for structural strength. Second, the solder layer connecting the VC-PCHS and the DBC is relatively large. Reducing $h_{\text{-shell(cond)}}$ can reduce thermal stress and improve the overall reliability.

The layout of SiC MOSFETs on the VC-PCHS is also optimized based on the thermal performance. As is shown in Fig. 9, when the distance between the dies (ΔX) is larger than 10 mm. its effect on junction temperature becomes insignificant. When $\Delta X \geq 15$ mm, it has no effect on the junction temperature at all. The position of dies on the VC-PCHS (ΔY) only has little influence on $T_{\text{j-ave}}$ unless the chips are too close to the edge. The parameters of the designed SiC module integrated with VC-PCHS are given in Table II.

TABLE II
PARAMETERS OF SIC MODULE DIRECTLY INTEGRATED VC-PCHS IN THIS ARTICLE

Parameters	Values
VC-PCHS size (L)×(W) ×(H)	60 mm×40 mm ×5 mm
Whole module size (L)×(W) ×(H)	120 mm×80 mm ×40 mm
Total Weight of VC-PCHS	63.8 g
Thickness of shell $h_{\text{-shell(evap)}}$	1 mm
Thickness of shell $h_{\text{-shell(cond)}}$	0.8 mm
Thickness of wick $h_{\text{-wick}}$	0.5 mm
Hight of vapor channel $h_{\text{-channel}}$	2.2 mm
Type of wick structure	Sintered Copper Powder
Prosity of the wick	0.7
Working fluid and filling weight	Water 1.5 g
Vacuum Degree	9.31 Pa (9.19×10^{-5} atm)
Distance between dies (ΔX)	15mm
Distance to the edge of VC-PCHS (ΔY)	10mm

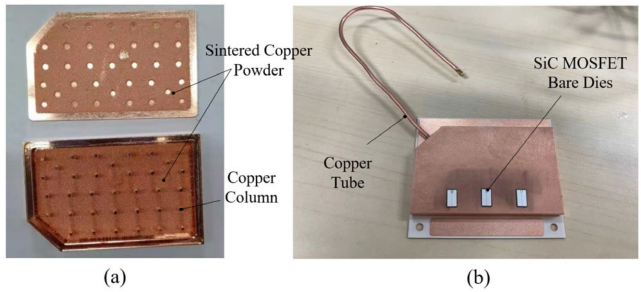

Fig. 10. (a) Interior structure of VC-PCHS. (b) SiC power module integrated with VC-PCHS before degassing and wire bonding.

C. Fabrication and Integration of VC-PCHS Into SiC Power Module

The fabrication and integration processes of VC-PCHS integrated SiC power module is shown in Fig. 11. First, the VC-PCHS is fabricated and vacuumed without injecting the working fluid. This is because a VC cannot withstand the high temperature inside the sintering furnace after it is filled with working fluid. Also, if the VC-PCHS is not vacuumed in the first place, the sintered copper powder will be oxidized by the remaining air inside the VC-PCHS during the soldering process, limiting its heat spreading performance. After the soldering process is finished, it is opened, injected with working fluid and vacuumed for the second time. This process is realized by a special copper filling tube welded at the corner of the VC-PCHS. As is shown in Fig. 10(b), this tube is longer than usual, allowing the second vacuuming and filling processes. It is removed when these processes are finished.

After all the integration process is finished, the size of the whole module including the baseplate and power terminals is 120 mm × 80 mm × 40 mm. Because the role that VC-PCHS plays in a power module is to spread the concentrated heat flux generated by the SiC dies to a larger area, the overall size of the

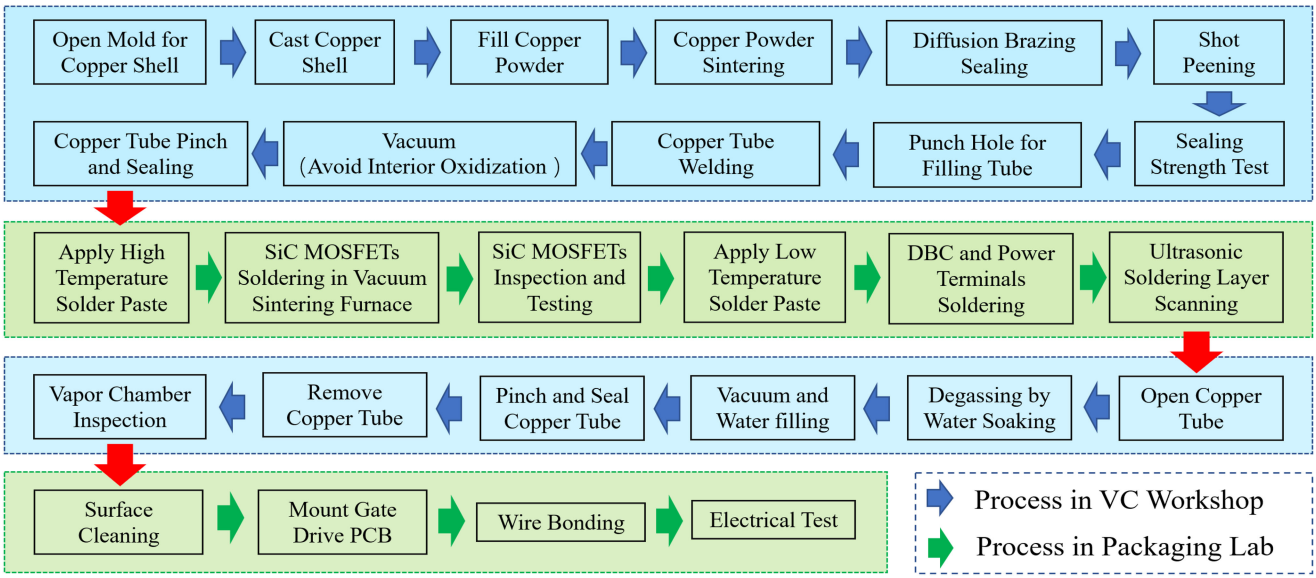

Fig. 11. Fabrication process flow of VC-PCHS and direct integration of SiC dies on VC-PCHS.

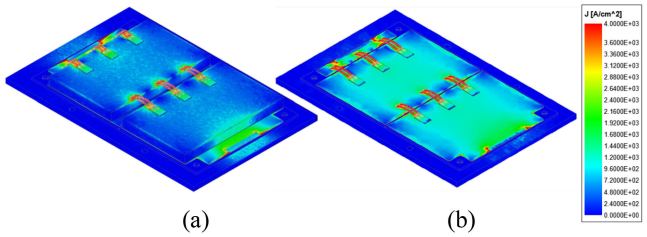

Fig. 12. Current distribution of (a)VC-PCHS integrated module and (b) conventional DBC module with the same layout considering skin and proximity effects at 100 kHz.

module including the VC-PCHS should be larger to achieve a better thermal performance. The power density of the VC-PCHS integrated module may be slightly smaller, but this module does not need complicated and power-consuming cooling systems to keep the junction temperature low. As a result, the overall power density, efficiency and reliability of the power converter are increased.

Calculations in Ansys Q3D show that the parasitic resistance and inductance inside the VC-PCHS integrated module are 0.59 mΩ and 26.5 nH, respectively. For the conventional module with the same layout, these numbers are 0.47 mΩ and 26.4 nH, respectively. Integrating VC-PCHS can increase the current-carrying ability of the module without introducing pathetic inductance. Fig. 12 illustrates the current density distribution at 200 A, 100 kHz (first harmonic current frequency through the module) considering skin and proximity effects. It can be found that the shell of VC-PCHS has a significantly smaller current density. Also, the current sharing among three paralleled dies is balanced and it is not affected due to the integration of VC-PCHS.

It is worth mentioning that this module in Fig. 5 is just a prototype, which is relatively easier to be fabricated and to demonstrate the thermal performance improvements. The electrical performance is not the focus of this article, and it can be

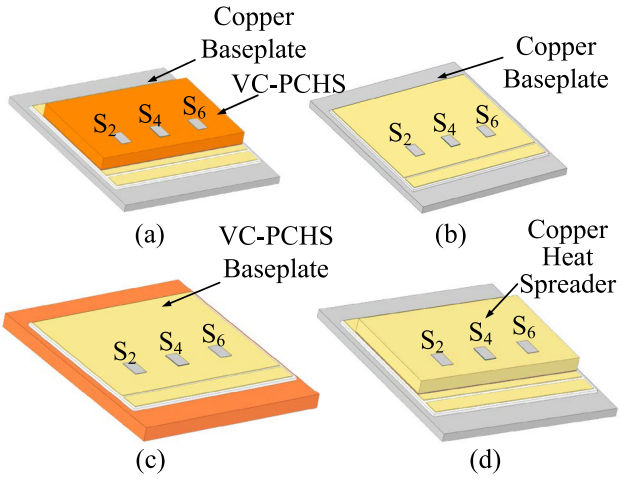

Fig. 13. Simulation models of (a) SiC module integrated with VC-PCHS. (b) SiC module using the conventional DBC substrate. (c) VC-PCHS baseplate module, and (d) SiC module using a copper plate as the heat spreader.

optimized by placing power terminals near each other on the VC-PCHS and by replacing bond wires with copper clips [39]. Also, because the VC-PCHS can be made into different shapes according to the need to optimize the layout of SiC chips, the parasitic resistance and inductance can be further reduced.

III. Simulation and Analysis

A. Simulation Model

Based on the working principles of VC-PCHS and the parameters of the designed VC-PCHS integrated SiC power module in previous sections, an FEA simulation model is built in Comsol Multiphysics software. The designed power module is symmetrical and preliminary simulations show that the temperature distribution of one side of the half-bridge only has a negligible

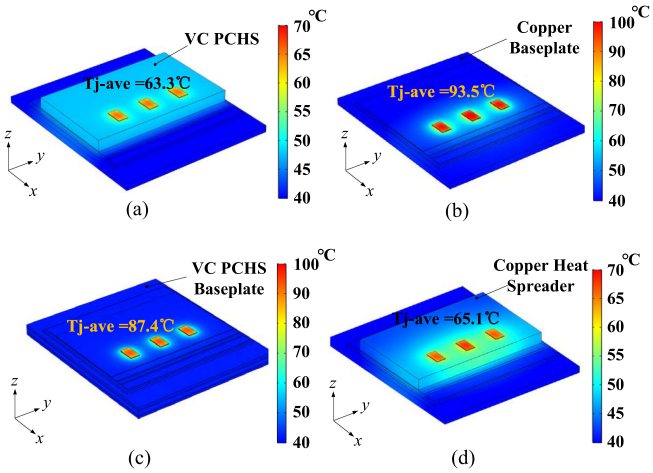

Fig. 14. Temperature distribution of different designs under 60 W power dissipation per die. (a) Power module directly integrated with VC-PCHS. (b) Conventional power module with copper baseplate. (c) Conventional module with VC-PCHS baseplate. (d) Module with a copper heat spreader.

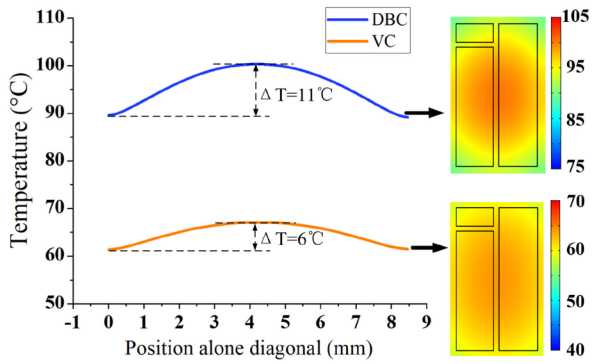

Fig. 15. Comparison of junction temperature distribution along the diagonal of a SiC MOSFET die under 60 W of power dissipation.

influence on the other side. As a result, only the lower side of the half-bridge is included in the simulation model, which can reduce the amount of FEM simulation by half. Bond wires and gate drive PCBs are removed to further simplify the calculation. When the number of elements exceeds 450 000, the temperature distribution remains almost unchanged. Finer mesh is adopted for thin structures such as dies, DBC, and wick inside VC-PCHS.

The simulation model is used to simulate the heat transfer and the solid mechanics of the power module. In order to calculate the distribution of thermal stress, the heat transfer problem is coupled with the solid mechanics problem under the Multiphysics interface in Comsol. To evaluate the thermal performance improvement of directly integrating VC-PCHSs into the SiC power module, three comparative designs are introduced. Design (b): conventional SiC power module with DBC substrate shown in Fig. 13(b). Design (c): SiC power module using VC-PCHS as baseplate shown in Fig. 13(c), which is similar to the structure proposed in [30]–[32]. Design (d): SiC power module using a layer of copper plate as the heat spreader shown in Fig. 13(d). For all the simulation models mentioned above, the bottom of the baseplate is assumed with

TABLE III
PARAMETERS OF THE SIMULATION MODELS

Parameters	Values
DBC Cu layer thickness	0.3 mm
DBC Al_2O_3 thickness	0.635 mm
Solder layer thickness	0.12mm
Half baseplate dimension	65 mm×80 mm ×3 mm
Power loss per die	60W
Thermal conductivity of wick	50 W/(m·K)
Thermal conductivity of solder	50 W/(m·K)
Thermal conductivity of vapor core	50 kW/(m·K)
Heat transfer coefficient of the bottom side	1500 W/(m^2·K)
Coolant temperature	20 °C

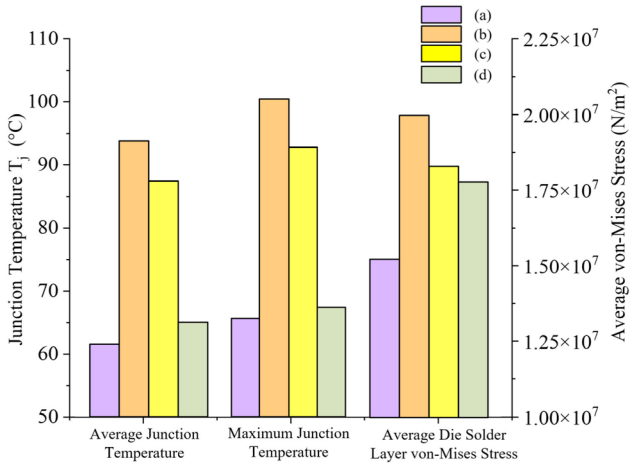

Fig. 16. Comparison of steady-state simulation results for four different designs.

a heat transfer coefficient of 1500 W/m^{2}K, representing the cooling performance provided by a liquid-cooled cold plate [22]. In real applications, the upper side of the DBC along with bond wires and power MOSFETs are encapsulated with silicone gel for electrical insulation. This encapsulation has poor thermal conductivity, so all other boundaries except for the baseplate are assumed adiabatic. Detailed parameters of the model are given in Table III.

1) Steady-State Simulation Result: The steady-state temperature distribution under the power loss of 60 W per die is shown in Fig. 14 and the results are summarized in Fig. 16. The average junction temperature is the volumetric average temperature value of three SiC MOSFETs. The average junction temperature of VC-PCHS integrated module (a) is 30.2 °C lower than the conventional module (b) and 24.1 °C lower than the VC-PCHS baseplate module (c). As is shown in Fig. 14(d), although a copper heat spreader can also provide a good heat spreading performance, the average thermal stress inside the solder is 18 MPa, which is 17% higher than that in VC-PCHS integrated module. The upper layer of the VC-PCHS is a copper shell of 1 mm thick. Although it is thicker than the top layer copper on DBC, the thermal stress is 30 % lower than the conventional module because of the lower junction temperature.

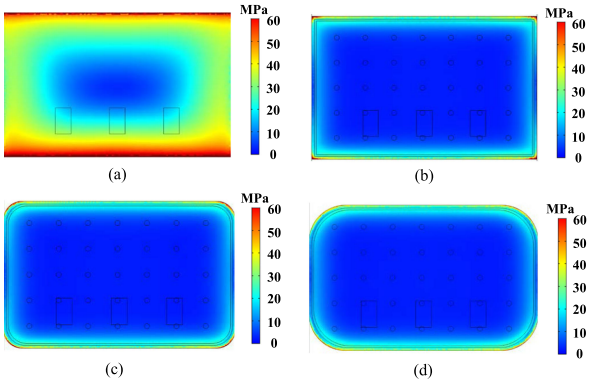

Fig. 17. Distribution of von Mises stress in the solder layer between the DBC and the heat spreader. (a) Copper heat spreader. (b) Vapor chamber phase-change heat spreader. (c) VC-PCHS with 5 mm rounded corners. (d) VC-PCHS with 10 mm rounded corners.

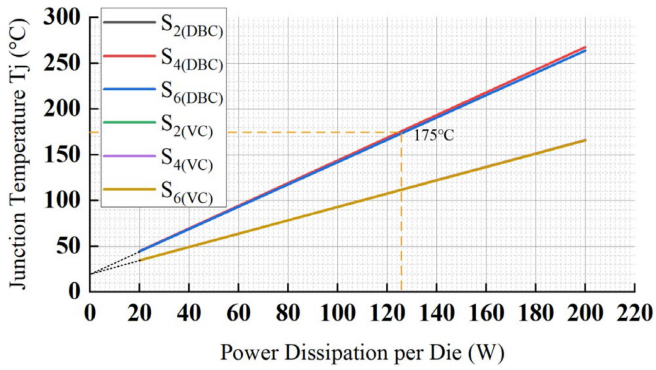

Fig. 18. Junction temperature of each SiC MOSFETs under different power dissipation under 20 °C coolant temperature.

The power devices inside the module are not isothermal and the center of the chip has a higher temperature than the edge. In real applications, keeping the maximum junction temperature low is more important. Comparing the maximum junction temperature, the advantage of the directly VC-PCHS integrated module becomes more obvious. It is reduced by 34.3 °C compared with the conventional module and 26.7 °C compared with the VC-PCHS baseplate module. This demonstrates that by directly integrating a VC-PCHS, the temperature distributes more evenly on SiC dies. As is proven in Fig. 15, because of the large equivalent thermal conductivity of the VC-PCHS, the SiC die has a much more uniform temperature distribution.

In order to integrate heat spreaders into power modules, one more solder layer jointing the heat spreader and the DBC is needed. So, the thermal stress in this layer needs to be studied to make sure that it will not become the bottleneck of the overall reliability of the power module. The distribution of von Mises stress is illustrated in Fig. 17. Adding a copper plate as the heat spreader will cause tremendous thermomechanical stress as shown in Fig. 17(a). The averaged volumetric von Mises stress is 28.6 MPa for copper heat spreader, which is 2.2 times as high as the VC-PCHS. Thanks to the thinner 0.8 mm copper shell at the condenser side of the VC-PCHS, the average von Mises stress is 12.8 MPa, which is even lower than that in the die solder layer of the SiC MOSFETs (15.1 MPa). This proves that integrating phase-change heat spreaders can significantly reduce the junction temperature but will not introduce excessive thermal stress. As is shown in Fig. 17(b), concentrated stress can be found at the corner of the solder layer. This problem can be alleviated by adopting rounded corners for the VC-PCHS as shown in Fig. 17(c) and (d), and by drilling stress relief holes around the edge of the DBC. To conclude, the hollow structure of the VC-PCHS acts as a buffer, relieving the thermal stress caused by the mismatch of CTE between materials while maintaining excellent heat-spreading performance owing to the phase change happening inside.

The junction temperatures under different power dissipations are evaluated for both the conventional module and VC-PCHS integrated module. The temperature curves in Fig. 18 overlap because of the uniformity in temperature. The advantage of VC-PCHS integrated module is more obvious as the heat flux increase. Even if under good cooling conditions, limited by the small die size of SiC chips, the conventional DBC module can only handle 126 W of power loss per die (398 W/cm^2) before the junction temperature exceeds the maximum rated temperature (175 °C). In contrast, under 200 W of power dissipation per die (632 W/cm^2), the junction temperature for the module with VC-PCHS is only 166 °C. Because the curves in Fig. 18 shows the linearity between the junction temperature and the power losses, the junction to ambient (coolant) $R_{\text{thj-a}}$ thermal resistance can be calculated as follows:

$$R_{thj-a} = \frac{T_{\text{jave}} - T_a}{P_{\text{loss}}} \tag{6}$$

where T_{jave} is the volumetric average temperature of the three paralleled dies and T_a is the coolant temperature which is 20 °C. The calculated $R_{\text{thj-a}}$ is 1.23 K/W for the DBC module and 0.72 K/W for the module with VC-PCHS, which is a 41% reduction.

B. Result Analysis

The reason why directly integrating a VC-PCHS can reduce the junction temperature is analyzed in this part.

According to Fourier's law, the heat flux vector can be expressed as

$$\overrightarrow{\phi_q} = -k\nabla T = -k \cdot \left(\frac{\partial T}{\partial x}, \frac{\partial T}{\partial y}, \frac{\partial T}{\partial z} \right) \tag{7}$$

where k is the thermal conductivity for homogeneous material. In this article, the heat flux generated by MOSFETs goes through different layers of the module and finally to the heat sink. So special attention is paid to the heat flux in the z-axis direction

$$\phi_{qz} = -k \cdot \left(\frac{\partial T}{\partial z} \right). \tag{8}$$

So, the temperature along the z-direction of a fixed point in the x–y plane $T(x_0,y_0,z)$ can be expressed as

$$T(x_0, y_0, z) = T(x_0, y_0, 0) + \int_0^z \frac{1}{k} \cdot \phi_{qz}(l) \cdot dl. \tag{9}$$

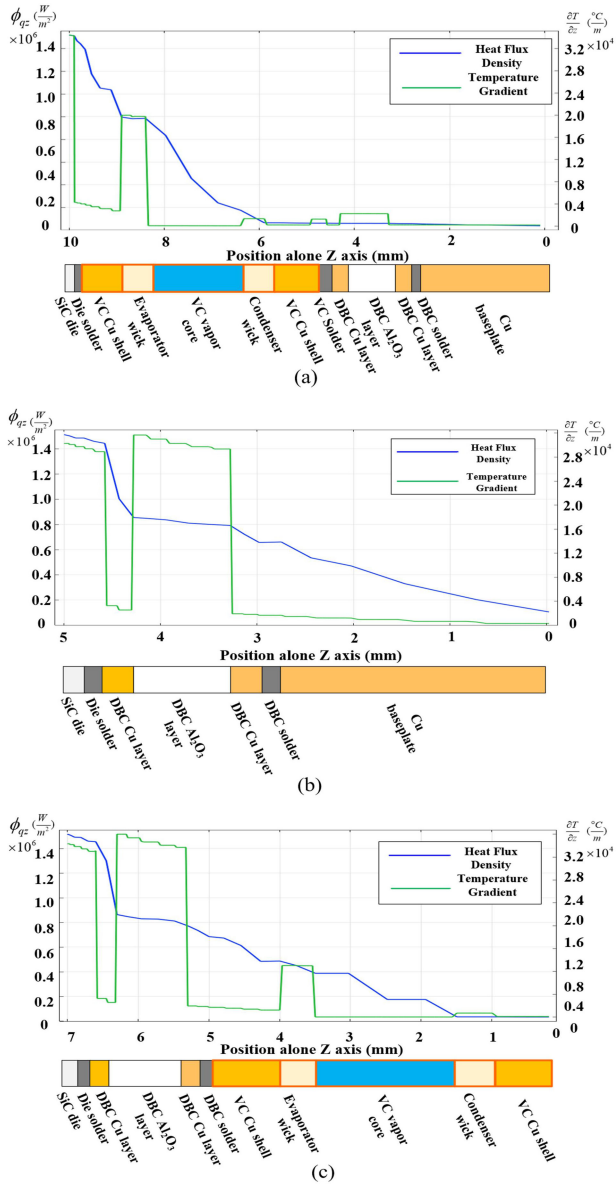

Fig. 19. Heat flux density and temperature gradient along the z-axis for (a) module directly integrated with VC-PCHS. (b) Conventional module, and (c) module integrated with VC-PCHS baseplate.

$T(x_0,y_0,0)$ is the temperature on the baseplate plane. Here, (x_0,y_0) is selected at the middle of the SiC chip. The temperature gradient and the heat flux along z-axis under the power dissipation of 60 W per die for the directly integrated VC-PCHS module, the conventional module and the VC-PCHS baseplate module are plotted in Fig. 19 (a), (b), and (c), respectively.

It can be seen that the heat flux density gradually decreases along the z-axis because of the heat spreading effect in x-y plane. As is shown in Fig. 19(a), in VC-PCHS integrated power module, the heat flux density along the z-axis drops much quicker than the conventional module and it is lower than 8 W/cm^2 after passing through the heat spreader. The Al_2O_3 ceramic in DBC has relatively poor thermal conductivity. For the conventional module, the heat flux that goes through the Al_2O_3 layer in DBC is around 85 W/cm^2, which is ten times higher than that of

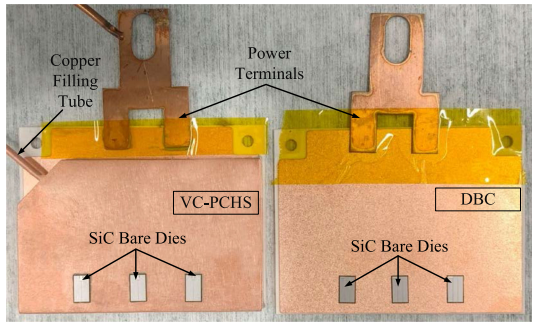

Fig. 20. Fabricated SiC module directly integrated with VC-PCHS (left) and the conventional DBC module (right).

VC-PCHS integrated module. As is demonstrated in (9), the high heat flux in materials with poor thermal conductivity will result in significant local temperature rise. This is also proven by Fig. 19(b), in which the temperature gradient in the Al_2O_3 layer is very high. In Fig. 19(a), for the module with VC-PCHS, the highest temperature gradient occurs in the capillary wick at the evaporator side inside the VC-PCHS. However, this layer is thin and will not result in considerable overall temperature rise. Meanwhile, the heat flux going through the Al_2O_3 layer is already small due to the heat spreading effect inside the vapor core. This also explains the reason why the junction temperature reduction of design (c) is not as obvious as design (a). As is shown in Fig. 19(c), although the VC-PCHS baseplate offers lower thermal resistance than the copper baseplate, the heat flux that goes through the Al_2O_3 layer in DBC is still quite high, resulting in the overall temperature rise.

To conclude, for thermal management in power modules, it is more efficient to evacuate the high heat flux near the junctions to avoid it goes through the insulation layer where the thermal conductivity is relatively low.

IV. Experiment and Analysis

A. Preparation and Experimental Setup

Several designed SiC power modules integrated with VC-PCHSs are fabricated using the process mentioned in Section II. The parameters of VC-PCHSs are given in Table II, which is consistent with the simulation model. In order to validate the thermal performance improvement by directly integrating VC-PCHSs, the conventional modules with exactly the same SiC MOSFET and layout are made. The fabricated SiC module directly integrated with VC-PCHS and conventional DBC as the baseline is shown in Fig. 20.

The experimental setup is shown in Fig. 21. A dc power supply is connected to the ac and dc-terminal on the substrate. The device under test (DUT) is cooled by a customized cold plate. A water chiller and heater with a pump is connected to the cold plate, providing circulating water at the flow rate of 12 L/min. An extremely thin thermal couple is placed at the bottom of the substrate to measure the case temperature. A fiber optic temperature sensor is used to measure the junction temperature. Because of the uneven distribution of temperature across the SiC

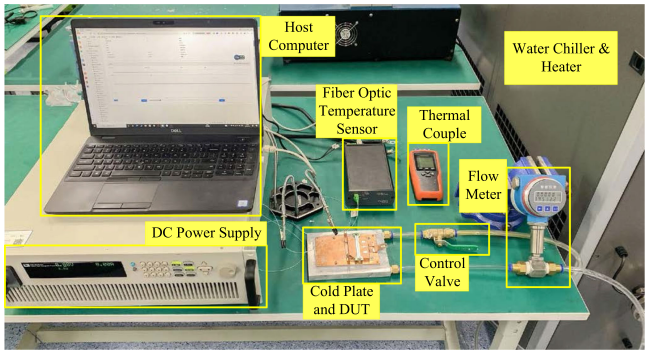

Fig. 21. Experimental setup in this article.

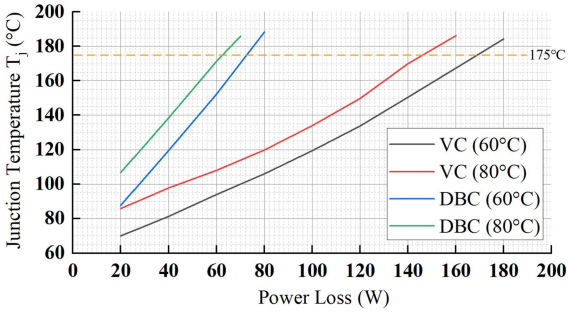

Fig. 23. Comparison of junction temperature for VC-PCHS module and conventional DBC module using 60 and 80 °C coolants.

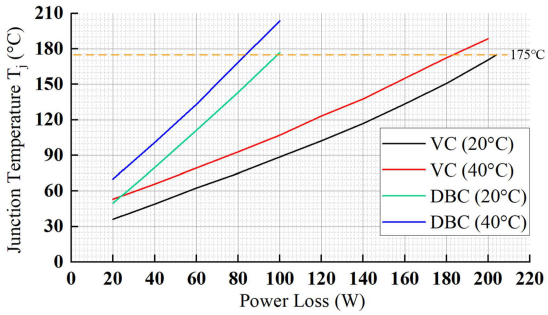

Fig. 22. Comparison of junction temperature for VC-PCHS module and conventional DBC module using 20 and 40 °C coolants.

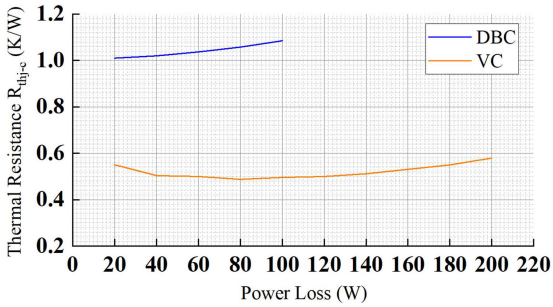

Fig. 24. Comparison of the junction to case thermal resistance $R_{\mathrm{thj\text{-}c}}$.

MOSFET bare dies, the head of the optics fiber is placed at the center of the die to make sure the maximum junction temperature T_j is measured. The host computer collects the data from the fiber optics sensor.

Because the body diode of the SiC MOSFET has a relatively large ON-resistance, it can be used to heat up the device with a reduced current value. According to the datasheet provided by CREE Wolfspeed [40], the body diode of the SiC MOSFET used in this article has a negative temperature coefficient, which will result in unbalanced current sharing. For the accuracy of the thermal characterization, only one SiC die is wire bonded in the experiment with the purpose of better control and measure the power loss on the MOSFET.

B. Experimental Results

The steady-state junction temperatures are measured under different power losses and coolant temperatures. As is illustrated in Fig. 22, the overall tendency and values of the measured temperature curve match with the simulations. The SiC die in VC-PCHS integrated module has a much lower junction temperature overall power dissipations and coolant temperatures. Especially under a high heat flux of 316 W/cm^2 (100 W per die) and 20 °C coolant temperature, the junction temperatures for the conventional module and the module with VC-PCHS are 176.8 °C and 88.7 °C, respectively, which is a 50% reduction. Under such cooling condition, the module with VC-PCHS can handle the extreme heat flux of 644 W/cm^2 (204 W per die) without exceeding the rated maximum junction temperature of 175 °C. The thermal performance of both the module with VC-PCHS and the conventional module is also tested under relatively poorer cooling conditions. As the typical coolant temperature circulating in electric vehicles is 65 °C [41], the experiment also includes 60 and 80 °C coolant temperatures. As illustrated in Fig. 23, the VC-PCHS can still handle 169 W (534 W/cm^2) of power dissipation under 60 °C coolant temperature and 146 W of power dissipation under 80 °C (461 W/cm^2) coolant temperature without passing 175 °C rated maximum temperature of SiC chips. In contrast, these values for the conventional DBC module are 72.5 W (229 W/cm^2) under 60 °C coolant temperature and 62.5 W (197 W/cm^2) under 80 °C coolant temperature. The module with VC-PCHS can handle more than 2.3 times higher power losses than the conventional module. Even if under such poor cooling conditions, there are no signs of degradation in the thermal performance for the PCHS. In the experiment, the stable operation of the VC-PCHS module in high temperature is confirmed under the power loss of 160 W and 80 °C coolant temperature. The minimum temperature of the whole VC-PCHS exceeds 130 °C without any deformation caused by the inner and outer pressure difference.

The case temperature T_c is measured by the thin thermal couple placed between the baseplate and the cold plate. The junction to case thermal resistance $R_{\mathrm{thj\text{-}c}}$ can be calculated using (6).

The steady-state thermal resistance of two modules under different power losses is demonstrated in Fig. 24. The conventional module is tested to 100 W due to the temperature limit of chips.

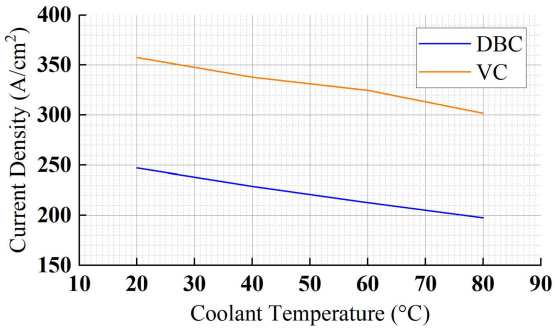

Fig. 25. Maximum continuous current density for the conventional DBC module and module integrated with VC-PCHS.

$R_{\text{thj-c}}$ of the VC-PCHS integrated module gradually decreases as the power losses increase from 20 to 80 W. This is because at low heat load, the water film in the wick structure inside the VC-PCHS is thick and the phase-change process in both the evaporator side and condenser side is at a low level [42]. As a result, the thermal resistance of R_{th3} and R_{th5} are relatively high. As the heat flux increases, the evaporation process is enhanced and the water film becomes thinner. Both R_{th3} and R_{th5} decrease. The VC-PCHS reaches its optimal working status under 80–120 W of heat load. The $R_{\text{thj-c}}$ is lower than 0.5 K/W in this range. As the heat flux continues to increase, there is a slight increase in the thermal resistance. There is no sharp rise in $R_{\text{thj-c}}$ even under 200 W (632 W/cm^2) of power dissipation, representing no total dry out happens inside the wick. On average, $R_{\text{thj-c}}$ for the module with VC-PCHS is 0.52 K/W, compared with 1.04 K/W for the conventional module, which is a 50% reduction.

The improvements in thermal performance for power modules can be transformed into higher current carrying capability in real applications. The continuous current capability is studied to quantify the impact of thermal performance improvements brought by VC-PCHS. The maximum continuous current density $J_{\max}$ can be calculated as

$$J = \frac{1}{A_{\text{die}}}\sqrt{\frac{P_{\max}}{R_{\text{DS-on}}}} \tag{10}$$

where A_{die} is the die surface area of CPM3-0900-0010A (7.26 × 4.36 mm^2), $P_{\max}$ is the maximum power dissipation at which the junction temperature reaches the rated maximum value of 175 °C, and $R_{\text{DS-on}}$ is the ON-resistance at the junction of 175 °C which is 16 mΩ according to the datasheet. The maximum continuous current densities with respect to coolant temperatures are shown in Fig. 25. It can be seen that regardless of the cooling conditions provided, the module with VC-PCHS can provide around 110 A/cm^2 (34.8 A per die) more continuous current carrying capability.

V. Conclusion

This article presents the direct integration of VC phase-change heat spreaders into SiC power modules to improve their thermal performance under high flux. Different from prior works, in this article, the VC-PCHSs are not only heat spreaders, but also conduct the drain current of SiC MOSFETs. The interior structures of VC-PCHSs are optimized considering the thermal performance, thermal stress, and mechanical strength. A new integration process of VC-PCHS with SiC power module is proposed and adopted. The steady-state thermal and mechanical simulations show that the module integrated with VC-PCHS can reduce the junction to coolant thermal resistance $R_{\text{thj-a}}$ by 41% and the von Mises stress in the die solder layer by 30%. Such thermal performance improvement can be attributed to VC-PCHS's high thermal conductivity. The z-direction heat flux from the SiC die is greatly reduced before it goes through the dielectric layer in DBC. Owing to the hollow structure and the phase-change loop inside the VC-PCHS, good thermal and thermomechanical performance can be achieved at the same time. The experiments validate the effectiveness of directly integrating the VC-PCHS into SiC modules, confirming a 50% reduction in junction to case thermal resistance $R_{\text{thj-c}}$ and a 110 A/cm^2 increase in continuous maximum current density. The safe operation of the module with VC-PCHSs is validated under an extremely high heat flux of 644 W/cm^2 and poor cooling conditions using 80 °C coolant temperature. Integrating VC-PCHSs not only solves the high heat flux generated by the smaller die size of SiC devices but also will not add any complexity and energy consumptions to the external cooling systems, which makes the VC-PCHS a practical choice in the packaging of SiC power modules. Moreover, the VC-PCHS's high flexibility in shape allows further optimizations of layout based on thermal and electrical performance.

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