Letters

Capacitive Couple-Based Transient Current Commutation in Solid-State Circuit Breakers

Reza Kheirollahi, *Student Member, IEEE*, Xin Zan, *Student Member, IEEE*, Shuyan Zhao, *Student Member, IEEE*, Hua Zhang, *Member, IEEE*, Sheng Zheng, *Senior Member, IEEE*, Xiaonan Lu, *Member, IEEE*, Al-Thaddeus Avestruz, *Member, IEEE*, and Fei Lu, *Member, IEEE*

***Abstract*—This letter presents a new auxiliary circuit to achieve transient current commutation (TCC) in dc solid-state circuit breakers (SSCBs). The auxiliary circuit consists of two parts: active injection circuits (AIC) and capacitive couplers. There are two contributions. First, coupling capacitors between AIC and the main branch are introduced to prevent short circuit failures in the auxiliary branch. Second, a boost converter-based resonant circuit is presented for AIC to achieve TCC in the main branch through couplers. The presented AIC tunes the duration time and amplitude of injected countercurrent pulses during dc current interruption. The working principle and design procedure of the auxiliary circuit are presented. The proposed topology is verified by experiments of a 2 kV/100 A dc SSCB prototype under load current interruption. The experimental results show that the injected pulse current through couplers reaches 110 A, and it decays to zero within 12.5 μs. The total reaction time interval including the communication delay and the AIC current rising delay is 108 μs. Meanwhile, the peak voltages across the main branch and the coupler reach 2099 V and 2193 V, respectively.**

***Index Terms*—Active injection circuits, capacitive couple-based transient current commutation, dc circuit breakers.**

I. Introduction

TO DEAL with the low inertia of dc systems, solid-state circuit breakers (SSCBs) present fast speeds within microseconds [1], [2]. Silicon-controlled rectifiers need transient current commutation (TCC) to cut dc currents OFF [3], [4]. TCC is also used in silicon carbide (SiC) MOSFET-based SSCBs to achieve a soft turn-OFF, which eliminates gate oscillations and power shock on the main switch during dc current interruption [5], [6]. The former enhances the reliability by preventing false turn-ON; whereas, the latter increases lifetime.

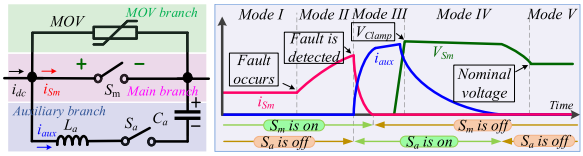

Fig. 1. DC circuit breaker with AIC [7]–[9]: circuit topology (left side) and conceptual waveforms during dc current interruption (right side).

Active injection circuits (AIC) are used to obtain TCC in SSCBs [4], [7], [8]. Fig. 1 indicates an SSCB with AIC during dc current interruption [7]–[9]. The main switch S_m conducts currents in a normal operating mode. The auxiliary branch involves a precharge capacitor and an inductor to generate countercurrent pulses, controlled by an injection switch S_a. Also, metal-oxide varistors (MOVs) clamp the voltage overshoots across S_m [10].

The operation of SSCB with AIC is shown in Fig. 1 under five modes in clearing a fault. As indicated in Fig. 1, AIC obtains TCC in the main switch during dc current breaking using a precharge capacitor C_a and an injection inductor L_a [7]–[9]. There are two strategies in charging C_a. The self-charging method [4], [8] presents simple operation but no flexibility on the initial voltage. External charging [5], [6], [11] requires an external dc source which is more challenging, but it benefits from higher flexibility in determining the amplitude and duration time of the injected pulse currents.

Although AIC obtains the possibility of utilizing high-power rating and fast solid-state switches, it puts reliability at risk. Fig. 2 shows possible failures in AIC circuits in self-charging [4], [8] and external charging topologies [5], [6], [11]. In Fig. 2(a), failure in AIC leads to a source-side short circuit; while, the failure in external charging of Fig. 2(b) bypasses the circuit breaker, leaving the dc system without any protection. As illustrated in Fig. 2, reliability issue in AIC arises due to failures in solid-state switches during operation. While the risk of these failures is relatively low, the consequences cause serious damages in dc systems.

Manuscript received September 29, 2021; revised November 6, 2021 and November 27, 2021; accepted December 7, 2021. Date of publication December 13, 2021; date of current version January 19, 2022. This work was supported by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award DE-AR0001114 in the BREAKERS program monitored by Dr. Isik Kizilyalli. *(Corresponding author: Fei Lu.)*

Reza Kheirollahi, Shuyan Zhao, Hua Zhang, and Fei Lu are with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA 19104 USA (e-mail: rk887@drexel.edu; sz568@drexel.edu; hua.zhang@drexel.edu; fei.lu@drexel.edu).

Xin Zan and Al-Thaddeus Avestruz are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: xinzan@umich.edu; avestruz@umich.edu).

Sheng Zheng is with Oak Ridge National Laboratory, Oak Ridge, TN 37830 USA (e-mail: zhengowen@ieee.org).

Xiaonan Lu is with the College of Engineering, Temple University, Philadelphia, PA 19122 USA (e-mail: xiaonan.lu@ieee.org).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3134461.

Digital Object Identifier 10.1109/TPEL.2021.3134461

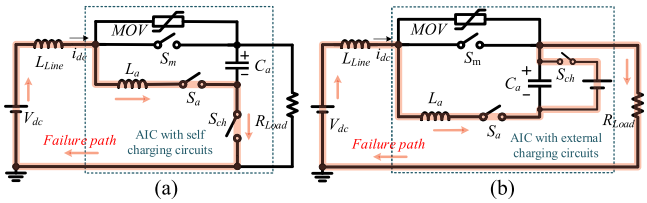

Fig. 2. Failure in AIC-based circuit breakers. (a) Self-charging topology [4], [8]. (b) External charging topology [5], [6], [11].

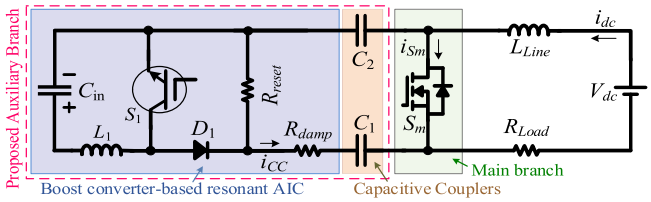

Fig. 3. Proposed capacitive couple-based auxiliary circuit in a dc system.

To solve the mentioned reliability issue at its root, a new auxiliary circuit is proposed for dc circuit breakers. The topology is shown in Fig. 3 where capacitive couplers (C_1 and C_2) are presented as a coupling interface between the AIC and the power line. Couplers protect SSCB from short circuit faults in the auxiliary branch, which enhances reliability. In addition, to achieve TCC in the main switch S_m, a boost converter-based resonant AIC is presented. The proposed AIC optimizes the coupler voltage, and it adjusts the countercurrent pulse in terms of amplitude and duration time.

II. Proposed Topology

Fig. 3 indicates the proposed AIC connected in parallel to main switch S_m. AIC circuit is a boost converter-based resonant circuit. S_1 is an IGBT switch, $R_{\rm reset}$ and $R_{\rm damp}$ are the couplers reset and damping resistors, illustrated in the next sections.

A. Working Principle

Fig. 4 shows the operating modes of the proposed SSCB, where S_m is an SiC MOSFET. Critical waveforms are also described in Fig. 5. Detailed information is as follows.

Mode I (*before* t_0): SSCB is OFF, meaning $i_{\rm dc} = i_{Sm} = 0$; S_m holds $V_{\rm dc}$; C_{in} charges to $V_{\rm aux}$, where $v_{S1} = V_{\rm aux}$. Each coupler ($C_1 = C_2$) holds ($V_{\rm aux}$+$V_{\rm dc}$)/2. There is a leakage current on $R_{\rm reset}$, but its value is negligible since $R_{\rm reset}$ is large.

Mode II ($t_0 \le t < t_1$): S_m turns ON, and dc current begins to increase in the system, finally reaching $i_{\rm Load} \approx V_{\rm dc}/R_{\rm Load}$. The voltage on couplers discharges through $R_{\rm reset}$, getting $V_{\rm aux}/2$ in a steady state.

Mode III ($t_0 < t < t_1$): SSCB continues in normal operation.

Mode IV ($t_1 \le t < t_2$): Short circuit fault occurs at the load side.

Mode V ($t_2 \le t < t_3$): SSCB detects the fault at $t = t_2$ and begins the interruption process by turning S_1 ON. i_{L1} starts to increase, and couplers further discharge on $R_{\rm reset}$. $t_{\rm rising} = t_3 - t_2$ is determined by $i_{\rm dc,max}$ aimed to be interrupted in the dc system under study.

Mode VI ($t_3 \le t < t_4$): S_1 turns OFF, meaning $i_{S1} = 0$ and $i_{L1} = i_{CC}$. The countercurrent pulse i_{CC} opposes i_{Sm}, meaning i_{Sm}-$i_{CC} \le 0$. The voltage on couplers begins to increase. i_{CC} ($= i_{L1}$) starts to decrease when v_{C1}+v_{C2}+$R_{\rm damp} \times i_{CC}$ is large than $V_{\rm aux}$.

Mode VII ($t = t_4$): S_m turns OFF at $t = t_4$ when i_{Sm} closes to zero, i_{CC} continues to flow through the body diode of S_m.

Mode VIII ($t_4 < t < t_5$): i_{Sm} reduces to zero. Fault current $i_{\rm dc}$ commutates to couplers ($i_{\rm dc} = i_{CC}$) and begins to decrease.

Mode IX ($t_5 \le t \le t_6$): Current in auxiliary branch i_{CC} and dc system $i_{\rm dc}$ reduce to zero, meaning $i_{dc} = i_{CC} = i_{L1} = 0$. S_m holds $V_{\rm dc}$, and voltage on each coupler is decreasing; finally returning to ($V_{\rm aux}$+$V_{\rm dc}$)/2 at $t = t_6$, and interruption completes.

B. Design Procedure

1) L_1, C_{in}, C_1, and C_2 Selection: Optimized L_1, $C_{\rm in}$, and capacitive couplers are formulated, and v_{C1} and v_{C2} are analyzed during dc current interruption. To simplify the design, it is assumed that $C_1 = C_2 = C$.

SSCB is designed to cut off $i_{\rm dc,max}$. To achieve TCC in S_m during *Mode VI*, peak current in L_1 ($i_{L1,\rm max}$) must be higher than $i_{\rm dc,max}$. Regarding a constant coefficient $\rho > 1$ and desired values of $t_{\rm rising} = t_3$-t_2 and $V_{\rm aux}$, L_1 is selected using

$$L_1 = (V_{\rm aux} \cdot t_{\rm rising}/\rho \cdot i_{\rm dc,max}) \tag{1}$$

To obtain a fast response speed in the proposed SSCB and reduce the current burden on solid-state switches S_m and S_1, $t_{\rm rising}$ should be minimized. To achieve this, L_1 should be reduced, and $V_{\rm aux}$ needs to be increased. In this case, Fig. 6 indicates $t_{\rm rising}$ for different L_1 and $V_{\rm aux}$ when $\rho = 1.1$ and $i_{\rm dc,max} = 100$ A. Given $V_{\rm aux}$, $t_{\rm rising}$, and L_1, $C_{\rm in}$ is chosen using

$$C_{\rm in} = \rho \cdot i_{\rm dc,max} \cdot t_{\rm rising}/\alpha \cdot V_{\rm aux} \tag{2}$$

where α is an acceptable discharge percentage in $C_{\rm in}$ during dc current interruption; α is considered as 20% in this letter.

During *Mode VI and VII* ($t_3 \le t \le t_4$), the current in the coupling capacitors is assumed constant. Considering $v_C(t = t_3) = V_{\rm aux}/2$, (3) is given as follows:

$$v_C(t_4) = V_0 \approx (V_{\rm aux}/2) + ((\rho \cdot i_{\rm dc,max}/C) \cdot T_c) \tag{3}$$

where $T_c = t_4 - t_3$. During *Mode VIII* ($t_4 < t < t_5$), (4) is derived regarding the KVL in the loop of $C_{\rm in}$-L_1-$R_{\rm damp}$-C_1-R_f -$V_{\rm dc}$-$L_{\rm Line}$-C_2 as follows:

$$\begin{cases} v_C(t) = B + e^{-\alpha_2 t}. \\ (D \cdot \sin(\omega_{d2} t) + A \cdot \cos(\omega_{d2} t)) for t_4 < t < t_5 \\ A = -\frac{V_{\rm aux}+V_{\rm dc}}{2}, B = V_0 - A, D = \frac{\rho \cdot i_{\rm dc,max}}{\omega_{d2} C} - \frac{\alpha_2 \cdot A}{\omega_{d2}} \\ \alpha_2 = R_e/2 \cdot L_e, \omega_{n2} = 1/\sqrt{L_e C}, \omega_{d2} = \sqrt{|{\alpha_2}^2 - {\omega_{n2}}^2|} \end{cases} \tag{4}$$

where $R_e = R_{\rm damp}$+R_f and $L_e = L_1$+$L_{\rm Line}$. Using (4), line current $i_{\rm dc}$ ($= i_{\rm fault} = i_{CC} = i_{C1} = i_{C2}$) are calculated during *Mode VIII* ($t_4 < t < t_5$) as illustrated in the following:

$$\begin{cases} i_{\rm dc}(t) = C \cdot e^{-\alpha_2 t} \cdot (E \cdot \cos(\omega_{d2} t) - F \cdot \sin(\omega_{d2} t)) \\ E = D \cdot \omega_{d2} - A \cdot \alpha_2 \text{and} F = D \cdot \alpha_2 + A \cdot \omega_{d2}. \end{cases} \tag{5}$$

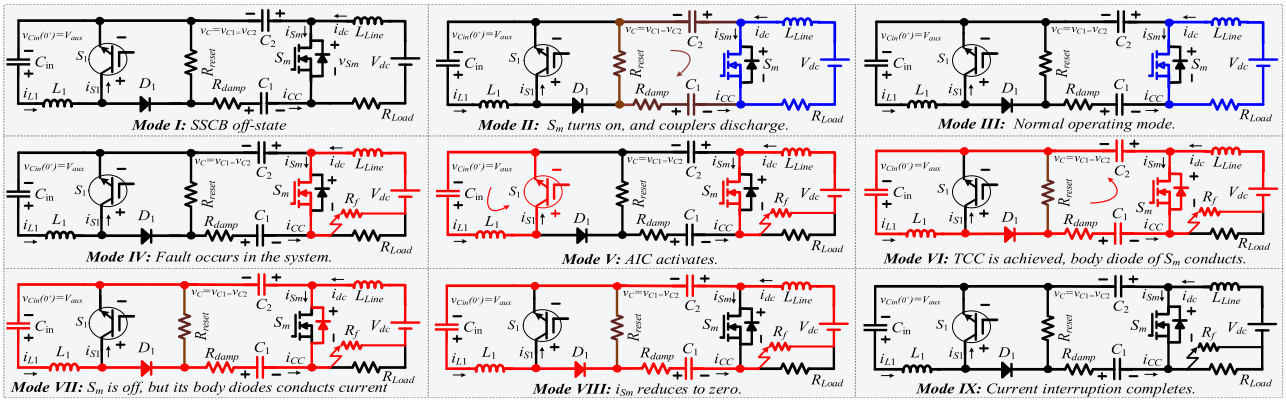

Fig. 4. Working principle of the proposed capacitive couple-based AIC.

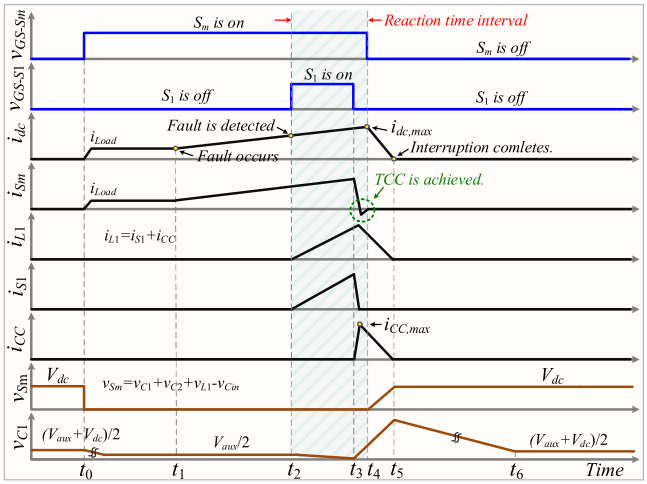

Fig. 5. Critical electrical waveforms during dc current interruption (V_{C1}=V_{C2}).

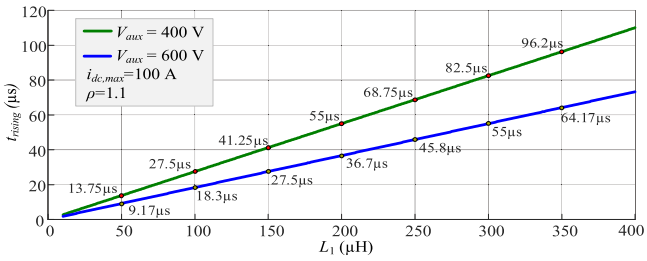

Fig. 6. $t_{\rm rising}$ for different values of L_1 and $V_{\rm aux}$.

Regarding (5), fault current reduces to zero within T_d

$$T_d = \pi \cdot \sqrt{L_e \cdot C}/2 \tag{6}$$

where $T_d = t_5 - t_4$ in Fig. 5. Given L_1 current in (5), v_{S1} is found as follows

$$v_{S1}(t) = V_{\rm aux} - L_1 \cdot (di_{\rm dc}(t)/dt). \tag{7}$$

v_{Sm} is calculated during *Mode VIII* as given in the following

$$v_{Sm}(t) = V_{\rm dc} - L_{\rm Line} \cdot (di_{\rm dc}(t)/dt) - R_f \cdot i_{\rm dc}(t). \tag{8}$$

Fig. 7. Simulated circuit in LTspice to emulate a short circuit interruption.

TABLE I
PROPOSED SSCB PROTOTYPE PARAMETERS

C_{in}	200 µF	V_{aux}	400 V	L_1	314 µH
R_{reset} (R_{damp})	3 kΩ (15 Ω)	C_s	200 nF	C_1 (C_2)	280 nF

Peak values of v_C ($= v_{C1} = v_{C2}$) is found by substituting $t = T_d$ in (4). Therefore, $C_1 = C_2$ are optimized to satisfy $v_C(T_d) < V_{C,\max}$, where $V_{C,\max}$ is the maximum allowable voltage on the couplers. If a snubber capacitor C_s is connected in parallel to S_m to slow down dv/dt, i_{CC} is updated as i'_{CC} below

$$i'_{CC}(t) = i_{dc} - C_s \cdot (dv_{Sm}/dt). \tag{9}$$

In dc systems, line inductor $L_{\rm Line}$ is added to increase the inertia. In this case, an MOV is paralleled to S_m as overvoltage protection. Hence, v_{Sm} is clamped to maximum clamping voltage of MOV $V_{\rm Clamp}$, and v_C is clamped to $(V_{\rm Clamp}+V_{\rm aux})/2$.

2) R_{reset} Selection: There are three criteria for $R_{\rm reset}$ selection:

a) leakage current should be minimized during the OFF-state (*Mode I*);

b) couplers' discharge current on S_m should be limited (*Mode II*); and

c) couplers should be reset quickly (*Mode II*). Considering $C_1 = C_2 = C$ and reset time interval as $t_{\rm reset}$, $R_{\rm reset}$ is found by

$$(V_{\rm dc} + V_{\rm aux})/(2 \cdot i_{\rm dc,max}) < R_{\rm reset} < (2 \cdot t_{\rm reset})/(5 \cdot C). \tag{10}$$

III. SIMULATION RESULTS

Simulations are conducted in LTspice. The circuit is shown in Fig. 7, and the parameters are listed in Table I. Fault switch S_f and the fault resistor R_f emulate a short circuit fault. Regarding the

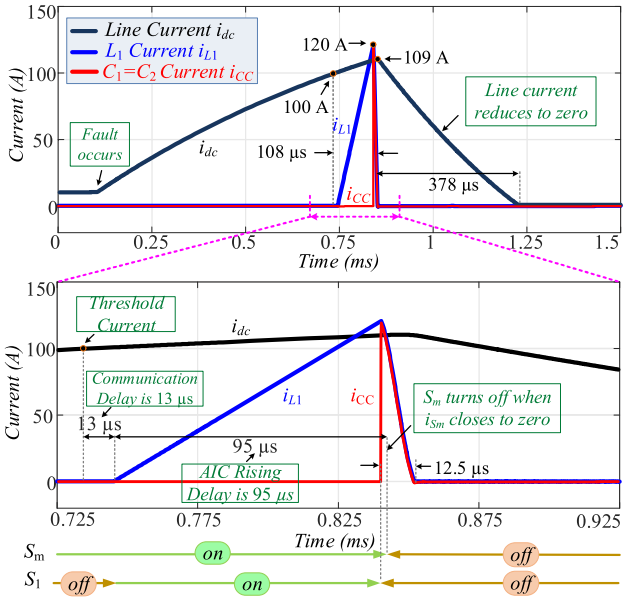

Fig. 8. Simulation results: current waveforms during fault interruption.

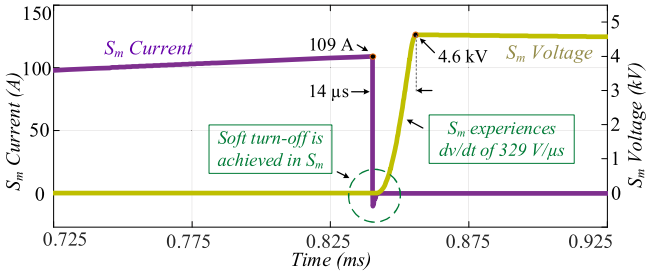

Fig. 9. Simulation results: S_m's voltage and current waveforms during fault interruption.

inserted 10 mH line inductor [12]–[13], three series-connected V661HA40 MOVs are used to protect S_m.

Fig. 8 shows the line current i_{Line}, auxiliary inductor current i_{L1}, and couplers current i_{CC} during dc current interruption. The fault occurs at $t = 100$ μs, and it reaches the threshold value of 100 A at $t = 732$ μs; then, SSCB begins to interrupt the fault current. The reaction time interval is 108 μs, and S_m turns OFF reliably at $t = 840$ μs, where the peak of i_{Line} and i_{CC} get 109 A and 120 A, respectively. The reaction interval includes 13 μs as communication delay between main and auxiliary branches and 95 μs as AIC current rising delay.

Fig. 9 indicates S_m's voltage and current during dc current breaking. S_m experiences a voltage rising rate of 329 V/μs and a peak voltage of 4.6 kV. Also, a complete soft turn-OFF is obtained for S_m. Besides, Fig. 10 shows voltage and current waveforms in each coupler, where the injected pulse width lasts for 12.5 μs, and the peak voltage reaches 2.58 kV.

IV. Experimental Validation

A. Hardware Description

Fig. 11 shows implemented main and auxiliary branches, and the parameters are the same as Table I. A 750 μF dc-link

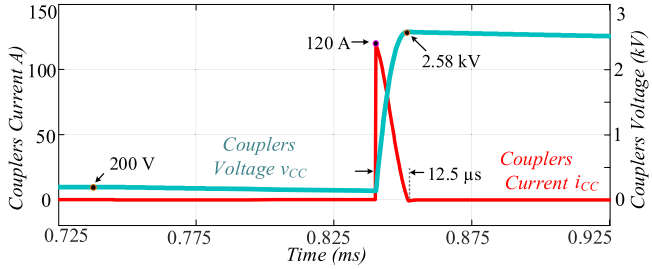

Fig. 10. Simulation results: C_1 and C_2 voltage and current waveforms during fault interruption.

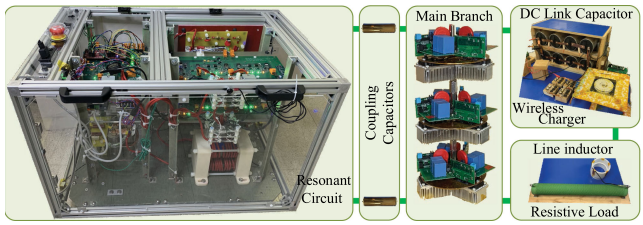

Fig. 11. Implemented prototype. DC link capacitor and its wireless charger, line inductor, resistive load, main branch, and boost-converter-based resonant circuit are shown. The structure is consistent with Fig. 3.

capacitor is used to generate the pulse current during the test. Also, as the load current interruption test is used to validate the proposed SSCB, the line inductor is reduced to 36.8 μH. For S_m, 9 CAB-450M12XM3 SiC MOSFET modules are connected in series and parallel in a 3×3 structure. For S_1, two 5SNG-0300Q170300 IGBT modules are connected in series which can stand a peak voltage up to 5 kV during transient; SiC C4D20120 diode is used for D_1. C_{in} is charged by a wireless inductive charger from a low voltage dc source [14], and its voltage (V_{aux}) is kept constant. It brings three advantages.

1) It obtains high voltage isolation.
2) It presents a high input-to-output voltage ratio.
3) Soft-switching and burst-switching mode are implemented to minimize the transient and steady-state power losses. Besides, to decelerate C_{in} discharge rate during SSCB ON-state, R_{reset} should be optimized using (10).

Fig. 12 indicates the control algorithms employed in the main and auxiliary branches, where optical-fiber cables are used to realize synchronization during dc current interruption process. Gate signals and optical-fiber transmitter lines (*Tx*) of the main and auxiliary branches are also indicated in Fig. 12. By turning S_m ON, load current flows through the system. Current interruption begins when the main branch sets the transmitter line (*Main_Tx*) at a high state for 13 μs, regarded as the communication delay. Next, the auxiliary branch acknowledges by setting the transmitter line (*Auxiliary_Tx*) at high state and turns S_1 ON for 95 μs, where L_1 current begins to increase. Then, S_1 turns OFF, and current commutation is achieved in S_m regarding Fig. 5. Finally, S_{m} turns OFF reliably under a zero power shock.

B. Interrupting DC Current

Fig. 13 shows the line current (i_{dc}) and S_m voltage (v_{Sm}) during dc current interruption. C_s snubber is connected across

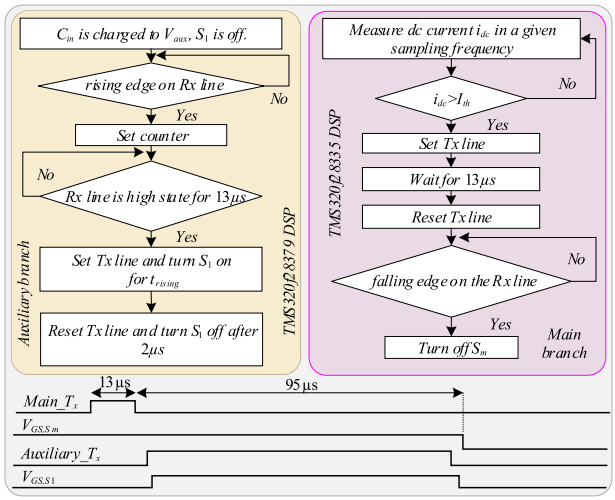

Fig. 12. Control algorithms and implemented synchronization.

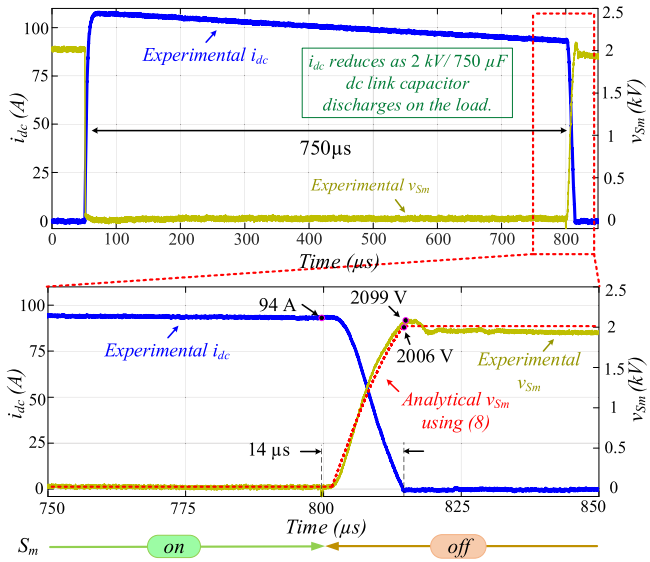

Fig. 13. Experimental and analytical results: line current ($i_{\rm dc}$) and S_m voltage (v_{Sm}).

S_m and $i_{\rm dc} = i_{CC}+i_{Sm}$. As indicated in this figure, $i_{\rm dc}$ reduces from 94 A to zero in 14 μs, which is close to the estimated value of 16 μs by (6). v_{Sm} begins to increase, and it reaches 2099 V in the same period. Compared with simulation results, v_{Sm} gets a lower peak voltage as the line inductor in experiments is much lower than its value in the simulations. Also, v_{Sm} experiences a reliable dv/dt of 150 V/μs, which helps to prevent false turn-ON in S_m. To verify the mathematical investigations of Section II-B, analytical v_{Sm} is also indicated in Fig. 13.

C. Achieving Zero Transient Power on S_m

Fig. 14 describes the operation of the proposed SSCB where the transient power across S_m is reduced to zero during dc current interruption, and a soft turn-OFF is realized in S_m. As indicated in Fig. 14, under achieving TCC, S_m turns OFF when i_{Sm} closes to zero. This helps to remove the induced voltage on the gate of

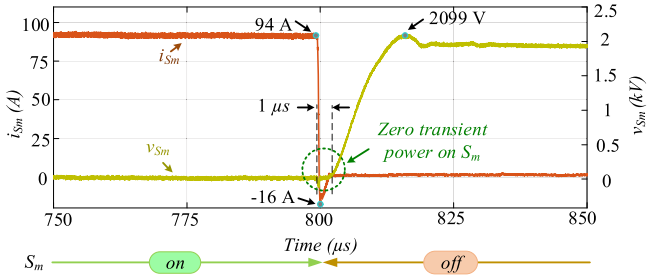

Fig. 14. Experimental results: S_m current (i_{Sm}) and voltage (v_{Sm}).

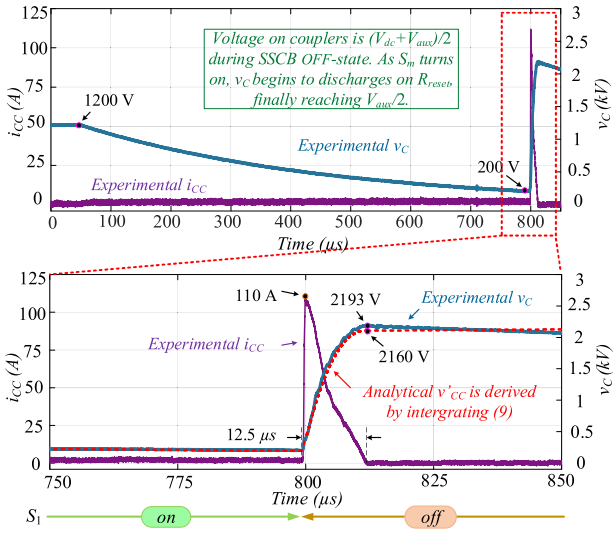

Fig. 15. Experimental and analytical results: couplers current (i_{CC}) and voltage (v_C).

S_m due to common impedance coupling in the source terminal of S_m [5], [6]. Also, when v_{Sm} starts to increase, i_{Sm} is zero, meaning zero power shock on S_m. In Fig. 14, the negative current in i_{Sm} flows through the body diode of S_m and obtains a safe margin to achieve soft turn-OFF.

D. Analyzing Capacitive Couplers Operation

Coupler voltage v_C ($= v_{C1} = v_{C2}$) and current i_{CC} are shown in Fig. 15 during dc current interruption. Peak current value reaches 110 A, and it reduces to zero in 12.5 μs. The voltage across each coupler starts from 190 V and finally gets the maximum value of 2193 V. Also, analytical equations are used to describe each coupler voltage, and the result is indicated in Fig. 15, where peak value across C_1 and C_2 reaches 2160 V, which is close to the experimental results, which further validates the analysis and mathematical investigation in Sections II and III.

V. Discussion on the Response Speed

The proposed SSCB has been tested under 2 kV dc bus voltage in interrupting 100 A short circuit fault and load current, where the reaction time interval was recorded as 13 + 95 μs = 108 μs during experiments. Compared with the reported 9.4 μs in [5] and 30 μs in [15], the reaction time of the proposed SSCB is relatively longer.

In practical applications, as the SSCB is mainly used to interrupt short circuit fault currents, the response time needs to be minimized. According to Fig. 12, the reaction interval of the proposed SSCB depends on:

1) digital synchronization delay $t_{\rm delay}$ between AIC and main branch, adjusted as 13 μs
2) AIC current rising delay $t_{\rm rising}$, which is 95 μs.

Digital synchronization time delay $t_{\rm delay}$ can be reduced significantly as needed. As indicated in Fig. 12, AIC acknowledges the main branch's request after 13 μs. As the TMS320F28379 DSP operating at 200 MHz controls the process in the AIC, it can handle the timing process in tens of operating frequency cycles, which theoretically reduces $t_{\rm delay}$. Besides, $t_{\rm rising}$ in AIC can be optimized by proper selection of $V_{\rm aux}$ and L_1 regarding the dc system inertia. As it is shown in Fig 6, $t_{\rm rising}$ can be reduced below 15 μs by selecting L_1 less than 50 μH for $V_{\rm aux}$ higher than 400 V. Therefore, the reaction time interval can be significantly minimized.

Mathematical investigations, LTspice simulations, and experimental results match satisfactorily and verify the effectiveness of the proposed SSCB in practice.

VI. Conclusion

A new capacitive couple-based auxiliary branch was presented in this letter. Implementing coupling capacitors acts as an interface between AIC and the main branch and prevents short circuit failures in the AIC, which enhances the reliability of SSCBs. Besides, a boost converter-based resonant AIC was presented to achieve TCC in the main switch through capacitive couplers. To validate the proposed SSCB and mathematical analysis, 2-kV/100-A prototype was implemented and tested successfully, achieving soft turn-OFF, zero transient power in the main switch, and enhancing reliability. The reaction time interval of the proposed SSCB is 108 μs which includes the digital synchronization time delay and the AIC current rising interval. The injected pulse current reaches 110 A to compensate the current in the main switch, and the dc line current reduces to zero within 14 μs. The reaction time of the proposed SSCB can be minimized by optimizing the synchronization delay and the passive components in the auxiliary branch. In addition, the design power density is another factor requiring more investigations in future research work.

Acknowledgment

The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

References

[1] Y. Ren, X. Yang, F. Zhang, F. Wang, L. M. Tolbert, and Y. Pei, "A single gate driver based solid-state circuit breaker using series connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2002–2006, Mar. 2019.

[2] R. Kheirollahi, S. Zhao, and F. Lu, "Fault current bypass-based LVDC solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 7–13, Jan. 2022.

[3] X. Xu, W. Chen, H. Tao, Q. Zhou, Z. Li, and B. Zhang, "Design and experimental verification of an efficient SSCB based on CS-MCT," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11682–11693, Nov. 2020.

[4] Z. Ayubu, J.-Y. Kim, J.-Y. Yu, S.-M. Song, and I.-D. Kim, "Novel bidirectional dc solid-state circuit breaker with operating duty capability," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9104–9113, Oct. 2021.

[5] R. Kheirollahi, H. Zhang, S. Zhao, and F. Lu, "A dc solid-state circuit breaker based on transient current commutation," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi: 10.1109/JESTPE.2021.3116605.

[6] R. Kheirollahi, H. Zhang, S. Zhao, J. Wang, and F. Lu, "Ultrafast solid-state circuit breaker with a modular active injection circuit," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, to be published, doi: 10.1109/JESTIE.2021.3087952.

[7] "High-voltage dc circuit breaker apparatus," European Patent EP0108279 (B1), Oct. 1983.

[8] J.-Y. Yu, J.-Y. Kim, S.-M. Song, Z. Ayubu, and I.-D. Kim, "New dc solid-state circuit breaker with natural charging operation," *IEEE Trans. Power Electron.*, vol. 68, no. 11, pp. 10360–10368, Nov. 2021.

[9] Olde *et al.*, "Commutation type DC breaker" U.S. Patent US5452170A, Sep. 1995.

[10] Y. D. Rodrigues, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

[11] Y. Wu, Y. Wu, F. Yang, M. Rong, and Y. Hu, "A novel current injection dc circuit breaker integrating current commutation and energy dissipation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2861–2869, Sep. 2020.

[12] J. Shu, S. Wang, J. Ma, T. Liu, and Z. He, "An active z-source dc circuit breaker combined with SCR and IGBT," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10003–10007, Oct. 2020.

[13] J. Shu, J. Ma, S. Wang, Y. Dong, T. Liu, and Z. He, "A new active thyristor-based DCCB with reliable opening process," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3617–3621, Apr. 2021.

[14] R. Kheirollahi, S. Zhao, H. Zhang, J. Wang, and F. Lu, "Wireless series-parallel capacitor charger for dc circuit breaker applications," in *Proc. IEEE PELS Workshop Emerg. Technol. Wireless Power Transf.*, San Diego, CA, USA, 2021, pp. 1–4.

[15] A. Ray, K. Rajashekara, S. N. Banavath, and S. K. Pramanick, "Coupled inductor-based zero current switching hybrid dc circuit breaker topologies," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5360–5370, Sep./Oct. 2019.