Analysis and Mitigation of the Common-Mode Noise in a Three-Phase SiC-Based Brushless DC Motor Drive With 120° Conduction Mode

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***Abstract*—The generation and propagation of the common-mode (CM) noise depends on the pulsewidth modulation (PWM) technique, parasitic capacitances, and rate of change of voltages imposed on the motor. In the literature, the CM noise analysis of the brushless dc (BLdc) drive operated with 120° conduction mode is reported neglecting the impact of the floating phase, and the analysis is restricted to low-voltage silicon-based drives. In this article, an in-depth theoretical analysis of the CM noise in the BLdc drive is presented considering two commonly used schemes in 120° conduction mode: six-step commutation and bipolar PWM. It is proven through experiments that the impact of the floating phase cannot be neglected especially with the high-voltage slew rate imposed by silicon carbide (SiC)-based inverters on the drives. By considering the impact of the floating phase, the CM noise in the BLdc drive is modeled through mathematical equations, and suitable equivalent circuits are presented. Finally, a step-by-step design procedure of the CM filter for the BLdc drive is presented. Experimental results on a three-phase star-connected SiC-based BLdc drive are provided to substantiate the analysis and CM filter design.**

***Index Terms*—Bipolar pulsewidth modulation (PWM), Brushless dc (BLdc) motor drive, common-mode (CM) noise, filters, silicon carbide (SiC).**

I. Introduction

BRUSHLESS dc (BLdc) motor drive with a trapezoidal back electromagnetic force (EMF) profile has been widely adopted in various industrial and residential applications because of its significant advantages such as high torque to weight ratio, better efficiency, and less acoustic noise [1]–[3]. Moreover, the BLdc motors that were so far confined to low-voltage drives (e.g., 48 V) are now in consideration for high-voltage drives (200 V and above) in applications, such as electric vehicles (EVs) and solar water pumps [4]. Extensive research has been carried on high-voltage BLdc motors to optimize the efficiency without compromising the power density and torque ripple [5]. Due to rapid advancement in semiconductor technology, wide-bandgap (WBG) power devices are preferred to achieve increased power density and efficiency in the power converter, even while operating in harsh environmental conditions [6]. Thus, WBG devices such as silicon carbide (SiC) and gallium nitride (GaN) are increasingly used for motor drive applications [7].

The operation of the SiC-based BLdc drive with a high switching frequency is desirable as it improves the torque ripple performance of the motor [8]. However, an increase in the switching frequency parallel with high operating voltages and faster switching transitions amplify the common-mode (CM) issues [9]. The CM voltages with a high-voltage slew rate (i.e., dv/dt) excite the motor's and converter's parasitic elements, leading to high-frequency leakage currents through the ground. The CM issue arising due to the ground current is referred as conducted CM noise, which can deteriorate the system performance and degrade the reliability of the whole system [10].

The instantaneous dv/dt responsible for the CM noise is dictated by both switching transients as well as pulsewidth modulation (PWM) methods [11]. The PWM methods used in the BLdc drive such as six-step commutation (SSC) and bipolar PWM (BPWM) are primarily derived from the 120° square-wave commutation technique [12]. In the three-phase BLdc motor drive with 120° commutation schemes, two phases of the motor conduct at any given time, while the third one remains floating. In [13] and [14], the CM noise analysis of the BLdc motor is performed by considering the excitation of parasitic elements due to high dv/dt associated with the two conducting phases. The existence of mutual inductance and parasitic capacitance between the conducting and floating phases leads to a significant CM noise from the floating phase, especially in high-voltage SiC-based BLdc motor drives; hence, it cannot be neglected. Moreover, the well-established CM noise propagation theory of the induction motor (IM) drive cannot be directly applied due to the operation of the BLdc motor with floating phase.

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CM filters are incorporated in the drive to limit the impact of the CM noise on the rest of the system, especially, communication channels and digital controllers. In [13] and [14], a CM noise mitigation technique using delay compensation for the BPWM-operated low-voltage three-phase BLdc drive is reported. Such active methods rely on precision sensing and signal conditioning of the CM voltage for mitigation of the noise. Moreover, the proposed active attenuation method is very specific and cannot be used for other PWM schemes. Unlike the active filters, the passive electromagnetic interference (EMI) filters are reliable and cost effective when designed appropriately as they are realized using passive elements such as inductors, capacitors, and damping resistors [15]. Although a passive attenuation method to suppress the EMI noise in the BLdc drive using various filter stages is reported in [16], step-by-step design procedure and experimental validation are missing.

Lack of in-depth analysis on the propagation of the CM noise and clear understanding of the source of the noise mislead the design of CM filters for high-voltage BLdc drives. Therefore, the effect of dv/dt in the high-voltage SiC-based three-phase BLdc motor drive is studied in this article. Particularly, the following two modulation methods in the 120° commutation mode are selected: SSC and BPWM.

The main contributions of this article are as follows.

1) The propagation of the CM noise and its source is analyzed with the help of a dummy parasitic impedance (DPI) network, which is designed to emulate the CM impedance of the motor up to the desired frequencies.
2) The significance of commutation and mutual inductance on the generation of the CM noise is studied. Based on the analysis and thorough experimental studies, a CM equivalent circuit is proposed for the SiC-fed high-voltage BLdc drive.
3) Through the analysis presented in this article, a conventional three-port CM filter is designed and validated for the BLdc drive.

The rest of this article is organized as follows. In Section II, the importance of the DPI network in analyzing the CM noise in the BLdc motor is explained along with its design and validation. The analysis of the CM noise for SSC and BPWM are presented in Section III along with the CM equivalent circuit. The design and validation of two commonly used CM filters are provided in Section IV. Finally, Section V concludes this article.

II. BLDC Drive and CM Issues

The BLdc motor is well known for its advantages, such as high torque to weight ratio, increased reliability due to the elimination of carbon brushes, high efficiency, and reduced EMI. The lumped parameter model of the BLdc motor is shown in Fig. 1(a). The circuit model considers the effect of phase-to-ground parasitic capacitors, C_{ag}, C_{bg}, and C_{cg}, and per-phase inductance and back EMF, which are modeled as Z_{mi} and e_i, respectively, where $i = a, b, c$. Two modulation schemes in the 120° commutation mode, SSC and BPWM are considered for CM analysis. The modulation schemes were well documented in [17], and are not repeated in this article for conciseness. The switching action

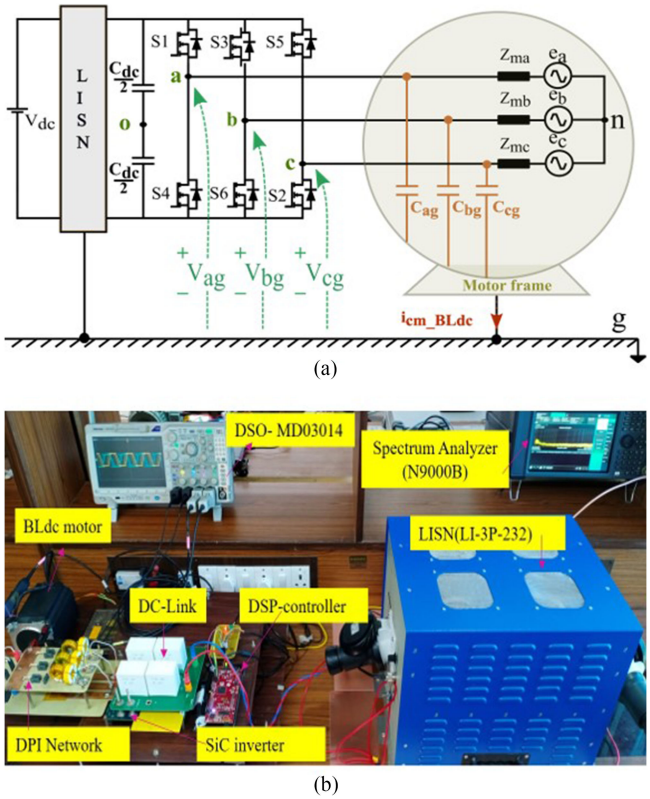

Fig. 1. (a) Circuit diagram of the SiC-based BLdc motor drive with phase-to-ground parasitic capacitances C_{ag}, C_{bg}, and C_{cg}. (b) Experimental setup of a three-phase BLdc drive with the DPI network.

of the active devices results in high dv/dt applied across the phase and ground terminals (v_{ag}, v_{bg}, and v_{cg}) of the motor. Such dv/dt excites the motor parasitic capacitances, causing inevitable ground currents, $i_{\text{cm\_BLdc}}$.

To understand the propagation of the CM noise in the BLdc drive, it is necessary to analyze the currents through C_{ag}, C_{bg}, and C_{cg} individually. As the parasitic components are not physical elements, it is impossible to measure the currents through them. Even if $i_{\text{cm\_BLdc}}$ is measured, the effect of dv/dt on each phase-to-ground parasitic capacitance of the motor and its contribution toward the $i_{\text{cm\_BLdc}}$ cannot be predicted. Therefore, a DPI network is proposed in this article to emulate the currents flowing through C_{ag}, C_{bg}, and C_{cg} up to a desired frequency. It is to be noted that the proposed DPI network is used as a platform to understand the propagation of CM currents in the BLdc drive, but not to accurately model the CM impedance.

A. DPI Network

A three-phase BLdc motor with the specifications shown in Table I is connected to a three-phase SiC-based inverter as shown in Fig. 1(b). A line impedance stabilization network (LISN) LI-3P-232 is connected on the dc side of the inverter to decouple the motor's CM noise and the noise from the dc source. High performance ac/dc current probes (TCP202 A) are used to measure the currents flowing from the motor frame to the ground. The current probe is particularly chosen as it has a measurement

TABLE I
SPECIFICATIONS OF THE BLDC MOTOR

Parameter	Value
Rated dc voltage, V_{dc}	310 V
Rated power, P	1.5 kW
Rated current, I	6.3 A
Nominal Toque, T	4.3 N•m
Rated Speed, N	3500 r/min
Number of poles	8
Torque constant, k_T	0.79 Nm/A
Back EMF constant, k_E	55 V/krpm

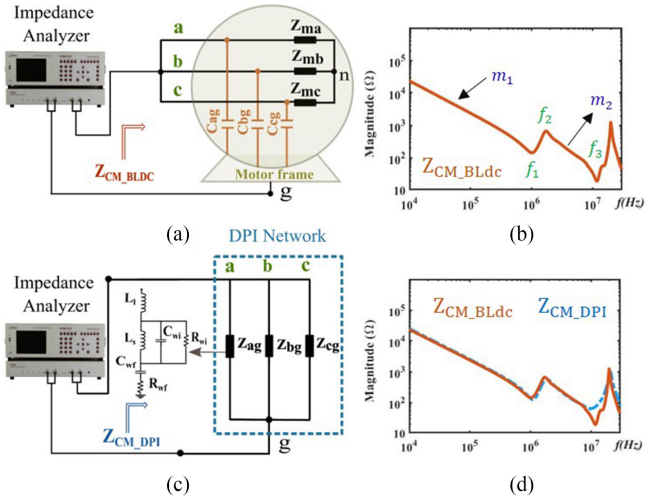

Fig. 2. (a) Circuit arrangement to measure the CM impedance of the motor. (b) Measured CM impedance of the motor. (c) Circuit arrangement to measure the impedance of the DPI network. (d) Measured impedance of the DPI network.

bandwidth of 50 MHz with a desired accuracy between 10 mA and 15 A. The digital signal processor TMS320F28379D is used for controlling the motor. The circuit arrangements to measure the motor CM impedance ($Z_{\text{CM\_BLdc}}$) using the network analyzer NH4L-IAI2 and the measured impedance are illustrated in Fig. 2(a) and (b), respectively. In this article, each phase of the DPI network is modeled as a fourth-order passive network, as shown in Fig. 2(c). The DPI network is designed to emulate the CM impedance of the motor to understand the propagation of the CM noise in the motor. From the measured impedance profile of $Z_{\text{CM\_BLdc}}$, the values of L_l, L_s, R_{wf}, R_{wi}, C_{wf}, and C_{wi} parameters of the DPI network are designed as follows.

1) At medium frequencies, the capacitance C_{wi} defines the slope m_2 in $Z_{\text{CM\_BLdc}}$, as shown in Fig. 2(b). Hence, C_{wi} is calculated from $Z_{\text{CM\_BLdc}}$ as

$$C_{wi} = \frac{1}{2\pi f |3Z_{\text{CM\_BLdc}}|_{\text{at } f}}, \quad \text{for} \quad f_2 \ll f \ll f_3. \tag{1}$$

2) At low frequencies, the combined capacitance $C_{wi} + C_{wf}$ defines the slope m_1. Thus, the expression of C_{wf} is written as

$$C_{wf} = \frac{1}{2\pi f |3Z_{\text{CM\_BLdc}}|_{\text{at } f}} - C_{wi}, \quad \text{for} \quad f \ll f_1. \tag{2}$$

3) The total capacitance $(C_{wi} + C_{wf})$ and the inductance L_s create a resonance at f_1, and R_{wf} defines the impedance Z_1 at this resonance frequency f_1. Thus, L_s and R_{wf} are calculated from f_1 and Z_1 as

$$L_s = \frac{1}{4\pi^2 f_1^2 (C_{wi} + C_{wf})}, \text{and} \tag{3}$$

$$R_{wf} = |3Z_{\text{CM\_BLdc}}|_{\text{at } f_1}. \tag{4}$$

4) At high frequencies, the inductance L_l creates a resonance with the series combination of C_{wf} and C_{wi} at f_3 as shown in Fig. 2(b). Thus, L_l is calculated from f_2 using

$$L_l = \frac{1}{4\pi^2 f_3^2 \left(\frac{C_{wi} C_{wf}}{C_{wi} + C_{wf}}\right)}. \tag{5}$$

5) L_s and C_{wi} create a resonance at f_2. R_{wi} defines the magnitude of $Z_{\text{CM\_BLdc}}$ at this frequency and is given as

$$R_{wi} = |3Z_{\text{CM\_BLdc}}|_{\text{at } f_2}. \tag{6}$$

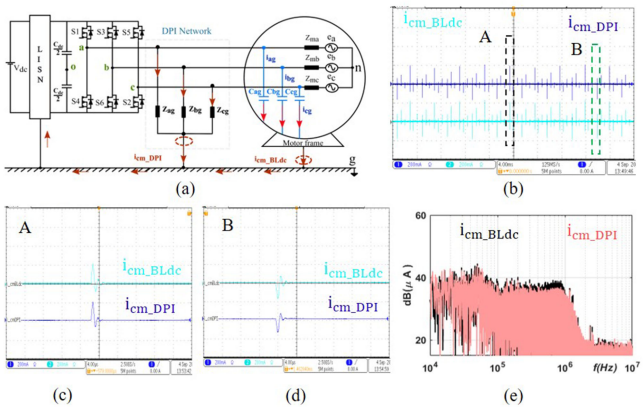

Fig. 3. (a) Circuit arrangement to measure $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$. (b) $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$. (c) Enlarged waveform showing positive peaks of $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$ current of the "A" region. (d) Enlarged waveform showing negative peaks of $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$ current of the "B" region. (e) Frequency spectrum of $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$.

As shown in Fig. 2(d), the CM impedance of the DPI network ($Z_{\text{CM\_DPI}}$) replicates the CM impedance of the BLdc motor, ($Z_{\text{CM\_BLdc}}$). From (1)–(6), the values of L_l, L_s, R_{wf}, R_{wi}, C_{wf}, and C_{wi} parameters are estimated to be 4 μH, 112 μH, 430 Ω, 2000 Ω, 144 pF, and 80 pF, respectively.

As the DPI network is modeled to predict the behavior of currents through C_{ag}, C_{bg}, and C_{cg}, the total ground current of the DPI network (i.e., $i_{\text{cm\_DPI}}$) and that of the BLdc motor (i.e., $i_{\text{cm\_BLdc}}$) shown in Fig. 3(a) should follow the same pattern. The experimental waveforms of $i_{\text{cm\_DPI}}$ and $i_{\text{cm\_BLdc}}$ for SSC are shown in Fig. 3(b)–(d). From Fig. 3(c), it is observed that both $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$ have their positive peaks at the same instant. While in Fig. 3(d), both $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$ have their negative peaks at the same instant. From the presented results, it is observed that the measured $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$ are identical; hence, the DPI network is used for further analysis. As shown in Fig. 3(e), the frequency spectrum of both $i_{\text{cm\_BLdc}}$ and $i_{\text{cm\_DPI}}$ are approximately identical up to 10 MHz. A maximum of 3 dB amplitude difference is seen in the frequencies between 10 kHz and 10 MHz, this would not alter the nature of the currents

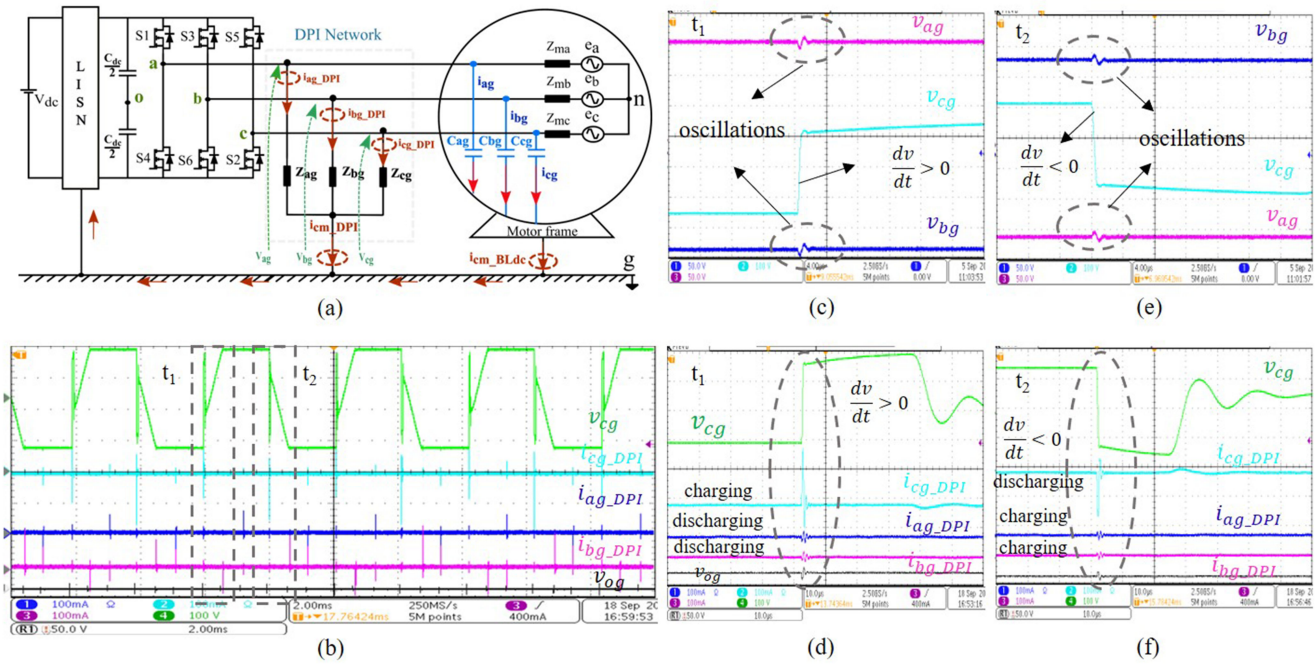

Fig. 4. (a) Three-phase BLdc drive with the DPI network for analyzing the CM currents. (b) v_{cg} along with the currents through each phase-to-ground of the DPI network (i.e., i_{ag_DPI}, i_{bg_DPI}, and i_{cg_DPI}). (c) Enlarged waveforms of v_{ag}, v_{bg}, and v_{cg} at t_1. (d) Enlarged waveforms of v_{cg}, i_{ag_DPI}, i_{bg_DPI}, and i_{cg_DPI} at t_1. (e) Enlarged waveforms v_{ag}, v_{bg}, and v_{cg} at t_2. (f) Enlarged waveforms of v_{cg}, i_{ag_DPI}, i_{bg_DPI}, and i_{cg_DPI} at t_2.

through the DPI and the motor ground parasitic capacitances as they are excited by the same source (i.e., same dv/dt).

III. Analysis of CM Noise in the BLDC Motor Drive

A. Six-Step Commutation (SSC)

To understand the propagation of CM currents in each phase of the SSC-operated BLdc drive, the DPI network is connected along with the motor, as shown in Fig. 4(a). In a fundamental cycle of the SSC, each phase undergoes two conduction and two floating periods [17]. For instance, the conduction and floating periods of the phase c during the positive half cycle of the fundamental period are illustrated in Fig. 4(b). Although the floating period is divided into commutation and back EMF periods, the high dv/dt during the commutation period dominates the transition and contributes to the CM noise. As shown in Fig. 4(b), the commutation instances t_1 and t_2 contributing to the CM noise are analyzed further. Following are the inferences from the experimental results.

1) The dv/dt in v_{cg} at t_1 and t_2 causes disturbances in v_{ag} and v_{bg}, as shown in Fig. 4(c) and (e). In particular, the noncommutating phases experience an opposite transition as that of the commutating phase. It can be understood that the commutations in any one of the phases is reflected as voltage oscillations in the remaining phases due to v_{og} fluctuation, thereby, exciting all the phases-to-ground parasitic capacitances (i.e., C_{ag}, C_{bg}, and C_{cg}).
2) At t_1, the currents i_{ag_DPI}, i_{bg_DPI}, and i_{cg_DPI} during commutation in the phase c, are shown in Fig. 4(d). At this instant, v_{cg} has positive dv/dt, while v_{ag} and v_{bg} experience negative dv/dt as explained earlier. Therefore, i_{cg_DPI} through Z_{cg} is a charging current that flows in the direction toward the ground, while the currents i_{ag_DPI} and i_{bg_DPI} are discharging currents and flow away from the ground.
3) It can be observed from Fig. 4(f) that the negative dv/dt in v_{cg} drives i_{cg_DPI} in the phase c of the DPI network. The positive dv/dt induced in v_{ag} and v_{bg} causes i_{ag_DPI} and i_{bg_DPI} in phases a and b of the DPI network.

The i_{ag_DPI}, i_{bg_DPI}, and i_{cg_DPI} are measured to provide an insight on the nature of i_{ag}, i_{bg}, and i_{cg} of the motor, respectively. Therefore, it can be concluded that all the three phases of the BLdc motor contribute to the CM noise in case of SSC. The direction of currents in each phase is dictated by the direction of dv/dt.

B. Bipolar Pulsewidth Modulation (BPWM)

In BPWM-operated BLdc drive, the high-side switches (S_1, S_3, and S_5) and the low-side switches (S_4, S_6, and S_2) are controlled using PWM signals [17]. Similar to the SSC, two out of the three phases of the motor are conducting, while the third phase remains floating in BPWM. Unlike the SSC, the pole of the conducting phase alternates between $\pm V_{\rm dc}/2$ with respect to "o" at the switching frequency (10 kHz) in BPWM. The dv/dt in the conduction period coupled with the parasitic elements of the motor causes undesirable $i_{\rm cm\_BLdc}$.

1) Effect of the Conducting Phase: The dv/dt in the conducting phase excites the corresponding phase-to-ground parasitic capacitance. In an ideal condition, the charging and discharging currents through the ground should become cancelled because of complementary pole voltages. As discussed in [13], due

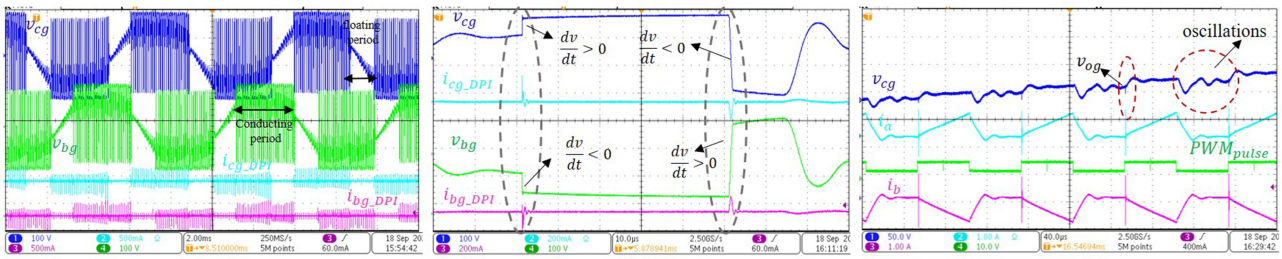

Fig. 5. Three-phase BLdc drive with the DPI network for analyzing the CM currents with BPWM. (a) v_{bg} and v_{cg} voltage waveforms indicating floating and conduction periods in v_{cg} along with corresponding DPI network currents i_{bg_DPI} and i_{cg_DPI}. (b) Enlarged waveforms of v_{bg} and v_{cg} showing positive and negative dv/dt instances in the conduction period along with i_{bg_DPI} and i_{cg_DPI} currents at that instances. (c) Effect of mutual inductance and capacitance, v_{og} and back EMF on v_{cg} in floating period along with i_a and i_b phase currents.

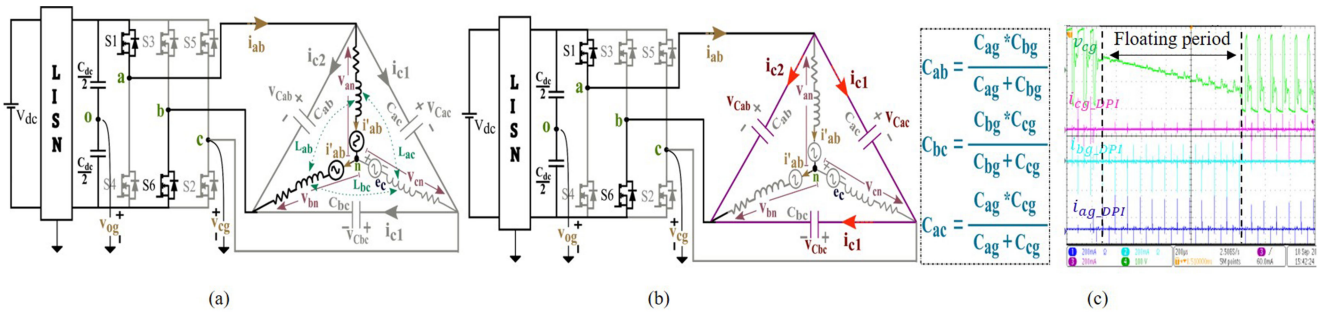

Fig. 6. (a) Circuit diagram for determining the effect of mutual inductance on the floating phase voltage v_{cg}. (b) Circuit diagram for determining the effect of ground parasitic capacitances on floating phase voltage v_{cg}. (c) DPI currents i_{ag_DPI}, i_{bg_DPI}, and i_{cg_DPI} at an instant when v_{cg} is floating.

to nonidealities in the turn-ON and turn-OFF transitions of the complementary switching devices, and propagation delays from the gate drivers, the resultant ground current will not be zero. The effect of dv/dt in the conducting phase of the motor in the BPWM case is captured in Fig. 5(a) and following are the inferences.

1) The waveforms of v_{bg}, v_{cg}, i_{bg_DPI}, and i_{cg_DPI} are illustrated in Fig. 5(a). It is observed that in the conduction period of v_{bg}, due to the dv/dt incurred through PWM switching, a nonzero i_{bg_DPI} flows through Z_{bg} of the DPI network. A similar observation is made for phase c.
2) The enlarged waveforms of v_{bg} and v_{cg} during the conduction period are shown in Fig. 5(b). The i_{bg_DPI} is seen at the instances where $dv/dt \neq 0$ during the conduction period of v_{bg}. A similar pattern is observed in i_{cg_DPI} with a finite dv/dt in v_{cg}, as shown in Fig. 5(b).

2) Effect of Floating Phase: As discussed in Section III-A, the floating period of the BLdc motor is divided into commutation and back EMF periods. The analysis of the CM noise during the commutation period in the BPWM case is similar to that of the SSC, i.e., dv/dt induced in the floating phase to ground voltage contributes to the $i_{\mathrm{cm\_BLdc}}$. However, unlike the back EMF period of SSC, the CM noise during the back EMF period of the BPWM case cannot be neglected. The factors contributing to the CM currents during the back EMF period are as follows:

1) the mutual inductance between the floating phase and conducting phases;
2) the phase-to-ground parasitic capacitance.

To understand the impact of mutual inductance during the back EMF period, the phase-to-ground voltage of the floating phase is derived from the simplified circuit shown in Fig. 6(a). By applying Kirchhoff's voltage law (KVL) to loop 1 connecting the nodes *g-o-a-n-c-g* and loop 2 connecting the nodes *g-o-b-n-c-g*, the voltage v'_{cg} is obtained as

$$v'_{cg} = (L_{bc} - L_{ac})\frac{di'_{ab}}{dt} + v_{og} + e_c \tag{7}$$

where L_{ac} and L_{bc} are the mutual inductances between phases c and a, and phases c and b, respectively. The self-inductance and the mutual-inductance are a function of angular position of rotor, θ_r [18], [19]. Considering the effect of θ_r, the mutual inductances of L_{bc} and L_{ac} are expressed as

$$L_{bc} = -M_s - L_g \cos\left(2\left(\theta_r + \frac{\pi}{6} - \frac{2\pi}{3}\right)\right) \tag{8}$$

$$L_{ac} = -M_s - L_g \cos\left(2\left(\theta_r + \frac{\pi}{6} + \frac{2\pi}{3}\right)\right) \tag{9}$$

substituting the value of L_{bc} and L_{ac} into (7), the simplified expression for v'_{cg} is expressed as

$$v'_{cg} = \sqrt{3}L_g \sin(2\theta_r + (\pi/3))\frac{di'_{ab}}{dt} + v_{og} + e_c \tag{10}$$

where L_g is the fluctuation in inductance with change in θ_r. From (10), i'_{ab} and θ_r influence the floating phase voltage and it is responsible for the CM noise during the back EMF period, as shown in Fig. 5(c).

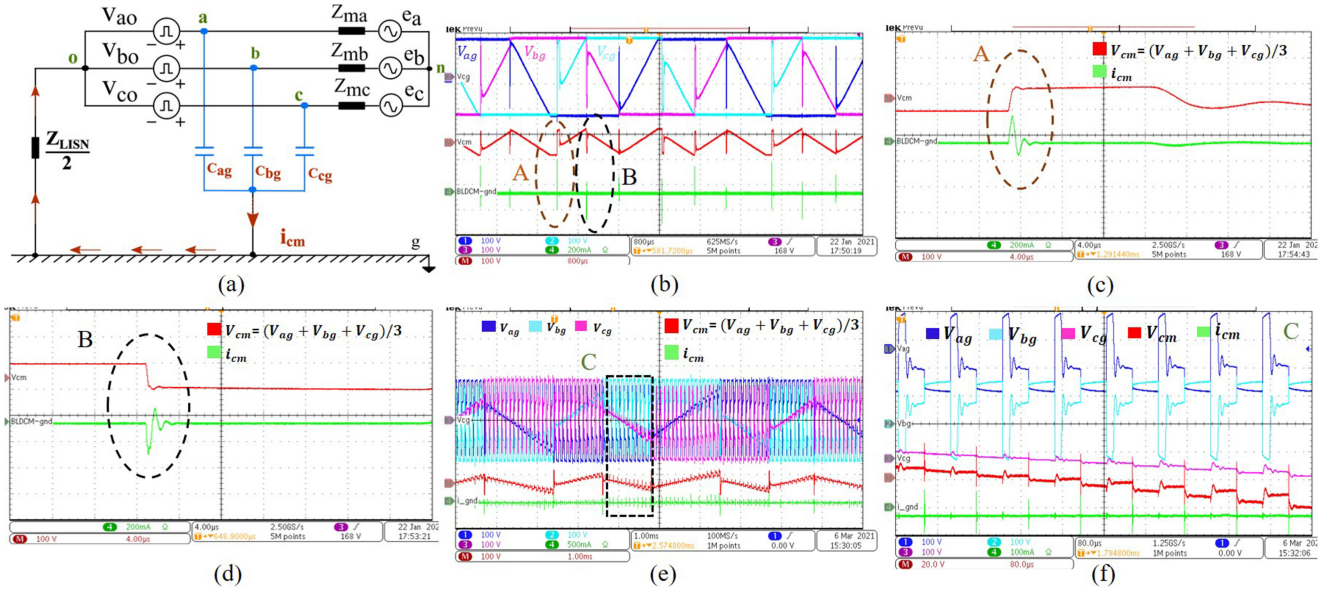

Fig. 7. Experimental waveform of v_{cm} and $i_{\text{cm\_BLdc}}$ for SSC and BPWM. (a) Three-phase CM equivalent circuit for both SSC and BPWM. (b) Waveforms of (v_{cm}) and ($i_{\text{cm\_BLdc}}$) along with phase-to-ground voltages (v_{ag}, v_{bg}, and v_{cg}). (c) Enlarged waveform showing the charging nature of $i_{\text{cm\_BLdc}}$ due to positive dv/dt in v_{cm}. (d) Enlarged waveform showing the discharging nature of $i_{\text{cm\_BLdc}}$ due to negative dv/dt in v_{cm}. (e) (v_{cm}) and ($i_{\text{cm\_BLdc}}$) profiles along with phase-to-ground voltages (v_{ag}, v_{bg}, and v_{cg}). (f) Enlarged waveforms of C region showing v_{ag}, v_{bg}, v_{cg}, v_{cm}, and i_{cm}.

To analyze the impact of the phase-to-ground parasitic capacitance on the CM noise, the considered equivalent circuit of the BLdc motor when the phase c is floating, is shown in Fig. 6(b). By applying the KVL to loop 1 connecting the nodes *g-c-b-o-g* and loop 2 connecting the nodes *g-c-a-o-g*, the voltage v''_{cg} is derived as

$$v''_{cg} = v_{og} + \frac{1}{2}(v_{C_{bc}} - v_{C_{ac}}) \tag{11}$$

where $v_{C_{bc}}$ and $v_{C_{ac}}$ are the voltages across C_{bc} and C_{ac}, respectively, and can be written as

$$v_{C_{bc}} = \frac{1}{C_{bc}} \int i_{c1}\, dt \;\text{ and }\; v_{C_{ac}} = \frac{1}{C_{ac}} \int i_{c1}\, dt. \tag{12}$$

Substituting (12) into (11), v''_{cg} can be simplified as

$$v''_{cg} = v_{og} + \frac{1}{2}\left(\frac{C_{ac} - C_{bc}}{C_{ac} * C_{bc}}\right) \int i_{c1}\, dt. \tag{13}$$

From (13), it can be understood that the high dv/dt oscillations in the back EMF period are because of the excitation of phase-to-ground capacitors (that act as phase-to-phase capacitors) during switching.

Thus, (7) and (13) provide an insight on the two components of the floating phase voltage due to mutual inductance v'_{cg} and capacitances between the phases v''_{cg} of the motor. Hence, the resultant floating phase voltage consists of the following: switching frequency component due to the mutual inductance and oscillation due to the capacitance between the phases; oscillations corresponding to v_{og}; and back EMF (e_c) component, as shown in Fig. 5(c). The waveforms of i_{ag_DPI}, i_{bg_DPI}, and i_{cg_DPI} when v_{cg} is floating is shown in Fig. 6(c). It is observed that all the three phase-to-ground impedances of the DPI network are energized during this instant. Therefore, it can be concluded that similar to the SSC case, all the three phases contribute to the CM noise in the BPWM-operated BLdc drive.

C. CM Equivalent Circuit

Considering the experimental data and the presented analysis, the CM equivalent circuit for the BLdc motor is proposed, as shown in Fig. 7(a). As discussed in Sections III-A and III-B, the parasitic capacitors between all phases and ground become excited simultaneously due to the dv/dt in each phase. Therefore, the CM equivalent circuit must consist of all pole voltages and phase-to-ground parasitic capacitances of the motor. Hence, $i_{\text{cm\_BLdc}}$ can be written as

$$\vec{i}_{\text{cm}} = \vec{i}_{ag} + \vec{i}_{bg} + \vec{i}_{cg}. \tag{14}$$

Since the time-varying nature of v_{ag}, v_{bg}, and v_{cg} causes the parasitic currents, the aforementioned equation can be rewritten as

$$\vec{i}_{\text{cm}} = \frac{\vec{v}_{ag}}{Z_{C_{ag}}} + \frac{\vec{v}_{bg}}{Z_{C_{bg}}} + \frac{\vec{v}_{cg}}{Z_{C_{cg}}} \tag{15}$$

where $Z_{C_{ag}} = 1/\omega C_{ag}$, $Z_{C_{bg}} = 1/\omega C_{bg}$, and $Z_{C_{cg}} = 1/\omega C_{cg}$.

If v_{cm} is the total CM voltage of the three-phase BLdc motor drive, the $i_{\text{cm\_BLdc}}$ in (15) can be modified as

$$\frac{\vec{v}_{\text{cm}}}{Z_{\text{cm}_{\text{BLdc}}}} = \frac{\vec{v}_{ag}}{Z_{C_{ag}}} + \frac{\vec{v}_{bg}}{Z_{C_{bg}}} + \frac{\vec{v}_{cg}}{Z_{C_{cg}}}. \tag{16}$$

Considering the symmetricity of the drive, the per-phase CM impedance is equal to thrice the $Z_{\text{CM\_BLdc}}$, therefore, v_{cm} is simplified as

$$\vec{v}_{\text{cm}} = \frac{\vec{v}_{ag} + \vec{v}_{bg} + \vec{v}_{cg}}{3}. \tag{17}$$

The measured v_{ag}, v_{bg}, and v_{cg} along with the v_{cm} in the case of SSC are shown in Fig. 7(b). It can be observed from the figure that only the floating periods of v_{ag}, v_{bg}, and v_{cg} appear in v_{cm} and dv/dt, which results in $i_{\text{cm\_BLdc}}$ only appearing during the commutation intervals. Also, the charging and discharging nature of $i_{\text{cm\_BLdc}}$ due to positive and negative dv/dt in v_{cm} are shown in Fig. 7(c) and (d), respectively. The experimental results confirm the analysis that the commutations during the floating period are responsible for $i_{\text{cm\_BLdc}}$ in SSC-operated BLdc drives.

The waveforms of v_{cm} and $i_{\text{cm\_BLdc}}$ for the BPWM case are shown in Fig. 7(e). Unlike SSC, in BPWM due to the effect of commutation, mutual inductance, and parasitic capacitance, the high dv/dt exist in the floating period (i.e., both commutation and back EMF period) of v_{ag}, v_{bg}, and v_{cg}. The effect of this high dv/dt in the floating period of v_{ag}, v_{bg}, and v_{cg} is seen in v_{cm}, which results in $i_{\text{cm\_BLdc}}$.

The v_{cm} and $i_{\text{cm\_BLdc}}$ waveforms are shown in Fig. 7(f). The experimental results confirm the analysis that both the commutation and back EMF periods with high dv/dt are responsible for $i_{\text{cm\_BLdc}}$ in the BPWM-operated BLdc drive.

Considering the analysis presented in this section, the required filters are discussed in the subsequent section to keep the CM noise within the acceptable limits suggested by EN550022 standards [20].

IV. CM Filter: Design and Validation

In the BLdc motor drive, it is generally believed that the ground current flows through only two phases at an instant. Therefore, the active compensation techniques were explored [13], ignoring the passive filtering techniques due to their disadvantage of under usage for two phase-to-ground excitations in a three-phase system. However, the presented analysis validates the current flow to the ground through all three phases for a three-phase BLDC drive. So, the passive CM filtration techniques are proven to be the feasible techniques for the three-phase BLDC drive, thus avoiding the complexity involved in active filtration techniques. Hence, in this section, the CM choke and *LC* filter are designed for validating the passive CM attenuation methods to reduce the CM noise.

The dc-link voltage of the BLdc motor drive is supplied either from a fixed or regulated voltage source depending on the application. The SSC is employed in applications where the dc-link voltage of the drive is regulated by a front-end converter to control the speed and torque of the motor, for instance, in solar water pumps [4], [21]. Therefore, the CM noise in the SSC case is measured with 150- and 310-V dc-link voltages, as shown in Fig. 8(a). Among the two considered dc-link voltages, 310 V is observed to be the worst-case scenario and is considered for the filter design. Similarly, the BPWM-operated BLdc motor drive will be fed with a fixed dc-link voltage, while the speed and torque are regulated by controlling the duty ratio. The CM noise of the drive in the BPWM case is obtained with different duty ratios (viz., 30%, 50%, 70%, and 100%) as shown Fig. 8(b). It can be observed from the figure that with an increase in the duty ratio, the CM noise increases, attaining a maximum when the duty ratio equals to 100% case. As shown in Fig. 8(a)

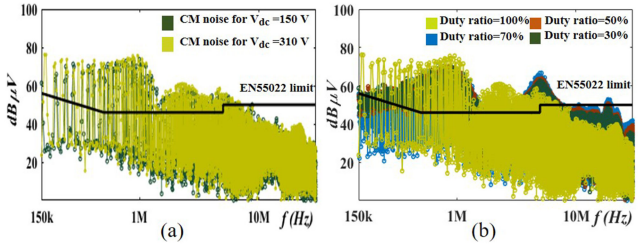

Fig. 8. Bare CM noise for (a) SSC case with 150 V and 310 V dc link voltages and (b) BPWM case with duty ratio of 30%, 50%, 70%, and 100%.

and (b), the CM noises in the BLdc drive in both SSC and BPWM cases do not comply with EN550022 standards. To meet the standards, a CM filter is placed between the inverter and motor terminals, as shown in Fig. 9(a). Two CM filter configurations, viz., CM choke and *LC* filter, are studied in this article. The attenuation requirements at any specific frequency is given by

$$\text{Attn}_{\text{reqcm}}(f)[\text{dB}\mu\text{V}] = A_{(\text{cm,max})}[\text{dB}\mu\text{V}] - \text{Limit}_{\text{EN55022 (AVG.)}} + 6\text{dB}\mu\text{V}(\text{margin}). \tag{18}$$

From the aforementioned equation, the attenuation required, excluding the 6-dB μ V margin, is calculated as 22.238 dB at 160 kHz by considering the frequency spectrum at 310 V (worst-case scenario) as shown in Fig. 8(a).

A. CM Choke

A simplified single-phase CM equivalent circuit, CM choke configuration, and simplified equivalent circuit with the CM choke are illustrated in Fig. 9(b)–(d), respectively. From Fig. 9(b) and (d), the attenuation offered by the CM choke is expressed as

$$\text{Attn.}_{\text{choke}} = 20\log\left(1 + \frac{Z_{\text{CM\_choke}}}{Z_{\text{CM\_BLdc}} + \frac{Z_{\text{LISN}}}{2}}\right). \tag{19}$$

From the aforementioned equation, it can be observed that with an increase in the impedance of the CM choke, the filter attenuation increases. Therefore, the CM choke should be designed such that

$$Z_{\text{CM\_choke}} + Z_{\text{CM\_BLdc}} >> Z_{\text{CM\_BLdc}}. \tag{20}$$

1) Design Guidelines for CM Choke: The following steps are suggested for the CM choke design in BLdc drives.

1) *Step 1*: From the $Z_{\text{CM\_BLdc}}$ plot shown in Fig. 9(e), the resonant frequency (f_r) is selected such that it is one third of the highest frequency component. In the figure, the highest frequency component is 160 kHz, therefore, f_r is fixed as 53.33 kHz. Selecting f_r less than one third of the highest frequency component favors the attenuation at the expense of the choke size.

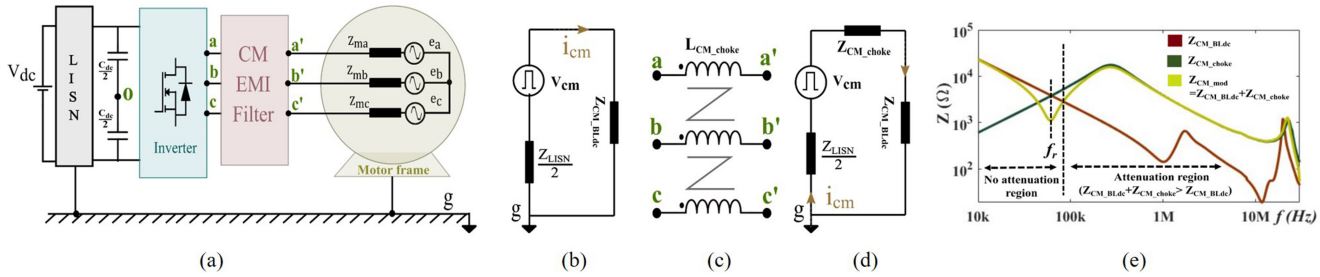

Fig. 9. (a) Block diagram of the three-phase BLdc drive with an EMI filter. (b) Simplified CM noise model for the BLdc motor. (c) CM choke configuration. (d) Simplified CM circuit with CM choke. (e) CM impedance profile of motor ($Z_{\text{CM\_BLdc}}$), CM choke ($Z_{\text{CM\_choke}}$), and motor CM choke ($Z_{\text{CM\_mod}}$).

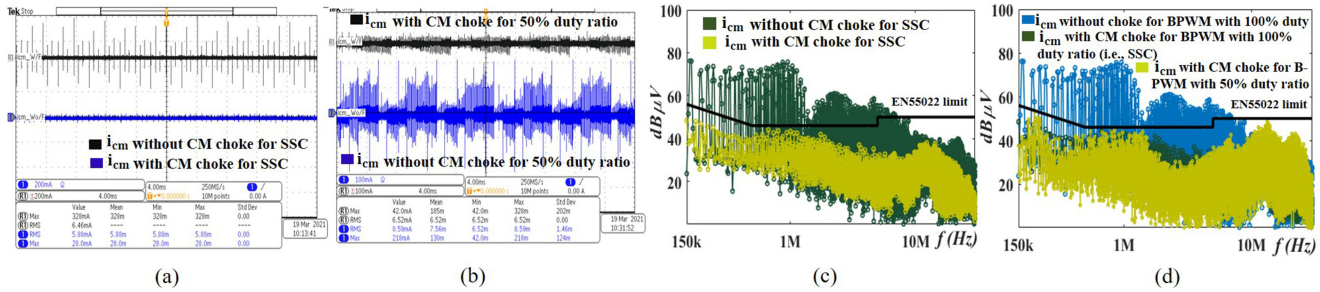

Fig. 10. Experimental results for SSC—dc voltage = 310 V, speed = 3500 r/min, and torque =0.316 N·m, and for BPWM—dc voltage = 310 V, speed = 1860 r/min, torque = 0.28 N·m, and duty = 50%. (a) Time-domain profile of $i_{\text{cm\_BLdc}}$ without and with a CM choke for SSC. (b) Time-domain profile of $i_{\text{cm\_BLdc}}$ without and with a CM choke for BPWM with 50% duty ratio. (c) Frequency-domain profile without and with a CM choke for SSC. (d) Frequency-domain profile without a CM choke for BPWM with 100% duty ratio and with a CM choke for BPWM with 100% and 50% duty ratio.

2) *Step 2*: The impedance of the CM choke is calculated at f_r as

$$Z_{\text{CM\_choke}} = Z_{\text{CM\_BLdc}}\big|_{f=f_r}. \tag{21}$$

3) *Step 3*: The inductance of the CM choke is obtained from $Z_{\text{CM\_BLdc}}$ as

$$L_{\text{CM\_choke}} = \frac{Z_{\text{CM\_choke}}}{2 \times \pi \times f_r} = \frac{Z_{\text{CM\_BLdc}}\big|_{f=f_r}}{2 \times \pi \times f_r}. \tag{22}$$

Following the design guidelines, a CM choke of 10 mH is required to attenuate the CM noise and meet the EN550022 standards. The modified CM impedance of the BLdc motor with CM choke, $Z_{\text{CM\_mod}}$, is shown in Fig. 9(e). It can be observed from this figure that the designed $Z_{\text{CM\_mod}}$ resonates at f_r and its impedance increases for frequencies beyond f_r. The measured i_{cm} profiles with and without the CM choke are presented in Fig. 10. Following are some of the inferences.

1) The i_{cm} profiles with and without CM choke for the SSC case are presented in Fig. 10(a). It can be seen from this figure that the peak of i_{cm} is reduced by 300 mA owing to the significant reduction in the CM noise.
2) The i_{cm} profiles with and without the CM choke for BPWM at the 50% duty cycle case are presented in Fig. 10(b). In this case, it is observed that the i_{cm} peak has been reduced by 176 mA.
3) The frequency spectrum of i_{cm} is shown in Fig. 10(c) for the SSC case, and in Fig. 10(d) for BPWM with 50% and 100% duty ratios.

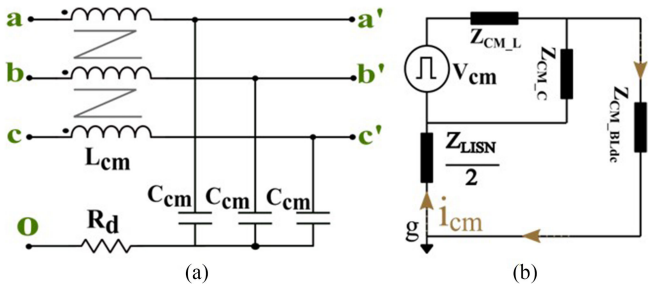

Fig. 11. (a) *LC* circuit configuration. (b) Simplified CM equivalent circuit with the *LC* circuit configuration.

The designed CM choke has successfully confined the CM noise within EN55022 limit.

Although CM choke has simple construction, its large inductance requirement limits its usage in applications having volume constraints.

B. LC Filter

The use of *LC* filters in three-phase drives are widely explored in the literature. Extending the same design procedure to the BLdc drive operated with 120° conduction mode might mislead the design value. It also results in one of the winding of the CM choke/capacitor underutilized at any given point of time due to the assumption that the CM current through the floating phase is zero [13]. With the presented analysis in Sections II and III, it is clear that all the three phases contribute to CM currents, and

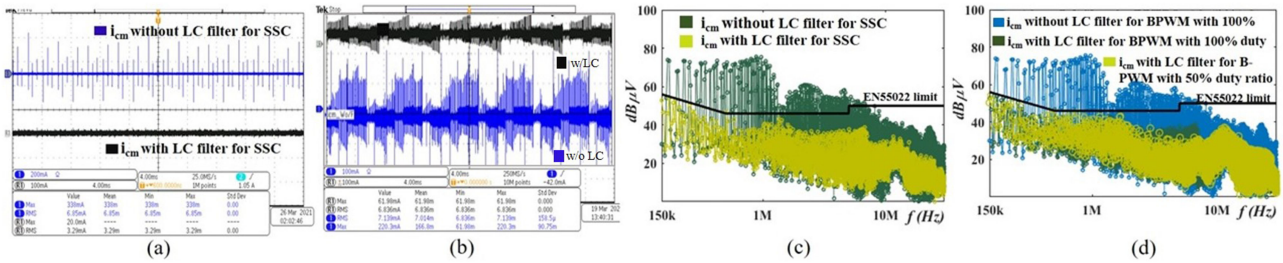

Fig. 12. Experimental results for SSC—dc voltage = 310 V, speed = 3500 r/min, and torque = 0.316 N·m, and for BPWM—dc voltage = 310 V, speed = 1860 r/min, torque = 0.28 N·m, and duty = 50%. (a) Time-domain profile of $i_{\text{cm\_BLdc}}$ without and with an *LC* filter for SSC. (b) Time-domain profile of $i_{\text{cm\_BLdc}}$ without and with an *LC* filter for BPWM with 50% duty ratio. (c) Frequency-domain profile without and with an *LC* filter for SSC. (d) Frequency-domain profile without an *LC* filter for BPWM with 100% duty ratio and with an *LC* filter for BPWM with 100% and 50% duty ratio.

therefore, the design procedure of the CM filter can be directly adapted from IM drives [22].

The connection and configuration of the *LC* filter are shown in Fig. 11(a), and a simplified single-phase CM equivalent circuit with an *LC* filter is shown in Fig. 11(b). Since $Z_{\text{CM\_}C}$ branch is capacitive, it offers less impedance to the noise compared with the combined impedances of the motor and LISN. Therefore, most of the $i_{\text{cm\_BLdc}}$ is diverted to the $Z_{\text{CM\_}C}$ branch, thereby, reducing the ground current through the motor.

1) Design of the LC Filter: The following guidelines are suggested for the design of the *LC* filter.

1) *Step 1*: The cut-off frequency (f_o) of the *LC* filter is calculated for the required attenuation (Attn_{reqcm}) as

$$f_o \leq \frac{f}{10^{(\text{Attn}_{\text{reqcm}}/40)}} \tag{23}$$

where f is the highest frequency component to be attenuated, i.e., $f = 160$ kHz.

2) *Step 2*: After calculating f_o, C_{cm} and L_{cm} are obtained as [22]

$$L_{\text{cm}} = \frac{1}{4\pi^2 f_o^2 (3C_{\text{cm}})}. \tag{24}$$

3) Step 3: The damping resistance, R_d, is chosen from the damping ratio, ζ, as [15]

$$R_d = 2\zeta \left(\sqrt{\frac{L_{\text{cm}}}{3C_{\text{cm}}}} \right). \tag{25}$$

For the required attenuation of 22.238 dB with SSC, the cut-off frequency, f_o, calculated using (23) is 44.48 kHz. The resultant filter parameters are $3C_{\text{cm}} = 4$ nF, L_{cm}= 3.2 mH, and $R_d = 75\ \Omega$. The measured i_{cm} profiles with and without the *LC* filter are presented in Fig. 12 . Following are some of the inferences.

1) The i_{cm} profiles with and without an *LC* filter for the SSC case are presented in Fig. 12(a). It can be seen from this figure that the peak of i_{cm} is reduced by 318 mA owing to the significant reduction in the CM noise.
2) The i_{cm} profiles with and without an *LC* filter for BPWM at 50% duty cycle case are presented in Fig. 12(b). In this case, it is observed that the i_{cm} peak has been reduced by 158 mA.
3) The frequency spectrum of i_{cm} is shown in Fig. 12(c) for the SSC case, and in Fig. 12(d) for BPWM with 50% and 100% duty ratios. The designed *LC* filter has successfully confined the CM noise within EN55022 limit.

V. Conclusion

Three-phase BLdc motors drives are becoming popular in high-voltage applications such as electric vehicles and solar water pumps. In this article, the propagation of the CM noise in the BLdc motor has been discussed with mathematical analysis and experimental validation. Two widely used modulation schemes for the BLdc motor are studied; SSC and BPWM. A DPI network is designed to emulate the motor phase-to-ground parasitic capacitances and provide insights on each phase-to-ground currents that contributes to the CM noise in the motor. From the analysis, a generalized CM equivalent circuit is proposed including all the three-phase-to-ground parasitic capacitances of the motor. The provided analysis clarifies the misconception of only two phases contributing to the CM current in the BLdc motor. Additionally, it is shown that the CM noise in the 120° modulation schemes is predominantly due to the floating phase of the motor, especially in high-voltage SiC-based BLdc drives. Finally, the design of the CM choke and *LC* filter (passive filter schemes) is presented to attenuate the CM noise in the BLdc motor drive.

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