# Analysis and Experimental Verification of an Isolated Half-Bridge Bidirectional DC−DC Converter

Matthias Schulz, *Member, IEEE*, and Stefan Ditze

***Abstract*—This article describes the analysis of a zero voltage switched isolated bidirectional half-bridge active-clamp current-fed push–pull converter for a power in the range of 1 kW. Combining the beneficial characteristics of active-clamping and advanced control scheme, this converter realizes soft-switching features for a hard-switching converter design. The technique utilizes the inductance and the clamp capacitor on the lower voltage (LV) side to create zero voltage switching conditions for the transistors on the higher voltage (HV) side. Additional overvoltage stress, voltage spikes, and reverse-recovery for the transistors on the LV side are reduced. By using the advanced control scheme, the effective turns ratio can be increased. The operating principles are analyzed in time-domain and validated by measurements.**

***Index Terms*—Bidirectional power conversion, dc–dc power converters, pulsewidth modulation, zero voltage switching (ZVS).**

## I. Introduction

In literature, several isolated bidirectional dc-dc topologies [1] have been proposed for applications like smart grids [2], automotive [3], [4], uninterruptible power supplies, or battery management [5], [6]. In addition, some well-known isolated unidirectional topologies (e.g., flyback) can be expanded to a bidirectional alternative with slight effort.

The flyback topology is mostly used as the dc-dc stage in low power switched-mode power supplies due to its galvanic isolation, simplicity, low number of components, wide voltage range, and cost-efficient assembly [7]. The output power can be increased up to the kW range using resonant und active-clamp circuits [8]–[11], but, in general, they are applied and optimized in unidirectional applications [12].

The *LLC* resonant converter is another well-established and proven topology in the group of isolated dc–dc converters for low and medium power. It can achieve high efficiency under nominal load due to the soft-switching capability of the higher voltage (HV) and lower voltage (LV) side power semiconductors [13], [14]. This topology operates with variable switching frequency $f_{\mathrm{sw}}$, and, therefore, designing an electromagnetic interference (EMI) input filter and finding an appropriate control structure over the full power range is challenging [15], [16]. This converter shows different transfer characteristics in forward and reverse directions, in which the *LLC* would no longer attain its soft-switching advantages [17]. An increased number of components is necessary to operate under soft-switching conditions in both directions of power flow [18].

Another prominent topology in the group of isolated bidirectional dc-dc converters is the dual active bridge (DAB) [3], [19]–[21]. With its simple structure, the DAB topology can achieve soft-switching on the HV and the LV sides, enabling converter designs with high efficiency and high power density. No additional reactive components are required if the transformer leakage inductance $L_{\mathrm{lk}}$ is advantageously utilized as the main energy transfer element. At part-load, however, soft-switching operation on HV and LV sides is limited to operating points close to unity voltage transfer ratio [21]. It also suffers from high reactive energy and increased turn-OFF power loss degrading the overall efficiency [3]. The voltage-fed dual active half-bridge (DAHB) [22] and the current-fed DAHB, depicted in Fig. 1 [23]–[27], offer a reduced number of power semiconductors compared to a DAB. The current-fed DAHB combines the properties of the voltage-fed DAHB (dashed outlined) and a nonisolated buck−boost topology, outlined with dash dot line. Soft-switching of the DAHB part can be ensured over a wider power range by controlling the voltage $V_{\mathrm{h}}$ via phase-shift $\varphi$. In step-down operation, $V_{\mathrm{h}}$ describes the input voltage for the buck−boost converter, which controls the voltage $V_{\mathrm{LV}}$ using the pulsewidth modulation further on. The conditions for zero voltage switching (ZVS) are shown in Fig. 1 based on $i_2$ and $i_{\mathrm{Lc}}$: at $t_0$, the current $i_2$ has to be negative, and at $t_1$, the characteristic point $I_{2,\mathrm{a}}$ has to be higher than $i_{\mathrm{Lc}}$ while $I_{2,\mathrm{b}}$ has to be positive and $I_{2,\mathrm{c}}$ should be less than $i_{\mathrm{Lc}}$ [28]. These advanced control schemes also reduce the reactive energy, but they are rather complex and the turn-OFF losses are not significantly lower [29], [30]. For both DAHB configurations, the current rating of the capacitors $C_3$ and $C_4$ are high for a low-voltage, high-current application up to 1 kW output power resulting in high component stress [22], [31].

In this article, we present the analysis of an active-clamped half-bridge current-fed push−pull (AC-HB-CF-PP) topology implementing a novel modulation scheme to achieve ZVS at the HV side transistors. Using a capacitive HB on the HV side, the stress on the primary of the transformer is reduced to half of HV side voltage. Furthermore, including a center-tapped

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Matthias Schulz is with the Department of Research in Energy and Electronics for Power Electronic Systems of Siemens, 91056 Erlangen, Germany (e-mail: schulzmatthias@siemens.com).

Stefan Ditze is with the Fraunhofer Institute for Integrated Systems and Device Technology IISB, 91058 Erlangen, Germany (e-mail: stefan.ditze@iisb.fraunhofer.de).

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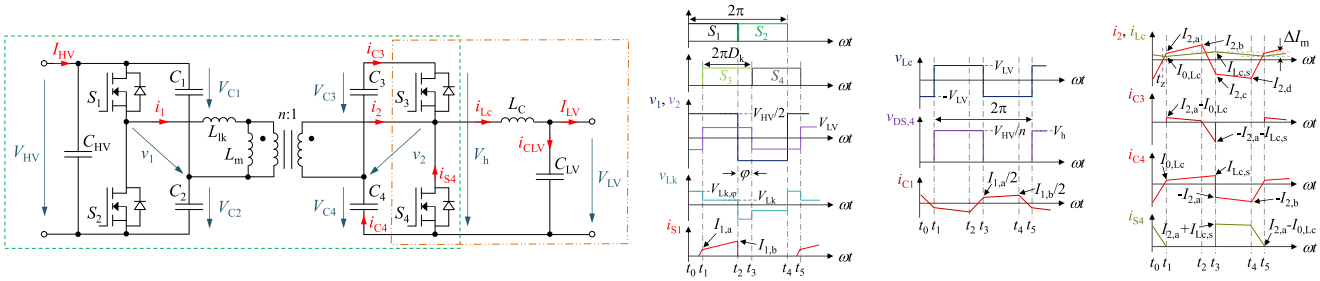

Fig. 1. Topology and waveforms of the dual active half-bridge in "voltage-fed–current-fed" configuration.

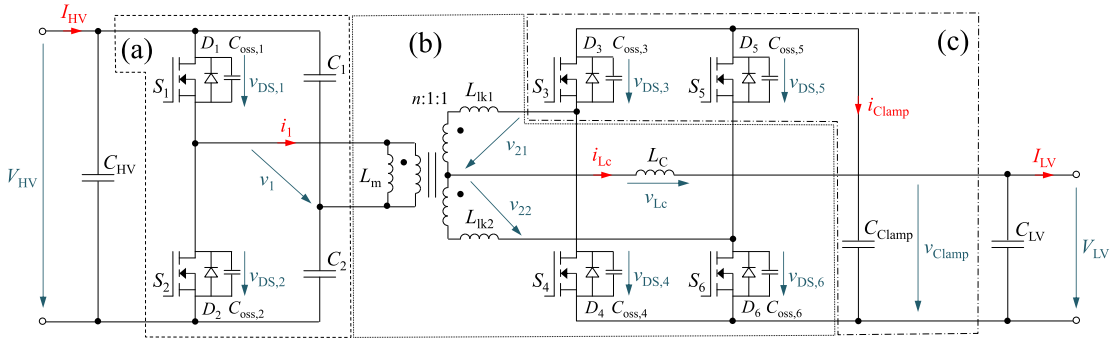


Fig. 2. Schematic of the half-bridge active-clamp current-fed push−pull converter. (a) HV side with capacitive half-bridge. (b) Center-tapped transformer with current-fed push−pull circuit. (c) Active-clamping circuit.

transformer, the passive components on the LV side can be designed volume optimized due to twice the switching frequency, which is seen by the components. Moreover, a low turns-ratio $n$ is favorable for a high-voltage, high-current converter regarding low winding losses. In order to reduce the LV side current ripple, an inductor $L_C$ is added in [32]. The novel modulation scheme described in this approach is based only on a duty cycle control $D_k$ instead of frequency modulation $f_{sw}$ and does not require phase shift modulation $\varphi$ to achieve soft-switching. As a result, the control parameters are reduced to one duty cycle, and, thus, one cascaded control structure is sufficient.

Based on the presentation of this topology in [33], in the following, we will complement the fundamental equations for the AC-HB-CF-PP topology in steady-state by a detailed analysis of the time-domain analytical equations for different time intervals in order to evaluate key current and voltage waveforms. The complex dependencies between the individual circuit components and control parameters to achieve ZVS on the HV side require a thorough and detailed analysis of these intervals. Taking into account the interaction with the existing parasitic components, a reliable and precise calculation of the design parameters for the AC circuit is made possible.

The operational principles for the AC-HB-CF-PP topology in steady-state are briefly recapped for step-down and step-up operation mode in Section II. A new modulation scheme enabling soft-switching of the HB transistors on the HV side in step-down operation mode is discussed and validated using a full order SPICE simulation model in Section III. In Section IV, the step-up operation mode is analyzed in detail, considering the effects described in Section III. In Section V, the proposed topology and the novel modulation scheme are experimentally verified using a 600 W lab prototype. Finally, Section VI concludes this article.

## II. Converter Topology and Operational Principle

The schematic of the proposed bidirectional AC-HB-CF-PP topology is shown in Fig. 2, which extends the bidirectional dc-dc converter presented by Xiao *et al.* [32] by a center-tapped transformer and a set of control parameters reduced to the duty cycle in cascaded control structure. This dc-dc converter combines an HB on the HV side (a) and a CF-PP circuit on the LV side (b), which are typically used as standalone versions in literature [34], [35]. The transistors $S_3$ and $S_5$ and the clamp capacitor $C_{Clamp}$ constitute the AC circuit [cf., area (c) in Fig. 2] [36]. The AC-HB-CF-PP topology has a certain similarity to the CF DAHB. In [37], the schematic of the AC-HB-CF-PP without the choke $L_C$ is shown and operated like the voltage-fed DAHB using phase-shift $\varphi$ modulation. Applying the novel modulation scheme, ZVS will be achieved by the pulsewidth modulation instead of phase shift modulation. Additionally, the inductance $L_C$ is used for achieving ZVS instead of the leakage inductance $L_{lk}$.

For the steady-state step-down and step-up analysis, the following assumptions are made.

1) All semiconductor switches and diodes exhibit ideal switching behavior.
2) Conduction resistances $R_{par}$ are implemented.
3) The transformer leakage inductances $L_{lk1}$ and $L_{lk2}$ are considered.

4) Magnetizing inductance $L_{\mathrm{m}}$ is infinite.
5) The parasitic capacitances $C_{\mathrm{oss},3}$, $C_{\mathrm{oss},4}$, $C_{\mathrm{oss},5}$, and $C_{\mathrm{oss},6}$ on the LV side are equal and named $C_{\mathrm{oss,LV}}$.
6) The parasitic capacitances $C_{\mathrm{oss},1}$ and $C_{\mathrm{oss},2}$ on the HV side are equal and denoted as $C_{\mathrm{oss,HV}}$.
7) The capacitances $C_{\mathrm{HV}}$, $C_1$, $C_2$, and $C_{\mathrm{LV}}$ are large and thus constant dc voltages $V_{\mathrm{HV}}$ and $V_{\mathrm{LV}}$ are assumed.

The nonlinear behavior of semiconductor capacitances is approximated by an equivalent time-dependent linear capacitance according to [38] for the analysis of ZVS processes. For this purpose, the capacitance–voltage characteristic is extracted from the datasheet of the transistor and the equivalent capacitance is calculated as a function of the applied reverse voltage [38].

### A. Traditional Step-Down Operation Mode

Generally, in step-down mode, the converter transfers power from the HV to the LV side. The HB switches $S_1$ and $S_2$ are controlled by the same duty cycle $D_{\mathrm{k}}$, which is shifted by half a period and the transistors $S_4$ and $S_6$ are used for active rectification. A comprehensive steady-state analysis of continuous conduction mode (CCM) as well as discontinuous conduction mode (DCM) based on the traditional step-down operation can be found in [33] and [39].

### B. Implemented Step-Up Operation Mode

Accordingly, the step-up mode is defined as power flow from the LV to the HV side, and, thus, the four currents $I_{\mathrm{HV}}$, $i_1$, $i_{\mathrm{Lc}}$, and $I_{\mathrm{LV}}$ marked in Fig. 2 change to a negative sign due to reversal of the power flow direction. In the step-up mode, the switches $S_4$ and $S_6$ of the PP circuit are responsible for the power transfer and the intrinsic diodes $D_1$ and $D_2$, respectively; in case of active rectification, $S_1$ and $S_2$ rectify the current $i_1$. In summary, the proposed topology implemented with a traditional modulation scheme exhibits equations similar to buck and boost converters [40].

### C. System Specification

For the analysis performed in the following, the proposed AC-HB-CF-PP topology is used as a galvanically isolated bidirectional converter between a 380 V and a 24 V bus, which represents the nominal operating point. The system specification and the varied design parameters are listed in Table I and are used in the analysis, in the SPICE simulation, and in the validation using measurements.

TABLE I
PARAMETERS OF SPICE SIMULATIONS

| Parameters | Symbol | Value |
|---|---|---|
| Nominal higher voltage | $V_{\mathrm{HV}}$ | 380 V |
| Nominal lower voltage | $V_{\mathrm{LV}}$ | 24 V |
| Nominal power | $P_{\mathrm{n}}$ | 600 W |
| Choke inductance | $L_{\mathrm{C}}$ | 2.2 µH |
| Half Bridge capacitances | $C_1$, $C_2$ | 10 µF |
| Clamp capacitance | $C_{\mathrm{Clamp}}$ | 4 µF |
| Switching frequency | $f_{\mathrm{sw}}$ | 100 kHz |
| Magnetizing inductance | $L_{\mathrm{m}}$ | 2.3 mH |
| Leakage inductance | $L_{\mathrm{lk1}}$, $L_{\mathrm{lk2}}$ | 16.3 nH |
| Drain-to-source capacitance $V_{\mathrm{HV}}$ | $C_{\mathrm{oss,HV}}$ | 0.1…3 nF |
| Drain-to-source capacitance $V_{\mathrm{LV}}$ | $C_{\mathrm{oss,LV}}$ | 2 nF |
| HV side parasitic resistance | $R_{\mathrm{par},1}$, $R_{\mathrm{par},2}$ | 80 mΩ |
| LV side parasitic resistances | $R_{\mathrm{par},3}$, $R_{\mathrm{par},4}$, $R_{\mathrm{par},5}$, $R_{\mathrm{par},6}$ | 5 mΩ |
| Turns ratio | $n$ | 7 |

## III. Novel Modulation Scheme to Achieve ZVS on the HV Side

In the following, the operational principle will be supplemented by an analytical investigation. According to [33] and [39], the operational principle of the AC-HB-CF-PP converter depends on the transistors parasitic capacitances $C_{\mathrm{oss}}$, the turns-ratio $n$, the choke inductance $L_{\mathrm{C}}$, output capacitors, and the momentary output power. In this section, in the first considered interval, the minimum dead-time to achieve ZVS on HV side is calculated using the progression of $v_{\mathrm{DS},1}$ and $v_{\mathrm{DS},2}$. In the second step, the influence of all relevant parasitic components on converter behavior is analyzed and the effect on achieving ZVS is investigated. Finally, the initial assumption of a constant voltage across the clamp capacitor during operation is verified. Additionally, in the following intervals, the behavior and the stress of the AC circuit is analyzed.

The key waveforms in step-down operation mode showing the principles of the novel modulation scheme are depicted in Fig. 3 and divided into eight intervals. A comparison with the waveforms of the CF DAHB in Fig. 1 shows visibly and distinctly differences. In the following, only the first four, $1_{\mathrm{a}}$–$4_{\mathrm{a}}$, and the transitions between them will be discussed in detail due to symmetry. All changes in the voltage and current waveforms depicted in Fig. 3 and for step-up mode in Fig. 18 are discussed using the corresponding equations and validated by SPICE simulation. The equations are ordered in the same sequence as the intervals appear in Figs. 3 and 18. The analysis of every interval begins always with the drain-to-source voltage $v_{\mathrm{DS},1}$ and concludes with the current through the transformer $i_1$ will be investigated. The influence of changing circuit parameters is discussed with the derived equations and illustrated using parameter plots and key waveforms are calculated in time-domain at different power levels. Various values of the output capacitance $C_{\mathrm{oss,HV}}$ are assumed for the HV side transistors. The effect on converter operation is shown in the following figures to validate the derived equations and to confirm the validity of the calculations.

The corresponding current paths of each interval are depicted in Fig. 4. In the following, additional equivalent circuits are used to derive the time-dependent equations, which will be validated with a full order SPICE model of the AC-HB-CF-PP topology. Parameters on the LV side, which are transferred to the HV side of the transformer during calculation, are denoted by the superscript " $'$ " .

As shown in Fig. 3, the volt-seconds applied to the choke $L_{\mathrm{C}}$ over one-half of a switching period in the advanced modulation scheme must be zero in steady-state. Therefore, the duty cycle $D_{\mathrm{Clamp}}$ of the clamping transistors $S_3$, respectively, $S_5$ is defined accordingly as

$$D_{\mathrm{Clamp}} = \frac{n\,V_{\mathrm{LV}}}{V_{\mathrm{HV}}}. \tag{1}$$

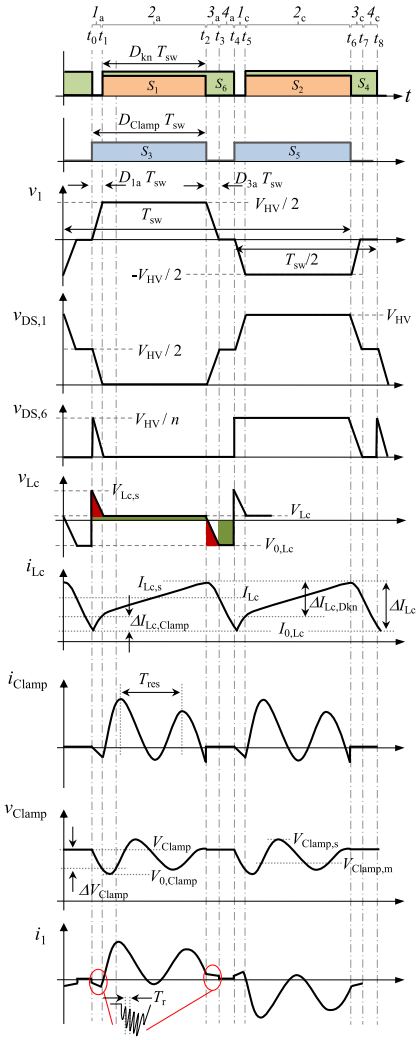


Fig. 3. Theoretical waveforms for the operation mode achieving soft-switching of transistors $S_1$ and $S_2$ in step-down direction.

Also, the dc offset $I_{0,\mathrm{Lc}}$ can be derived based on Fig. 3

$$I_{0,Lc} = \frac{P_{\mathrm{LV}}}{V_{\mathrm{LV}}} - \frac{V_{\mathrm{LV}}\ (0.5 - D_{\mathrm{Clamp}})}{2\ L_C\ f_{\mathrm{sw}}}. \tag{2}$$

### A. *Interval $1_a$ of Zero Voltage Switching* ($t_0 \ldots t_1$)

Turning ON $S_3$ applies the voltage $V_{\mathrm{Clamp}}$ to the center-tap of the transformer LV sides. $V_{\mathrm{Clamp}}$ can be calculated as

$$V_{\mathrm{Clamp}} = \frac{V_{\mathrm{HV}}}{n}. \tag{3}$$

Across the inductor $L_{\mathrm{C}}$, the difference between $V_{\mathrm{Clamp}}$ and $V_{\mathrm{LV}}$ can be measured as $v_{\mathrm{Lc}}$. Due to this voltage increase, the current $i_{\mathrm{Lc}}$ shows a higher slope in interval $1_{\mathrm{a}}$ compared to subsequent ones. By switching $V_{\mathrm{Clamp}}$ hard to the center-tap, the condition of conducting $D_4$ or $D_6$ is not maintained. Transistors $S_4$ and $S_6$ take the full blocking voltage $V_{\mathrm{Clamp}}$ in this interval, whereby $v_{\mathrm{DS},4}$ is constant and $v_{\mathrm{DS},6}$ decreases to zero by the end of $1_{\mathrm{a}}$.

TABLE II
INTERVAL $1_{\mathrm{A}}$: START AND END CONDITIONS

| | $v_{\mathrm{DS},1}$ | $v_{\mathrm{DS},2}$ | $v_{\mathrm{DS},5}$ | $v_{\mathrm{DS},6}$ | $v_1$ |
|---|---|---|---|---|---|
| **start (0)** | $V_{\mathrm{HV}}/2$ | $V_{\mathrm{HV}}/2$ | 0 | $V_{\mathrm{Clamp}}$ | 0 |
| **end (1)** | 0 | $V_{\mathrm{HV}}$ | $V_{\mathrm{Clamp}}$ | 0 | $V_{\mathrm{HV}}/2$ |

According to Fig. 4(a), the current $i_{\mathrm{Clamp}}$ comprises two partial currents and the circuit can be simplified to the subcircuits in Fig. 5 with corresponding start and end conditions summarized in Table II. The parasitic resistance $R_{\mathrm{par},3}$ is included and the leakage inductances $L_{\mathrm{lk1}}$ and $L_{\mathrm{lk2}}$ are transferred to the HV side of the transformer and combined to $L_{\mathrm{lk}}$. The capacitance $C_{\mathrm{Clamp}}$ is large, and, thus, a constant dc voltage $V_{\mathrm{Clamp}}$ is assumed.

In Fig. 5(a), the current path to supply the LV side and to discharge $C_{\mathrm{oss},1}$ is depicted. The current $i_{\mathrm{Lc}}$ enables ZVS of transistor $S_1$ at the end of $1_{\mathrm{a}}$ and the following equations can be derived from Fig. 5(a):

$$C_{\mathrm{oss,HV}} \frac{\mathrm{d}v_{\mathrm{DS,S2}}}{\mathrm{d}t} = \frac{i_1}{2} = \frac{i_{Lc}}{2\ n} \tag{4}$$

$$v_1 + V_{\mathrm{C2}} - v_{\mathrm{DS},2} = 0 \tag{5}$$

$$L_C \frac{\mathrm{d}i_{Lc}}{\mathrm{d}t} + v_{21} + V_{\mathrm{LV}} - V_{\mathrm{Clamp}} = 0 \tag{6}$$

whereby $v_{21}$ is equal to $v_1/n$ and $V_{\mathrm{C2}}$ is equal to $V_{\mathrm{HV}}/2$.

Starting the analysis at the drain-to-source voltage $v_{\mathrm{DS},1}$ of Fig. 3, to achieve ZVS at the end of the interval $1_{\mathrm{a}}$, this voltage must be zero at time instant $t_1$, while at the same time, $v_{\mathrm{DS},2}$ is equal to $V_{\mathrm{HV}}$. Using (4)–(6) and the start conditions $v_{\mathrm{DS},2}(0)$ and $i_{0,\mathrm{Lc}}$, $v_{\mathrm{DS},2}(t_0 \ldots t_1)$ can be expressed as

$$v_{\mathrm{DS},2}(t) = \sqrt{x_1} I_{0,\mathrm{Lc}} \sin(\omega\ t) + x_2 \cos(\omega\ t) + x_3$$
$$\text{for} \quad \frac{V_{\mathrm{HV}}}{2} \le v_{\mathrm{DS},2} \le V_{\mathrm{HV}} \tag{7}$$

where

$$x_1 = \sqrt{\frac{L_C}{2\ C_{\mathrm{oss,HV}}}} \tag{8}$$

$$\omega = \frac{1}{\sqrt{2\ L_C\ C_{\mathrm{oss,HV}}}\ n} \tag{9}$$

$$x_2 = n\ (V_{\mathrm{LV}} - V_{\mathrm{Clamp}}) \tag{10}$$

$$x_3 = n\ (V_{\mathrm{Clamp}} - V_{\mathrm{LV}}) + V_{\mathrm{C2}}. \tag{11}$$

The slope expressed in (7) is also valid for $v_{\mathrm{DS},1}$, which decreases to zero until the end of interval $1_{\mathrm{a}}$. The voltage $v_{\mathrm{DS},1}$ can be used to calculate the duty cycle $D_{1\mathrm{a}}$ by determining the zero-crossing

$$v_{\mathrm{DS},1}(D_{1a}T_{\mathrm{sw}}) = -\sqrt{(x_1\ i_{0,\mathrm{Lc}})^2 + {x_2}^2}$$
$$\sin\left(\omega\ D_{1a}T_{\mathrm{sw}} + \tan^{-1}\left(\frac{x_2}{x_1\ i_{0,\mathrm{Lc}}}\right)\right) - x_3 + V_{\mathrm{HV}} = 0$$
$$\text{for} \ \frac{V_{\mathrm{HV}}}{2} \ge v_{\mathrm{DS},1} \ge 0\ \mathrm{V}. \tag{12}$$

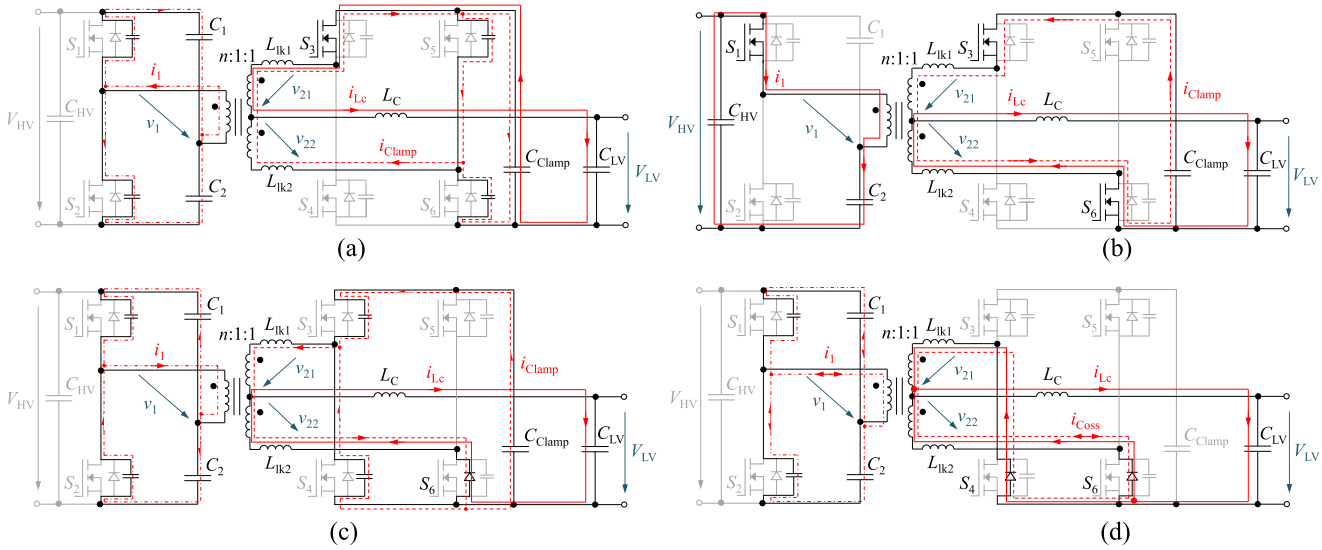


Fig. 4. Equivalent circuits of each operational mode by implemented advanced modulation scheme in the AC-HB-CF-PP converter. (a) $1_a$. (b) $2_a$. (c) $3_a$. (d) $4_a$.

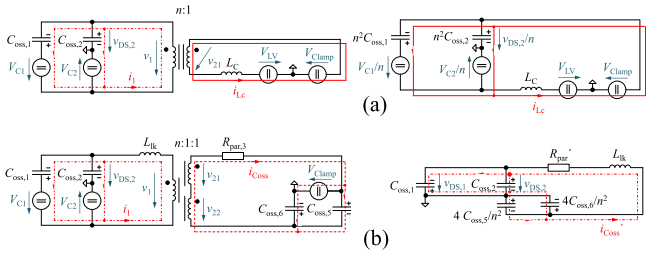


Fig. 5. Equivalent subcircuits of interval $1_a$. (a) $i_{Lc}$ current path and impact on the transformer primary as well as the secondary transferred schematic. (b) Flow of parasitic capacitor charge through the converter, completed by transferred schematic.

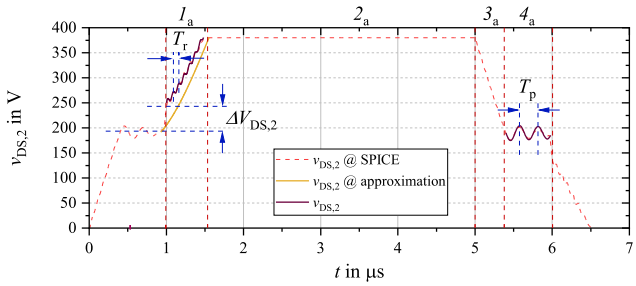


Fig. 7. Drain-to-source voltage $v_{DS,2}$ including LV side parasitic capacitances $C_{oss,LV}$ of 2 nF. Due to $C_{oss,LV}$, the voltage $v_{DS,2}$ jumps at $t_0$ about $\Delta V_{DS,2}$ and the period time of $T_r$ is 70.4 ns; the operating point is at $P_{LV}$ of 230 W.

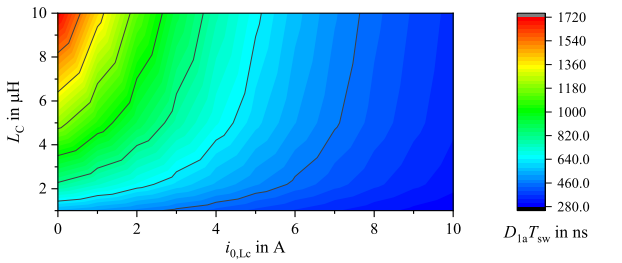


Fig. 6. Parasitic capacitance $C_{oss,HV}$ is set to 1.4 nF in this example; thereby, a minimum of 280 ns has to be considered to achieve soft-switching at full load. With decreasing $p_{LV}$, the dead-time $D_{1a}T_{sw}$ increases and a higher inductance $L_C$ reduces the current ripple $\Delta I_{Lc}$ and increases the dead-time for achieving ZVS especially in the area of low $p_{LV}$.

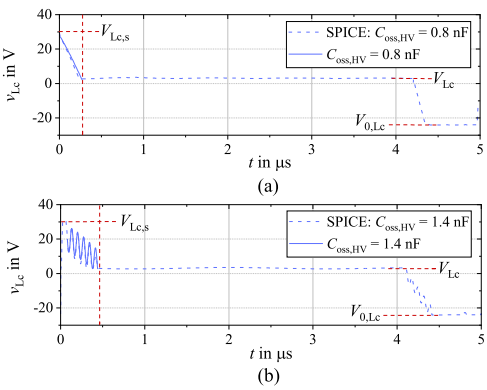


Fig. 8. Calculation and simulation of the voltage across the inductor $v_{Lc}$; the output power on LV side is chosen to 250 W. (a) Neglecting the LV side parasitic capacitances $C_{oss,LV}$. (b) LV side parasitic capacitances $C_{oss,LV}$ of 2 nF are added to the transistors S3-S6, so additional to (25) also (26) is valid.

The condition for achieving soft-switching (12) assumes the nominal voltage values $V_{HV}$, $V_{Clamp}$, and $V_{LV}$. The length of interval $1_a$ represented by $D_{1a}T_{sw}$ depends on the parasitic capacitance $C_{oss,HV}$, which is set to 1.4 nF in Fig. 6, the inductance $L_C$, and the momentary output power $p_{LV}$ in the form of $i_{0,Lc}$. To achieve soft-switching for the HV side transistors, the dead-time has to be considered before the channel can be turn-ON at 0 V.

Fig. 6 shows larger differences in the dead-time over the inductance range at lower power, with increasing power the values equalize. With decreasing $p_{LV}$, the length $D_{1a}T_{sw}$ increases, but the absolute length although depends on the chosen inductance

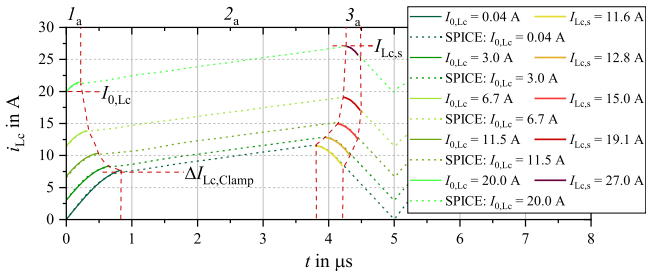


Fig. 9. Inductor current waveforms for $C_{\mathrm{oss,HV}}$ of 1.8 nF at increasing output power $p_{\mathrm{LV}}$. $C_{\mathrm{oss,LV}}$ capacitors are neglected, $V_{\mathrm{Clamp}}$ is averaged to 52 V, and as already mentioned in Fig. 6, how the length of interval $1_{\mathrm{a}}$ and $3_{\mathrm{a}}$ decreases with higher output power is presented.

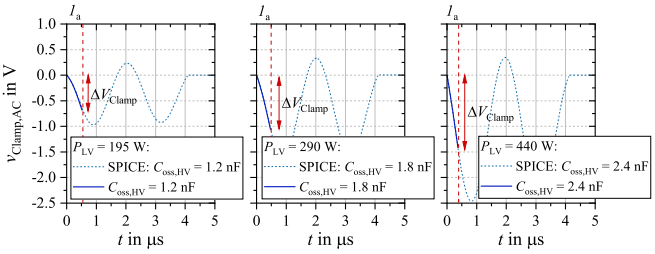


Fig. 10. Simulated waveforms of $v_{\mathrm{Clamp}}$ in AC depiction and calculated slope $\Delta V_{\mathrm{Clamp}}$ for different $C_{\mathrm{oss,HV}}$ and increasing output power; all parasitic $C_{\mathrm{oss,LV}}$ are neglected.

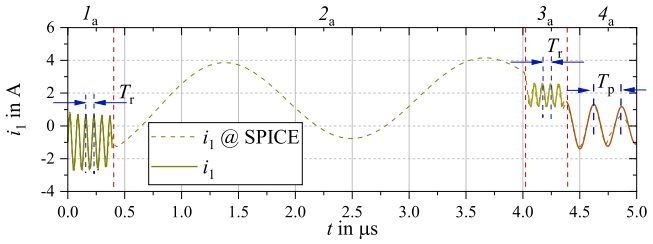


Fig. 11. Simulation result of $i_1$ at 250 W output power $P_{\mathrm{LV}}$; $T_{\mathrm{r}}$ is measured to 70.3 ns and calculated with (22) to 70.5 ns; the parasitic oscillation is superposed on the transformed current $i_{\mathrm{Lc}}$ in $1_{\mathrm{a}}$. The period time $T_{\mathrm{p}}$ in simulation is 235 ns and calculated by (71) to 238 ns in $4_{\mathrm{a}}$.

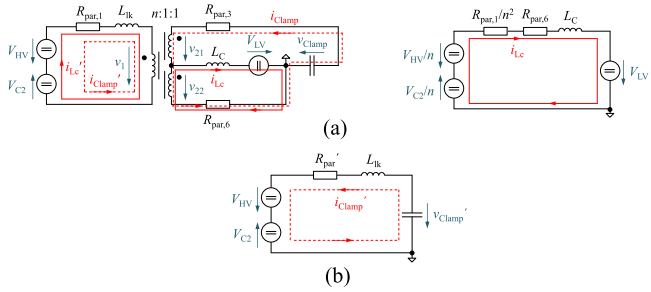


Fig. 12. Schematic diagrams of interval $2_{\mathrm{a}}$. (a) Energy transfer from the HV to the LV bus. (b) Resonance between leakage inductance and clamp capacitor.

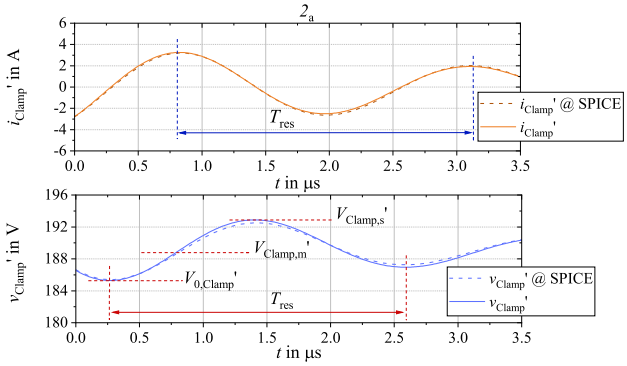


Fig. 13. Waveforms of $i_{\mathrm{Clamp}}'$ and $v_{\mathrm{Clamp}}'$ of SPICE simulation and calculation. $v_{\mathrm{Clamp}}'(0)$ is 187.2 V, $i_{\mathrm{Clamp}}'(0)$ is $-2.8$ A, $T_{\mathrm{res}}$ can be calculated with (45) and measured to 2.3 $\mu$s, and the choke current $i_{\mathrm{Lc}}$ is neglected.

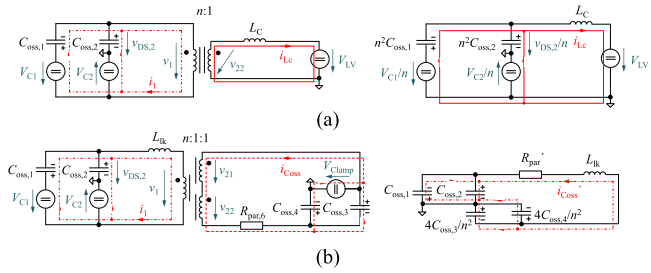


Fig. 14. Subcircuits in transferred schematic of the first interval $3_{\mathrm{a}}$ of inductor demagnetization. (a) Current path to the lower voltage side. (b) Oscillation path recharging the parasitic capacitances.

$L_{\mathrm{C}}$. As a result, a higher $L_{\mathrm{C}}$ reduces the current ripple $\Delta I_{\mathrm{Lc}}$ but expands the length of interval $1_{\mathrm{a}}$.

Due to the sudden charging of the parasitic capacitance $C_{\mathrm{oss},6}$ at $t_0$ in Fig. 3, the drain-to-source voltage $v_{\mathrm{DS},6}$ peak occurs. The amplitude is twice of the maximum voltage on the transformer LV side $v_{21}$, which can be expressed as

$$V_{21,\mathrm{s}} = V_{22,\mathrm{s}} = \frac{V_{\mathrm{HV}}}{2\,n}. \tag{13}$$

Being transferred to the HV side, this voltage causes a voltage drop at transistor $S_1$ and a voltage step $\Delta V_{\mathrm{DS},2}$ at transistor $S_2$, which can be calculated as

$$V_{\mathrm{DS},2} = \frac{n\,V_{21,\mathrm{s}}}{4} \tag{14}$$

and seen in Fig. 7. After this voltage step, the slope of the waveform is the same as that calculated by (7), which is based on the subcircuit in Fig. 5(a). Only the start condition is not $V_{\mathrm{HV}}/2$, and $\Delta V_{\mathrm{DS},2}$ has to be added. The parasitic oscillation $v_{\mathrm{DS},2,\mathrm{AC}}$ can be derived by the equivalent subcircuit in Fig. 5(b). In (7), $v_{\mathrm{DS},2,\mathrm{AC}}$ is neglected but shown in Fig. 7 as high frequency part and can be expressed by

$$v_{\mathrm{DS},2,\mathrm{AC}}(t) = -\frac{1}{4}c\,\mathrm{e}^{-\alpha t} \left( \frac{i_{C\mathrm{oss}}'(0)\;L_{\mathrm{lk}} + v_{\mathrm{DS},2}(0)\;C_{\mathrm{oss}}'\,R_{\mathrm{par}}'}{2\,C_{\mathrm{oss}}'\,L_{\mathrm{lk}}\,\omega_e} \sin(\omega_e t) + v_{\mathrm{DS},2}(0)\cos(\omega_e t) \right) \tag{15}$$

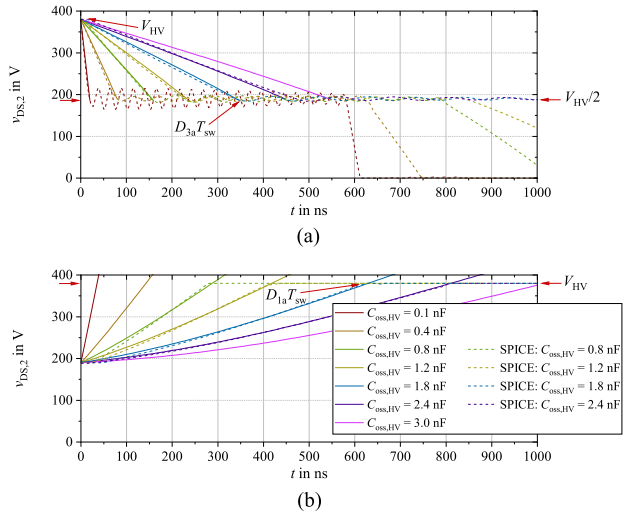


Fig. 15. Comparison between calculated $v_{DS,2}$ and SPICE simulation for different $C_{oss,HV}$ at an output power of 250 W. (a) Interval $3_a$: the maximum choke current $I_{Lc,s}$ is nearly 13.4 A, $V_{Clamp}$ is 54.2 V; at the assigned horizontal line, $v_{DS,2}(t)$ reaches $V_{HV}/2$. (b) Interval $1_a$ is significantly longer, whereby $I_{0,Lc}$ is between 3.6 and 7.5 A.

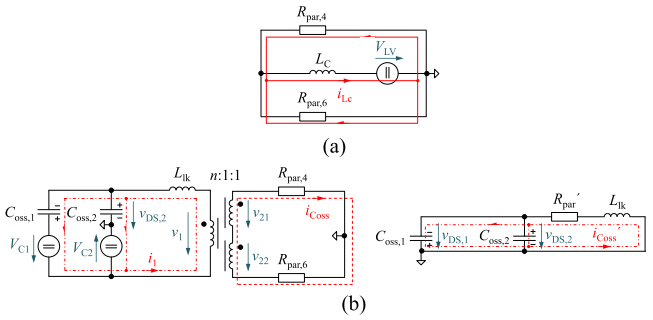


Fig. 16. Subcircuits of interval $4_a$. (a) Output circuit of the inductor current $i_{Lc}$ with freewheeling path through $D_4$ and $D_6$. (b) Equivalent circuit of the additional parasitic oscillation $i_{Coss}$ transferred to the higher voltage side.

whereby the constant factor $c$ represents the voltage across the HV side capacitors in the series connection of the subcircuit and is defined as

$$c = \frac{4\, C_{oss,LV}}{C_{oss,HV}\, n^2}. \tag{16}$$

The damping part $\alpha$ and the resonance frequency $\omega_e$ are given by

$$\alpha = \frac{R_{par}'}{2\, L_{lk}} \tag{17}$$

$$\omega_e = \sqrt{\omega_0{}^2 - \alpha^2}. \tag{18}$$

The parasitic resistance can be transferred to $R_{par}'$ as

$$R_{par}' = \frac{n^2}{4} R_{par,3}. \tag{19}$$

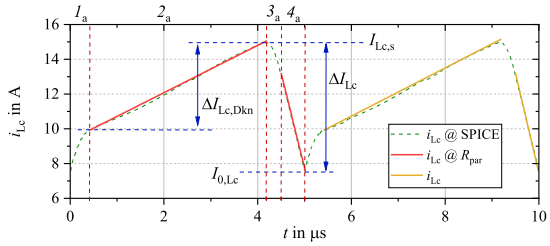


Fig. 17. Time-dependent waveform of $i_{Lc}$ as simulated dotted curve as well as calculated for $2_a$ and $4_a$ by (37) and (67) including $R_{par}$ and simplified according to (38) as well as (68) and marked with $i_{Lc}$ for an output power of 250 W. All parasitic elements like $L_{lk}$, $C_{oss}$, and $R_{par}$ are implemented in the simulation model. $\Delta I_{Lc}$ is measured in SPICE to 7.1 A and calculated by (68) to 6.6 A.

The ideal resonance $\omega_0$, which is valid without damping elements, can be calculated in interval $1_a$ as

$$\omega_0 = \frac{1}{\sqrt{L_{lk}\, C_{oss}'}}. \tag{20}$$

The transferred parasitic capacitance $C_{oss}'$ can be written by

$$C_{oss}' = \frac{1}{\frac{n^2}{8\, C_{oss,LV}} + \frac{1}{2\, C_{oss,HV}}}. \tag{21}$$

In combination with $L_{lk}$, the period $T_r$ is defined as follows:

$$T_r = 2\pi \sqrt{L_{lk}\, C_{oss}'}. \tag{22}$$

In Fig. 7, the approximation of $v_{DS,2}$ as well as the waveform resulting from adding the parasitic capacitances $C_{oss,LV}$ is depicted. Both progressions reach the same end condition and length of interval $1_a$. As a result, the calculated $\Delta V_{DS,2}$ of 47.5 V and the simulated one are also in good agreement, and the voltage step is independent of the parasitic elements.

The slope of the drain-to-source voltage $v_{DS,2}$ in (7) can be transferred to the voltage across the choke $v_{Lc}$. The peak voltage $V_{Lc,s}$ can be calculated as

$$V_{Lc,s} = \frac{V_{HV}}{n} - V_{LV}. \tag{23}$$

The peak voltage $V_{Lc,s}$ at the beginning of interval $1_a$ is independent of parasitic capacitances, as shown in Fig. 8. The voltage at $t_1$ is named $V_{Lc}$ and can be expressed as

$$V_{Lc} = \frac{V_{HV}}{2\, n} - V_{LV}. \tag{24}$$

Therefore, the time-dependent slope $v_{Lc}(t_0 \ldots t_1)$ including voltage $V_{Lc}$ is

$$v_{Lc}(t) = \frac{V_{HV} - v_{DS,2}(t)}{n} + V_{Lc}. \tag{25}$$

The same high-frequency oscillation as well as at $v_{DS,1}$ and $v_{DS,2}$ can be observed at $v_{Lc}$, which is shown in Fig. 8(b). Therefore, the following correlation is evaluated:

$$v_{Lc,AC}(t) = \frac{1}{n}\, v_{DS,2,AC}(t). \tag{26}$$

In Fig. 8(b), the slope of (25) is added with the AC part $v_{Lc,AC}$ mentioned in (26). Subsequently, the LV side parasitic

capacitances are not relevant for the energy transfer in this interval $1_a$ and, therefore, the length of the interval depends on $C_{\mathrm{oss,HV}}$.

The voltage across the choke $v_{\mathrm{Lc}}$ has an impact on the slope in interval $1_a$ for the inductor current $i_{\mathrm{Lc}}$. As depicted next in Fig. 3, it can be calculated from Fig. 5(a) and written by

$$i_{Lc}(t) = \sqrt{\frac{2\,C_{\mathrm{oss,HV}}}{L_C}}\; n\;(V_{\mathrm{Clamp}} - V_{\mathrm{LV}})\sin(\omega\, t) + i_{0,Lc}\cos(\omega\, t). \tag{27}$$

Here, $i_{0,\mathrm{Lc}}$ represents the start value of $i_{\mathrm{Lc}}$, which is rising with increasing output power on LV side and can be calculated with (2) depicted in Fig. 9. The shown difference of the inductor current $\Delta I_{\mathrm{Lc,Clamp}}$ depends also on the momentary power $p_{\mathrm{LV}}$ and can be expressed as

$$\Delta I_{Lc,\mathrm{Clamp}} = i_{Lc}(t_1) - I_{0,Lc}. \tag{28}$$

During interval $1_a$, the clamp capacitor $C_{\mathrm{Clamp}}$ is discharged to supply the LV side load and to achieve soft-switching on the HV side. In order to clamp the drain-to-source voltages and to verify the assumption of a constant dc value $V_{\mathrm{Clamp}}$, a detailed consideration of the slope $\Delta V_{\mathrm{Clamp}}$ is to be considered in addition to (4)−(6)

$$i_{Lc}(t_0 \ldots t_1) = C_{\mathrm{Clamp}}\frac{\mathrm{d}v_{\mathrm{Clamp}}}{\mathrm{d}t}. \tag{29}$$

The resulting second-order differential equation has the form

$$v_{\mathrm{Clamp}}(t_0 \ldots t_1) = a\,\sinh(xt) - b\cosh(xt) + c \text{ with } a,\ b, c\,\epsilon\, R. \tag{30}$$

Fig. 10 shows the AC part of the clamp capacitor voltage $v_{\mathrm{Clamp}}$ as a simulated waveform as well as calculated. The voltage drop $\Delta V_{\mathrm{Clamp}}$ is marked and typically in the range of Volts. Nonidentical operating points show that $\Delta V_{\mathrm{Clamp}}$ increases with rising output power despite the higher $C_{\mathrm{oss,HV}}$.

For the traditional and the novel modulation scheme, (31) is applied for sizing the minimum value of $C_{\mathrm{Clamp}}$, which is derived using an energy balance

$$C_{\mathrm{Clamp}} = \frac{2\,L_C\,{I_{\mathrm{LV}}}^2}{\left(V_{\mathrm{BR,DSS,LV}} - \frac{V_{\mathrm{HV}}}{n}\right)^2} \tag{31}$$

with $V_{\mathrm{BR,DSS,LV}}$ being the drain-to-source breakdown voltage of LV side transistors. Using the traditional modulation scheme, the rms value of $i_{\mathrm{Clamp}}$ depends only on the resonance between $C_{\mathrm{Clamp}}$ and $L_{\mathrm{lk}}$. Using the novel modulation scheme, $i_{\mathrm{Clamp}}$ is equal to $i_{\mathrm{Lc}}$ in interval $1_a$ and behaves like the traditional modulation scheme in interval $2_a$. In consequence, the rms value is higher now, but, in general, both modulation schemes show the same behavior. Increasing $C_{\mathrm{Clamp}}$ more than the calculated minimum value of (31), the rms values of $i_{\mathrm{Clamp}}$ as well as $i_1$ are getting lower. In this article, the minimum value of $C_{\mathrm{Clamp}}$ is implemented and stated in Table I.

In Fig. 3, the HV side current through the transformer $i_1$ is depicted and superposed by a parasitic oscillation in interval $1_a$. From Fig. 5(b), the parasitic current, which is transferred on the HV side $i_1(t_0 \ldots t_1)$, can be derived as

$$i_1(t) = \frac{i_{Lc}(t)}{n}. \tag{32}$$

The resistance $R_{\mathrm{par}}{}'$, inductor $L_{\mathrm{lk}}$, and capacitor $C_{\mathrm{oss}}{}'$ in series are the reasons for the following form of $i_1$ in interval $1_a$:

$$i_1(t) = -\frac{I_{0,Lc}}{n} + \frac{I_{\mathrm{LV}}}{n}\,\mathrm{e}^{-\alpha t}\sin(\omega_{\mathrm{e}}\, t) \tag{33}$$

whereby $\alpha$ can be calculated by (17) and $\omega_{\mathrm{e}}$ by (18).

Fig. 11 shows the simulation result of $i_1$. Based on (33), $i_1(t_0 \ldots t_1)$ is calculated, and the period $T_{\mathrm{r}}$ is derived using (22). On HV side between $t_0 \ldots t_1$, no energy will be transferred to the LV side. The parasitic capacitance $C_{\mathrm{oss},1}$ will be discharged, what is superposed by a resonance oscillation caused by $C_{\mathrm{oss,LV}}$.

### B. Active-Clamp Mode $2_a$ ($t_1 \ldots t_2$)

The channels of both transistors $S_1$ and $S_6$ are switched ON under ZVS condition at $t_1$. Switching losses occur if $S_1$ is turning ON before $t_1$. Turning ON $S_1$ at a time after $t_1$, higher peak currents in $2_a$ occur, but all drain-to-source voltages are clamped, which can be observed in Fig. 3. The resulting two independent current paths $i_{\mathrm{Clamp}}$ and $i_{\mathrm{Lc}}$ on LV side are depicted in Fig. 4(b) and can be divided into the subcircuits in Fig. 12.

From Fig. 12, the following three equations can be determined:

$$\frac{\mathrm{d}i_1}{\mathrm{d}t} = \frac{V_{\mathrm{HV}} - V_{\mathrm{C2}} - v_1 - R_{\mathrm{par},1}\,i_1}{L_{\mathrm{lk}}} \tag{34}$$

$$\frac{\mathrm{d}i_{Lc}}{\mathrm{d}t} = \frac{v_{22} - V_{\mathrm{LV}} - R_{\mathrm{par},6}\;(i_{Lc} - i_{\mathrm{Clamp}})}{L_C} \tag{35}$$

$$\frac{\mathrm{d}v_{\mathrm{Clamp}}}{\mathrm{d}t} = \frac{i_{\mathrm{Clamp}}}{C_{\mathrm{Clamp}}}. \tag{36}$$

Hence, in this interval, energy will be transferred from the HV side to the load on the LV side. Fig. 12(a) can be used to analyze the current ripple $\Delta I_{\mathrm{Lc,Dkn}}$, given by

$$I_{Lc,\mathrm{Dkn}} = \frac{\left(\frac{V_{\mathrm{HV}}}{n} - \frac{V_{\mathrm{C2}}}{n} - V_{\mathrm{LV}} - \left(\frac{R_{\mathrm{par},1}}{n^2} + R_{\mathrm{par},6}\right) I_{\mathrm{LV}}\right)\;(t_2 - t_1)}{L_C} \tag{37}$$

$$I_{Lc,\mathrm{Dkn}} \approx \frac{V_{Lc}\,D_{\mathrm{kn}}\,T_{\mathrm{sw}}}{L_C}. \tag{38}$$

Equation (37) is a first-order differential equation with a long time constant. An approximation by (38) can be done, whereby the voltage drop across the parasitic resistances is neglected. $D_{\mathrm{kn}}$ represents the duty cycle for interval $2_a$. In Fig. 17, the approximation is validated by plotting the AC part of $i_{\mathrm{Lc}}$ including $R_{\mathrm{par}}$ (37) and without (38). The deviation between both solid lines and the dotted line is almost negligible for small resistances in the range of the stated value in Table I. The peak current $I_{\mathrm{Lc,s}}$ can be summarized as

$$I_{Lc,\mathrm{s}} = I_{0,Lc} + \Delta I_{Lc,\mathrm{Clamp}} + \Delta I_{Lc,\mathrm{Dkn}} = 0 \tag{39}$$

whereby the dc offset $I_{0,\mathrm{Lc}}$ can be calculated by (2) and $\Delta I_{\mathrm{Lc,Clamp}}$ follows (28).

TABLE III
INTERVAL $2_A$: START AND END CONDITIONS

| | $v_{\mathrm{Clamp}}$ | $i_{\mathrm{Clamp}}{}'$ |
|---|---|---|
| **start (0)** | $V_{\mathrm{Clamp}}$ - $\Delta V_{\mathrm{Clamp}}$ | $i_{\mathrm{Lc}}(t_1)/n$ |
| **end (1)** | $V_{\mathrm{Clamp}}$ | 0 |

TABLE IV
INTERVAL $3_A$ AND $4_A$: START AND END CONDITIONS

| | $v_{\mathrm{DS},1}$ | $v_{\mathrm{DS},2}$ | $v_{\mathrm{DS},3}$ | $v_{\mathrm{DS},4}$ | $v_1$ |
|---|---|---|---|---|---|
| **start (0)** | 0 | $V_{\mathrm{HV}}$ | 0 | $V_{\mathrm{Clamp}}$ | $V_{\mathrm{HV}}$ |
| **end (1)** | $V_{\mathrm{HV}}/2$ | $V_{\mathrm{HV}}/2$ | $V_{\mathrm{Clamp}}$ | 0 | $V_{\mathrm{HV}}/2$ |

From Fig. 12(b), the resonance waveforms $i_{\mathrm{Clamp}}$ and $v_{\mathrm{Clamp}}$ can be derived and expressed by

$$L_{\mathrm{lk}}\frac{\mathrm{d}i_{\mathrm{Clamp}}{}'}{\mathrm{d}t}+i_{\mathrm{Clamp}}{}'\,R_{\mathrm{par}}{}'+v_{\mathrm{Clamp}}{}'+V_{\mathrm{C2}}-V_{\mathrm{HV}}=0 \tag{40}$$

$$\frac{4\,C_{\mathrm{Clamp}}}{n^2}\,\frac{\mathrm{d}v_{\mathrm{Clamp}}{}'}{\mathrm{d}t}=i_{\mathrm{Clamp}}{}'. \tag{41}$$

The following additional assumptions to (17), (18), and (20) are necessary to simplify the analysis further:

$$v_{\mathrm{Clamp}}{}'=\frac{n\,v_{\mathrm{Clamp}}}{2} \tag{42}$$

$$C_{\mathrm{Clamp}}{}'=\frac{4\,C_{\mathrm{Clamp}}}{n^2} \tag{43}$$

$$R_{\mathrm{par}}{}'=R_{\mathrm{par},1}+\frac{n^2}{4}\,(R_{\mathrm{par},3}+R_{\mathrm{par},6}) \tag{44}$$

$$T_{\mathrm{res}}=\frac{2\,\pi}{\omega_e} \tag{45}$$

$$\omega_0=\frac{1}{\sqrt{L_{lk}\,C_{\mathrm{Clamp}}{}'}}. \tag{46}$$

On the HV side, the transferred currents $i_{\mathrm{Lc}}{}'$ and $i_{\mathrm{clamp}}{}'$ are superposed, as shown in Fig. 12(a). The part of current $i_1$, which occurs due to the resonance between $C_{\mathrm{Clamp}}$ and $L_{\mathrm{lk}}$, transferred to the HV side can be written in time-dependent form as

$$i_{\mathrm{Clamp}}{}'(t)=\mathrm{e}^{-\alpha t}\left(\frac{V_{\mathrm{HV}}-\alpha\,L_{\mathrm{lk}}\,i_{\mathrm{Clamp}}{}'(0)-V_{\mathrm{C2}}-v_{\mathrm{Clamp}}{}'(0)}{\omega_{\mathrm{e}}\,L_{\mathrm{lk}}}\sin(\omega_{\mathrm{e}}t)+i_{\mathrm{Clamp}}{}'(0)\cos(\omega_{\mathrm{e}}t)\right) \tag{47}$$

with the start and end conditions given in Table III.

In contrast, the transferred voltage across the clamp capacitor $v_{\mathrm{Clamp}}{}'$ can be expressed as

$$v_{\mathrm{Clamp}}{}'(t)=V_{\mathrm{HV}}-V_{\mathrm{C2}}+e^{-\alpha t}\left(\frac{i_{\mathrm{Clamp}}{}'(0)\,\frac{1}{C_{\mathrm{Clamp}}{}'}+\alpha\,(-V_{\mathrm{HV}}+V_{\mathrm{C2}}+v_{\mathrm{Clamp}}{}'(0))}{\omega_{\mathrm{e}}}\sin(\omega_{\mathrm{e}}t)+(V_{\mathrm{C2}}-V_{\mathrm{HV}}+v_{\mathrm{Clamp}}{}'(0))\cos(\omega_{\mathrm{e}}t)\right). \tag{48}$$

Fig. 13 shows the comparison between the simulated waveforms in SPICE and the time-domain equations considering the parasitic resistances as given in Table I. Therefore, only interval $2_{\mathrm{a}}$ is depicted. For $i_{\mathrm{Clamp}}{}'(t)$ and $v_{\mathrm{Clamp}}{}'(t)$, the same parameters are valid and the output power is set to 290 W. The clamp voltage appears on the LV side with a scaling factor of half of $n$. As mentioned above, $C_{\mathrm{Clamp}}$ is chosen to a minimum value regarding to (31). The period time $T_{\mathrm{res}}$ increases and mainly the amplitude of $i_{\mathrm{Clamp}}$ in Fig. 13 decreases, if the value of $C_{\mathrm{Clamp}}$ rises. In consequence, the rms value of $i_{\mathrm{Clamp}}$ and all derived currents decrease.

The duty cycle $D_{\mathrm{kn}}$, and, therefore, the length of interval $2_{\mathrm{a}}$, is finally defined as follows:

$$D_{\mathrm{kn}}=D_{\mathrm{Clamp}}-D_{1\mathrm{a}}\,. \tag{49}$$

### C. Analysis of Turn-OFF in $3_a$ ($t_2 \ldots t_3$)

At $t_2$, the transistor $S_1$ and, simultaneously, transistor $S_3$ are switched OFF, preventing an energy transfer to the LV side as well as the oscillation between $C_{\mathrm{Clamp}}$ and $L_{\mathrm{Lk}}$. Fig. 4(c) shows the current paths during this first interval of demagnetization of the inductor of $L_{\mathrm{C}}$ in the form of the topology schematic. Even in interval $3_{\mathrm{a}}$, the circuit can be divided into two single subcircuits: one for the power transfer to the LV side and the second, representing an additional radio frequency (RF) oscillation between HV and LV converter sides, as depicted in Fig. 14. The following equations can be derived:

$$C_{\mathrm{oss,HV}}\,\frac{\mathrm{d}v_{\mathrm{DS},2}}{\mathrm{d}t}=\frac{i_{\mathrm{Coss,HV}}}{2}=\frac{i_{Lc}}{2\,n} \tag{50}$$

$$v_1+V_{\mathrm{C2}}-v_{\mathrm{DS},2}=0 \tag{51}$$

$$L_C\frac{\mathrm{d}i_{Lc}}{\mathrm{d}t}-v_{22}+V_{\mathrm{LV}}=0. \tag{52}$$

Starting the analysis according to Fig. 3, the relation between $v_1$ and $v_{22}$ is the same as in interval $1_{\mathrm{a}}$, and, therefore, $v_{22}$ is equal to $v_1/n$. Using (50)–(52) and the start condition $v_{\mathrm{DS},2}(0)$ in Table IV, the drain-to-source voltage $v_{\mathrm{DS},2}(t_2 \ldots t_3)$ can be expressed as

$$v_{\mathrm{DS},2}\,(t)=y_1-y_2 I_{Lc,\mathrm{s}}\sinh(\omega\ t)+y_3\cosh(\omega\,t) \tag{53}$$

whereby

$$y_1=n\,V_{\mathrm{LV}}+V_{\mathrm{C2}} \tag{54}$$

$$y_2=\sqrt{\frac{L_C}{2\,C_{\mathrm{oss,HV}}}} \tag{55}$$

$$y_3=v_{\mathrm{DS},2}(0)-V_{\mathrm{C2}}-n\,V_{\mathrm{LV}}. \tag{56}$$

In Fig. 15, the decrease of the drain-to-source voltage $v_{\mathrm{DS},2}$ from $V_{\mathrm{HV}}$ to $V_{\mathrm{HV}}/2$ is compared to the length of interval $1_{\mathrm{a}}$. Equation (53) is validated by a SPICE simulation based on different values for $C_{\mathrm{oss,HV}}$ at the same output power $P_{\mathrm{LV}}$. The plotted progressions in Fig. 15(b) are based on (7), showing that interval $1_{\mathrm{a}}$ is significantly longer than interval $3_{\mathrm{a}}$.

The end of interval $3_a$ is achieved as soon as $v_{DS,2}(1)$ is reached and the corresponding length can be calculated by

$$D_{3a} = \operatorname{arsinh}\left(\frac{V_{HV}}{2\,y_2}\right)\omega\,T_{sw}. \tag{57}$$

Equation (57) is an approximation and can be implemented because the hyperbolic sin is the dominant part in (53) and the difference in the period under consideration is negligible. Similar to interval $1_a$, the length of this interval decreases with lower $C_{oss,HV}$.

As Fig. 3 shows, the drain-to-source voltage $v_{DS,6}$ is furthermore zero in CCM, and the voltage $v_{DS,4}$, in contrast, decreases although to zero in this interval. The correlation between the drain-to-source voltages on HV and LV side is already described in interval $1_a$. Therefore, the next waveform in Fig. 3 is the inductor current $i_{Lc}$. The current through the inductor $i_{Lc}(t_2 \ldots t_3)$ can be expressed as

$$i_{Lc}(t) = 2\,I_{Lc,s} - \Big(I_{Lc,s}\cosh(\omega t) + \sqrt{\tfrac{2\,C_{oss,HV}}{L_C}}\,(V_{HV} - V_{C2} - n\,V_{LV})\,\sinh(\omega t)\Big). \tag{58}$$

In Fig. 9, (58) is also validated for a HV side parasitic capacitance $C_{oss,HV}$ of 1.8 nF. The calculation and the results from SPICE simulation are in good agreement over the full output power range.

The high-frequency oscillation of $i_1$ in Fig. 3 and represented by the subcircuit in Fig. 14(b) has the same period $T_r$ as the oscillation in interval $1_a$; thus, (22) can be used to calculate the period $T_r$. In this interval, the parasitic capacitances $C_{oss,3}$ and $C_{oss,4}$ are recharged instead of $C_{oss,5}$ and $C_{oss,6}$. Especially, the parasitic resistances on LV side damp the amplitude of the RF oscillation, and the transferred value in $3_a$ can be calculated by

$$R_{par}{}' = \frac{n^2}{4} R_{par,6}. \tag{59}$$

The $R_{par}{}'$, inductor $L_{lk}$, and capacitor $C_{oss}{}'$ in series are the reason for the following form of $i_{Coss}{}'$ in interval $3_a$:

$$i_{Coss}{}'(t) = \frac{I_{Lc,s}}{n} - \frac{i_1(t_2)}{4\,n} e^{-\alpha t}\sin(\omega_e\,t). \tag{60}$$

$C_{Clamp}$ supplies no power to the LV side and $S_6$ conducts the inductor current $i_{Lc}$. In addition, the amplitude is half of the output current $I_{LV}$, which can be explained by the different start conditions between intervals $1_a$ and $3_a$. The waveforms in simulated and calculated form are also depicted in Fig. 11 based on the HV side current $i_1$ showing a smaller amplitude in $3_a$ compared to $1_a$. The oscillation can also be measured in $i_{Clamp}$ and the current through the lower side transistors $S_4$ and $S_6$. This is also true for voltages that are not clamped during this interval, such as $v_1$, $v_{DS,3}$, or $v_{DS,4}$.

### D. Freewheeling Phase $4_a$ ($t_3 \ldots t_4$)

At $t_3$, the condition for $D_4$ to conduct is fulfilled and the current $i_{Lc}$ is split between the transistors $S_4$ and $S_6$. As Fig. 4(d) shows, this interval can also be divided into two subcircuits, which are shown in Fig. 16.

Based on the subcircuit in Fig. 16(b), the following equations can be derived:

$$C_{oss,HV}\,\frac{dv_{DS,1}}{dt} = \frac{i_{Coss}{}'}{2} \tag{61}$$

$$L_{lk}\,\frac{di_{Coss}{}'}{dt} + R_{par}{}'\,i_{Coss}{}' + v_{DS,1} = 0. \tag{62}$$

As Fig. 3 shows, the drain-to-source voltages $v_{DS,1}$ and $v_{DS,2}$ are, on average, $V_{HV}/2$. An overlapped parasitic oscillation is depicted in Fig. 7, which can be calculated by

$$v_{DS,2}(t) = \frac{V_{HV}}{2} - \frac{I_{LV}}{Z_{RLC}}\,e^{-\alpha t}\sin(\omega_e\,t) \tag{63}$$

with

$$Z_{RLC} = \sqrt{R_{par}{}'^2 + \left(\omega_{0,4a}\,L_{lk} - \frac{1}{\omega_{0,4a}\,C_{oss,HV}}\right)^2} \tag{64}$$

describing the impedance of the series resonance circuit in Fig. 16(b).

The ideal resonance $\omega_{0,4a}$ is

$$\omega_{0,4a} = \frac{1}{\sqrt{2\,L_{lk}\,C_{oss,HV}}}. \tag{65}$$

The drain-to-source voltages $v_{DS,4}$ and $v_{DS,6}$ are zero and the voltage across the inductor $L_C$ reaches its minimum of $-V_{LV}$. From Fig. 16(a), the losses in the parasitic resistances can be derived as

$$(R_{par,4} + R_{par,6})\,i_{Lc}(t) + L_C\frac{di_{Lc}}{dt} = -V_{LV} \tag{66}$$

and, hence, the slope of the inductor current in interval $4_a$ can be expressed by

$$i_{Lc}(t) = \frac{(L_C\,V_{LV} + i_{Lc}(t_3)\,L_C\,(R_{par,4} + R_{par,6}))}{L_C\,(R_{par,4} + R_{par,6})}\,e^{-\frac{(R_{par,4}\,+\,R_{par,6})\,(t_5\,-\,t_4)}{L_C}} - \frac{V_{LV}}{R_{par,4} + R_{par,6}}. \tag{67}$$

Neglecting the resistances in (67) in the intervals $3_a$ and $4_a$, the choke current can be approximated by

$$i_{Lc}(t) \approx I_{Lc,s} - \frac{V_{LV}\,(1.5 - D_{Clamp})\,(t_5 - t_3)}{L_C}. \tag{68}$$

Fig. 17 shows the inductor current $i_{Lc}$ as a simulated waveform, whereby, in $4_a$, $i_{Lc}$ is calculated by (67) and the approximation according to (68).

The parasitic oscillation $i_{Coss}{}'$ is caused from the leakage inductance $L_{lk}$ and forms a series resonance tank consisting of $R_{par}{}'$, $C_{oss,1}$, and $C_{oss,2}$ depicted in Fig. 16(b). This leads to

$$i_1(t) = \frac{I_{LV}}{n}\,e^{-\alpha t}\cos(\omega_e\,t) \tag{69}$$

whereby $\alpha$ can be calculated from (17) and $\omega_e$ from (18). The damping part of the oscillation is the parasitic resistances transferred to the HV side

$$R_{par}{}' = \frac{n^2}{4}\,(R_{par,4} + R_{par,6}). \tag{70}$$

The period of this resonance can be calculated by

$$T_{\mathrm{p}} = 2\,\pi\,\sqrt{2\,L_{\mathrm{lk}}\,C_{\mathrm{oss,HV}}}\,. \tag{71}$$

The measured and calculated progression of $i_1$ is plotted in Fig. 11, showing that the calculated period $T_{\mathrm{p}}$ and amplitude are in good agreement with the result from SPICE simulation.

For the step-down operation, the novel modulation scheme for the AC-HB-CF-PP topology is analyzed in detail in this section. The principle to achieve ZVS is described based on analytical equations and key waveforms. As a result, the responsible interval $1_{\mathrm{a}}$ can be shortened by selecting a lower $C_{\mathrm{oss,HV}}$, and with increasing output power $P_{\mathrm{LV}}$, the optimal dead-time is reduced. Achieving ZVS is possible over the full power range without additional effort. The evaluation shows that reducing the parasitic elements $L_{\mathrm{lk}}$ and $C_{\mathrm{oss,LV}}$ suppresses the parasitic oscillations on converter waveforms.

## IV. Step-Up Operation Mode

After discussion of the novel modulation scheme in step-down mode, the operation principle in step-up mode will be analyzed. The transistors $S_4$ and $S_6$ of the PP circuit are responsible for the power transfer. The intrinsic diodes $D_1$ and $D_2$, or, in case of active rectification, $S_1$ and $S_2$, rectify the current $i_1$. The modulation scheme as well as the resulting current and voltage waveforms in step-up mode are depicted in Fig. 18. Overall, in half of the period $T_{\mathrm{sw}}$, the converter passes three intervals $1_{\mathrm{b}}$–$3_{\mathrm{b}}$, which repeat in the second half of $T_{\mathrm{sw}}$. In the following, a more detailed analysis of the intervals $1_{\mathrm{b}}$–$3_{\mathrm{b}}$ as well as the transition between them will be done according to Fig. 18. Thereby, the descriptions of [33] and [39] will be complemented by the following equations.

### A. Switching Under Hard Condition $1_b$ ($t_0 \ldots t_1$)

At $t_0$, the transistor $S_4$ is switched OFF and $S_6$ conducts the full current $i_{\mathrm{Lc}}$. Due to this switching operation, the parasitic capacitances $C_{\mathrm{oss},1}$, $C_{\mathrm{oss},2}$, $C_{\mathrm{oss},3}$, and $C_{\mathrm{oss},4}$ can adapt their amount of charge for the next steady-state mode. Like interval $3_{\mathrm{a}}$ in the step-down mode, two subcircuits can be analyzed in $1_{\mathrm{b}}$ (cf., Fig. 14). In step-up mode, $v_{\mathrm{DS},2}$ reaches $V_{\mathrm{HV}}$ and $v_{\mathrm{DS},1}$ reaches zero at $t_1$. Thereby, the start and end conditions in steady-state of Table IV must be interchanged.

For the time-dependent form of the drain-to-source voltage $v_{\mathrm{DS},1}$ in Fig. 19, (53) can be used as well. Compared with the step-down mode, $v_{\mathrm{DS},1}(0)$ exhibits more oscillation depending on $R_{\mathrm{par}}$ from the previous interval $3_{\mathrm{d}}$. These oscillations are caused by the leakage inductance $L_{\mathrm{lk}}$ and the parasitic capacitances $C_{\mathrm{oss,HV}}$, damped by the parasitic resistances $R_{\mathrm{par},4}$ and $R_{\mathrm{par},6}$.

Therefore, first, in Fig. 19, the start condition of the drain-to-source voltage $v_{\mathrm{DS},1}(0)$ will be analyzed for different parasitic resistances. The reason for the oscillation, in the interval before, with higher amplitude than in step-down mode will be analyzed in Section IV-C. By using the value of $v_{\mathrm{DS},1}(0)$ from SPICE simulation at $t_0$, Fig. 19 shows that simulation and (53) are still equal.

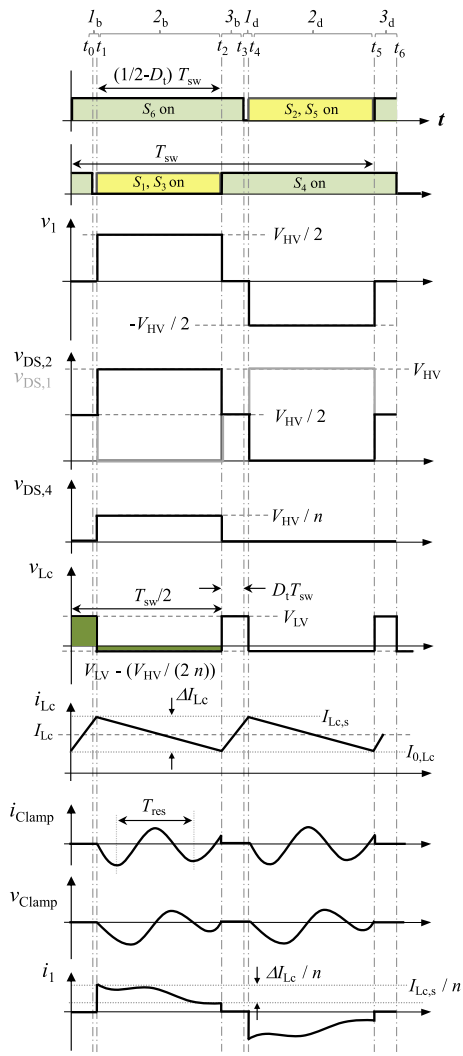


Fig. 18. Theoretical waveforms for the step-up operation.

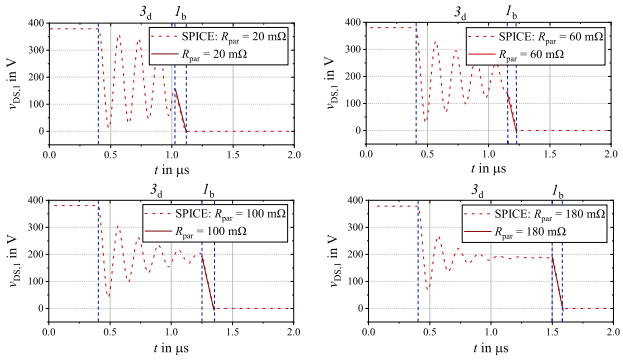


Fig. 19. Evaluation of $v_{\mathrm{DS},1}$ in interval $1_{\mathrm{b}}$ depending on different parasitic resistances $R_{\mathrm{par}}$ from the previous interval $3_{\mathrm{d}}$. With increasing $R_{\mathrm{par}}$, the start condition voltage at $t_0$ converges toward $V_{\mathrm{HV}}/2$.

The same parasitic capacitance $C_{\mathrm{oss,HV}}$ of 1.4 nF is chosen in Fig. 20 for step-up mode as for Fig. 6, which shows the first interval in step-down mode. At the same output power, the length of the interval is shorter in step-up mode, which is also validated through Fig. 15. In step-up mode, the start condition is changed from $I_{0,\mathrm{Lc}}$ to $I_{\mathrm{Lc,s}}$, even though the relation between relevant

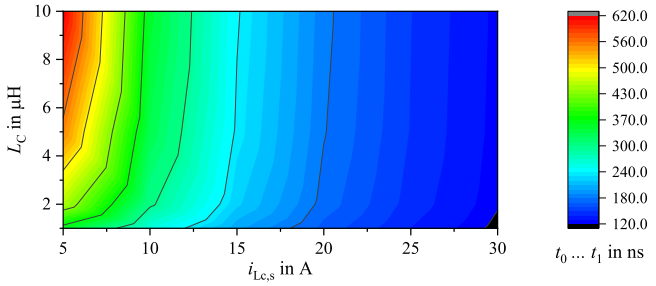


Fig. 20. Time duration of interval $1_b$ depends on the parasitic capacitance $C_{oss,HV}$, the choke inductance $L_C$, and the momentary peak current $i_{Lc,s}$; $C_{oss,HV}$ is set to 1.4 nF. With increasing power from part-load to nominal load the length become more and more independent from $L_C$.

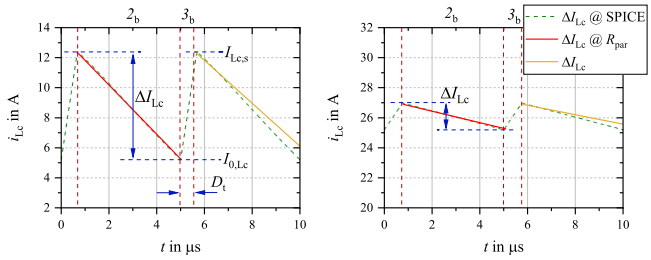


Fig. 21. Current $i_{Lc}$ in interval $2_b$ at different parasitic resistances as well as chokes. (a) $L_C = 2.2$ µH, $P_{HV} = 200$ W, $R_{par1} = 185$ mΩ, and $R_{par6} = 50$ mΩ. (b) $L_C = 10$ µH, $P_{HV} = 600$ W, $R_{par1} = 85$ mΩ, and $R_{par6} = 25$ mΩ.

voltages are not equal in (7) and (53). Using a higher value of the choke inductance $L_C$ especially in part-load, a difference in length of the interval is depicted in Fig. 20. At higher load, the length becomes independent of the power and the inductance; the minimum length itself depends on $C_{oss,HV}$.

On the waveforms of $v_{DS,6}$, $v_{Lc}$, $i_{Lc}$, $i_{Clamp}$, $v_{Clamp}$, and $i_1$, this interval does not have an impact; so a detailed analysis is neglected for interval $1_b$.

### B. Active-Clamp Mode $2_b$ ($t_1$...$t_2$)

At $t_1$, the channel of transistor $S_1$ can be switched ON under ZVS and also transistor $S_3$ is switched ON. Therefore, Fig. 12 is valid for step-up mode, but the start conditions of the clamp capacitor parameters are different compared to the step-down mode. The oscillation across the clamp capacitor $v_{Clamp}$ starts and ends at $V_{Clamp}$, and the current $i_{Clamp}$ begins and ends at zero.

The drain-to-source voltage $v_{DS,4}$ jumps to $V_{Clamp}$ according to (3) and $v_{Lc}$ to the negative voltage shown in Fig. 18. As a result of the negative voltage, the slope of the current $\Delta I_{Lc}$ can be expressed by (72), whereby the following approximation can be done by neglecting the parasitic resistances, as is the case of step-up mode as well:

$$I_{Lc} \approx \frac{V_{LV} - \frac{V_{HV}}{2\,n}}{L_C}\,(1 - D_t)\,\frac{T_{sw}}{2}. \tag{72}$$

The duty cycle $D_t$ represents the length of interval $3_b$, which will be described in (73).

Fig. 21 shows the comparison between the SPICE result and both (37) and (72). By varying parasitic resistances, choke inductance $L_C$, and momentary output power $P_{HV}$, Fig. 17 is supplemented. The approximation can be used for resistances shown in Table I; with higher values, the deviation will increase and (37) should be used instead.

Due to Fig. 18, considering the volt-seconds applied to $L_C$ over $T_{sw}/2$, and using Fig. 3, the duty cycle $D_t$ in step-up mode can be derived as

$$D_t = \frac{1}{2} - \frac{nV_{LV}}{V_{HV}}. \tag{73}$$

Due to the validation of (72), the dc offset $I_{0,Lc}$ of the inductor current can be calculated by the averaged current $I_{Lc}$ minus half of $\Delta I_{Lc}$. The maximum inductor current $I_{Lc,s}$ is the addition of $I_{Lc}$ and half of $\Delta I_{Lc}$.

Next, in Fig. 18, the clamp current $i_{Clamp}$ as well as the voltage across the clamp capacitor $v_{Clamp}$ is depicted. For step-up mode, the HV side is transferred to the LV side to determine the resonance waveform resulting from the leakage inductance $L_{lk}$ and the clamping capacitor $C_{Clamp}$. The parasitic resistances $R_{par}$ in this interval can be summarized to

$$R_{par} = R_{par,3} + R_{par,6} + \frac{4\,R_{par,1}}{n^2}. \tag{74}$$

For calculation of the clamp current $i_{Clamp}$ and clamp voltage $v_{Clamp}$ in reference to the LV side, further assumptions are made

$$L_{lk}{}' = \frac{4\,L_{lk}}{n^2} \tag{75}$$

$$V_{HV}{}' = \frac{2\,V_{HV}}{n} \tag{76}$$

$$V_{C2}{}' = \frac{2\,V_{C2}}{n} \tag{77}$$

$$\omega_0 = \frac{1}{\sqrt{L_{lk}{}'\,C_{Clamp}}} \tag{78}$$

$$\alpha = \frac{R_{par}}{2\,L_{lk}{}'}. \tag{79}$$

By replacing the variables, which are defined for step-up mode analysis, (47) for $i_{Clamp}$ and (48) for $v_{Clamp}$ can be used.

Simulated and calculated progressions of $i_{Clamp}$ as well as $v_{Clamp}$ are depicted in Fig. 22. The time $T_{res}$ is calculated as 2.3 µs and is the same as in the step-down example in Fig. 13. The voltages across the transistors are clamped in this interval; so the parasitic output capacitances $C_{oss,LV}$ have no negative effect on $2_b$.

The HV side current $i_1$ can be calculated by the summation of $i_{Clamp}$ and $i_{Lc}$ transferred to the HV side.

### C. Interval $3_b$ of Freewheeling Current ($t_2$...$t_3$)

At $t_2$, first, transistor $S_3$ turns OFF and, after a short dead-time, transistor $S_4$ turns ON under hard-switching condition. As mentioned in Section IV-A, the drain-to-source voltage $v_{DS,2}$ as well as the HV side current $i_1$ shows a frequency oscillation with high amplitude in interval $3_b$, which is similar to interval $4_a$ in Section III-D. Therefore, the drain-to-source voltage $v_{DS,1}$ can

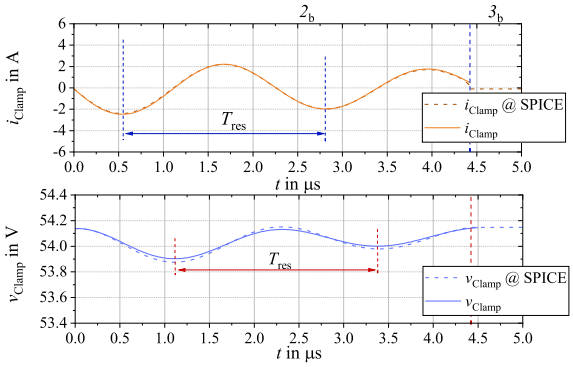


Fig. 22. Comparison of simulated and time-dependent calculated $i_{\mathrm{Clamp}}$ and $v_{\mathrm{Clamp}}$ waveform. In SPICE, all parasitic elements are implemented and, in calculation, following start conditions are used: $i_{\mathrm{Clamp}}(0)$ is equal to $-100$ mA; $v_{\mathrm{Clamp}}(0) = 54.1$ V. For $C_{\mathrm{oss,HV}}$, a value of 800 pF is chosen, but like $T_{\mathrm{res}}$ shows, this has no effect on $i_{\mathrm{Clamp}}$ compared to the example in step-down mode.

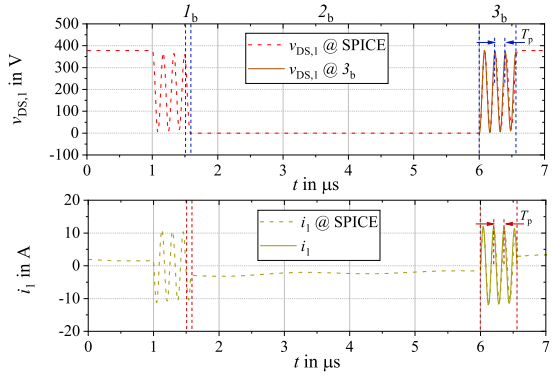


Fig. 23. Drain-to-source voltage $v_{\mathrm{DS,1}}$ and HV side transformer current $i_1$ in interval $3_{\mathrm{b}}$. $i_1(0)$ is set to 1.6 A and $v_{\mathrm{DS,1}}(0)$ is 190 V. $T_{\mathrm{p}}$ is calculated with (71) to 159 ns and measured in SPICE to 161 ns.

be expressed with

$$v_{\mathrm{DS,1}}(t) = \frac{V_{\mathrm{HV}}}{2} - e^{-\alpha t} \left( \frac{i_{\mathrm{Coss}}(0)\ L_{\mathrm{lk}} + v_{\mathrm{DS,1}}(0)\ C_{\mathrm{oss,HV}}\ {R_{\mathrm{par}}}'}{2\ C_{\mathrm{oss,HV}}\ L_{\mathrm{lk}}\ \omega_{\mathrm{e}}} \sin(\omega_{\mathrm{e}}\ t) + v_{\mathrm{DS,1}}(0)\ \cos(\omega_{\mathrm{e}}\ t) \right) \tag{80}$$

whereby $v_{\mathrm{DS,1}}(0)$ is equal to $V_{\mathrm{HV}}/2$ and $\omega_{\mathrm{e}}$ can be calculated by (18). The series resistance ${R_{\mathrm{par}}}'$ and the ideal resonance $\omega_0$ can be written as

$${R_{\mathrm{par}}}' = \frac{n^2}{4}\left(R_{\mathrm{par,4}} + R_{\mathrm{par,6}}\right) \tag{81}$$

$$\omega_0 = \frac{1}{\sqrt{L_{\mathrm{lk}}\ 2\ C_{\mathrm{Coss,HV}}}}. \tag{82}$$

In this interval, both voltages $v_{\mathrm{DS,4}}$ and $v_{\mathrm{DS,6}}$ are zero, and the voltage $V_{\mathrm{LV}}$ is applied across the choke $v_{\mathrm{Lc}}$. Therefore, the slope of the increasing inductor current $i_{\mathrm{Lc}}$ is higher than the slope of the decreasing current in interval $2_{\mathrm{b}}$ before. To calculate the slope of current $i_{\mathrm{Lc}}$, (67) can be used. The approximation for the ripple current $\Delta I_{\mathrm{Lc}}$ is expressed by

$$\Delta I_{Lc} \approx \frac{V_{\mathrm{LV}}\ D_{\mathrm{t}}\ T_{\mathrm{sw}}}{L_C}. \tag{83}$$

The transformer current on HV side $i_1$ in Fig. 18 can be calculated by

$$i_1(t) = e^{-\alpha t} \left( \frac{-i_1(0)\ R_{\mathrm{par}} + 2\ v_{\mathrm{DS,1}}(0)}{2\ L_{\mathrm{lk}}\ \omega_{\mathrm{e}}} \sin(\omega_{\mathrm{e}}\ t) + {i_{\mathrm{Coss}}}'(0) \cos(\omega_{\mathrm{e}}\ t) \right). \tag{84}$$

In Fig. 23, the calculated drain-to-source voltage $v_{\mathrm{DS,1}}$ and the current $i_1$ on the HV side is validated with simulation. The operating point is chosen as 380 W on the HV side and the parasitic capacitance $C_{\mathrm{oss,HV}}$ is 800 pF. At the end of interval $2_{\mathrm{b}}$, the channel of transistor $S_1$ can turn-OFF at 0 V so that active rectification stops. The intrinsic diode of $S_1$ is blocking at $t_2$

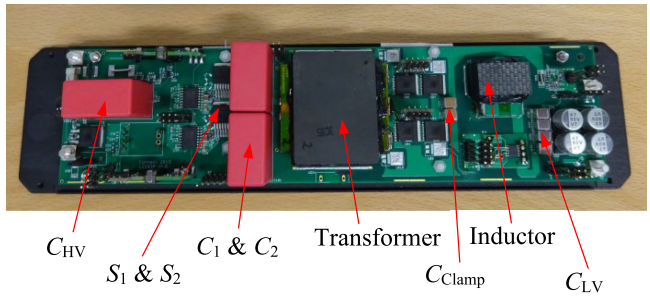


Fig. 24. Photography of the power board of the dc-dc converter prototype.

and, at the same time, the transistor $S_4$ is switched hard from the voltage $V_{\mathrm{Clamp}}$ into the ON-state. In step-down mode interval $3_{\mathrm{a}}$, $v_{\mathrm{DS,2}}$ decreases slowly to $V_{\mathrm{HV}}/2$, while in step-up mode, the transition is faster and an oscillation with higher amplitude occurs.

As with step-down mode, the converter also works in either DCM or CCM during step-up operation. The converter enters DCM as soon as the polarity of the inductor current $i_{\mathrm{Lc}}$ is reversed. In step-up mode, this does not change current or voltage waveforms as it does in step-down mode because of the CF-PP circuit on the LV side. Finally, in step-up mode, the part-load is presumably less efficient than in step-down mode because of the circulating reactive energy. In the next section, the analysis will be validated by measurements.

## V. Measurement Results

The preceding theoretical analysis is validated in this section by measurements. The voltage $V_{\mathrm{HV}}$ is set to 380 V and $V_{\mathrm{LV}}$ to 24 V. The prototype in Fig. 24 uses the semiconductors listed in Table V.

### A. Measured Waveforms

In Fig. 25, the waveforms with the traditional modulation of the AC-HB-CF-PP topology in step-down mode are shown. The duty cycle $D_{\mathrm{k}}$ of the HV side transistors controls the converter and the AC circuit clamps the voltages across the LV side

TABLE V
SEMICONDUCTORS SPECIFICATION

| Components | Symbol | Part Number |
|---|---|---|
| HV Switches | $S_1$, $S_2$ | SiC MOSFETs: C3M0065090J[a] |
| LV Switches | $S_3$, $S_4$, $S_5$, $S_6$ | Si MOSFETs: FDMT80080DC[b] |

[a]Cree, Silicon Carbide Power MOSFET C3M0065090J, Datasheet, Rev. A, June 2015.
[b]Fairchild, FDMT80080DC N-channel Dual Cool 88 Power Trench MOSFET, Datasheet, Rev. 1.0, July 2015.

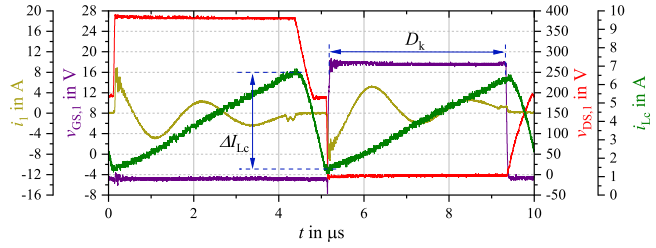


Fig. 25. Traditional modulation scheme with hard switched transistor $S_1$ at time instant 5 $\mu$s. The current ripple $\Delta I_{Lc}$ is measured to 6 A; the LV side output power $P_{LV}$ is chosen as 96 W.

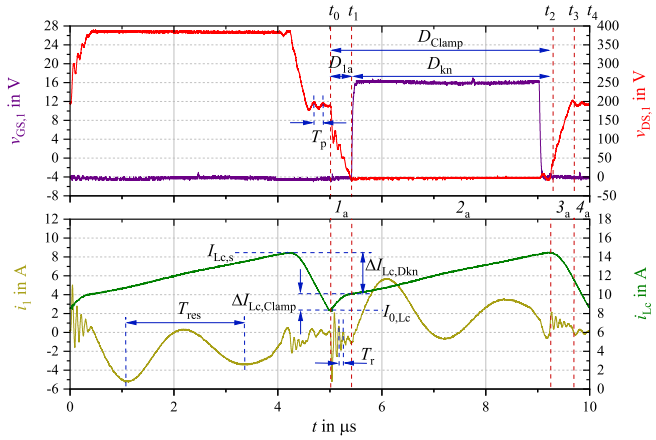


Fig. 26. Output power $P_{LV}$ is set to 290 W and an additional capacitor of 1 nF is implemented in parallel to the SiC transistor; overall, 1.4 nF is integrated; ZVS can be seen at $t_1$ when the channel of transistor $S_1$ is switched ON.

transistors. Using this modulation scheme, however, the HV side transistors are hard switched, which is depicted in Fig. 25 at 5 $\mu$s. Additionally, the resonant current $i_{Clamp}$ jumps to the start value, as shown in Fig. 25 on the basis of the HV side transformer current $i_1$. The theoretical ripple current $\Delta I_{Lc}$ is 6 A, which agrees with the measured value and an adjusted duty cycle $D_k$ of 42% is achieved in Fig. 25.

To evaluate the SPICE model and the theoretical analysis of the novel modulation scheme, Figs. 26 and 27 are used, which are measured at 290 W. Using the traditional modulation scheme, the rms value of $i_{Clamp}$ at this operating point is calculated as 1.9 A and with the novel one as 6.2 A.

In Fig. 26, the gate-to-source voltage $v_{GS,1}$, the drain-to-source voltage $v_{DS,1}$, the HV side current through the transformer $i_1$, and the inductor current $i_{Lc}$ are depicted as in Fig. 25 before. The parasitic capacitance $C_{oss,HV}$ of the prototype is measured as approximately 400 pF. The analysis in Section III

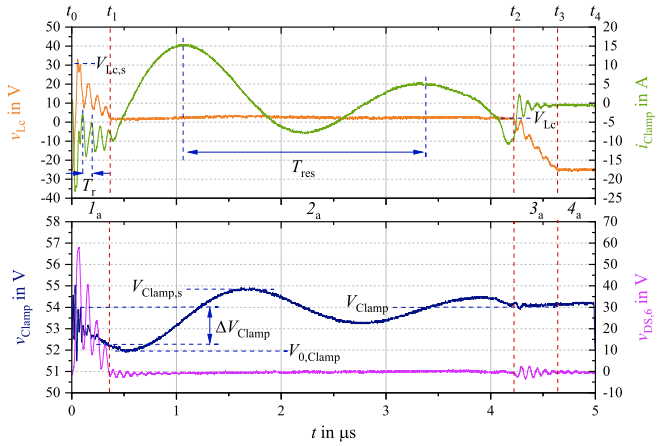


Fig. 27. Half of the period as in Fig. 26 in which the voltage peak of $v_{DS,6}$ at $t_0$ is depicted; between $t_0$ and $t_1$, the current on the HV side is measured, whereby the energy transfer from HV to LV side joins in interval $2_a$.

TABLE VI
STEP-DOWN: THEORETICAL ANALYSIS VERSUS MEASUREMENT RESULTS

| | Equation | Analytical | Measurement |
|---|---|---|---|
| $I_{0,Lc}$ | (2) | 7.8 A | 8.3 A |
| $I_{Lc,s}$ | (39) | 14.9 A | 14.8 A |
| $\Delta I_{Lc,Clamp}$ | (28) | 1.9 A | 1.9 A |
| $\Delta I_{Lc,Dkn}$ | (37) | 5.2 A | 4.6 A |
| $D_{1a}$ | (12) | 4% | 4.3% |
| $D_{kn}$ | (49) | 38.8% | 38.2% |
| $D_{Clamp}$ | (1) | 42.8% | 42.5% |
| $T_{res}$ | (45) | 2.3 µs | 2.3 µs |
| $T_r$ | (22) | 72 ns | 70 ns |
| $T_p$ | (71) | 216 ns | 180 ns |
| $V_{Clamp}$ | (3) | 54 V | 54 V |
| $\Delta V_{Clamp}$ | (30) | 1 V | 1.3 V |
| $V_{0,Clamp}$ | (48) | 52.8 V | 52 V |
| $V_{Clamp,s}$ | (48) | 54.3 V | 54.8 V |
| $V_{Lc,s}$ | (23) | 30.3 V | 30 V |
| $V_{Lc}$ | (24) | 3.4 V | 2.9 V |

shows that interval $1_a$ is very short for such a small drain-to-source capacitance. The additional variation of $C_{oss,HV}$ to 1.4 nF is achieved by using additional multilayer ceramic capacitors (MLCCs) connected in parallel, which are not necessary for the design of the AC-HB-CF-PP topology. They are implemented only to confirm the validity of the calculations over a wide range and further pronounce the ZVS in interval $1_a$. Thus, the converter efficiency in Section V-B is measured without additional MLCCs.

Table VI presents a comparison of the calculated and measured values together with the corresponding equations. The associated measured characteristic parameters are depicted in Figs. 26 and 27.

The same operating point as shown in Fig. 26 but half of the period time $T_{sw}$ is depicted in Fig. 27, showing the voltage across the inductor $v_{Lc}$, the clamp current $i_{Clamp}$, the voltage across the clamp capacitor $v_{Clamp}$, and the drain-to-source voltage $v_{DS,4}$. The value of the clamp voltage $v_{Clamp}$ in the second valley in simulation and in measurement drops from $V_{Clamp}$ by 750 mV. The resulting damping of the oscillation in theory, simulation, and measurement is nearly the same. The resonance frequency

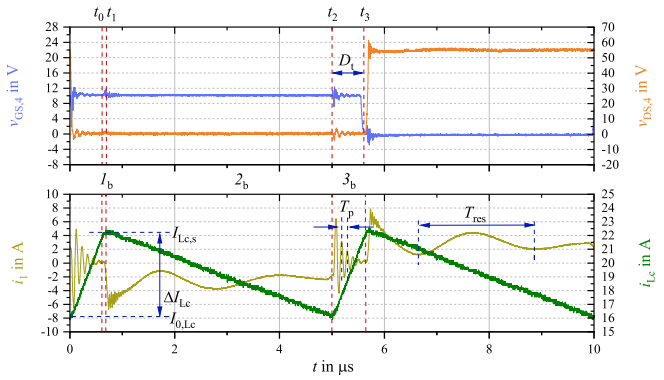


Fig. 28. Waveforms for the operating point at 430 W $P_{\mathrm{HV}}$ in step-up mode.

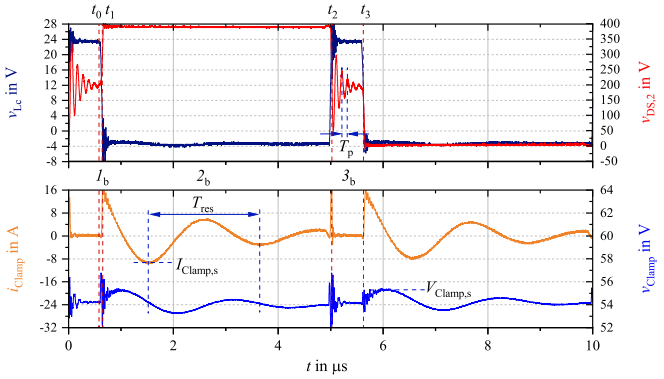


Fig. 29. Besides the voltage across the inductor $v_{\mathrm{Lc}}$, the drain-to-source voltage $v_{\mathrm{DS},2}$ across transistor $S_2$, the clamp current $i_{\mathrm{Clamp}}$, and the voltage across the clamp capacitor $v_{\mathrm{Clamp}}$ are depicted for step-up mode and 430 W.

is equal so that identical start and end conditions are depicted. The characteristic voltage peaks, which occur using the novel modulation scheme and described in Section III-A, are shown based on the voltages $v_{\mathrm{Lc}}$ and $v_{\mathrm{DS},6}$. The voltage increase is superimposed with a high-frequency oscillation due to $C_{\mathrm{oss,HV}}$, $C_{\mathrm{oss,LV}}$, and $L_{\mathrm{lk}}$. Measured and calculated values are in good agreement.

Instead of the waveforms just shown, for which parallel capacitances are implemented, in Figs. 28 and 29, only the parasitic capacitances $C_{\mathrm{oss}}$ of the HV side transistors are used. The operating point $P_{\mathrm{HV}}$ at 430 W on the HV side is chosen for step-up mode. Besides the gate-to-source voltage $v_{\mathrm{GS},4}$, the drain-to-source voltage $v_{\mathrm{DS},4}$, the HV side transformer current $i_1$, and the inductor current $i_{\mathrm{Lc}}$ are shown. By using the AC technique, $v_{\mathrm{DS},4}$ has the voltage $V_{\mathrm{Clamp}}$ as blocking voltage. Turn-ON of the transistor $S_4$ occurs under hard-switching condition, represented as $t = 0$. Turning OFF can be done soft. As mentioned before, for lower $C_{\mathrm{oss,HV}}$, the length of the interval is shorter, which can be seen in step-up mode based on $1_{\mathrm{b}}$. Table VII lists the values for the characteristic parameters marked in both figures.

Fig. 29 shows the voltage across the inductor $v_{\mathrm{Lc}}$, the drain-to-source voltage $v_{\mathrm{DS},2}$ of transistor $S_2$, the clamp current $i_{\mathrm{Clamp}}$, as well as the voltage across the clamp capacitor $v_{\mathrm{Clamp}}$ at the same operating point of 430 W on the HV side. Based on $v_{\mathrm{DS},2}$, it is shown that the oscillation is higher in interval $3_{\mathrm{b}}$ as in the step-down mode in interval $4_{\mathrm{a}}$ but more damped as in Fig. 23, which includes only the parasitic resistances of the transistors. A comparison with Fig. 19 led to conclude an equivalent $R_{\mathrm{par}}$ of approximately 100 mΩ in the prototype design. The calculated and measured duty cycle $D_{\mathrm{t}}$ show, in Table VII, a deviation of 0.6%, which results from a voltage drop with increasing output power $P_{\mathrm{HV}}$. The higher damping effect also confirms the deviation between both $I_{\mathrm{Clamp,s}}$.

TABLE VII
STEP-UP: THEORETICAL ANALYSIS VERSUS MEASUREMENT RESULTS

| | Equation | Analytical | Measurement |
|---|---|---|---|
| $D_{\mathrm{t}}$ | (73) | 6% | 6.6% |
| $I_{0,\mathrm{Lc}}$ | (2) | 14.6 A | 16.0 A |
| $I_{\mathrm{Lc,s}}$ | (39) | 21.3 A | 22.2 A |
| $\Delta I_{\mathrm{Lc}}$ | (83) | 6.7 A | 6.2 A |
| $T_{\mathrm{p}}$ | (71) | 116 ns | 120 ns |
| $T_{\mathrm{res}}$ | (45) | 2.3 µs | 2.3 µs |
| $I_{\mathrm{Clamp,s}}$ | (47) | -12 A | -9 A |
| $V_{\mathrm{Clamp,s}}$ | (48) | 54.5 V | 55 V |

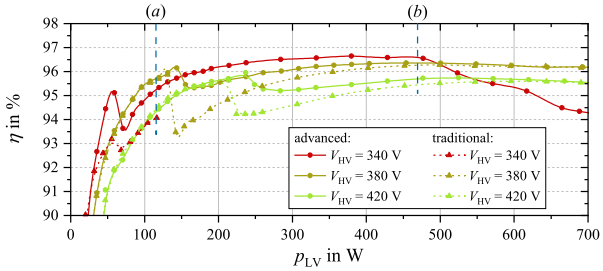


Fig. 30. Efficiency curves for the full grid voltage range of the prototype at a constant LV side voltage of 24 V; the traditional modulation scheme with hard switched as well as the novel and advanced one with soft-switched transistors $S_1$ and $S_2$ are shown.

The subcircuits derived in the sections before can be used to describe the AC-HB-CF-PP topology for step-down and step-up modes. They allow a detailed evaluation of achieving ZVS, falling and rising times, as well as upcoming oscillations at voltage and current waveforms from part to nominal load.

### B. *Efficiency Curves*

The efficiency measurements in Fig. 30 show the power range in which the novel and advanced modulation scheme is advantageous compared to the traditional hard switched scheme. The boundary between DCM and CCM is also depicted, namely at the point on which the efficiency decreases short and rises again. The higher efficiency of the AC-HB-CF-PP in the lower power range is a good characteristic for example in an application in a commercial building because of the high partial load percentage over a day. Over the full power range, the voltage level of 340 V is more efficient than the higher level of 420 V. Since the switching losses are proportional to the level of the switched voltage, this behavior is plausible. With increasing output power, the conduction losses are becoming more dominant. The efficiency curves of the advanced modulation scheme and the traditional one are nearly identical at both ends of the power range (part-load and nominal load). Therefore, the novel modulation scheme has three characteristics which increase efficiency.

TABLE VIII
COMPARISON OF STEP-DOWN MODE BETWEEN THE PROPOSED AC-HB-CF-PP AND OTHER ISOLATED BIDIRECTIONAL DC/DC CONVERTER TOPOLOGIES

| Topology | Semi-conductors | Passives (ind. / cap.) | Efficiency (W / %) | Voltage ratio ($V_{HV}/V_{LV}$) | Modulation schemes |
|---|---|---|---|---|---|
| **Flyback** | | | | | |
| [7] | 3 | 2 / 3 | 50 / 83 | 24/12 | → Use an auxiliary circuit to achieve ZCS |
| [8] | 2 | 2 / 4 | 750 / 96.4 | 300/300 | → Partial resonant flyback |
| [9] | 4 | 2 / 4 | 60 / 93.5 | 24/24 | → Active-clamp flyback |
| [11] | 5 | 2 / 2 | 200 / 91 | 380/24 | → 2-switch flyback |
| [12] | 6 | 3 / 4 | 500 / 94.2 | 400/24 | → Combination of a buck-boost and a forward-flyback converter |
| **ZVS by active clamping:** The clamp capacitor is in resonance with the leakage inductance. To achieve ZVS at the main transistor, the energy in the inductance $L_{lk}$ has to be greater than the energy stored in the parasitic capacitor $C_{oss,HV}$: $L_{lk}\, i_1^2 > C_{oss,HV}\, v_{DS,1}^2$ | | | | | |
| **Resonant** | | | | | |
| [17] | 6 | 2 / 4 | 580 / 94 | 400/48 | → *LLC* with frequency modulation $f_{sw}$ |
| [18] | 8 | 2 / 4 | 480 / 96 | 400/48 | → *CLLC* with frequency modulation $f_{sw}$ |
| **ZVS by using the inductive gain region:** Obtaining sufficient inductive energy in the transformer ($L_m + L_{lk}$) by the peak magnetizing current $I_{m,s}$: $(L_m + L_{lk})\, I_{m,s}^2 > 2\, C_{oss,HV}\, V_{HV}^2$ | | | | | |
| **DAHB** | | | | | |
| [26] | 4 | 4 / 6 | 500 / 97 | 48/48 | → Voltage-fed DAHB with built-in filters and phase-shift modulation $\varphi$ |
| [24] | 4 | 3 / 6 | 600 / 93.6 | 350/30 | → Current-fed DAHB with phase-shift modulation $\varphi$ |
| [23] | 6 | 5 / 9 | 500 / 92 | 400/45 | → Three-port current-fed and voltage-fed DAHB with phase-shift modulation $\varphi$ and duty-cycle $D_k$ control |
| **ZVS by shaping the transformer current:** Using the voltage-fed DAHB, the characteristic points of the transformer current $I_{1,a}$ and $I_{1,b}$, must have the same sign. For the current-fed DAHB the current waveforms have to fulfill following conditions: $t_0$: $I_{2,d} < 0$ A, $t_1$: $I_{0,Lc} < I_{2,a}$, $t_2$: $I_{2,b} > 0$ A, $t_3$: $I_{2,c} < I_{Lc,s}$ | | | | | |
| **Proposed topology** | 6 | 2 / 4 | 600 / 96.6 | 380/24 | → Duty cycle $D_k$ modulation<br>→ Soft switching capability on HV and LV side over full power range<br>→ Burst mode and pulse skipping in part-load |
| **ZVS by using the current $i_{Lc}$:** An active-clamping circuit on LV side is used to supply the load during ZVS on HV side. Equation (12) has to be fulfilled. | | | | | |
| **Applications** | Low Voltage Battery Chargers [7], Low-power DC Uninterruptible Power Supplies [9], Low Power [10], Electric Scooter [12], Multi-port Applications [13], Inductive Charging [14], Energy Storage Systems [16], Uninterruptible Power Supply (UPS) System [18], Three-port Applications like Solar and Battery Energy Generation and Hybrid Energy Storage Systems [23], Distributed Battery Energy Storage [25], Automotive Systems [26], DC Microgrid Applications [33], Mobile Battery [39], On Board Charger [41], and Vehicle-to-Grid [42]. | | | | |

1) The boundary between DCM and CCM is shifted to higher output power.
2) The rectifier on LV side employs zero current switching (ZCS) for turn-ON also at full output power $P_{LV}$.
3) Transistors $S_1$ and $S_2$ turn-ON at 0 V over the full power range.

Two additional operating points that are relevant for a $V_{HV}$ voltage of 340 V are marked in Fig. 30. Point (*a*) represents the maximum power that can be achieved with the traditional modulation scheme. The reason is that the output power $P_{LV}$ is transferred by the duty cycle $D_k$, which represents the ON-time of the HV side transistor $S_1$, respectively $S_2$. In the prototype, the limit for the maximum duty cycle $D_k$ is set to 49%, which is reached at this point of operation. Using (1), which not only represents $D_{Clamp}$ for the novel modulation scheme but also $D_k$ of the traditional one, a maximum duty cycle $D_k$ of 55.6% is calculated for the full power range, which is not feasible. Thus, the converter cannot work over the full HV range, if the turns-ratio depicted in Table I is used. The second point (*b*) marks the output power at which the efficiency for $V_{HV} = 340$ V begins to decrease rapidly. At this operating point, the same situation as with the traditional modulation scheme occurs: the duty cycle $D_{kn}$ reaches 49%, the maximum valid duty cycle HV side in the prototype of the dc-dc converter. Nevertheless, due to operation in CCM and the novel modulation scheme, $D_{Clamp}$ can be increased further and $V_{LV}$ remains constant. The significant drop in efficiency is caused by hard switched HV side transistors and increasing stress on the clamping capacitor. In interval $1_a$, $C_{Clamp}$ has to supply the load, which increases with higher output power as well as the energy, which is necessary to supply the LV side. As a result, operation in this mode is only feasible by using the clamp capacitor $C_{Clamp}$ as an additional voltage source, which is described by the authors in [39].

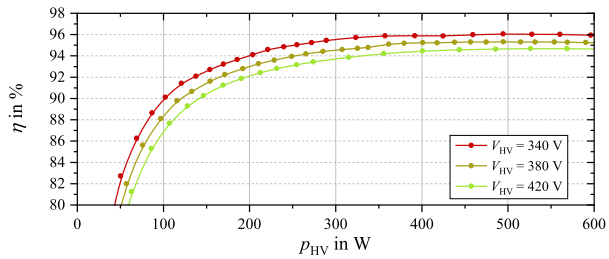


Fig. 31. Efficiency curves in step-up mode: The dominant switching losses in this operation mode are very obvious because the efficiency is higher at 340 V compared to 420 V.

For step-up operation, the traditional modulation scheme is used for a CF-PP topology utilizing the AC circuit to reduce the stress of the LV side transistors. In Fig. 31, the step-up efficiency over the full grid voltage is depicted. It is obvious that the switching losses are the dominant part in this operation mode because the efficiency at 340 V is higher compared to 420 V. The turns ratio given in Table I is in step-up mode sufficient to fulfill a constant voltage over the full power range on HV side of the transformer. Therefore, the AC-HB-CF-PP topology can

be used both with the novel modulation scheme in step-down as well as in step-up mode with a traditional one, over the full power range. However, in part-load, the efficiency is lower for step-up than for step-down mode. At the end of Section IV, the authors already mentioned that in step-up mode, the reactive power is needed for operation at part-load. Missing soft-switching capability and accruing conduction losses decrease the efficiency in this power range. At nominal power, the deviation between step-down and step-up mode is 0.5%, whereby step-up efficiency is lower. In this power range, the hard-switching operation of the transistors on the LV side occurs additionally. Therefore, the part-load behavior in step-up mode has to be investigated in further publications. The main focus should be a reduction of the reactive power, for example, by using other modulation schemes [43]. Nevertheless, at nominal load in step-up mode, the prototype of the AC-HB-CF-PP topology shows efficiencies in the same range as their counterparts [32], [44].

### C. Topology Classification

A comprehensive comparison between the proposed topology and other galvanically isolated bidirectional dc-dc converter topologies is shown in Table VIII. Based on an extensive literature study, a comparison of the numbers of components, efficiency, power, and voltage ratio of the bidirectional topologies flyback, resonant converter, and voltage and CF DAHB are summarized, which will be compared to the AC-HB-CF-PP in the following. Considering the application of semiconductors and passive components on the primary and secondary sides, the proposed topology is located in the mid-range compared to the previously mentioned converters. The flyback topology can also fulfill the power and voltage range requirements discussed in this article [11], [12], but hardware and control effort are more complex instead of the AC-HB-CF-PP topology and using the novel modulation scheme. Capable of soft-switching, the resonant converter achieves high efficiency at the nominal operating point and shows a good EMI behavior, and the leakage inductance can be advantageously used in resonant operation. The dc-dc converter shown in [17] and [18] have similar requirements and also different step-down and step-up characteristics like the AC-HB-CF-PP topology. The voltage-fed DAHB exhibits a high capacitor stress due to high ripple current, and similar to the voltage-fed DAHB, the CF DAHB requires different modulation methods and current waveforms to achieve the highest efficiency at each operating point. In the power range of 1 kW, [45] uses already the full-bridge topology. The AC-HB-CF-PP proposed in this article shows a plain design with similar component count and a simple control structure using one duty cycle for controlling the power transfer and achieving soft-switching. The laboratory demonstrator attains a high efficiency of more than 95% over a wide range of the output power, a power density of 9.5 W/in$^3$, and good EMI behavior [39].

## VI. Conclusion

A novel and advanced modulation scheme for step-down operation of a bidirectional and isolated AC-HB-CF-PP converter is introduced in this article. The AC circuit in combination with the LV side inductor $L_C$ is used to achieve ZVS of the HV side transistors in step-down mode over the full power range. Additional overvoltage stress, voltage spikes, and reverse-recovery for the transistors on the LV side will be reduced. By using the advanced modulation scheme, the effective turns ratio of the transformer can be extended over the traditional one in step-down mode. For step-down and step-up modes, the topology is analyzed in time-domain and validated by measurements. The measured peak efficiencies of the prototype are 96.6% in step-down operation and 96.1% in step-up mode. Compared with the bidirectional types of the flyback, *LLC*, and DAHB, this article shows an interesting alternative for converter topologies in the power range of 1 kW.

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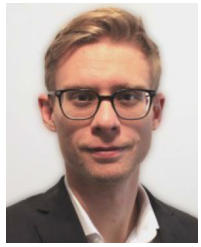
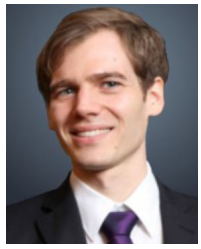


**Matthias Schulz** (Member, IEEE) received the B.Eng. degree in electrical engineering and information technology from the University of Applied Science Amberg-Weiden, Amberg, Germany, in 2012, and the M.Sc. degree in electrical engineering from Friedrich-Alexander University Erlangen-Nuremberg, Erlangen, Germany, in 2015. He is currently working toward the Ph.D. degree in electrical engineering with Friedrich-Alexander University Erlangen-Nuremberg, Erlangen, Germany.

He is currently an Electrical Engineer with Siemens AG, Erlangen, Germany. From 2015 to 2020, he was an Electrical Engineer with the Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany. His current research interests include power electronic systems for ac and dc.

Mr. Schulz is the recipient of a Best Paper Award from the IEEE PELS Society.



**Stefan Ditze** received the Diploma degree in electrical engineering from the University Stuttgart, Stuttgart, Germany, in 2008.

He started his career with the Department of Vehicle Electronics, Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany. Since 2021, he has been a Team Leader of the Group RF Power Electronics and Electromagnetic Compatibility (EMC). His research interests include high-frequency power conversion, soft-switching topologies, resonant converters, inductive power transfer systems, wide-bandgap semiconductor devices, design automation, advanced optimization methods, and EMC simulation.