An Integrated Synchronization and Control Strategy for Parallel-Operated Inverters Based on *V–I* Droop Characteristics

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***Abstract*—Voltage–current (*V–I*) droop control is becoming a promising alternative to achieve proper power sharing among the parallel-operated voltage-sourced inverters (VSIs). Compared with the conventional droop control, this method has a simpler structure and a better dynamic performance because it saves the power loop (including the low-pass filters). However, due to the absence of the power loop related to the system frequency, the synchronization of VSIs becomes an intractable issue. To tackle this, a communication-free algorithm to synchronize and control the VSIs is proposed. Initially, the principle of *V–I* droop control is presented straightforwardly based on the virtual impedance. Then, a synchronization algorithm is incorporated into the *V–I* droop controller for accurate power sharing. This algorithm adaptively adjusts the phase step of each VSI according to the phase differences between VSI and the ac bus. In this way, the phase differences of each VSI to the ac bus eventually converge to an identical value, thus realizing the synchronization of VSIs. A detailed parameter design method is also implemented considering both system stability and power quality. Finally, the proposed strategy is validated experimentally using a three-parallel-VSIs system.**

***Index Terms*—Synchronization algorithm, virtual impedance, voltage-current droop, voltage-sourced inverter.**

I. Introduction

DROOP control has become the focus of research in recent years due to its advantages of communication-free and high reliability. It has been widely used in UPS and islanded microgrid fields to realize the independent operation of islanding systems and the accurate power distribution among voltage-sourced inverters (VSIs) [1]–[3]. However, the traditional power droop control method has the following three main problems.

1) Low-pass filters (LPF) in the power calculation loop of the conventional power droop controller deteriorate the dynamic response [4].
2) The conventional droop control is vulnerable to voltage, frequency and power fluctuations due to *P–f* / *Q–V* (or *Q–f* / *P–V*) droop characteristics. Especially in low voltage networks, where short lines with small impedance are adopted, a small deviation in voltage and frequency will cause large power oscillation and even instabilities [5]–[7].
3) The different and unknown output impedances and line impedances may lead to power coupling and low power sharing accuracy [8].

To overcome the above problems, several improved droop control methods have been proposed, which are well-reviewed in [9], including the variants of droop control methods, the virtual structure-based methods, the construct- and compensate-based methods, and the hybrid droop/signal-injection-based methods. Among them, virtual impedance is a typical method that can realize power decoupling and improve power sharing accuracy [10], [11]. The virtual impedances simulate the actual impedances by subtracting the voltage drop of the virtual impedances from the voltage reference. Therefore, the virtual impedances can be changed accordingly to be pure inductive, pure resistive, or inductive–resistive [12], [13]. However, when designing virtual impedances, the value of output impedances and line impedances should be known in advance. Although the line impedances can be obtained through measurements or the grid parameter estimator proposed in [14], it is difficult to accurately acquire the output impedances, due to the harmonic injection and signal acquisition error. To tackle this, the feed-forward compensation of output currents becomes a more practical and effective way, in which the output impedance is eliminated by feeding forward the output current [15].

Although virtual impedance-based droop control methods are effective when decoupling the power and enhancing the power sharing accuracy, the inherent poor dynamics and nonlinearity introduced by the power loop can not be eliminated. To further improve the performance of the parallel-operated VSIs, *V–I* droop characteristic-based methods are proposed to achieve a

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proper power distribution among VSIs through voltage control, rather than power control [16]–[22]. With the absence of power calculation and power droop loop, the proposed *V–I* droop control has the following advantages.

1) Due to the absence of LPF in the power loop, the *V–I* droop control possesses better dynamics [16]–[20].
2) Unlike the nonlinear power droop controller, the *V–I* droop controller is essentially a linear voltage controller. As a result, it has simpler system features and is more straightforward when designing the droop coefficients [17].
3) Compared with the conventional droop control, it enhances stability since adding a *V–I* droop loop is equivalent to providing increased damping [20]. Eigenvalue analysis also shows that the proposed method features improved damping [18].

Recently, the above advantages of *V–I* droop characteristic-based control have been well validated and widely recognized. However, the obstacle of this method is that with the power loop removed, the resilient synchronization mechanism of VSIs is also eliminated. To handle this, one VSI is set as a master and a synchronized signal is sent to all other VSIs (slave VSIs) in [16], such operation reduces the reliability of the system. Guan *et al.* [17] reveal that when a phase-locked loop (PLL) is applied in a distributed manner to collect local output voltage phase angle, rather than the phase of ac bus voltage, the VSI is inherently endowed an $I_{oq}-\omega$ droop characteristic. In this case, the exit of any VSI will not affect the normal operation of other VSIs, but the applied PLL will limit the control bandwidth and deteriorate system stability. In [18]–[20], a global positioning system (GPS) is utilized as a time reference. In this case, the accurate power sharing is affected by the GPS delay, and the failure of the GPS leads to the collapse of the entire system. Accordingly, Zhao and Yang [21] propose a self-synchronous method based on local information. However, the circulating current between VSIs during the transient process has not been considered. Although the circulating current is suppressed through a transient large resistance in [22], the synchronization is only a one-time operation. Due to which, the phase error between VSIs is inevitable during the regular calibration gaps. The virtual oscillator control (VOC) has been carried out recently in [23] and [24], which applies the oscillator synchronization characteristic to parallel inverters control without communication. However, VOC adopts a completely different baseline controller compared with the common-used dual-loop control.

In summary, the *V–I* droop characteristic-based method is a promising alternative to control the parallel-operated VSIs, however, the existing synchronization methods are either unreliable or inaccurate. Therefore, a communication-free synchronization strategy is proposed to facilitate the development of *V–I* droop control. This synchronization strategy adaptively adjusts the phase step of each VSI according to the phase difference between VSI and the common ac bus. In this way, the phase differences of each VSI to the ac bus eventually converge to an identical value, thus realizing the synchronization of each VSI. The main advantages of the proposed synchronization method can be summarized as follows.

1) *It Possesses High Accuracy*: The parallel-operated VSIs are strictly synchronized by using local measurements, and this method will not be affected by perturbations, such as VSI switches and load changes.
2) *It Enables Soft Hot-Swap Capability*: The presynchronization and synchronization can be achieved with the same controller.
3) *It Endows Excellent Reliability*: The exit of any VSI will not affect the normal operation of other VSIs.

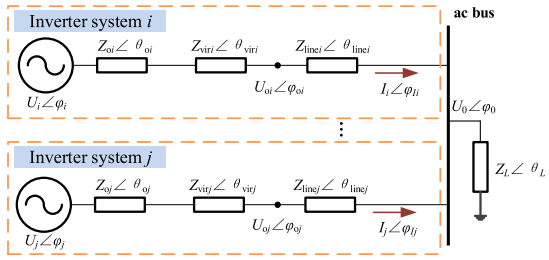

Fig. 1. Equivalent circuit of parallel VSIs.

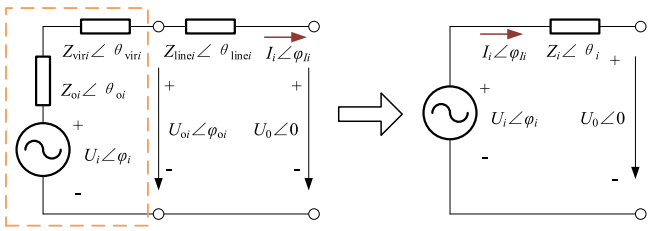

Fig. 2. Equivalent circuit of single VSI.

The rest of this article is organized as follows. In Section II, the power flow of the parallel system is analyzed when the virtual complex impedances are applied. The principle of *V–I* droop controller is presented straightforwardly with a universal parameter design method in Section III. Section IV proposes a synchronization algorithm with detailed analysis and full validation. Experiments are conducted in Section V to verify the effectiveness of the proposed synchronization method and power sharing strategy. Finally, Section VI concludes this article.

II. Power Flow Analysis of the Parallel System

The equivalent circuit diagram of parallel VSIs is shown in Fig. 1, and the simplified circuit of a single VSI is presented in Fig. 2. Where, $U_0\angle\varphi_0$ is the ac bus voltage ($U_0\angle0$ is assumed as a reference), $Z_L\angle\theta_L$ is the load impedance, $U_i\angle\varphi_i$ and $U_j\angle\varphi_j$ are the no-load output voltages, $U_{oi}\angle\varphi_{oi}$ and $U_{oj}\angle\varphi_{oj}$ are the output voltages, $I_i\angle\varphi_{Ii}$ and $I_j\angle\varphi_{Ij}$ are the output currents, $Z_{oi}\angle\theta_{oi}$ and $Z_{oj}\angle\theta_{oj}$ are the inherent output impedances, $Z_{viri}\angle\theta_{viri}=R_{viri}+jX_{viri}$ and $Z_{virj}\angle\theta_{virj}=R_{virj}+jX_{virj}$ are the virtual impedances, $Z_{linei}\angle\theta_{linei}=R_{linei}+jX_{linei}$ and $Z_{linej}\angle\theta_{linej}=R_{linej}+jX_{linej}$ are the line impedances of VSI#*i* and VSI#*j*, respectively. The combined impedance $Z_i\angle\theta_i=R_i+jX_i$ is the sum of $Z_{oi}\angle\theta_{oi}$, $Z_{viri}\angle\theta_{viri}$, and $Z_{linei}\angle\theta_{linei}$.

According to Fig. 2, the active power P_i and reactive power Q_i provided by VSI$_i$ to the load can be obtained as

$$\begin{cases} P_i=\frac{U_iU_0}{Z_i}\cos(\theta_i-\varphi_i)-\frac{{U_0}^2}{Z_i}\cos\theta_i \\ Q_i=\frac{U_iU_0}{Z_i}sin(\theta_i-\varphi_i)-\frac{{U_0}^2}{Z_i}\sin\theta_i. \end{cases} \tag{1}$$

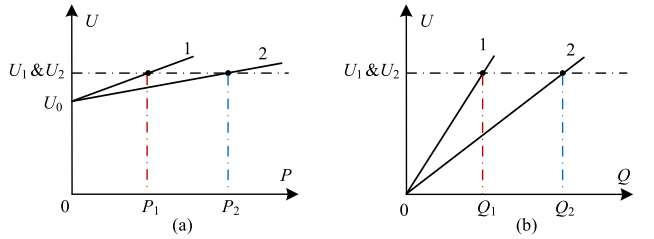

Fig. 3. Effect of combined resistances on power sharing. (a) *P–U* curves. (b) *Q–U* curves.

Since $Z_i\angle\theta_i$ is very small relative to $Z_L\angle\theta_L$, we have $\sin\varphi_i \approx \varphi_i$,$\cos\varphi_i \approx 1$. Substitute them into (1), and we can get

$$\begin{cases} P_i = \frac{U_0}{Z_i}[(U_i - U_0)\cos\theta_i + U_i\varphi_i\sin\theta_i] \\ Q_i = \frac{U_0}{Z_i}[(U_i - U_0)\sin\theta_i - U_i\varphi_i\cos\theta_i]. \end{cases} \tag{2}$$

For the combined impedance $Z_i\angle\theta_i$, on the one hand, the inherent output impedance $Z_{oi}\angle\theta_{oi}$ is usually unknown and different from each other that affected by plant and control parameters. Due to the harmonic injection and signal acquisition error, it is also difficult to accurately acquire the inherent output impedance. To eliminate the output impedance, a feed-forward loop of output current is adopted in this article. On the other hand, since the line impedance $Z_{\text{line}i}$ is practically very small in small-scale systems, a larger $R_{\text{vir}i}$ becomes the predominant component of $Z_i\angle\theta_i$ [17]. However, a virtual complex impedance Z_{vir} composed of a virtual resistance R_{vir} and a virtual inductance L_{vir} is preferred when the line impedances can be easily obtained through measurements or a grid parameter estimator [14]. In this case, L_{vir} is designed to counteract the line inductance L_{line}, whereas R_{vir} is constructed to realize the power sharing among VSIs. Thereafter, $Z_i\angle\theta_i$ will be determined only by the combined resistance R_i. Substitute $Z_i\angle\theta_i = R_i$ into (2), then we can present

$$\begin{cases} P_i = \frac{U_0}{R_i}(U_i - U_0) \\ Q_i = -\frac{U_iU_0}{R_i}\varphi_i. \end{cases} \tag{3}$$

For each VSI, U_0 is identical, and U_i can also be controlled to be equal. Therefore, according to (3), the output active power P_i of each VSI is inversely proportional to its combined resistance R_i. If the voltage phase φ_i of each VSI can be unified, then the output reactive power Q_i is also inversely proportional to the combined resistance R_i.

Fig. 3 takes two VSIs as an example to further illustrate the principle that R_i affects the power distribution among VSIs. In Fig. 3, curves 1 and 2 are the relation curves between the output power and the voltage magnitudes of VSI#1 and VSI#2, respectively. The slopes of the curves represent the combined resistances. Since $U_1 = U_2$ can be easily realized by the voltage controller, if R_1:R_2 = 2:1, then we can get P_1:P_2 = 1:2. Similarly, if $\varphi_1 = \varphi_2$ is achieved, then we have Q_1:Q_2 = 1:2. It is apparent that combined resistances determine the power sharing ratio of VSIs, which plays the role of the droop coefficient in the traditional droop control.

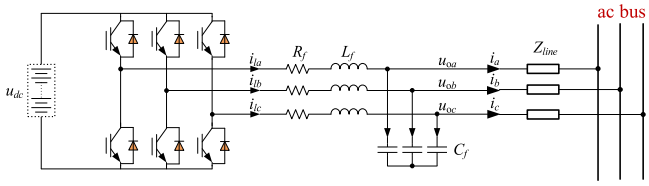

Fig. 4. Circuit diagram of VSI connected to the ac bus.

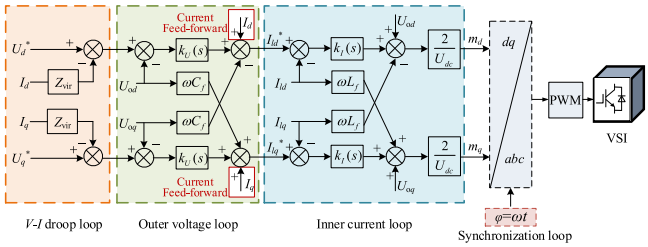

Fig. 5. Block diagram of *V–I* droop controller.

In conclusion, the proper power sharing among VSIs can be achieved when the combined impedances of VSIs are resistive and the combined resistances are correspondingly proportional; and the voltage phases of VSIs are synchronized. In the following Sections III and IV, the *V–I* droop controller and the synchronization strategy are presented, respectively, to address the above two issues.

III. Design of the *V–I* Droop Controller

A. Control Loop Design

The detailed structure of a VSI connected to the ac bus is shown in Fig. 4, where L_f is the filter inductance, R_f is the resistance of the filter inductor, C_f is the filter capacitance, Z_{line} is the line impedance, u_{dc} denotes the dc voltage, $u_{o\,abc}$ represents the output three-phase voltage, and i_{labc} and i_{abc} are the inductor three-phase current and output three-phase current, respectively.

The block diagram of the *V–I* droop controller in frequency-domain and *dq*-frame is presented in Fig. 5 to control the VSI depicted in Fig. 4, where superscript $*$ denotes the corresponding reference value, $K_I(s) = k_{pI} + k_{iI}/s$ and $K_U(s) = k_{pU} + k_{iU}/s$ are the compensators of current loop and voltage loop, respectively. As can be seen, the *V–I* droop controller is based on voltage/frequency (*V/f*) control where the output voltage references are provided by the droop loop and the frequency is offered by the synchronization loop. Besides, it is noted that the output impedance of VSI is suppressed through the current feed-forward loop.

B. Parameters Design

According to [25], the formulas to calculate the compensator parameters in the current loop are given as

$$k_{pI} = L_f/\tau_i \tag{4}$$

$$k_{iI} = R_f/\tau_i \tag{5}$$

where τ_i is the time constant of the current loop, which should be small enough to improve the fast response-ability of the current loop, while large enough to ensure that the bandwidth $1/\tau_i$ is less than the switching angular frequency of the inverter.

In addition, the compensator parameters of the voltage loop are obtained by the following formulas [26] as:

$$k_{pU} = \frac{C_f}{\tau_i}\left(\frac{1-\sin\gamma}{1+\sin\gamma}\right)^{\frac{1}{2}} \tag{6}$$

$$k_{iU} = \frac{C_f}{{\tau_i}^2}\left(\frac{1-\sin\gamma}{1+\sin\gamma}\right)^{\frac{3}{2}} \tag{7}$$

where the phase margin γ is typically chosen as 40°–50°.

As for the combined resistance, a larger R_i will improve the power sharing accuracy, whereas it will cause a larger magnitude deviation of the ac bus voltage. Therefore, the value of R_i should be restricted by the voltage quality requirement of the ac bus. According to Fig. 2, when $Z_i\angle\theta_i = R_i$, only if $\varphi_i = \varphi_{Ii}$, the ac bus voltage has a minimum magnitude of $U^* - I_iR_i$. In this case, R_i can be selected as

$$R_i \le \frac{U^* - U_{0\min}}{I_{i\max}} \tag{8}$$

where $U_{0\min}$ is the minimum voltage magnitude permitted by the ac bus, $I_{i\max}$ is the maximum output current of VSI#i. $U^* = U_N$ and $U_{0\min} = 0.93U_N$ are adopted in this article, which conforms to IEEE std. 1547−2003 [27]. The ac bus voltage deviation can also be compensated through a secondary control, which ensures that the voltage deviation is regulated toward zero after every change of load or generation inside the microgrids [19].

IV. Proposed Synchronization Algorithm

According to the analysis conducted in Section II, the accurate reactive power sharing requires that the voltage phase of each VSI is the same. The traditional PLL-based approach adopts a master VSI to offer a fixed reference phase angle. However, due to the dispersion of VSIs, each slave VSI can only synchronize to the ac bus, rather than the master VSI. In this case, the phase of each slave VSI is unable to be equalized to the phase of the master VSI. Besides, when the PLL-based master–slave method is applied, once the master VSI is out of operation due to failures or maintenances, another normal VSI must be switched to be the master VSI. Otherwise, the system will turn into an abnormal operation. To tackle the aforementioned issues, a novel synchronization method is proposed, which can precisely synchronize all VSIs, and the exit of any VSI will not affect the normal operation of other VSIs.

A. Principle of the Proposed Synchronization Algorithm

The key purpose of the synchronization algorithm is to equalize the voltage phases of all VSIs, so as to ensure that the reactive power is strictly distributed according to the droop coefficients. To achieve this, a communication-free algorithm to synchronize the VSIs is proposed. The algorithm adaptively adjusts the phase step of each VSI according to the phase difference between each VSI and the ac bus. In this way, the phase differences of each

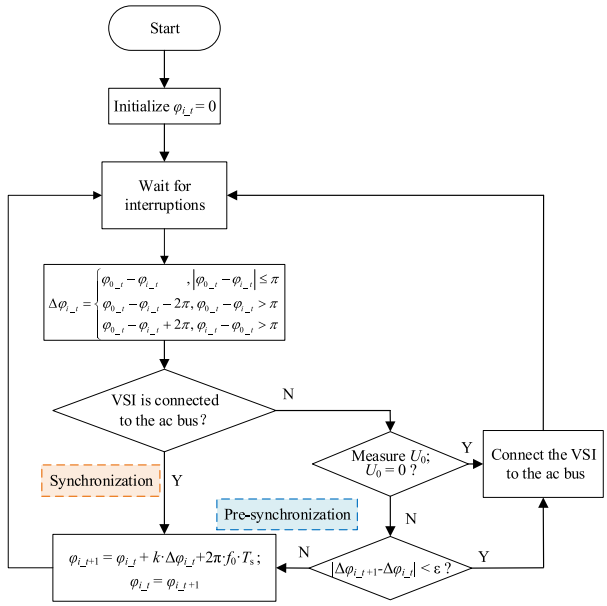

Fig. 6. Flowchart of the synchronization algorithm.

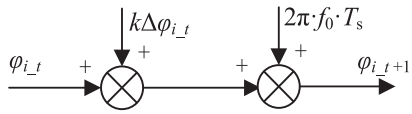

Fig. 7. Equivalent diagram of the synchronization control.

VSI to the ac bus will eventually converge to an identical value, thus realizing the synchronization of each VSI.

The flowchart and the control diagram of the proposed synchronization algorithm are shown in Figs. 6 and 7, respectively. As can be seen, the control expression of the synchronization algorithm is presented as

$$\varphi_{i\_t+1} = \varphi_{i\_t} + k\Delta\varphi_{i\_t} + 2\pi f_0 T_s. \tag{9}$$

Being

$$\Delta\varphi_{i\_t} = \begin{cases} \varphi_{0\_t} - \varphi_{i\_t} & , \ |\varphi_{0\_t} - \varphi_{i\_t}| \le \pi \\ \varphi_{0\_t} - \varphi_{i\_t} - 2\pi, & \varphi_{0\_t} - \varphi_{i\_t} > \pi \\ \varphi_{0\_t} - \varphi_{i\_t} + 2\pi, & \varphi_{i\_t} - \varphi_{0\_t} > \pi \end{cases}$$

where subscript t denotes the corresponding value at the interruption of t, while subscript $t+1$ denotes the corresponding value at the interruption of $t+1$; k is the proportional coefficient, f_0 is the fundamental frequency, and T_s represents the interruption period.

The steps of synchronous control are as follows. Firstly, set the initial phase angle as $\varphi_{i\_t} = 0$. Then check whether the VSI#i has been connected to the ac bus, if so, enable the synchronization algorithm as shown in (9). If not, measure the ac bus voltage. If $U_0 = 0$, it means that it is the first VSI to be connected and can be connected directly. If $U_0 \neq 0$, presynchronization is needed to suppress the inrush current. When the presynchronization is completed (i.e., $|\Delta\varphi_{i\_t+1}\text{-}\Delta\varphi_{i\_t}| < \varepsilon$, where ε is a minimum

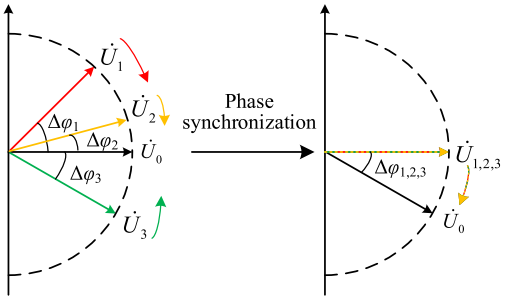

Fig. 8. Phase synchronization process.

value very close to zero) and the VSI is connected, the synchronization can be activated. As can be seen from Fig. 6, the presynchronization and synchronization adopt the same control algorithm of (9), that is, the proposed control algorithm can achieve both presynchronization and synchronization.

Fig. 8 shows the phase synchronization process with the proposed algorithm. Take a 3-VSI system as an example, initially, VSI#1 and VSI#2 are leading ac bus, while VSI#3 is lagging, which means $\Delta\varphi_1$ and $\Delta\varphi_2$ are negative, and $\Delta\varphi_3$ is positive. Therefore, according to the proposed algorithm, the voltage phase of VSI#1 and VSI#2 will decrease, while the voltage phase of VSI 3 will increase proportionately to $\Delta\varphi_1$, $\Delta\varphi_2$ and $\Delta\varphi_3$, respectively. Finally, all VSIs will synchronize with each other. Since if the VSIs are not synchronized, the phase differences $\Delta\varphi_i$ are not the same, i.e., the phase steps $k\Delta\varphi_i$ are not the same, which means that the VSIs will continue changing their phase accordingly, until all VSIs are synchronized. It is noted that since the ac bus voltage is generated by the connected VSIs in an islanded microgrid, although all VSIs will be synchronized eventually, the VSIs may not be synchronized to the ac bus due to the inductive loads.

B. Convergence Analysis

Variance σ^2 is introduced to further characterize the degree of synchronization of VSIs. If the variance of VSI phases decreases, it indicates that VSIs tend to be synchronized. The variance difference can be presented as

$$\begin{aligned}\Delta\sigma_{t+1}^2 = \sigma_{t+1}^2 - \sigma_t^2 &= \frac{1}{N}\sum_{i=1}^{N}\left(\varphi_{i\_t+1} - \sum_{i=1}^{N}\frac{\varphi_{i\_t+1}}{N}\right)^2 \\ &\quad - \frac{1}{N}\sum_{i=1}^{N}\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)^2 \\ &= \frac{1}{N}\sum_{i=1}^{N}\left[(\varphi_{i\_t} + k\Delta\varphi_{i\_t}) - \sum_{i=1}^{N}\frac{(\varphi_{i\_t} + k\Delta\varphi_{i\_t})}{N}\right]^2 \\ &\quad - \frac{1}{N}\sum_{i=1}^{N}\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)^2 \\ &= \frac{1}{N}\sum_{i=1}^{N}\left[\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)\right. \\ &\quad + \left.\left(k\Delta\varphi_{i\_t} - \sum_{i=1}^{N}\frac{k\Delta\varphi_{i\_t}}{N}\right)\right]^2 \\ &\quad - \frac{1}{N}\sum_{i=1}^{N}\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)^2 \\ &= \frac{1}{N}\sum_{i=1}^{N}\left[2\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)\right. \\ &\quad \times \left(k\Delta\varphi_{i\_t} - \sum_{i=1}^{N}\frac{k\Delta\varphi_{i\_t}}{N}\right) \\ &\quad + \left.\left(k\Delta\varphi_{i\_t} - \sum_{i=1}^{N}\frac{k\Delta\varphi_{i\_t}}{N}\right)^2\right]. \end{aligned} \tag{10}$$

Since $\Delta\varphi_{i\_t} = \varphi_{0\_t}$ - φ_{i_t}, we have

$$k\Delta\varphi_{i\_t} - \sum_{i=1}^{N}\frac{k\Delta\varphi_{i\_t}}{N} = -k\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right). \tag{11}$$

Substitute (11) into (10), then we can get

$$\begin{aligned}\Delta\sigma_{t+1}^2 &= \frac{1}{N}\sum_{i=1}^{N}\left\{2\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)\right. \\ &\quad \times \left[-k\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)\right] + \left.\left[k\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)\right]^2\right\} \\ &= \frac{-2k + k^2}{N}\sum_{i=1}^{N}\left(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N}\right)^2 \le 0, \quad (0 < k < 2). \end{aligned} \tag{12}$$

It can be seen from (12) that as long as k is in the range of (0, 2), the variance difference is less than or equal to 0, and it is equal to 0 only if $\sum_{i=1}^{N}(\varphi_{i\_t} - \sum_{i=1}^{N}\frac{\varphi_{i\_t}}{N})^2 = 0$. In other words, the variance of the voltage phases of VSIs will decrease until all VSIs are synchronized.

From the derivation process, it also can be concluded that as long as the φ_{0_t} is identical for each VSI, all VSIs will be synchronized finally. Therefore, the proposed synchronization method can realize both presynchronization and synchronization. Besides, it can also be pointed out that the synchronous reference point can be any point in the grid, as long as the φ_{0_t} is the same for all VSIs. And a synchronous reference point that is physically closer to all VSIs is the preferred option, as opposed to a relatively distant ac bus. However, it is also because of this that the presynchronization is a quasi-synchronization, in which the disconnected VSIs are synchronized to the connected VSIs, rather than the ac bus. Since the phase difference between the connected VSIs and the ac bus is very small, the inrush current caused by a new VSI connection is negligible.

TABLE I
SYSTEM PARAMETERS

Circuit parameters	Value	Control parameters	Value
Rated capacity S	2.2 kVA	Voltage reference U_d^*	311 V
DC voltage U_{dc}	650 V	Voltage reference U_q^*	0 V
Rated ac voltage U_N	380 V	Time constant of current loop τ_i	1 ms
Fundamental frequency f_0	50 Hz	Current proportional term k_{pI}	1.8
Switch frequency f_s	10 kHz	Current integral term k_{iI}	10
Filter resistance R_f	10 mΩ	Voltage proportional term k_{pU}	0.011
Filter inductance L_f	1.8 mH	Voltage integral term k_{iU}	1.9
Filter capacitance C_f	27 uF	Phase margin of voltage loop γ	45°
Line#1 impedance Z_{line1}	1 Ω + 1.2 mH	Cutoff frequency ω_c	417.8 rad/s
Line#2 impedance Z_{line2}	1 Ω	Interruption cycle T_s	0.1 ms
Line#3 impedance Z_{line3}	1.2 mH	proportional coefficient k	0.001
Load#1 impedance Z_{load1}	(57 + j12.6) Ω	Virtual#1 impedance Z_{vir1}	2 Ω - 1.2 mH
Load#2 impedance Z_{load2}	(115 + j24.7) Ω	Virtual#2 impedance Z_{vir2}	2 Ω
		Virtual#3 impedance Z_{vir3}	3 Ω - 1.2 mH

C. Proportional Coefficient Design

The selection of a proportional coefficient should maintain the frequency within an allowable deviation range. According to (9), the steady state frequency deviation can be given as

$$|\Delta f| = \frac{k\,|\Delta\varphi_{i\_t}|}{2\pi T_s} \le |\Delta f_{\max}|\,. \tag{13}$$

Then, the range of k is presented as

$$k \le \frac{2\pi\,|\Delta f_{\max}|\,T_s}{|\Delta\varphi_{i\_t}|}. \tag{14}$$

The maximum allowable frequency deviation introduced by the proposed synchronization algorithm is chosen as $|\Delta f_{\max}| = 0.2$ Hz [27]. In this case, the phase change introduced by the proposed synchronization algorithm is far smaller than that introduced by the constant frequency (50 Hz) control, i.e., the proposed synchronization control will not bring a phase jump issue. Based on (3), $\Delta\varphi_{i\_t}$ is determined as

$$\Delta\varphi_{i\_t} = -\frac{Q_i R_i}{U_i U_0}. \tag{15}$$

The range of k is not necessary to strictly follow (14), since the frequency deviation can also be compensated through a secondary control [19].

D. Validation of the Proposed Synchronization Algorithm

A mathematical model of a three-VSI system is developed in MATLAB to validate the proposed synchronization algorithm. The circuit diagram of parallel-VSIs is shown in Fig. 1, and the related circuit parameters and the calculated control parameters are given in Table I. In this case, only load#1 is adopted. The simulation results of the presynchronization and synchronization cases are shown in Fig. 9(a) and (b) respectively, in which t_i denotes the running time of VSI#i since it was connected. The simulation process is the same for presynchronization and synchronization cases: VSI#1 connect firstly, then VSI#2 connect, and VSI#3 connect finally. However, the ac bus voltage is only generated by VSI#1 in the presynchronization case, that is to say, VSI#2 and VSI#3 only activate the synchronization algorithm, but do not connect to the ac bus. Whereas, in the synchronization case, VSI#2 and VSI#3 are connected to the ac bus with the activated synchronization algorithm. Assume that the initial phase angles of VSI#2 and VSI#3 are 0 relative to $2\pi f_0 t_1$. Therefore, we only need to observe the increment of phases, i.e., $k\Delta\varphi_i\ t_i$, to determine if VSIs are synchronized. It can be seen from Fig. 9 that in both cases, VSIs will be synchronized eventually, which is consistent with the previous convergence analysis.

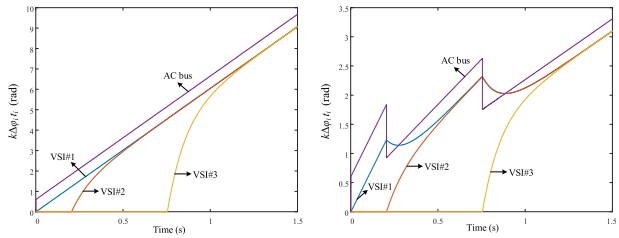

Fig. 9. Simulation results of the proposed algorithm. (a) Presynchronization case. (b) Synchronization case.

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed scheme, a detailed islanded experimental microgrid setup is built. As shown in Fig. 10, the setup consists of a dc source, three parallel-connected VSIs, *LC* filters, line impedances, resistive and inductive loads, a dSPACE1006 platform. The circuit parameters and control parameters are given in Table I. Considering that PLL is a common synchronization method and master–slave scheme is widely adopted when controlling the parallel-operated VSIs [16], the PLL-based master–slave scheme is selected as the benchmark. By comparing with the traditional PLL-based master–slave method [28], the effectiveness of the proposed synchronization method and the excellent current sharing performance in different scenarios of the proposed *V-I* droop controller are validated.

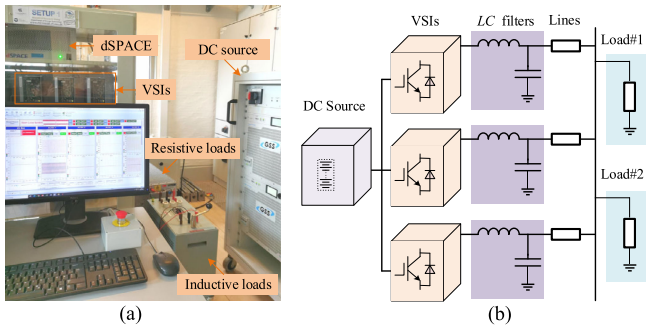

Fig. 10. Experimental setup and circuit diagram. (a) Experimental setup in laboratory. (b) Circuit diagram of the testing setup.

A. Synchronization Performance

The experimental validation of the proposed synchronization strategy is a two-step process. First, the performance in the presynchronization case is explored, in which the new VSIs are not connected to the ac bus. Then, the performance in the synchronization case is studied, in which the new VSIs are connected to the ac bus. In both cases, the synchronization performances of the proposed strategy are compared with the performances when a traditional PLL-based master–slave method is adopted.

1) Presynchronization Performance: Initially, VSI#1 (the master VSI for PLL-based master–slave method) supplies power to load#1, while VSI#2 and VSI#3 (slave VSIs for PLL-based master–slave method) are not started and disconnected. Then, VSI#2 starts and the presynchronization is activated simultaneously. Finally, VSI#3 starts and the presynchronization is activated. In the following text, the presynchronization process of VSI#3 is demonstrated and analyzed. Fig. 11(a.1) shows the presynchronization of VSI#3 when the traditional PLL-based master–slave method is adopted, which starts at $t = 0.02$ s. Whereas, Fig. 11(a.2) presents the enlarged waveforms when the presynchronization is completed at about $t = 0.985$ s. In contrast, Fig. 11(b.1) and (b.2) exhibit the presynchronization process when the proposed synchronization method is applied. It can be seen from the enlarged phase waveforms in Fig. 11(a.2) and (b.2) that the synchronization of slave VSIs to the ac bus is realized when PLL is used, while the synchronization between VSIs is realized by the proposed synchronization method. It can also be observed that the phase difference between the ac bus and the up-connecting VSIs is only 0.01 rad, which will not cause an inrush current.

2) Synchronization Performance: When the aforementioned presynchronization process is completed, the synchronization process is activated. Initially, VSI#1 supplies power to load#1, while VSI#2 and VSI#3 are presynchronized but disconnected. Then, VSI#2 is connected to the ac bus. Finally, VSI#3 is connected to the ac bus. In the following text, the synchronization process of VSI#3 is demonstrated and analyzed. Fig. 12(a.1) shows the synchronization of VSI#3 when the traditional PLL-based master–slave method is adopted, which starts at $t = 0.02$ s. However, Fig. 12(a.2) presents the enlarged waveforms when the presynchronization is completed at about $t = 0.97$ s. In contrast, Fig. 12(b.1) and (b.2) exhibit the presynchronization process with the proposed synchronization method. As depicted in Fig. 12(a.1) and (b.1), thanks to the excellent performance of presynchronization, no harmful transient occurs when VSI#3 is connected both with the PLL and the proposed method. However, when the PLL is adopted, the slave VSIs are synchronized to ac bus, rather than the master VSI#1, as shown in Fig. 12(a.2). In this case, the reactive power will not be accurately shared according to the analysis in Section II. On the contrary, the proposed method can realize the synchronization of each VSI, which is clearly displayed in Fig. 12(b.2).

B. Current Sharing Performance

Current sharing performances of the proposed controller is tested with different scenarios, including VSI connections, load changes, current sharing ratio changes, and VSI#1 exit.

1) VSI Connections: The experimental process of the VSI connections scenario is shown in Fig. 13. Initially, VSI#1 supplies power to load#1, while VSI#2 and VSI#3 are presynchronized but disconnected; then at $t = 2$ s, VSI#2 is connected to the ac bus; and at $t = 4.4$ s, VSI#3 is connected to the ac bus. Fig. 13 shows the experimental results to compare the performance of the PLL-based master–slave controller and the proposed controller. As can be seen from Fig. 13(a.1) and (a.2), with the PLL, although the direct current is evenly shared, the quadrature current can not be accurately distributed. The reason is that VSI#2 and VSI#3 are synchronized to the ac bus. In this case, according to (3), VSI#2 and VSI#3 will not output reactive power. Therefore, VSI#1 affords the whole quadrature current of the load. Besides, the phase differences between VSIs will cause reactive circulations, which further deteriorates the quality of the output quadrature currents, as can be observed in Fig. 13(a.2). In contrast, with the proposed synchronization method, not only the direct current is properly shared, but also the quadrature current is accurately distributed among VSIs, as presented in Fig. 13(b.1) and (b.2). Note that the phase difference between the no-load output voltage of VSI and the ac bus voltage is not zero when inductive loads are connected. Therefore, according to (3), the reactive power is not equal to zero, i.e., the quadrature current is not zero. As for the system frequency, since VSI#1 adopts constant frequency control in the PLL-based master–slave method, the system frequency can be accurately controlled to 50 Hz, as exhibited in Fig. 13(a.3). With the proposed method, although the system frequency is variable, it can be found from Fig. 13(b.3) that the system frequency is in the desired range of (50.05 Hz, 50.07 Hz), thanks to the proper design of k.

2) Load Changes: Initially, VSI#1, VSI#2, and VSI#3 operate in parallel with the same power rates to supply load#1; Then at $t = 1.6$ s, load#2 is connected to the ac bus; and at $t = 4.2$ s, load#2 is disconnected. The current sharing performance during the scenario of load changes is depicted in Fig. 14. Similarly, with the PLL-based master–slave method, although the direct current is properly shared when load changes, the quadrature current is output by VSI#1 alone. However, the proposed method can achieve the desired distribution of both direct current and quadrature current during the whole process.

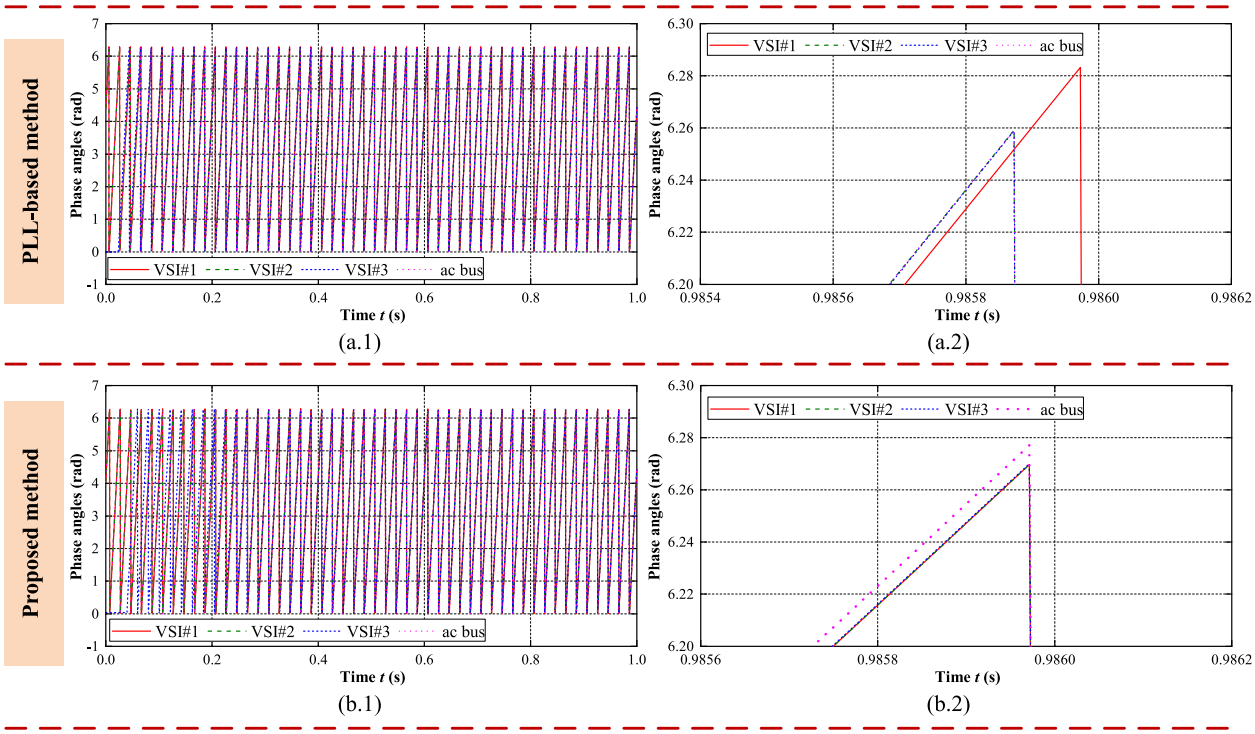

Fig. 11. Experimental results of the presynchronization process. (a.1) Phase angles of the no-load output voltages and ac bus voltage during the presynchronization process with the traditional PLL-based master–slave method. (a.2) Enlarged phase angles when the presynchronization is completed with the traditional PLL-based master–slave method. (b.1) Phase angles of the no-load output voltages and ac bus voltage during the presynchronization process with the proposed synchronization method. (b.2) Enlarged phase angles when the presynchronization is completed with the proposed synchronization method.

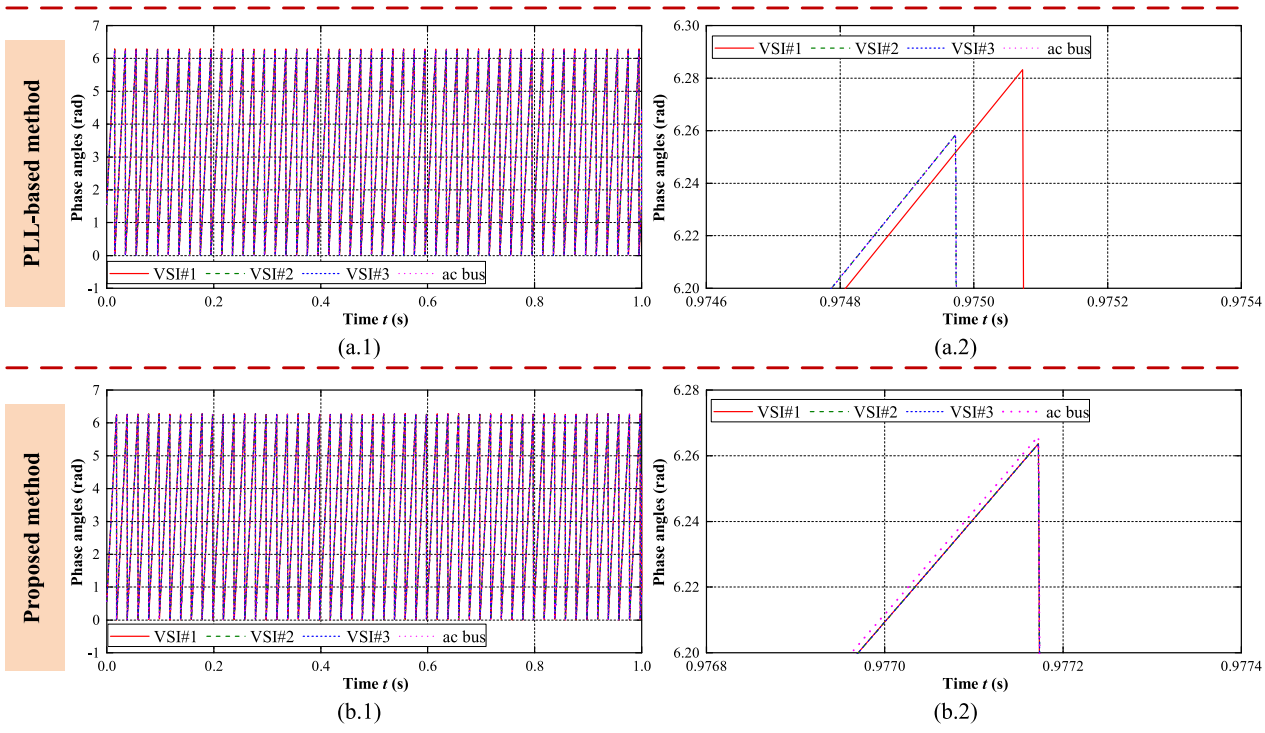

Fig. 12. Experimental results of the synchronization process. (a.1) Phase angles of the no-load output voltages and ac bus voltage during the synchronization process with the traditional PLL-based master–slave method. (a.2) Enlarged phase angles when the synchronization is completed with the traditional PLL-based master–slave method. (b.1) Phase angles of the no-load output voltages and ac bus voltage during the synchronization process with the proposed synchronization method. (b.2) Enlarged phase angles when the synchronization is completed with the proposed synchronization method.

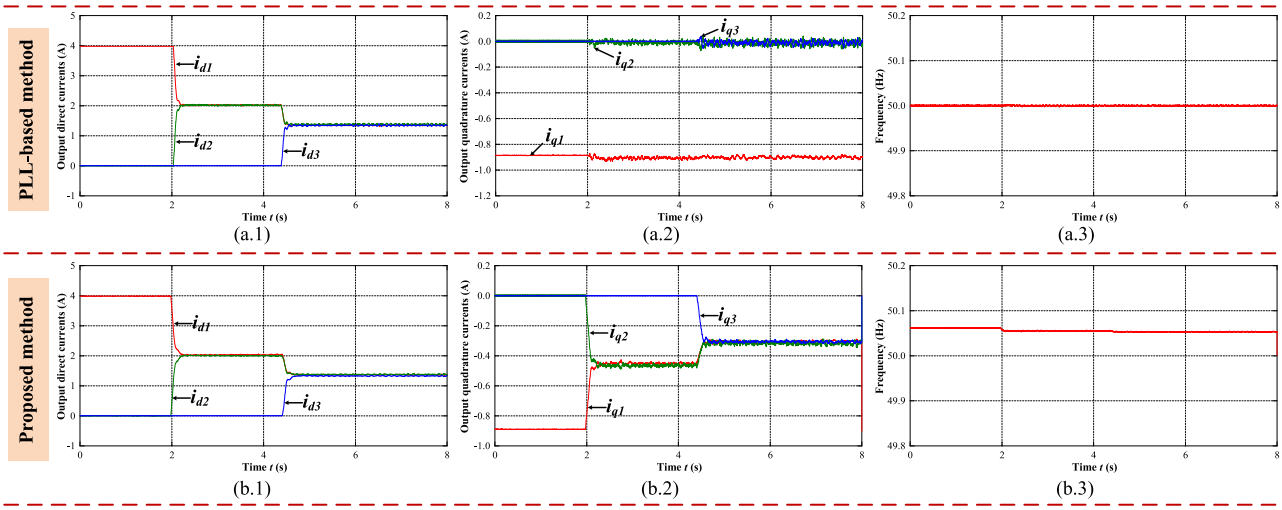

Fig. 13. Experimental results of the current sharing performance in VSI connections scenario. (a.1) Output direct currents with the PLL-based master–slave method. (a.2) Output quadrature currents with the PLL-based master–slave method. (a.3) AC bus frequency with the PLL-based master–slave method. (b.1) Output direct currents with the proposed method. (b.2) Output quadrature currents with the proposed method. (b.3) AC bus frequency with the proposed method.

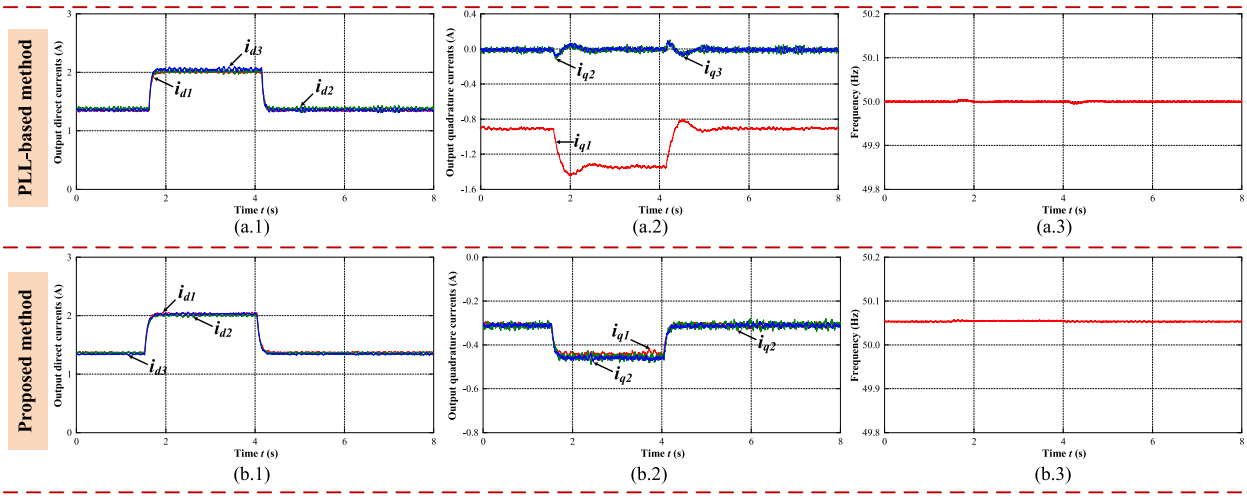

Fig. 14. Experimental results of the current sharing performance in load changes scenario. (a.1) Output direct currents with the PLL-based master–slave method. (a.2) Output quadrature currents with the PLL-based master–slave method. (a.3) AC bus frequency with the PLL-based master–slave method. (b.1) Output direct currents with the proposed method. (b.2) Output quadrature currents with the proposed method. (b.3) AC bus frequency with the proposed method.

3) Ratio Changes: The current sharing performance during the scenario of current sharing ratio changes is depicted in Fig. 15. In the beginning, VSI#1, VSI#2, and VSI#3 operate in parallel with load#1; then at $t = 1.6$ s, the current sharing ratio is changed from 1:1:1 to 3:2:1 by changing the combined resistance from $(R_1, R_2, R_3) = (3\ \Omega, 3\ \Omega, 3\ \Omega)$ to $(R_1, R_2, R_3) = (1\ \Omega, 1.5\ \Omega, 3\ \Omega)$; and at $t = 5.6$ s, the sharing ratio is changed back to 1:1:1. As depicted in Fig. 15(a.1) and (b.1), with both methods, the output direct currents of VSI#1, VSI#2 and VSI#3 change from approximately $(i_{d1}, i_{d2}, i_{d3}) = (1.35\ \text{A}, 1.35\ \text{A}, 1.35\ \text{A})$ to $(i_{d1}, i_{d2}, i_{d3}) = (0.67\ \text{A}, 1.35\ \text{A}, 2.5\ \text{A})$ after the ratio alteration, and restore to $(i_{d1}, i_{d2}, i_{d3}) = (1.35\ \text{A}, 1.35\ \text{A}, 1.35\ \text{A})$ when the ratio recovers. It can also be observed from Fig. 15(b.2) that with the proposed method, the output quadrature currents of VSI#1, VSI#2 and VSI#3 are properly distributed, changing from $(i_{q1}, i_{q2}, i_{q3}) = (-0.32\ \text{A}, -0.32\ \text{A}, -0.32\ \text{A})$ to approximately $(i_{q1}, i_{q2}, i_{q3}) = (-0.16\ \text{A}, -0.32\ \text{A}, -0.48\ \text{A})$ after the ratio alteration, and restore to $(i_{q1}, i_{q2}, i_{q3}) = (-0.32\ \text{A}, -0.32\ \text{A}, -0.32\ \text{A})$ when the ratio recovers. However, the quadrature current can not be shared when the PLL-based master–slave method is applied, as shown in Fig. 15(a.2).

4) VSI#1 Exit: Fig. 16 presents the transient response during the disconnecting of VSI #1. In the beginning, VSI#1, VSI#2 and VSI#3 operate in parallel with load#1; then at $t = 1.8$ s, VSI #1 is disconnected from the ac bus, while VSI#2 and VSI#3 still track the phase of the ac bus voltage. As can be found in Fig. 16(a.3), with the PLL-based master–slave method, the system frequency increases and eventually reaches the upper limit of the PLL (set as 55 Hz) when VSI#1 exits. The reason is that, when VSI#1 exits, the ac bus voltage is generated by VSI#2 and VSI#3 themselves and the phase of ac bus voltage is always ahead of the phases of VSI#2 and VSI#3 under inductive loads, a positive feedback mechanism is formed. In conclusion, when the traditional PLL-based master–slave method is adopted, not

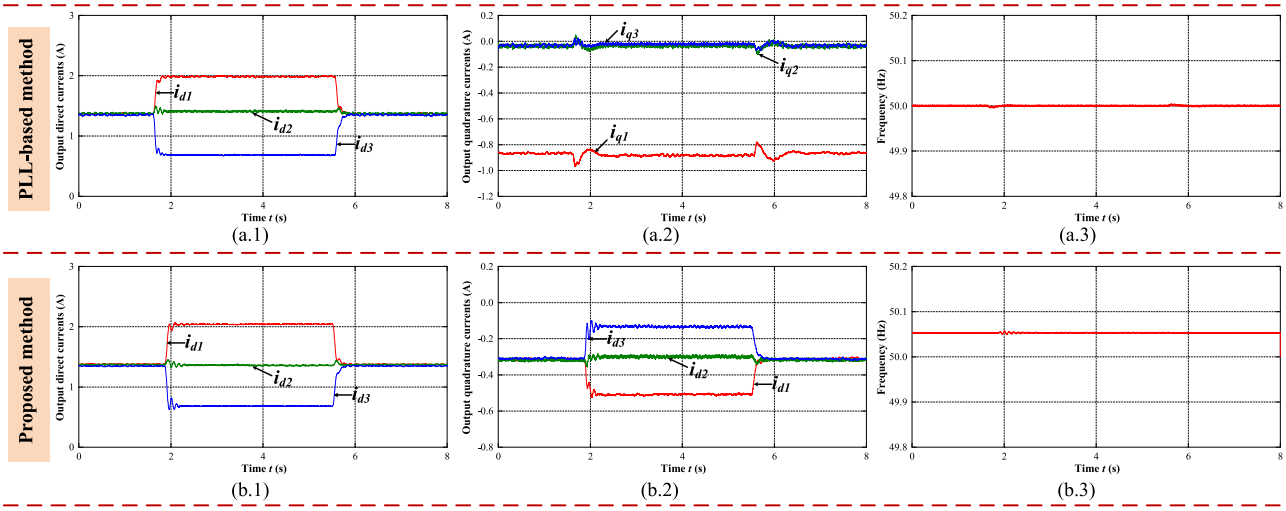

Fig. 15. Experimental results of the current sharing performance in ratio changes scenario. (a.1) Output direct currents with the PLL-based master–slave method. (a.2) Output quadrature currents with the PLL-based master–slave method. (a.3) AC bus frequency with the PLL-based master–slave method. (b.1) Output direct currents with the proposed method. (b.2) Output quadrature currents with the proposed method. (b.3) AC bus frequency with the proposed method.

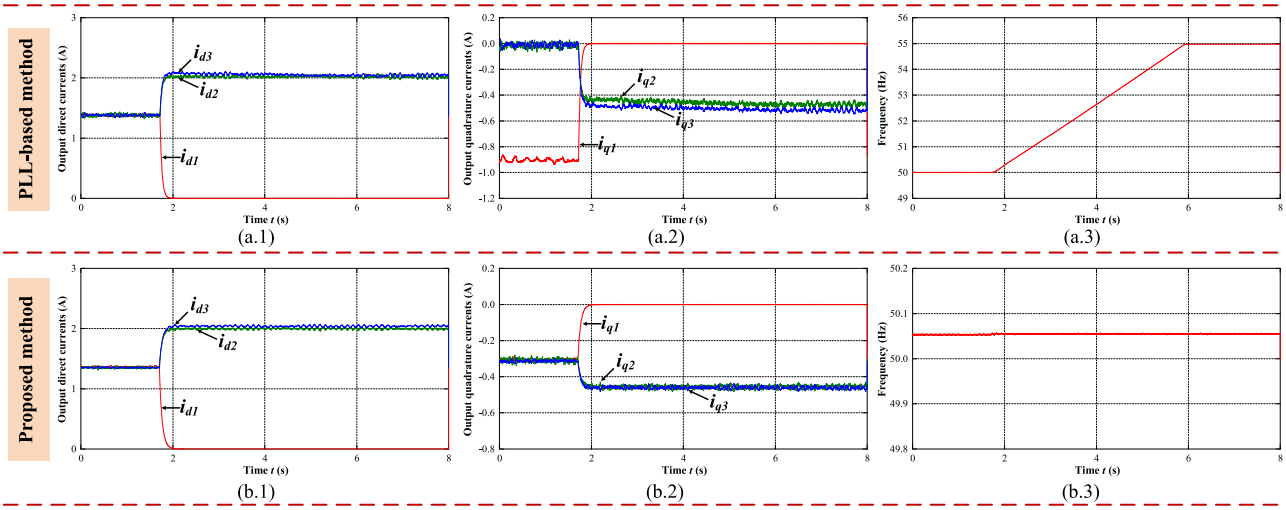

Fig. 16. Experimental results of the current sharing performance in VSI#1 exit scenario. (a.1) Output direct currents with the PLL-based master–slave method. (a.2) Output quadrature currents with the PLL-based master–slave method. (a.3) AC bus frequency with the PLL-based master–slave method. (b.1) Output direct currents with the proposed method. (b.2) Output quadrature currents with the proposed method. (b.3) AC bus frequency with the proposed method.

TABLE II
PERFORMANCE COMPARISON

	Traditional	***V-I* droop**		
	***P-V/Q-f* droop**	**PLL-based master-slave method**	**PLL-based distributed method [17]**	**Proposed method**
Control capability	Works well with resistive line impedance	Works well with resistive line impedance	Works well with resistive line impedance	Works well with resistive line impedance
Transient response	Slow, due to the LPF in power loop [4]	Fast, but the limited bandwidth of PLL may worsen it	Fast, but the limited bandwidth of PLL may worsen it	Fast
Plug and play feature	Yes, but an extra pre-synchronization loop is required [29]	Yes	Yes	Yes
Computation burden	High, due to the power calculation and power droop loop	High, due to the reference-frame transformations and trigonometric computations of PLL	High, due to the reference-frame transformations and trigonometric computations of PLL	Low
System characteristic	Non-linear, due to the power calculation loop	Non-linear, due to the PLL	Non-linear, due to the PLL	Linear

only the accurate sharing of reactive current cannot be realized, but also the system will turn to abnormal operation when the master VSI exits. However, with the proposed method, the output direct currents and quadrature currents of VSI #2 and VSI #3 increase from (i_{d2}, i_{d3}) = (1.35 A, 1.35 A) and (i_{q2}, i_{q3}) = (−0.32 A, −0.32 A) to (i_{d2}, i_{d3}) = (2.02 A, 2.02 A) and (i_{q2}, i_{q3}) = (−0.48 A, −0.48 A), respectively, to share the extra currents. Besides, the system frequency is stabilized at 50.055 Hz.

In summary, the experimental results reveal that, compared with the PLL-based master–slave method, the proposed control strategy endows excellent synchronization and current-sharing performance under various scenarios. The prominent features of the proposed strategy compared with the other droop control (including the traditional *P–V*/*Q–f* droop control, the PLL-based master–slave method and the PLL-based distributed method presented in [17]) are also given in Table II.

VI. Conclusion

In this article, a communication-free strategy to synchronize and control the parallel-operated VSIs is proposed, which endows accurate current sharing performance and ensures high reliability. First, by analyzing the power flow of the parallel system, the principle of *V–I* droop control is introduced straightforwardly. Then, a synchronization algorithm is incorporated into the *V–I* droop controller for accurately sharing the reactive power. This synchronization strategy adaptively adjusts the phase step of each VSI according to the phase differences between VSI and the ac bus. In this way, the phase differences of each VSI to the ac bus eventually converge to an identical value, thus realizing the synchronization of each VSI. The proposed algorithm can achieve both presynchronization and synchronization, and the exit of any VSI will not affect the normal operation of the whole system. Experimental results validate the excellent behavior of the proposed controller. However, there are still some limitations of the proposed strategy. Since the voltage phase of the ac bus is required in this controller, the proposed method is especially suitable for a cluster of centralized VSIs, in which the line impedances are negligible and the ac bus voltage can be easily obtained. In addition, it is also applicable to small-scale microgrids with low line impedance, where the ac bus voltage can be dragged to the terminal of VSI by the predominant virtual resistance. However, in large-scale microgrids, the grid parameters or communication lines are required to obtain the ac bus voltage and to better design the virtual complex impedances.

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