A Three-Terminal Submodule Based High DC Conversion Ratio System With Self-Balance Feature

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***Abstract*—The input series output parallel (ISOP) and input parallel output series (IPOS) systems have been extensively researched and applied in academia and industry due to the high dc conversion ratio. Practically, the ISOP and IPOS systems faced challenges, such as relatively immature high-voltage (HV) isolated high-frequency transformer (HFT), high reliability on HV isolated control system, difficulties in the auxiliary power supply (APS), start-up process, and bypass circuit/strategy. To overcome the above-mentioned challenges without adding complexities, this article proposes the three-terminal submodule (3TSM) as the fundamental SM for high dc conversion ratio step-up/step-down applications. Thanks to the 3TSM, the system is with self-balance feature, HV isolated HFTs are unnecessary, the control system is simplified (no matter in open or closed loop). Besides, commercial APSs can be adopted directly to the SM input capacitors without the unstable "runaway" phenomenon. A bypass circuit is also proposed to retain the power of APS when the SM is bypassed. A 2SM step-down and step-up prototype, together with a subsequent 10-kV input 1 kV/1 kW output converter is built to validate the effectiveness and practical feasibility of the proposed system.**

***Index Terms*—Self-balance feature, soft-switching, three-terminal submodule (3TSM).**

I. Introduction

RECENTLY, there has been a growing interest in power up to the bottom of the ocean floor for the submarine observation network [1]–[3]. The submarine observation network is divided into the coast station converter and the subsea converter. The coast station converter is a low-voltage dc (LVdc) input and a high-voltage dc (HVdc) output. The subsea converter is an HVdc input and an LVdc output. These two converters are interconnected by a photoelectric composite cable copper wire. In this application, the input series output parallel (ISOP) and input parallel output series (IPOS) systems, which use multiple submodules (SMs) in series and/or parallel at both the input and output sides, have been extensively researched and applied in academia and industry due to the advantages of redundancy, modular and scalable, sharing of SMs, reduced filter volume, and more crucially, the high dc conversion ratio [1], [4]–[10].

Although there are other types of high dc conversion ratio converters reported in [11]–[13], most of these topologies are not scalable or standardized. Some other topologies [14], [15] are only suitable for small power applications. The above-mentioned topologies have few advantages compared with the IPOS/ISOP systems. The system diagram of ISOP and IPOS systems and the typical diagram of SM topologies are depicted in Fig. 1. In the ISOP and IPOS systems, the HV-side SMs are in series, thus, SM sharing control (SHC) is required. Without SHC, the SM voltages in the HV side may diverge (i.e., the "runaway" phenomenon), and the voltage stress of one SM can be high enough to break down the power switches. The equilibrium among the SMs is widely studied and various SHC approaches have been proposed [5]–[8], [16]–[21]. As for the ISOP system, input voltage feedforward control [16] and wireless input voltage sharing (IVS) control [17] are specific implementations of IVS where all the input voltages of SMs are sampled. To transform the HV sampling circuit to the LV side, the cross feedback output current sharing (OCS) control [18], inverse droop control [19], and output current differential control [20] are specific implementations of OCS where the output current is sampled to rebalance the SMs. Three-loop decoupled control is proposed in [8] where the IVS loop can be designed independently. As for the IPOS system, input current sharing or output voltage sharing should be satisfied to achieve SHC. Practically, the SHC methods mentioned above require multiple voltage and current sensors, and the control system is very complex. To reduce the system complexity, common duty ratio control is proposed in [5] and [7] where every SM shares the same control signal. Although SHC is not achieved perfectly among the SMs due to parameter mismatch, the unstable "runaway" phenomenon is eliminated.

Although the ISOP and IPOS systems are theoretically modular, they are faced with multiple challenges practically. Generally, one terminal of the high voltage side is grounded to be the reference. The grounded terminal is denoted as the red sign in Fig. 1. Due to the SM connection, the galvanic isolation voltage of the transformer is much greater than the operation voltage, and designing these HV isolated transformers (together with bobbin, isolation, wires, and thermal) are challenging, both in medium-voltage low-power [22], [23] and high-power applications [24], [25]. When the system voltage rises, the HV isolated HFTs have to be redesigned.

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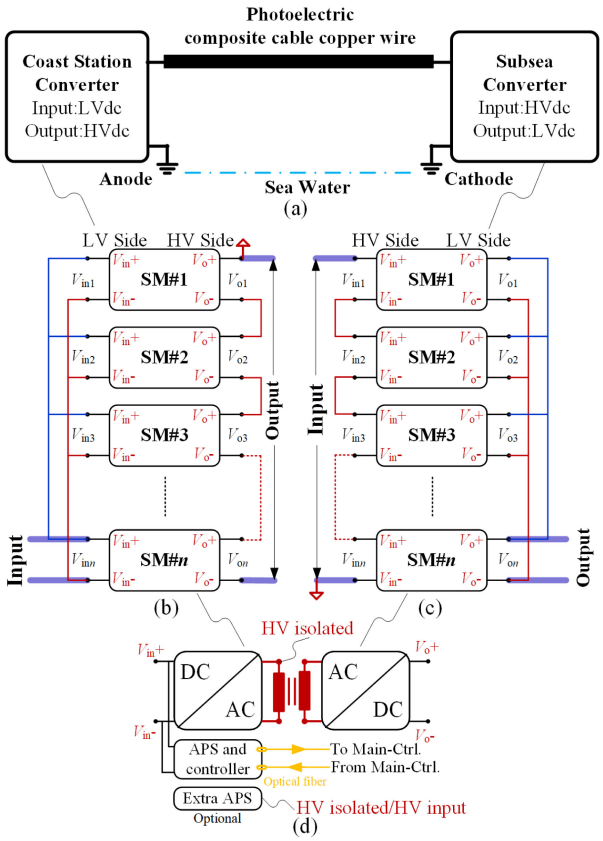

Fig. 1. (a) Diagram of the submarine observation network. (b) System diagram of the IPOS system to be a typical solution to the coast station converter. (c) System diagram of the ISOP system to be a typical solution to the subsea converter. (d) Typical diagram of SM topology of the IPOS/ISOP system.

On the other hand, the control system diagrams of the ISOP and IPOS systems are generally the main controller (Main-Ctrl.) and subcontroller (Sub-Ctrl.) structure, and these two controllers locate on the HV/LV and LV/HV side. As a result, HV feedback is inevitable if the system is in a closed loop, which requires a lot of optical fibers to deal with the HV isolation [see Fig. 1(d)]. The ISOP system is faced with another challenge of the auxiliary power supply (APS) for the primary switch driver and the controller in each SM. In Fig. 1(d), where the APSs are paralleled to the SM input capacitors, there will be a "runaway" phenomenon during the startup process due to the APS constant power load characteristic [8]. Although adding dummy load helps the convergence of the input voltages, the power loss is unacceptable. If the APSs are connected to the HV bus (i.e., the extra HV isolated and HV input APS), HV devices are inevitable [26], [27]. As for other types of APSs, either the structure or the control is complex [28].

Moreover, when an SM is bypassed due to fault, the APS is also down, which will cause the "black SM" condition (the SM cannot be sensed or controlled by the Main-Ctrl.), a significant adverse effect on the system reliability.

To overcome the above-mentioned challenges without adding complexities, this article proposes the three-terminal SM (3TSM) for high dc conversion ratio step-up (similar to IPOS) and step-down (similar to ISOP) applications. With 3TSM, HV isolated HFTs can be replaced by LV isolated HFTs, the control system is simplified, and the complex HV optical fiber feedback circuit can be replaced by simple LV resistive divider sampling feedback. Besides, commercial APSs can be directly paralleled to the SM input capacitors without "runaway" phenomenon. A bypass circuit is also proposed to retain the power of APS when an SM is bypassed.

Due to the self-balanced characteristic of the 3TSMs, the self-balanced 3TSM chain can be obtained. The self-balanced 3TSM chain can be extended arbitrarily with modular and standardized 3TSMs. An extra converter can be adapted to the self-balanced 3TSM chain with flexible feedback control and wide adjustable output voltage.

The rest of this article is organized as follows. The derivation and analysis of the proposed system are introduced in Section II. In Section III, a comprehensive comparison between the proposed system and the ISOP system is made. Then, the experimental results are presented in Section IV. Finally, Section V concludes this article.

II. Derivation and Analysis of the Proposed System

A. Derivation of the Proposed System

The root reason for the above challenges in ISOP and IPOS systems is brought by the SM connection method (i.e., the parallel connection in the LV side increases the galvanic isolation voltage of the SM HFTs). To solve this, neither the input side nor the output side of the SMs should be connected in parallel. However, it creates another problem since we cannot collect the output power of SMs with different voltage potentials. As a result, the output power of one SM should be stored and then transmitted, which creates a different power flow.

Fig. 2 illustrates the derivation and evolution of power flows. The left subplot of Fig. 2(a) depicts the SM power flow of the ISOP and IPOS systems with HV isolated HFTs (directly from the input to the output). To avoid HV isolated HFTs, several LV isolated HFTs are required and the potential intermediate carrier is the adjacent SM. Every SM can be the carrier, and the further the two SMs, the higher the galvanic isolation requirement of the SM HFTs. When no SM is used as the carrier, the system is equivalent to the ISOP/IPOS system. In the rest of this article, the adjacent SM carrier is taken as an example. In this condition, the SMs are cascaded sequentially, and the system power flow is depicted in Fig. 2(b).

On combining the SM cascaded method and the input series or output series connection method in step-down and step-up applications, the SM only needs three terminals, and the SM is termed as the 3TSM. A typical diagram of the 3TSM is depicted in Fig. 2(c). The negative input terminal $V_{\rm in}-$ and the positive output terminal $V_{\rm o}+$ in the 3TSM are connected. As will be analyzed in the following, the 3TSM features a self-balance characteristic.

The self-balanced 3TSM chain can be obtained via modular and standardized 3TSMs. The self-balanced 3TSM chain is depicted in Fig. 2(d). Choose three of the four terminals and the system can be changed to the step-down or step-up system. When Terminal#1 and Terminal#4 are selected as the input

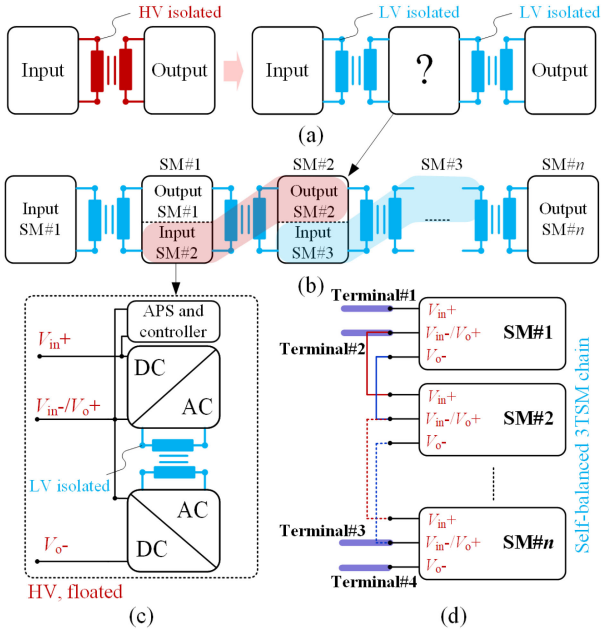

Fig. 2. Derivation and evolution of the power flow of the proposed topology. (a) Replace the HV isolated HFTs with multiple LV isolated HFTs. (b) Power flow of the proposed system with the adjacent SM as the intermediate carrier. (c) Typical diagram of the 3TSM with the adjacent SM as the intermediate carrier. (d) Typical diagram of the self-balanced 3TSM chain.

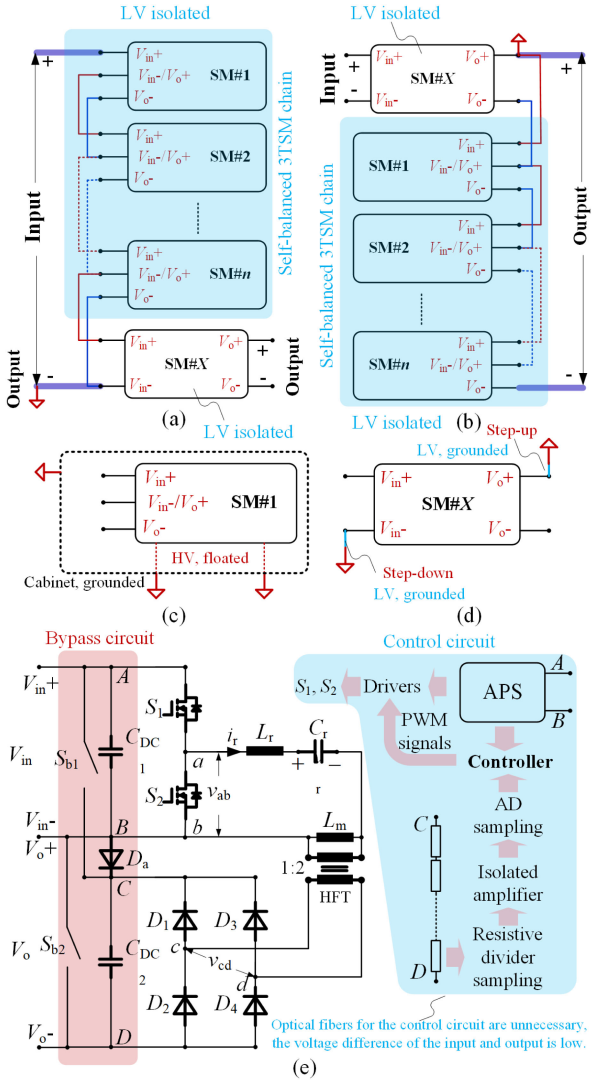

Fig. 3. Diagram of the proposed system with the self-balanced 3TSM chain and the extra converter SM#*X*. (a) Step-down system. (b) Step-up system. (c) Galvanic isolation of the SMs in the self-balanced 3TSM chain. (d) Galvanic isolation of the extra converter SM#*X*. (e) Typical SM topology and the control circuit in the self-balanced 3TSM chain.

terminals while Terminal#3 and Terminal#4 are selected as the output terminals, the proposed topology is an *n*-stage step-down system. Similarly, when Terminal#1 and Terminal#2 are selected as the input terminals while Terminal#1 and Terminal#4 are selected as the output terminals, the proposed topology is an *n*-stage step-up system.

An extra converter [i.e., SM#*X* in Fig. 3(a) and (b)] can be adapted to the self-balanced 3TSM chain for flexible feedback control or wide adjustable output voltage. The extra converter can be chosen flexibly according to the system performance requirement. The extra converter is placed to be closest to the ground to alleviate the galvanic isolation requirement [see Fig. 3(d)]. The SMs in the self-balanced 3TSM chain are all floated and they are with HV referenced to the ground. However, the voltage potential differences inside the SM are low. As a result, the HFTs, as well as the feedback circuit, are all LV isolated. In Fig. 3(c), the galvanic isolation from the SM to the SM cabinets needs to be considered when all the cabinets are grounded. This issue can be solved by using epoxy resin, polytetrafluoroethylene, or silicone rubber for the HV isolation materials.

A typical SM topology in the self-balanced 3TSM chain, as well as the control circuit, is depicted in Fig. 3(e), where C_{DC1} and C_{DC2} are two dc capacitors, S_1 and S_2 are two MOSFETs, and D_1, D_2, D_3, and D_4 are four diodes. Resonant capacitor C_{r}, resonant inductor L_{r}, and excitation inductor L_{m} compose the resonant tank where $L_{\mathrm{m}} = (m-1)\,L_{\mathrm{r}}$.

Because two MOSFETs compose a half-bridge while the four diodes compose a full-bridge, the turn ratio of the HFT is selected as 1:2 to create an almost unity gain. The input and output voltages are denoted as V_{in} and V_{o}, respectively. The resonant current, resonant voltage, and excitation current are denoted as i_{r}, v_{r}, and i_{m}. The input and output voltages of the resonant tank are denoted as v_{ab} and v_{cd}, respectively. The resonant frequency of L_{r} and C_{r} is denoted as f_{r} and the resonant frequency of L_{r}, L_{m}, and C_{r} is denoted as f_{m}. The bypass circuit is shown in the red shade and the bypass circuit contains two bypass switches S_{b1} and S_{b2} and an antireverse diode D_{a}. In normal operation, S_{b1} and S_{b2} are both open and D_{a} is forward biased. When an SM is failed and needs to be bypassed, S_{b1} and S_{b2} close simultaneously, and D_{a} is reverse biased. The control circuit is shown in blue shade. The APS is paralleled to C_{DC1}, and it powers the drivers for MOSFETs and the controller in the SM.

The output voltage V_{o} can be measured through a resistive divider sampling circuit. Afterward, the sampling signal is transmitted through a differential isolated amplifier for LV galvanic

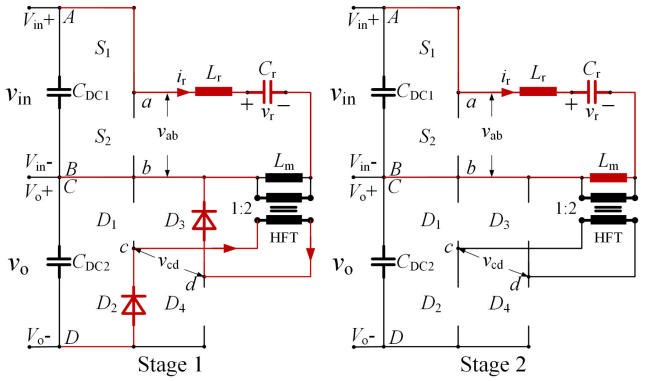

Fig. 4. Equivalent circuits of the proposed 3TSM in two stages.

isolation to the analog to digital sampling circuit. Finally, the digital result is sent to the controller. The pulsewidth or the pulse frequency of the control signal can be adjusted to regulate the output voltage V_o.

B. Analysis of the Proposed 3TSM

In normal operation when the switching frequency f_s is slightly smaller than f_r, there are two stages in the half switching period (i.e., when S_1 is OFF and S_2 is ON). The equivalent circuits of the two stages are depicted in Fig. 4.

In Stage 1, the resonant components are L_r and C_r. Denote i_r, v_r, i_m, and v_{cd} in Stage 1 as $i_{r1}(t)$, $v_{r1}(t)$, $i_{m1}(t)$, and $v_{cd1}(t)$. L_m is positively clamped by the output voltage, and $i_{m1}(t)$ increases linearly from the initial value. Denote the duration in Stage 1 as t_1, the expressions of $v_{r1}(t)$, $i_{r1}(t)$, $i_{m1}(t)$, and $v_{cd1}(t)$ are given as

$$i_{r1}(t) = \left(\frac{v_{in} - v_{r1}(0)}{Z_r} - \frac{v_o}{2Z_r}\right)\sin(\omega_r t) + i_{r1}(0)\cos(\omega_r t) \tag{1}$$

$$v_{r1}(t) = v_{in} - \frac{v_o}{2} - \left(v_{in} - v_{r1}(0) - \frac{v_o}{2}\right) \times \cos(\omega_r t) + i_{r1}(0) Z_r \sin(\omega_r t) \tag{2}$$

$$i_{m1}(t) = i_{m1}(0) + \frac{v_o \omega_r t}{2L_m} \tag{3}$$

$$v_{cd1}(t) = v_o \wedge 0 < t < t_1. \tag{4}$$

The resonant angular frequency ω_r and characteristic impedance Z_r in Stage 1 are given as

$$\omega_r = 2\pi f_r = \sqrt{\frac{1}{L_r C_r}}, Z_r = \sqrt{\frac{L_r}{C_r}}. \tag{5}$$

In Stage 2, L_m joins the resonance and the resonant components are L_r, L_m, and C_r. i_r, v_r, i_m, and v_{cd} in Stage 2 are denoted as $i_{r2}(t)$, $v_{r2}(t)$, $i_{m2}(t)$, and $v_{cd2}(t)$. In Stage 2, there is $i_{r2}(t) = i_{m2}(t)$. $v_{cd2}(t)$ can be calculated by the voltage division law. $v_{cd2}(t)$ should not exceed the output voltage where

$$v_{cd2}(t) \le v_o \wedge 0 < t < t_2. \tag{6}$$

Denote the duration in Stage 2 as t_2, the expressions of $v_{r2}(t)$, $i_{r2}(t)$, $i_{m2}(t)$, and $v_{cd2}(t)$ are given as

$$v_{r2}(t) = v_{in} - (v_{in} - v_{r2}(0))\cos(\omega_m t) + i_{r2}(0) Z_m \sin(\omega_m t) \tag{7}$$

$$i_{r2}(t) = i_{m2}(t) = \left(\frac{v_{in} - v_{r2}(0)}{Z_m}\right) \times \sin(\omega_m t) + i_{r2}(0)\cos(\omega_m t) \tag{8}$$

$$v_{cd2}(t) = \frac{2L_m}{L_m + L_r}\left((v_{in} - v_{r2}(0)) \times \cos(\omega_m t) - i_{r2}(0) Z_m \sin(\omega_m t)\right). \tag{9}$$

The resonant angular frequency ω_m and characteristic impedance Z_m in Stage 2 are given as

$$\omega_m = 2\pi f_m = \sqrt{\frac{1}{(L_m + L_r) C_r}}, Z_m = \sqrt{\frac{L_m + L_r}{C_r}}. \tag{10}$$

The continuity characteristic of $v_r(t)$, $i_r(t)$, and $i_m(t)$ in the two stages can be expressed as

$$i_{r1}(t_1) = i_{r2}(0), i_{m1}(t_1) = i_{m2}(0), v_{r1}(t_1) = v_{r2}(0). \tag{11}$$

The symmetric characteristic of $v_r(t)$, $i_r(t)$, and $i_m(t)$ in the two stages can be expressed as

$$-i_{r1}(0) = i_{r2}(t_2), -i_{m1}(0) = i_{m2}(t_2), -v_{r1}(0) = v_{r2}(t_2). \tag{12}$$

The sum of t_1 and t_2 equals the half switching period, where

$$t_2 + t_2 = \frac{T_s}{2} = \frac{1}{2f_s}. \tag{13}$$

The power transmission equations are given as

$$p_{in} = \frac{2v_{in}}{T_s}\left(\int_0^{t_1} i_{r1}(t)dt + \int_0^{t_2} i_{r2}(t)dt\right)$$
$$p_{out} = \frac{2v_o}{T_s}\int_0^{t_1}(i_{r1}(t) - i_{m1}(t))\,dt. \tag{14}$$

Assume that there is no power loss during the power conversion, the power balance equation is given as $p = p_{in} = p_{out}$. On combining (1)–(14), the relation of v_o and v_{in} with the change of p, and T_s can be obtained [29]. The voltage gain M is denoted as $M = v_o/v_{in}$. Two examples are used to analyze the power flow of the 3TSM in the step-down system and the step-up system. The system diagrams and the corresponding power flow graphs are depicted in Fig. 5(a) and (b), respectively.

The typical waveforms of these two systems are depicted in Fig. 6. In Fig. 6, s_1 and s_2 denote the control signals of MOSFETs S_1 and S_2. i_1, i_2, and i_3 are the terminal currents. As for the step-down and step-up systems, the only difference is the terminal currents i_1, i_2, and i_3 while the resonant waveforms are identical.

As for the step-down system, i_1, i_2, and i_3 are given as

$$i_1 = \frac{p_{in}}{v_{in}} + \frac{i_r}{2}; i_2 = -\frac{p_{in}}{v_{in}} - \frac{i_r}{2}; i_3 = -\frac{p_{in}}{v_{in}} + \frac{i_r}{2}. \tag{15}$$

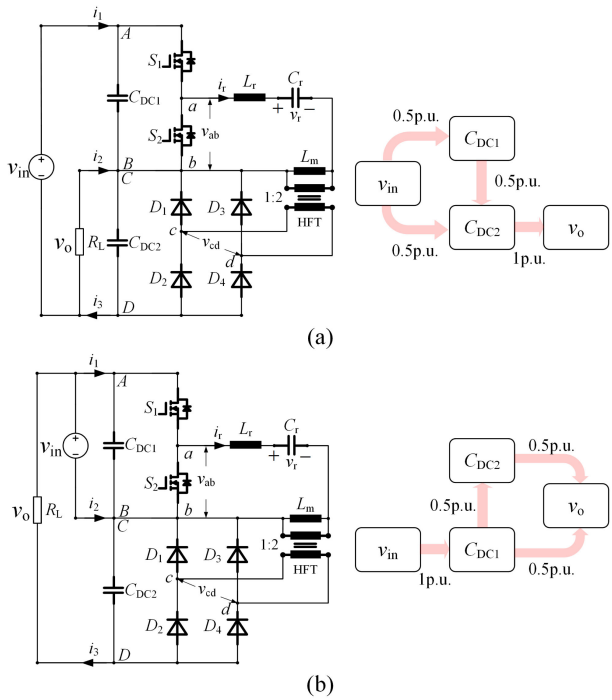

Fig. 5. (a) Circuit diagram and power flow graph of the step-down system. (b) Circuit diagram and power flow graph of the step-up system.

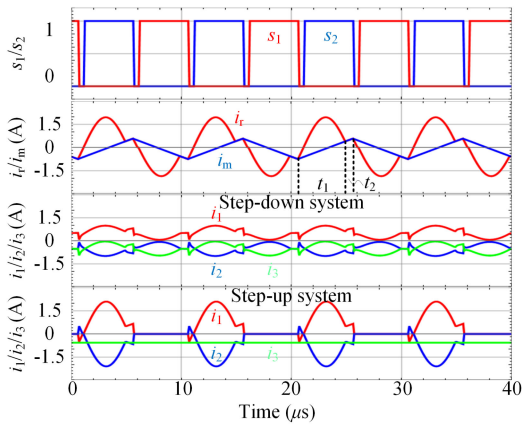

Fig. 6. Typical waveforms of the step-down system and the step-up system.

As for the step-up system, i_1, i_2, and i_3 are given as

$$i_1 = i_r \cdot s_2; i_2 = -i_r \cdot s_2; i_3 = -\frac{p_{out}}{v_o}. \tag{16}$$

In (16), s_2 denotes the control signal of MOSFET S_2 in the circuit as depicted in Fig. 5.

C. Terminal Characteristic of the Proposed 3TSM

The terminal characteristic of the proposed 3TSM can be explained by its equivalent circuit as depicted in Fig. 7. In Fig. 7, there are two symbols of the transformer. The transformer with two curves is the "ac transformer" (the left subplots in Fig. 7), and it is used to analyze the detailed operation characteristic of the SM. The transformer with two lines is the "dc transformer" (the right subplots in Fig. 7), and it is used to describe the output characteristic of the SM.

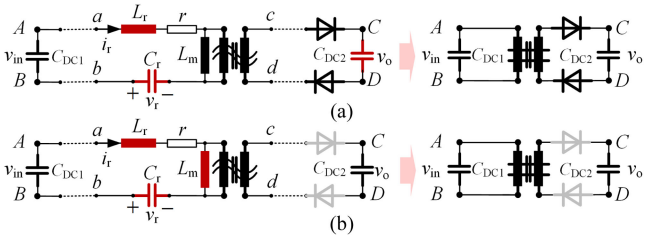

Fig. 7. Equivalent and simplified circuits of the 3TSM. (a) When $v_{in} > v_o$. (b) When $v_{in} < v_o$.

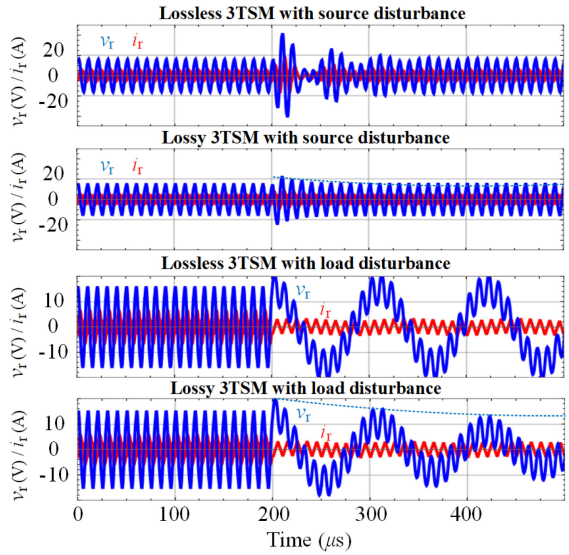

Fig. 8. Terminal characteristic of the proposed 3TSM with source and load disturbance at $t = 200$ μs.

In Fig. 7, r denotes the lumped resistance that converted all the ohmic losses. In the left subplot of Fig. 7(a) when $v_{in} > v_o$ is caused by load or input voltage increase, the diodes conduct and the load is equivalently paralleled to the secondary side of the ac transformer. Thus, the resonant components in this process are L_r, C_r, and C_{DC2}. On the other hand, when $v_{in} < v_o$ is caused by load or input voltage decrease, the diodes turn OFF and the energy cannot flow from the primary side to the secondary side. Therefore, the resonant components in this process are L_r, C_r, and L_m. When we only consider the relation of input and output voltages, the equivalent circuit can be simplified and depicted as the right subplot in Fig. 7. The transformers in the simplified circuit are dc transformers only to express isolation.

The dynamic process of the proposed 3TSM, including the lossless case ($r = 0$), and the lossy case ($r \neq 0$) with source disturbance and load disturbance at $t = 200$ μs are depicted in Fig. 8. As for the first subplot in Fig. 8 when the 3TSM is with input voltage step-up, the instantaneous power balance of the ac transformer is broken and resulted in the energy accumulation in C_r and L_r (high spikes of i_r and v_r in the first few cycles) when there is very few damping. As for the second subplot in Fig. 8 when the 3TSM is lossy, the instantaneous power imbalance can be consumed by r to reduce the spikes of i_r and v_r. As for the third subplot when the 3TSM is with load shedding, the energy circulates between C_r, L_r, and L_m. As for the fourth subplot in

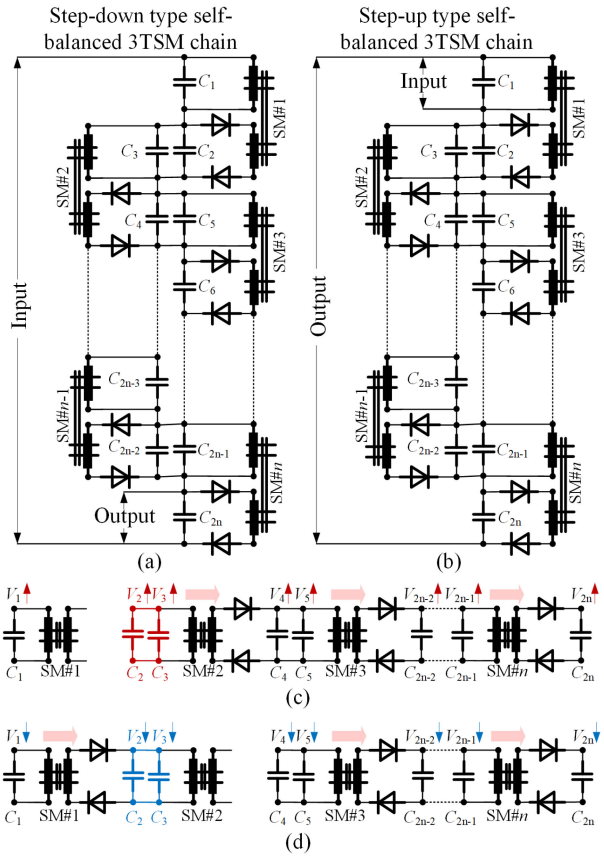

Fig. 9. Schematic diagram of (a) step-down type self-balanced 3TSM chain and (b) step-up type self-balanced 3TSM chain. (c) Power flow analysis when V_2 and V_3 increase. (d) Power flow analysis when V_2 and V_3 decrease.

Fig. 8 when the 3TSM is lossy, the envelopes of i_r and v_r shrink because r consumed part of the input energy.

D. Steady-State Analysis of the Proposed Self-Balanced 3TSM Chain

Consider the proposed self-balanced 3TSM chain consisting of n 3TSMs, the 3TSM input and output capacitors are denoted as $C_1, C_3, C_5, \ldots, C_{2n-1}$ and $C_2, C_4, C_6, \ldots, C_{2n}$. The 3TSM input and output voltages are denoted as $V_1, V_3, V_5, \ldots, V_{2n-1}$ and $V_2, V_4, V_6, \ldots, V_{2n}$. The schematic diagram of the proposed step-down and step-up type self-balanced 3TSM chains are depicted in Fig. 9(a) and (b), respectively. The power flow analyses when the 3TSM with input voltage increase or decrease are depicted in Fig. 9(c) and (d).

In Fig. 9(c) when V_2 (also V_3) increases, the energy cannot be delivered through the HFT in SM#1. As a result, V_1 will increase until $V_1 = V_2$. During this time, the power transmission through HFT in SM#2 increases, and the input and output voltages of all SMs will also increase. Similarly, when V_2 (also V_3) decreases in Fig. 9(d), the energy cannot be delivered through HFT in SM#2, and the input and output voltages of all SMs will decrease. Similar results in the step-up system can also be obtained. Although the self-balanced 3TSM chain is in an open loop, the IVS of SMs is automatically achieved, like in a closed loop.

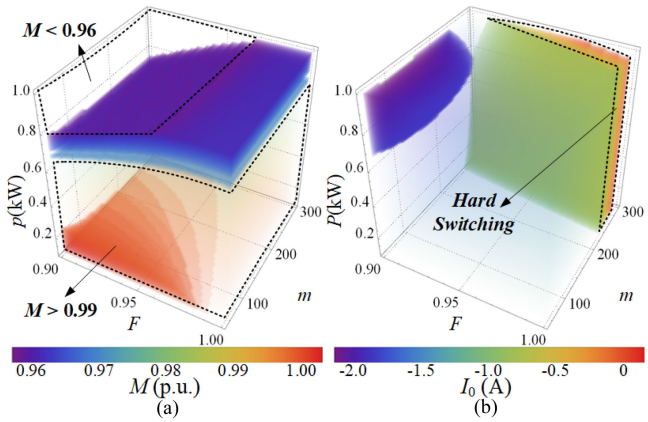

Fig. 10. (a) Three-dimensional (3-D) density map of M with the change of p, F, and m. (b) 3-D density map of I_0 with the change of p, F, and m.

E. Parameter Design of the Proposed 3TSM

The main design goal of the self-balanced 3TSM chain is to achieve high efficiency, and good SM IVS under different operation conditions. In other words, the SM is required to be load-independent, insensitive to circuit parameter mismatches, and with high efficiency.

Solving the equation set from (1) to (14), the initial values and the operation waveforms can be numerically obtained. The 3-D density map of the SM voltage gain M with the change of power transmission p, normalized switching frequency $F = f_s/f_r$, and inductor ratio $m = L_m/L_r$ is depicted in Fig. 10(a).

Generally, the SM operates with f_s slightly smaller than f_r. It can be observed from Fig. 10(a) that M is slightly smaller with unity. To make M closer to unity within a wide output power range, m should be designed as a relatively large value [see the red region with $M > 0.99$]. On the other hand, if we denote the initial resonant current when turning ON the MOSFET as I_0, the 3-D density map of I_0 with the change of p, F, and m is depicted in Fig. 10(b). Sufficient I_0 is required to fully charge and discharge the parasitic capacitors during the deadtime considering the parasitic capacitors of the MOSFET. A higher m results in a smaller I_0 (regardless of the negative sign) under the same input voltage condition (the input voltage is set as 300 V in Fig. 10). The recommended value of m is around 200. Hence, the resonant parameters can be designed as $L_r = 2.8\ \mu$H, $C_r = 620$ nF, and $L_m = 560\ \mu$H when f_s is around 100 kHz.

III. Comparison Between the ISOP Systems and the Step-Down Type Self-Balance 3TSM Chain

Because the ISOP system is more challenging in practical implementation and some difficulties in the IPOS system can also be found in the ISOP system, a comprehensive comparison of the ISOP system and the step-down type self-balanced 3TSM chain is made in this section from the following aspects.

1) Hardware circuit evaluation, including the SM galvanic isolation condition, the difficulties in the startup circuit, bypass circuit, APS circuit, and feedback circuit in the closed-loop control.

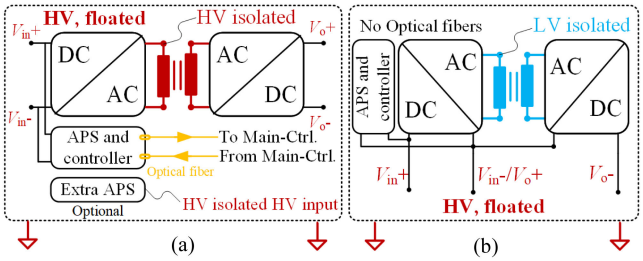

Fig. 11. Simplified SM topologies in (a) ISOP system and (b) proposed 3TSM.

2) Control system evaluation, including the startup strategy, bypass strategy, control system complexity, and the difficulties in the implementation of IVS with parameter mismatch.
3) System performance evaluation, including system power rating, and efficiency comparison.

A. Hardware Circuit Evaluation

1) SM Galvanic Isolation Condition: The simplified SM topologies in the ISOP system and the proposed topology are depicted in Fig. 11. As can be observed, the galvanic insulation requirements of the SM in the ISOP system (HV isolated HFTs, optional extra APSs if the commercial APSs are not adopted to the SM input capacitors, optical fibers for information interaction, etc.) are much rigid than that of the proposed 3TSM, indicating that the components in the proposed 3TSM (LV isolated HFTs, commercial APSs, etc.) are cheaper and more reliable. Meanwhile, the PCB layout of the proposed 3TSM is much easier with a narrower creep distance and a compact design. The dashed lines in Fig. 11 denote the cabinets of the SM, and the HV side of the ISOP SM and the proposed 3TSM are all HV floated. Insulation materials between the SM and the SM cabinets should be concerned for safety operation.

2) APS and Startup Analysis: In the ISOP system, extra APSs circuits, bypass circuits, and startup circuits need to be designed. On the contrary, commercial APSs can be applied to the SM capacitors in the proposed topology with simple bypass circuits, and no extra startup circuits are needed. The reason is given as follows.

Consider both the systems where the APSs are directly applied to the SM input capacitors. During the startup process, the main circuit is not activated. Hence, the APSs in different SMs form an input series output independent system as depicted in the left subplot of Fig. 12(a). The commercial APS generally adopts output voltage closed-loop control and its input power is determined by the load condition (also known as the constant power load characteristic). The constant power load characteristic can be explained by Fig. 12(b), where

$$P_{\mathrm{CPL}} = i_{\mathrm{CPL}} \cdot v_{\mathrm{CPL}} = \mathrm{const.} \tag{17}$$

Denote the steady-state operation point of the CPL as (i_{CPL}, v_{CPL}), the incremental impedance of CPL r_{CPL} can be calculated as

$$r_{\mathrm{CPL}} = \frac{dv_{\mathrm{CPL}}}{di_{\mathrm{CPL}}} = -\frac{(v_{\mathrm{CPL}})^2}{P_{\mathrm{CPL}}} < 0. \tag{18}$$

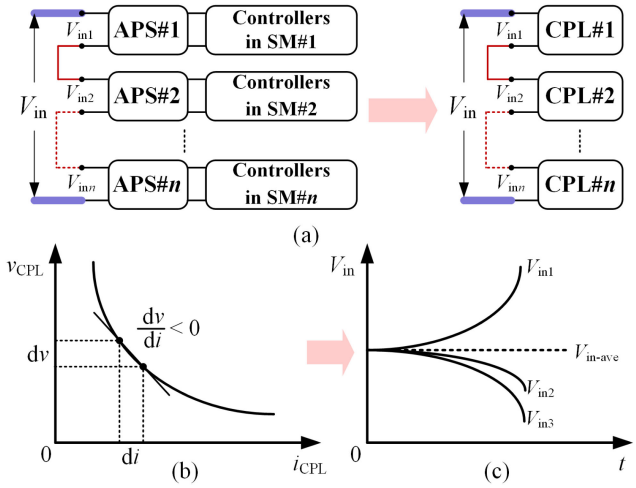

Fig. 12. (a) Equivalent circuit of the input series system with APSs paralleled to the SM input capacitors. (b) Negative incremental impedance characteristic of the CPL. (c) Input voltage divergent phenomenon during the startup process.

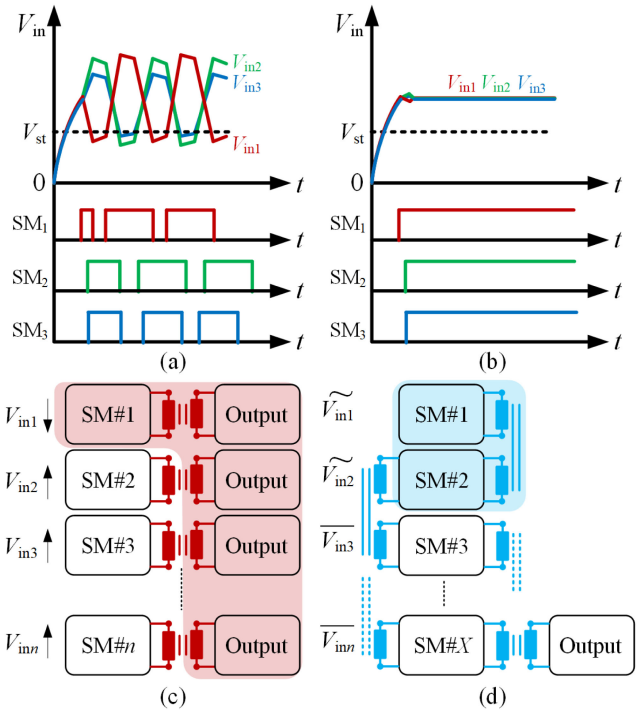

Fig. 13. Impact of the startup time deviation of APSs in (a) ISOP system and (b) proposed step-down type topology. The power flow analysis during the startup process in (c) ISOP system and (d) proposed step-down type topology.

The negative r_{CPL} of each SM will induce input voltage diverge, and this phenomenon is depicted in Fig. 12(c). It has to be noted that the negative resistance effect is inevitable in all the input series systems (including the proposed self-balance 3TSM chain) as long as the SM APS is powered by the SM input capacitors. To mitigate the negative resistance effect, the SM start-up time should be minimized.

Another problem caused by commercial APS is that the circuit parameter mismatch leads to startup time deviation. This phenomenon is depicted in Fig. 13 where SM_1, SM_2, and SM_3 are the operation flag of the three APSs. Fig. 13(a) shows

a 3SM ISOP system when SM#1 first completes the startup process. SM#1 will provide the whole energy to the output [see Fig. 13(c)]. As a result, V_{in1} decreases rapidly and the APS in SM#1 is switched OFF when V_{in1} is smaller than the minimum startup voltage V_{st}. During this process, the input voltages of other SMs increase. Usually, the restart time of the commercial APSs is around 2–5 s. As a result, the APSs will be in the start–stop mode and the system fails to startup. Fig. 13(b) shows the 3TSM APSs under the same condition. The impact of startup time deviation is mitigated because the power flow in the proposed system is sequentially rather than directly [see Fig. 13(d)]. When SM#1 first completes the startup process, the energy will not be transmitted to the load. Due to the characteristic of the proposed 3TSM, V_{in1} and V_{in2} will have a much smaller fluctuation while the other SMs are almost not affected.

3) Bypass Circuit Analysis: Because the topology is input series connected, the "input bypass" method is the only feasible way when the SM fault occurs. Practically, the MOSFET fault is one of the most common faults, and the fault detection method in the SM MCU is given as follows.

1) When the open circuit fault occurs, the SM input voltage increases because the current flows out of the input capacitor is zero. Hence, the MOSFET open circuit fault can be detected by the SM input voltage. When the SM input reaches the predefined overvoltage threshold, the two bypass switches are closed to bypass this SM.
2) When the short circuit fault occurs, this fault can be detected by the MOSFET driver like 2ED020I12-F2. The drain current of the MOSFET increases rapidly when the short circuit fault occurs and the output pulse will be disabled when the desaturation pin reaches 9 V. Afterward, the driver pulse is pulled down to −5 V and the MOSFET is turned OFF. The SM MCU receives this fault and enables the bypass switches to bypass this SM.

It has to be mentioned that the APSs are paralleled to the input capacitors and the bypass switch is controlled by a relay powered by the SM APS. Although an extra HV isolated APS can solve the startup and bypass difficulties, in some applications where the extra APS has to obtain power from the HV bus, the design of APSs is also faced with similar challenges (HV devices, HV isolated HFTs, etc.).

In the ISOP systems, the topology of SMs with bypass function is depicted in Fig. 14 (the SM topology is chosen as the *LLC* resonant converter for an example). The bypass function is implemented through a bypass switch S_{b1} (normally open) and an antireverse diode D_{a1}. The input voltage and the voltage of input capacitors of the two SMs are denoted as v_{in1}, v'_{in1} and v_{in2}, v'_{in2}, respectively. If SM#1 fails and needs to be bypassed, S_{b1} closes and D_{a1} is reverse biased. Hence, C_{DC1} is equivalent to being removed from the system instead of being short. However, APS#1 will continuously consume the energy on C_{DC1} until v'_{in1} is below V_{st} of APS#1. As a result, the controllers in SM#1 are also down and S_{b1} will be open and reconnect the failed SM#1. As a result, v_{in1} is charged rapidly and v_{in1} can be high enough to break down the power switches in SM#1.

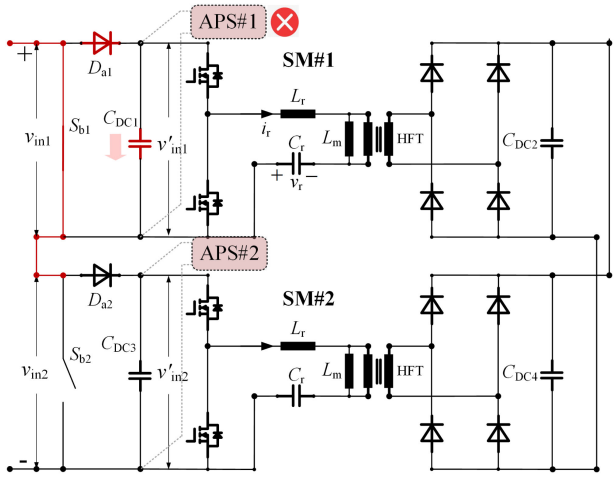

Fig. 14. Equivalent circuit of a 2SM ISOP system when SM#1 is bypassed.

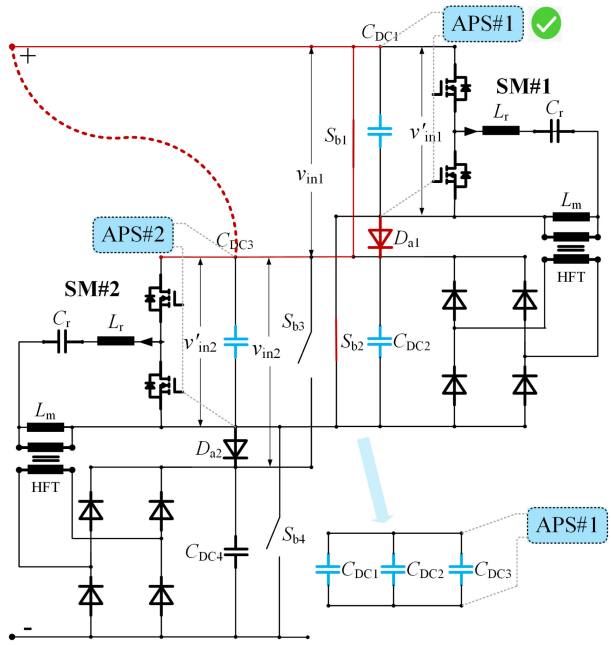

Fig. 15. Equivalent circuit of a 2SM proposed system when SM#1 is bypassed.

As depicted in Fig. 15, the proposed topology requires two bypass switches S_{b1} and S_{b2} (normally open), and the antireverse diode D_{a1} is connected to the common terminal. When SM#1 fails and needs to be bypassed, it can be observed that C_{DC1}, C_{DC2}, and C_{DC3} are all in parallel, and the input terminal is equivalently connected to the input terminal of SM#2 (illustrated as the red dashed line). Therefore, there is $v'_{\mathrm{in1}} = v_{\mathrm{in2}} = v'_{\mathrm{in2}}$, and ASP#1 is still working to retain the power of the controllers and the two bypass switches S_{b1} and S_{b2} in SM#1.

B. Control System Evaluation

1) Control System Complexity: The typical simplified control system diagram of the ISOP system and the proposed system are depicted in Fig. 16.

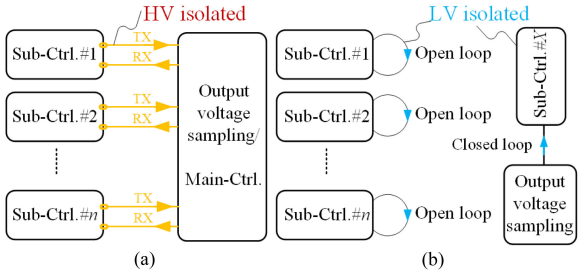

Fig. 16. Typical simplified control system diagram of (a) ISOP system and (b) proposed 3TSM.

The control system of the ISOP system requires many optical fibers for information interaction as long as the system is in closed loop because the output voltage sampling circuit locates on the LV side. On the contrary, the 3TSMs are all in open loop and the closed-loop controlled extra converter locates in the LV side. Hence, the complex ISOP control structure can be replaced by a simple LV feedback control.

2) Implementation of IVS With Parameter Mismatch: As for the input series structure, IVS should be guaranteed when the system is operating, otherwise, the SM input voltages will diverge. It is extremely crucial for the ISOP system because when all the SMs are in closed-loop control, the equivalent input impedance of every SM is negative. In other words, the ISOP system is naturally unstable without extra IVS control. The IVS implementation can be achieved via sensing the SM input voltages or output currents as mentioned in Section I.

As a result, the safe operation of ISOP is highly dependent on the control system. One communication failure seriously affects the reliability of the system. For example, if the transport fiber (TX) of Sub-Ctrl. #1 fails, the operation state of SM#1 cannot be sent to the Main-Ctrl. On the other hand, when the receive fiber (RX) fails, Sub-Ctrl. #1 cannot obtain the operation command sent by the Main-Ctrl. When there is input/output disturbances or instruction change, the input voltage of SM#1 might continuously increase or decrease. These phenomena are also called the "black SM." For safety concerns, the ISOP system has to be stopped when "black SM" occurs. As for the proposed topology, the interaction of different SMs is unnecessary. Besides, the topology is self-balanced without extra IVS control. Hence, there is no need to worry about the unstable impact brought by the control system.

IVS of SMs is affected by parameter mismatches, which will in turn affect the input voltage of SMs. With the designed circuit parameter, a 4SM system is simulated and the impact is depicted in Fig. 17, where the x-axis denotes the deviation of the resonant parameters percentage and the y-axis denotes the SM input voltage deviation percentage (IVD%). IVD% is determined by the ratio of the SM input deviation voltage to the average SM input voltage. It can be observed from Fig. 17 that IVD% increases when the resonant parameters are away from the rated value. The impact of C_{r} or L_{r} is similar while the impact of L_{m} is much smaller. With the designed resonant parameters, IVD% is smaller than 1.5% at 10% maximum resonant parameter mismatch, which is much smaller than the ISOP systems as reported in [2].

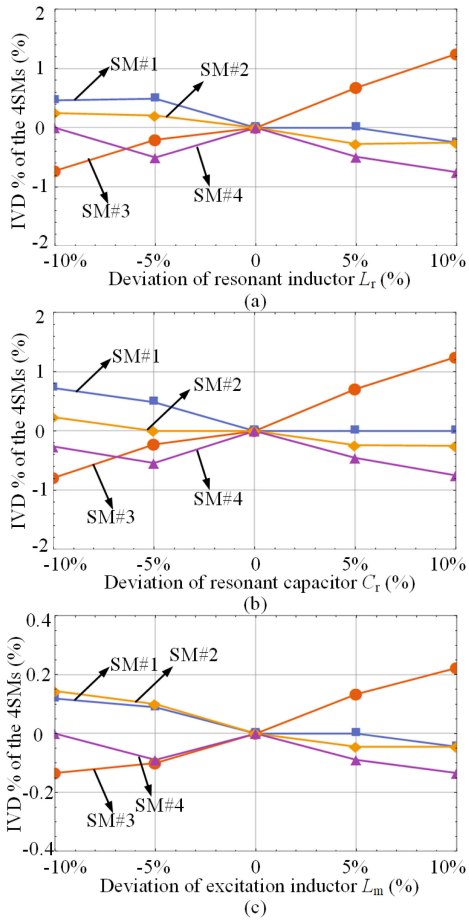

Fig. 17. Diagram of the SM input voltage deviation (IVD%) versus resonant parameter deviations. (a) Impact of L_{r}. (b) Impact of C_{r}. (c) Impact of L_{m}.

C. System Performance Evaluation

The power transmission characteristics of the ISOP system and the proposed topology are different. Take a six-SM system for example, the power flow of the ISOP system, the proposed topology with adjacent SM/every two SMs/every three SMs as the intermediate carrier are depicted in Fig. 18. In Fig. 18, the bold SMs in the proposed system denote the extra converters. The outputs of all the extra converters are parallel to the load.

As for the four different topologies, the power flows of the SMs can be expressed as

$$p_{\mathrm{ISOP}} = \left[1\,1\,1\,1\,1\,1\right]; p_{\mathrm{3TSM-1}} = \left[1\,2\,3\,4\,5\,6\right]$$
$$p_{\mathrm{3TSM-2}} = \left[1\,1\,2\,2\,3\,3\right]; p_{\mathrm{3TSM-3}} = \left[1\,1\,1\,2\,2\,2\right]. \quad (19)$$

The galvanic isolation voltage of the SMs for the four different topologies can be expressed as

$$V_{\mathrm{ISOP}} = \left[\tfrac{6}{6}\,\tfrac{5}{6}\,\tfrac{4}{6}\,\tfrac{3}{6}\,\tfrac{2}{6}\,\tfrac{1}{6}\right]$$
$$V_{\mathrm{3TSM-1}} = \left[\tfrac{1}{6}\,\tfrac{1}{6}\,\tfrac{1}{6}\,\tfrac{1}{6}\,\tfrac{1}{6}\,\tfrac{1}{6}\right]$$
$$V_{\mathrm{3TSM-2}} = \left[\tfrac{1}{3}\,\tfrac{1}{3}\,\tfrac{1}{3}\,\tfrac{1}{3}\,\tfrac{1}{3}\,\tfrac{1}{3}\right]$$
$$V_{\mathrm{3TSM-3}} = \left[\tfrac{1}{2}\,\tfrac{1}{2}\,\tfrac{1}{2}\,\tfrac{1}{2}\,\tfrac{1}{2}\,\tfrac{1}{2}\right] \quad (20)$$

where the system input voltage is set as the rated value.

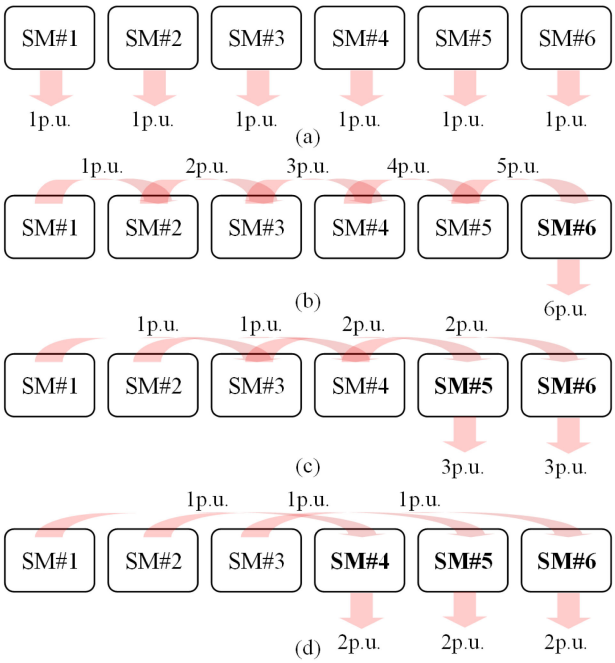

Fig. 18. (a) Power flow of the ISOP system. (b) Power flow of the proposed system with the adjacent SM as the intermediate carrier. (c) Power flow of the proposed system with every two SMs as the intermediate carrier. (d) Power flow of the proposed system with every three SMs as the intermediate carrier. (The bold SMs in the proposed system denotes the extra converters SM#*X*.)

Equations (19) and (20) show that in the proposed system, the sum of the power of all SMs is greater than the equivalent power of the system. In other words, the efficiency of the proposed system is lower than the ISOP system under the premise of equivalent efficiency of SMs, especially when the adjacent SM is used as the intermediate carrier. However, the galvanic isolation voltage of the SMs in the proposed system is greatly reduced.

From the above comparisons, the ISOP system and the proposed system have advantages and disadvantages. In high power applications (megawatts or tens of megawatts), such as medium-voltage dc applications or offshore wind power plants, the ISOP system is suitable. In these conditions, the transformer structure, magnetic core, windings and wires, isolation material, and cooling systems need to be specially designed [22]–[25]. In high-reliability applications, such as the undersea observatories power supply or other commercial high input voltage dc sources, the proposed system is suitable. The engineers can choose the appropriate topology and control system design according to different scenarios and requirements based on the comparison of the two system characteristics summarized in Table I.

TABLE I
COMPARISON OF THE ISOP SYSTEM AND THE PROPOSED SYSTEM

Comparison items	ISOP system	Proposed system
SM isolation	High	Low
APSs and Startup circuit	Difficult	Easy
Bypass circuit	Potential risk	Safe
Control system complexity	Complex	Simple
Cost of IVS implementation	High	Zero
SM power rating	Equal	Not equal
System power rating	High	Low
System efficiency	High	Medium

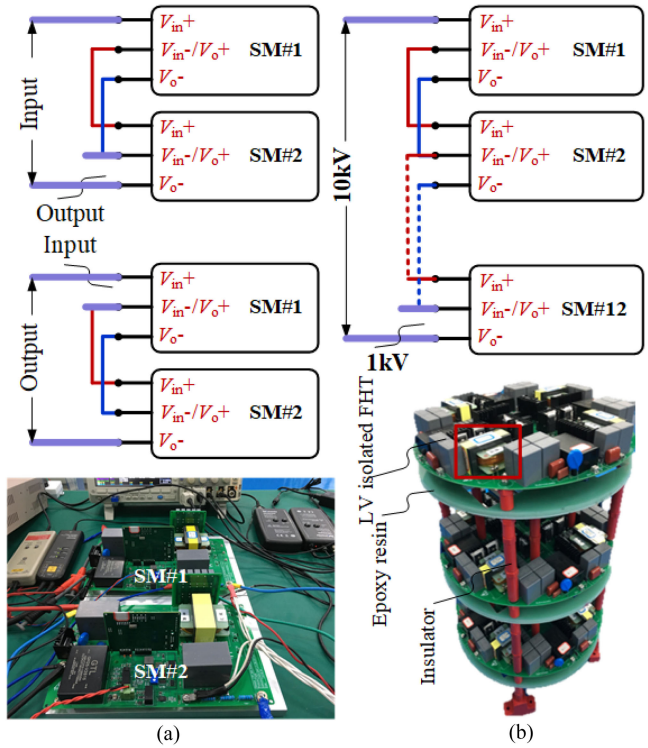

Fig. 19. (a) 2SM step-down and step-up type self-balanced 3TSM chain proof-of-principle prototype. (b) 10-kV input 1 kV/1 kW output converter continued to use the proposed step-down self-balanced 3TSM chain.

TABLE II
SYSTEM SPECIFICATION OF THE TWO CONVERTERS

Items	2SMs proof-of-concept experimental prototype	12SM 10 kV converter
Input voltage	300 V/ 150 V	10 kV
Output voltage	150 V/ 300 V	1 kV
Power rating	300 W	1 kW
Peak Efficiency	98%	85%
Self-startup voltage	800 V/2SM	7.2 kV/12SM

IV. EXPERIMENTAL RESULT

The 3TSM based step-down system and step-up system consisting of two SMs proof-of-concept experimental prototypes, together with a subsequent 10-kV input 1 kV/1 kW output converter, are built to verify the effectiveness and feasibility of the above analysis.

The prototypes are depicted in Fig. 19. In Fig. 19(b), the 10-kV converter contains 4 boards and 12SMs (2 for backup). The tested condition is 10-kV input and 1 kV/1 kW output and the self-startup voltage is set as 7.2 kV. The system specifications of the two converters are summarized in Table II.

Because the main subject of this article is to verify the feasibility of the proposed self-balanced 3TSM chain in the step-down system and step-up applications, the following experiments are based on the 2SM design prototype as depicted in Fig. 19(a).

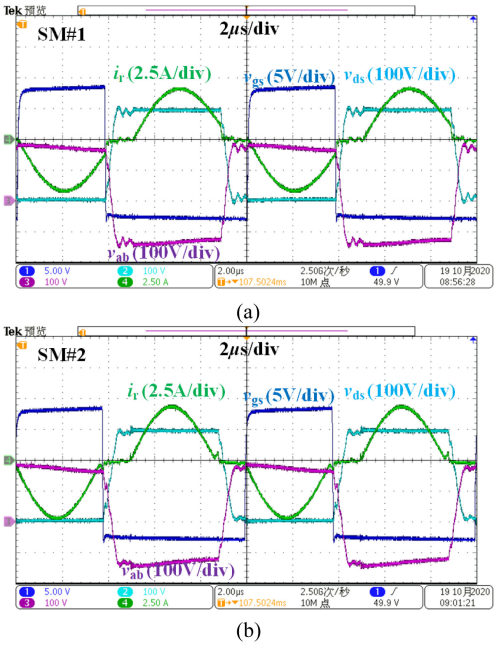

Fig. 20. Key waveforms of the two SMs with 300-V input and 250-Ω load. (a) Steady-state waveforms of SM#1. (b) Steady-state waveforms of SM#2. (Ch1: the gate driver $v_{\rm gs}$ of the MOSFET, 5 V/div; Ch2: the drain–source voltage of the MOSFET $v_{\rm ds}$, 100 V/div; Ch3: the input voltage of the HFT $v_{\rm ab}$, 100 V/div; Ch4: the resonant current $i_{\rm r}$, 2.5 A/div).

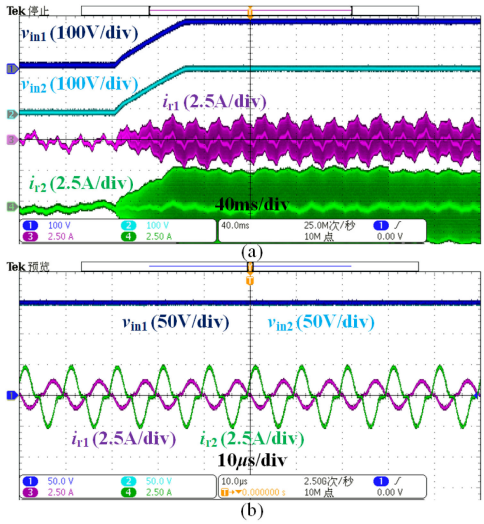

Fig. 21. Key waveforms of the 2SM step-down system. (a) Startup waveforms with 300 V input voltage step-up. (b) Steady-state waveforms with 300-V input and 250-Ω load. (Ch1: the input voltage of SM#1 $v_{\rm in1}$, 50 V/div; Ch2: the input voltage of SM#2 $v_{\rm in2}$, 50 V/div; Ch3: the resonant current of SM#1 $i_{\rm r1}$, 2.5 A/div; Ch4: the resonant current of SM#2 $i_{\rm r2}$, 2.5 A/div).

In Fig. 19(a), the primary and secondary dc capacitors are both 22 μF film capacitors. SiC MOSFETs C2M0080170P and diodes C5D25170H are applied. The resonant capacitor board consists of nine 47 nF and six 33 nF MMKP capacitors in parallel (621 nF in total). The leakage inductor of the HFT is adopted as the resonant inductors, which are 2.86 μH and 2.81 μH for the two SMs. The excitation inductors of the two SMs are 500 μH and 522 μH, respectively. The parameter difference of the two SMs is brought by the HFT. The material of the HFT is PC95/EEP70B and the turn ratio is 1:2 to create the unity voltage gain. The 10-kV converter continued to use the 3.5 kV galvanic isolation voltage HFTs, and the epoxy resin board and insulators are adopted for different SMs [see the green board and red pillars in Fig. 19(b)]. The switching frequency $f_{\rm s}$ is around 100 kHz and the controller is the digital signal processor F280049CPMSR from Texas Instruments.

A. Experimental Waveforms of the Two SMs

The input dc source is a 300-V dc source and the output dc load is Chroma 350-V electronic load. The efficiency can be obtained via the dc source input power and the electronic load output power. When the SMs are in steady state with 300-V input and 250-Ω load, the key waveforms are depicted in Fig. 20 where the purple, green, light blue, and navy blue lines denote the input voltage of the HFT $v_{\rm ab}$ (100 V/div), the resonant current $i_{\rm r}$ (2.5 A/div), the drain–source voltage of MOSFET $v_{\rm ds}$ (100 V/div), and the gate driver $v_{\rm gs}$ (5 V/div) of the two SMs. As can be seen, the ZVS-ON of MOSFETs are achieved since $v_{\rm ds}$ has already dropped to zero before the rising of $v_{\rm gs}$. The turning-OFF current is around 0.3 A, and the turning-OFF loss is very tiny. The secondary diode can achieve zero-current switching and there is no reverse recovery. The diode conduction loss of the secondary diodes is also low. In normal operation, the antireverse diode is conducted and it will bring extra condition loss. As for the used diode C5D25170H from CREE, the typical forward drop is 1.5 V and the conduction loss is very small. The efficiencies of these two SMs are both as high as 97.5% and 97.9%, respectively.

B. Experimental Waveforms of the 2SM Step-Down and Step-Up Systems

Limited by the voltage range of the dc source and electronic load, in the 2SM step-up experiment, the input voltage is 150 V and the output voltage is around 300 V. In the 2SM step-down experiment, the input voltage is 300 V and the output voltage is around 150 V. The waveforms of the 2SM step-down system with 300-V input and 250-Ω load are depicted in Fig. 21. In Fig. 21(a), the navy blue and light blue lines denote the input voltage of the two SMs, $v_{\rm in1}$ and $v_{\rm in2}$ (100 V/div). The purple and green lines denote the resonant current of the two SMs $i_{\rm r1}$ and $i_{\rm r2}$ (2.5 A/div). It can be observed that when the input voltage is with a 300-V step-up in 60 ms, the input voltage is perfectly shared by $v_{\rm in1}$ and $v_{\rm in2}$. Moreover, the rising slopes of $v_{\rm in1}$ and $v_{\rm in2}$ are almost identical. To create an identical working condition for the two SMs in the 2SM step-up system, the input voltage is changed to 150 V and the load is decreased to 1000 Ω. The key waveforms are depicted in Fig. 22. Since the input voltage is reduced by half, the step-up response time is also reduced from 60 to 30 ms. Because the power transmission of SM#1 is twice that of SM#2, the amplitude of $i_{\rm r1}$ is approximately twice that of $i_{\rm r2}$.

The self-startup waveforms of the 2SM step-down system with 800 V input voltage with zero load (500-kΩ dummy load) and 1000 Ω load are depicted in Fig. 23, where the purple and

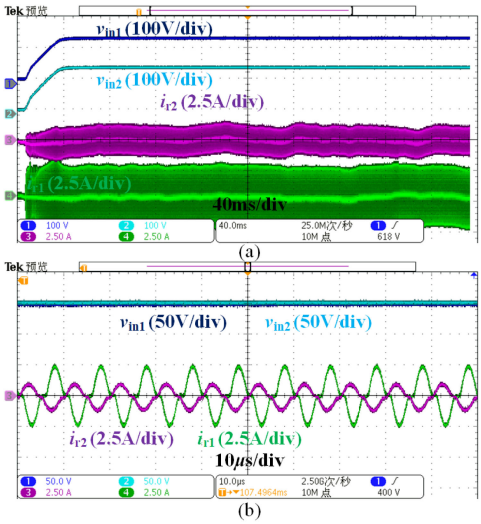

Fig. 22. Key waveforms of the 2SM step-up system. (a) Startup waveforms with 150 V input voltage step-up. (b) Steady-state waveforms with 150-V input and 1000-Ω load. (Ch1: the input voltage of SM#1 v_{in1}, 50 V/div; Ch2: the input voltage of SM#2 v_{in2}, 50 V/div; Ch3: the resonant current of SM#2 i_{r2}, 2.5 A/div; Ch4: the resonant current of SM#1 i_{r1}, 2.5 A/div).

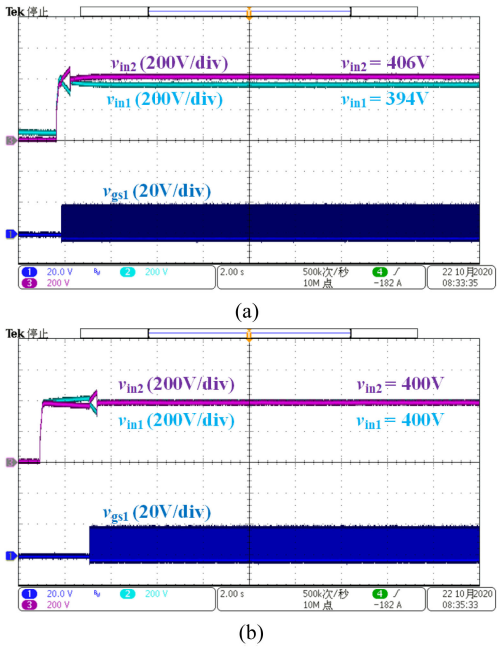

Fig. 23. Self-startup waveforms of the 2SM step-down system with 800 V. (a) Self-startup with zero load. (b) Self-startup with 1000-Ω load. (Ch1: the gate signal of SM#1 v_{gs1}, 20 V/div; Ch2: the input voltage of SM#1 v_{in1}, 200 V/div; Ch3: the input voltage of SM#2 v_{in2}, 200 V/div).

light blue lines denote the input voltage of the two SMs, v_{in1} and v_{in2} (200 V/div), and the navy blue line denotes the gate signal of SM#1 v_{gs1} (20 V/div). When there is zero load during startup, the startup delay caused by the APS is around 0.5 s and the steady-state values of v_{in1} and v_{in2} are $v_{\mathrm{in1}} = 394$ V and $v_{\mathrm{in2}} = 406$ V. The reason for these differences is the finite L_{m} and the light load voltage gain is slightly greater than unity.

When there is 1000-Ω load during startup, the startup delay caused by the APS is around 3 s. As can be seen, the unstable

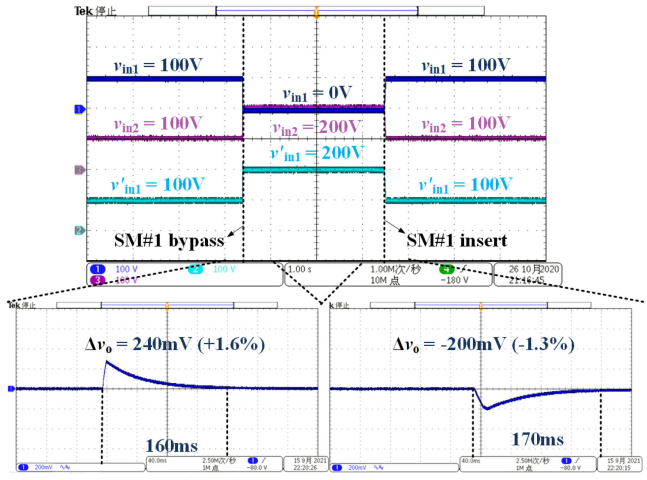

Fig. 24. *M* bypass and insert waveforms of the 2SM step-down system with 200 V input voltage. (Ch1: the input voltage of SM#1 v_{in1}, 100 V/div; Ch2: the voltage of the input capacitor in SM#1 v_{in1}, 50 V/div; Ch3: the input voltage of SM#2 v_{in2}, 100 V/div). The bottom two waveforms show the system output voltage dynamic processes.

runaway exists when the system is not running. When SM#1 is running, v_{in1} and v_{in2} are balanced immediately and the input voltage is perfectly shared ($v_{\mathrm{in1}} = v_{\mathrm{in2}} = 400$ V).

Due to the tight coupling characteristic of the SMs in the self-balanced 3TSM chain, the SMs output voltage varies when the converter input voltage changes. Although the SMs in the self-balanced 3TSM chain can regulate its output voltage, this capability is relatively weak. The system output voltage is adjusted through the extra converter.

Generally, the dynamic process of the SMs in the open-loop controlled self-balanced 3TSM chain is much faster than the extra converter, and the system dynamic performance is closely related to the topology and feedback circuit design.

In the SM bypass and insert experiment, a flyback converter is adopted as the extra converter. The reference voltage of the flyback converter is 15 V. The dynamic performance of the 2SM step-down system output voltage when SM#1 is bypassed or inserted is depicted in the bottom part in Fig. 24. In Fig. 24, the navy blue, purple, and light blue lines denote v_{in1}, v_{in2}, and v'_{in1} (100 V/div). The definition of v'_{in1} is given in Fig. 15. In the normal operation process, the input voltage of the two SMs are perfectly shared and there is $v_{\mathrm{in1}} = v_{\mathrm{in2}} = v'_{\mathrm{in1}} = 100$ V. When SM#1 is bypassed, both v_{in2} and v'_{in1} increase to 200 V input voltage while v_{in1} is reduced to zero.

When SM#1 is bypassed, the system output voltage overshoot Δv_{o} is 240 mV, which is $+1.6\%$ higher than 15 V. The dynamic process is around 160 ms. Similarly, when SM#1 is inserted, the input voltages of the two SMs are shared again and there is $v_{\mathrm{in1}} = v_{\mathrm{in2}} = v'_{\mathrm{in1}} = 100$ V. The system output sag Δv_{o} is -200 mV, which is 1.3% lower than 15 V. The dynamic process is around 170 ms.

C. Experimental Curves

The experimental curves of the two SMs step-down system and step-up system are depicted in Fig. 25.

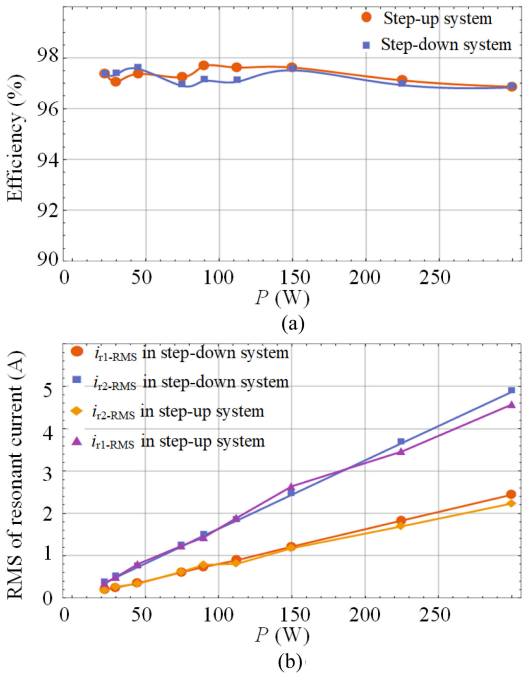

Fig. 25. Experimental curves of the 2SM step-down system and step-up system. (a) Efficiency curves. (b) RMS value of resonant current curves.

As for the efficiency curve in Fig. 25(a), the peak efficiency is achieved with 300-V input, 150-Ω load for the step-down system and 150-V input, 1000-Ω load for the step-up system, which are 97.6% and 97.8%, respectively. With the increase of load, the efficiency curves of the systems are relatively smooth. As for the RMS value of resonant current $i_{\text{r1-RMS}}$ and $i_{\text{r2-RMS}}$ in the two SMs, the curves are depicted in Fig. 25(b), where the red, blue, purple, and orange lines denote $i_{\text{r1-RMS}}$, $i_{\text{r2-RMS}}$ for the step-down and step-up systems, respectively. Approximately, $i_{\text{r2-RMS}}$ is twice of $i_{\text{r1-RMS}}$ in the step-down system and half in the step-up system except for the light load conditions because the almost unchanged excitation current takes up the majority of resonant current.

V. Conclusion

Practically, the ISOP and IPOS systems face many challenges. To overcome these challenges without adding complexities, this article proposed the 3TSM based high dc conversion ratio step-up and step-down systems. In the proposed systems, the HV isolated HFT and the HV feedback system were unnecessary. The APS configuration, bypass circuit/strategy, and the control system were simplified. The operation principle and circuit characteristics of the 3TSM and the 3TSM based step-up and step-down system were analyzed in detail. A comprehensive comparison of the 3TSM based step-down system and the ISOP system was presented for the engineers in practical implementation. Finally, the feasibility and effectiveness of the proposed 3TSM based step-up system and step-down system were verified by a 2SM proof-of-concept experiment prototype under various operating conditions. Subsequently, a 10-kV input 1 kV/1 kW output converter was also built with LV isolated HFTs, commercial APSs, and a simple resistive divider sampling circuit. The 10-kV converter verified the self-balanced and self-startup characteristics of the proposed topology.

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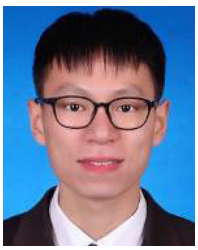

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