A Three-Phase Active-Front-End Converter System Enabled by 10-kV SiC MOSFETs Aimed at a Solid-State Transformer Application

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***Abstract*—The use of high-voltage silicon carbide (SiC) devices can eliminate multilevel and cascaded converters and their complicated control strategies, making converter systems simple and reliable. A three-phase two-level voltage-source converter system serves as a simple converter system for interfacing any dc source to a three-phase grid. However, when the high-voltage devices are used in two-level converters, they are exposed to a high-voltage peak stress and a high dv/dt (up to 100 kV/μs). Operating these semiconductor devices at these stress levels requires careful design not only of the semiconductor die and the module, but also of the gate drivers, busbars, and passive filters. This article demonstrates the operation of 10-kV SiC MOSFETs and discusses the design considerations, advantages, and challenges associated with the operation of the three-phase two-level medium-voltage converter system used as the active-front-end converter system. Reliable operation of the medium-voltage converter system requires the development of reliable high-voltage modules and auxiliary parts, such as gate drivers, busbars, inductors, voltage and current sensors, and proper design of the controller system. Successful tests demonstrating continuous field operation of the medium-voltage active-front-end converter at a nominal rating of 7.2-kV dc-link voltage is demonstrated for the first time in the literature. The results indicate that these devices can accelerate the growth and deployment of medium-voltage SiC devices for field operation, as demonstrated by the operation inside the mobile container.**

***Index Terms*—Active-front-end converter (AFEC) system, gate driver, medium voltage (MV), silicon carbide (SiC) devices, solid-state transformer, XHV-6.**

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I. Introduction

CONVENTIONALLY, integrated gate commutated thyristors (IGCTs) and gate turn-OFF transistors are used for medium-voltage (MV) grid-connected applications [1], [2]. Silicon (Si) insulated gate bipolar transistors (IGBTs) have a limitation on the maximum voltage and are limited to 6.5 kV [3]. For grid-tied applications, at a distribution voltage level, more than 4.16 kV, the use of two-level converters is not possible with a silicon-based power semiconductor device [4]. It becomes necessary to consider three-level/five-level neutral-point-clamped (NPC) converters or flying-capacitor-clamped converters for maintaining a voltage of $<$4 kV across the devices considering the safe operating area of these Si IGBTs [5]. The safe operating voltage (defined by the safe operating area) of an Si IGBT module reduces drastically with an increase in current, which does not allow a high-blocking-voltage operation at increased power levels. These devices also have a limitation on the switching frequency to less than 1 kHz owing to their slower switching speeds. In addition, for high-voltage silicon-based IGBT or IGCT converters, deionized water cooling is imperative for high-power applications ($>$2 MVA) due to limitations in the maximum operating junction temperature, as well as high switching losses [6].

With the advancement of wide-bandgap semiconductors, power devices, such as silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) and SiC IGBTs, are now available with blocking voltages up to 15 kV [7]. SiC-based devices can operate at higher switching frequencies ($>$5 kHz) without significant switching losses [8]–[10]. Higher switching frequency enables a reduction in the size of the passive filters, improving the power density of the converter system. With SiC-based converter systems, it is possible to build converters even up to 7 MVA without liquid cooling due to lower losses and higher maximum operating junction capability of SiC-based devices. These SiC MOSFETs exhibit a safe operating area for all

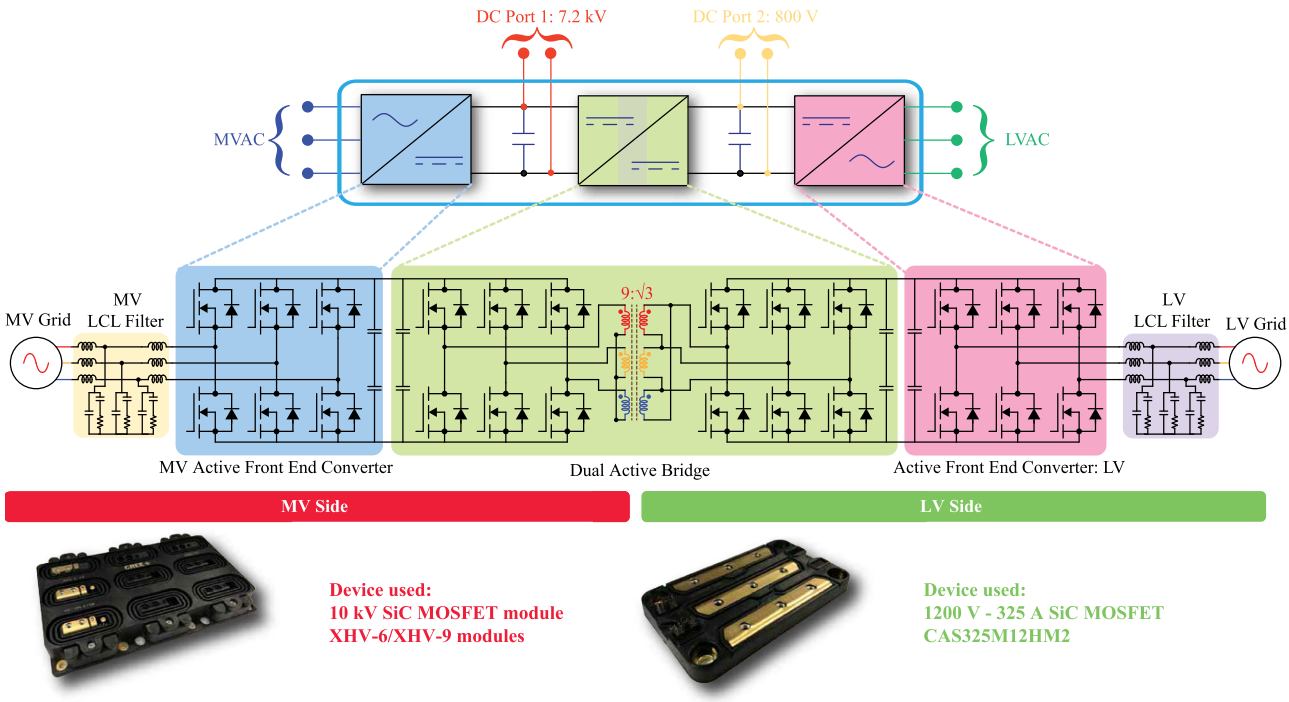


Fig. 1. Schematic of the hardware implementation of the overall system architecture. The MUSE-SST consists of three parts: MV AFEC, DAB, and LV AFEC.

values within their voltage and current ratings, which avoids any derating in higher power applications. These SiC-MOSFET-based MV converter systems find applications in power converters for renewable integration (photovoltaic integration), active filters, ship power systems, and solid-state transformers, where power density is one of the most important factors taken into consideration [11]–[15].

An MV solid-state transformerless intelligent power substation (TIPS) enabled by 15-kV SiC IGBTs is demonstrated in [11] and [16]. The TIPS is aimed at integrating an MV distribution grid (13.8 kV) with a low-voltage (LV) grid (480 V). A three-level NPC structure is used as the building block for the MV converter systems. The use of 15-kV IGBTs ensures a lower conduction loss than similarly rated MOSFETs [8]. However, the switching frequency for the active-front-end converter (AFEC) is limited to 5 kHz, owing to the large tail current for the IGBTs. An isolated front-end 6.6-kV/400-V ac–dc solid-state transformer is designed and demonstrated in [17]. However, it employs an input series-output paralleled arrangement of multiple LV converter cells. Recently, a 10-kV SiC-MOSFET-based 7 kV to 400-V dc–dc transformer is demonstrated in [9]. An MV transformerless grid-connected (13.8 kV) dc–ac converter design is presented in [18]. A 1-MVA solid-state power substation based on 10-kV SiC MOSFETs is presented by General Electric, which is half the size and one-fourth the weight of a comparable conventional 60-Hz transformer [19].

A Gen3 10-kV SiC-MOSFET-enabled mobile utility support equipment based solid-state transformer (MUSE-SST) for interfacing a 4.16-kV grid to a 480-V grid is introduced in [20] and [21]. The MUSE-SST consists of three power conversion stages, as shown in Fig. 1:

1) MV ac–dc stage: medium-voltage active-front-end converter (MV-AFEC);
2) MV dc/LV dc stage: dual active bridge (DAB);
3) LV dc–ac stage: low-voltage active-front-end converter (LV-AFEC).

In the MUSE-SST system, the three-phase 4.16-kV grid voltage is rectified by a three-phase two-level inverter to a dc voltage level of 7.2 kV. For the MV side, a grid voltage rating of 4.16 kV requires a peak phase voltage of 3.4 kV, which, in turn, requires a dc link of approximately 6.8 kV of dc bus, assuming an operating modulation index of 1 with a sinusoidal pulsewidth modulation (PWM) technique. However, considering a 5% drop in the ac-side filter and operating a modulation index of 0.8, the dc bus is designed to operate at 7.2 kV with space vector modulation. A dc–dc stage is used in cascade with the rectifier to provide galvanic voltage isolation required for grid interconnection and to step down the voltage from MV to LV levels. The dc–dc stage is followed by a dc–ac stage to connect to the lower voltage grid (480-V grid). The MV stage is isolated from the LV stage using three MV high-frequency transformers, which form a part of the dc–dc stage. It should be noted that three single-phase high-frequency transformers connected in a star/delta configuration are used. The choice of using three single-phase transformers to one three-phase transformer arises from the required basic lightning impulse insulation (BIL) voltage rating of the transformers. According to the IEEE Standard for Insulation Coordination [22], BIL is defined as the electrical strength of insulation expressed in terms of the crest value of a standard lightning impulse under standard atmospheric conditions. The design of the three-phase transformer has a higher requirement on the BIL rating as compared with three single-phase

TABLE I
BIL RATING REQUIREMENTS OF TRANSFORMERS

Transformer	*Voltage rating (peak)*	*BIL rating requirement*
Single-phase	4800 V	26.66 kV
Three-phase	7200 V	40 kV

TABLE II
PARAMETERS OF THE MV CONVERTER SYSTEM

Parameter	*Value*
Dc-link voltage	7.2 kV
Peak current	25 A
RMS current	17 A
Maximum power	100 kW
Switching frequency	10 kHz

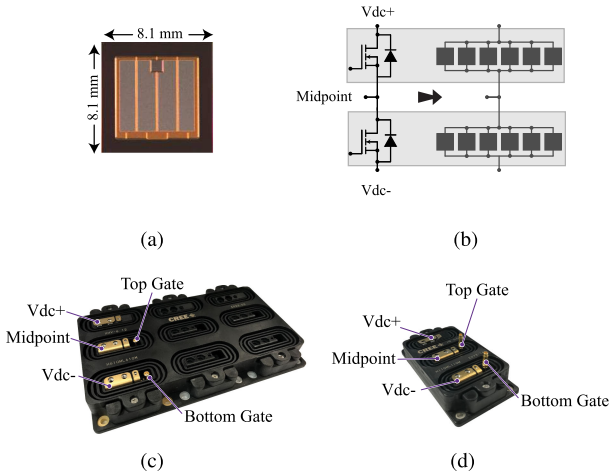


Fig. 2. (a) Picture of a bare die. Reproduced from [27]. (b) Six 10-kV SiC MOSFET dies in parallel packaged in the form of a half-bridge in an XHV module enabling a total RMS current rating of 50 A at 150 °C. (c) 10-kV SiC MOSFET packed in an XHV-6 module. The first submodule is populated, and the other two submodules are kept unpopulated. (d) 10-kV SiC MOSFET packed in an XHV-9 module.

transformers due to the higher voltages (line voltage) seen by the three-phase transformer as compared with the single-phase transformer, where it experiences the phase voltage. Table I gives the BIL ratings required by the individual transformers as determined by IEC 60076-1 [23], [24]. The voltage rating for the transformers is provided based on the peak voltage across the high-frequency transformers. For a dc-link voltage of 7200 V, the line-to-neutral voltage is 4800 V, and the line-to-line voltage is 7200 V. In addition, single-phase transformers exhibit greater modularity as compared to the three-phase transformers.

The MV and LV power converter systems are built as three-phase systems for each of the power conversion stages, which serve as building blocks for the MUSE-SST. Table II presents the important parameters for the MV converter system. The system is enabled by Wolfspeed Gen3 10-kV SiC-based MOSFETs in an extra high voltage (XHV) module on the primary side and 1200-V 325-A CAS325M12HM2 high-performance Wolfspeed modules on the secondary side [25].

The use of 10-kV SiC MOSFETs in simple two-level converters brings along a lot of challenges in terms of MV insulation, thermal management, and high-dv/dt considerations. This requires careful design consideration of the 10-kV SiC-MOSFET-based MV power converters. In [26], the design and assessment methodology of a 10-kV SiC-MOSFET-based half-bridge module is carried out considering the effect of the high-voltage insulation and high dv/dt exhibited by the devices on the gate drivers. However, the effect of this high dv/dt on other parts of the system, which includes the controller implementation and the magnetic design, is not discussed.

This article focuses on the design considerations, advantages, and challenges associated with the design and operation of the MV-AFEC stage of the MUSE-SST system. This includes the design of the gate drivers, busbars, and other auxiliary systems. The efficiency of the system is also estimated using simulations and measured via back-to-back tests. Thermal considerations that are essential for the system are also provided.

The rest of this article is organized as follows. Section II introduces the 10-kV XHV power module used for building the MV converter systems. Conduction and switching loss data are also provided using static and dynamic characterization of the devices. Section III focuses on the design and development of a two-level three-phase converter system, which acts as the building block for the MV-AFEC and the MV side of the dc–dc stage. Section IV provides hardware challenges associated with developing the MV-AFEC system, including the issues in implementing the inductive filter and issues in sensing voltages and currents in a high-dv/dt environment. Section V gives a brief idea regarding the controller design for the MV-AFEC system. Experimental verification of the operation of the three-phase two-level MV converter system is validated in Section VI. Efficiency estimation of the MV converter system is given in Section VII. Finally, Section VIII concludes this article. Appendixes A and B are provided, showing a brief derivation of the transfer functions of the converter system. Stability analysis of the MV converter with an active load is also provided. The appendixes are followed by references.

II. GEN3 10-KV SIC MOSFET-BASED XHV POWER MODULES

The building block for the MV converter system is the Gen3 10-kV SiC MOSFET packaged in an XHV power module, as shown in Fig. 2. Two XHV packages are currently available, namely, XHV-6 and XHV-9. XHV-6 consists of three half-bridges in a single package, while the XHV-9 package is a half-bridge configuration. Each switch position can accommodate up to six 10-kV SiC MOSFET dies in parallel. However, the number of dies that could be populated is selected according to the user's requirement. The internal schematic of the module is shown in Fig. 2(b). The MV converter systems employ XHV-6/XHV-9 modules. Each switch position is populated with six dies (total RMS current rating of 50 A at 150 °C).

The static characterization of the devices is carried out in the laboratory at different temperatures with a B1505A Power Device Analyzer from Keysight technologies. The ON-state resistance of the MOSFET module is measured for a

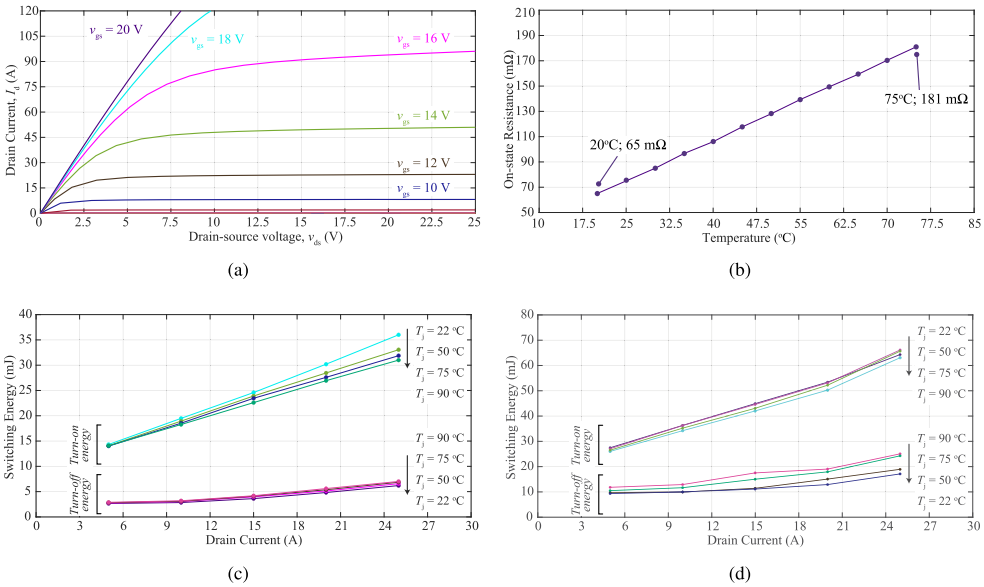


Fig. 3. (a) Measured I–V characteristics of the 10-kV SiC MOSFET module at room temperature ($T = 25\,^{\circ}$C). (b) Variation of ON-state resistance with temperature. (c) Switching energy of the device at various currents and temperatures for a dc-link voltage of 3.5 kV. (d) Switching energy of the device at various currents and temperatures for a dc-link voltage of 7.2 kV.

gate voltage of +15 V as recommended by the manufacturer. Fig. 3(b) shows the variation of ON-state resistance with temperature.

Double-pulse tests are carried out to estimate the turn-ON and turn-OFF switching energy of the 10-kV SiC MOSFET modules [28]. The double-pulse tests are carried out on the same converter system to ensure that the commutation loop inductance during the double-pulse tests does not vary significantly compared to the actual converter operation, thus providing an accurate loss estimation. The sole difference between both the test setups is the addition of a low inductive current shunt, SSDN-005, M4× 8 mm, stud input from T&M Research Products, Inc. (to measure the current during double-pulse tests). This causes a minor variation in the commutation loop inductance ($<$ 20 nH) for both setups. However, for 10-kV MOSFETs, since the operating voltage is high and the current is low, a slight change in the commutation loop inductance does not affect the losses significantly, unlike LV high-current devices [29]. The voltage measurement for the double-pulse tests is carried out using a CIC Research based high-voltage differential probe (DP10-10K-16kV-C), which offers voltage measurement up to 16-kV RMS and 20-kV peak and a bandwidth of 120 MHz [30].

The variation of turn-ON and turn-OFF switching energy with respect to temperature and drain current is shown in Fig. 3(c) and (d) for a dc-link voltage of 3.5 and 7.2 kV, respectively. The ON-state gate voltage is kept at +15 V (as recommended by the manufacturer), and the gate resistance is kept at 20 Ω to ensure a maximum dv/dt of 40 kV/μs [31]. It should be noted that the maximum switching speed is limited to 40 kV/μs due to the fact that an increase in switching speed does not decrease the effective switching losses of the device beyond a certain value owing to the additional current through the parasitic capacitance present in practical inductor designs [32]. This is further explained in Section IV.

TABLE III
THERMAL LIMITS WITH DIFFERENT SWITCHING FREQUENCIES FOR AN OPERATING DC-LINK VOLTAGE OF 7.2 KV FOR A 10-KV SIC MOSFET

f_{sw} (kHz)	i_d (A) (RMS)	P_{cond} (W)	P_{sw} (W)	$T_{j,max}$ (°C)
1	35.3	377	81	151.2
2	31.66	301.9	147.3	149.2
5	23.84	172.15	277.1	150.7
10	16.39	82.22	371.56	151.9

*Data are based on the device losses from Fig. 3(d) and the current heatsink design, which has a heatsink to ambient thermal resistance of 0.026 °C/W. The RMS device current rating of 10.7 A translates to 100-kW operation of the MV system.

It should be noted that high values of switching energy loss limit the maximum current during hard-switched applications. With a heatsink to ambient thermal resistance of 0.026 °C/W (as explained later), a maximum junction temperature of 150 °C, and an ambient temperature of 25 °C, the maximum operating range for the 10-kV SiC MOSFET modules is calculated in Table III for an operating dc-link voltage of 7.2 kV. This proves that even if the devices are rated for higher currents, the maximum current needs to be limited to account for the switching loss in the devices, especially in hard-switching applications. The junction-to-case thermal resistance for these 10-kV SiC MOSFETs (with six parallel dies) is 0.078 °C/W for each 10-kV SiC MOSFET [33]. In [33], the thermal resistance of 18 parallel dies is shown. The value is adjusted for six parallel dies.

III. DESIGN AND DEVELOPMENT OF THE MV CONVERTER SYSTEM

The MV converter system is referred to as a medium-voltage power block (MVPB) and consists of a three-phase two-level converter system. With a two-level MV converter, each of the

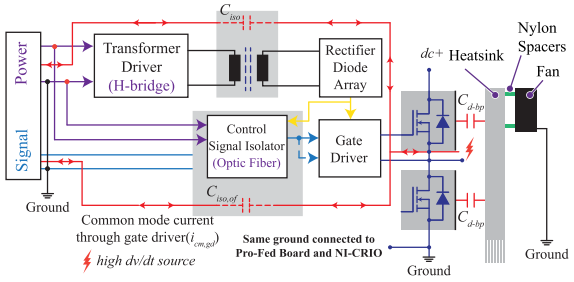


Fig. 4. Schematic representation of the CM current path for the high-side gate driver and the heatsink in a half-bridge configuration [34]. (x can be any component, including gate driver isolation transformer, signal isolator, or the heatsink).

power semiconductor devices experiences the full dc-link voltage. Operating these devices at high-voltage levels requires the MV SiC devices to operate reliably and requires careful design considerations of the auxiliary systems.

A. Common-Mode Current Considerations

MV converters are generally plagued with common-mode (CM) current issues, which need to be accounted for while designing and running the system [31], [34]. Due to the high dv/dt exhibited by these devices, the parasitic capacitance across various components is of paramount importance. These CM currents flow through the ground and might lead to disruptions in the control ground, since the controller and the protection board is connected to the same ground. This can compromise the signal integrity [31], [34]. Since the MV devices exhibit a high dv/dt, controlling the effective parasitic capacitance reduces the CM currents, thus maintaining signal integrity.

Special design considerations need to be carried out for designing gate drivers to have an ultralow capacitive coupling across the isolation transformer. Careful consideration needs to be taken to achieve this since the gate driver calls for high-voltage isolation and a small footprint to make the design usable. According to the MV requirements, an optimized gate driver is designed, and extensive testing is carried out to validate its operation in converters, as shown in [31]. The CM current path in the MV system is shown in Fig. 4. In order to eliminate the CM current through the fan, nonconducting nylon spacers are provided between the heatsink and the fan to disrupt the path of the CM currents. In addition, the electrical ground of the fan is adequately isolated from the gate driver signal ground by providing discrete paths for these CM currents.

B. Busbar Design Considerations

The design considerations for the busbar start off with the placement of the capacitors and the devices. For MV converters, it is challenging to build capacitors with high capacitance value and high energy density [35]. Furthermore, it is imperative to have low series inductance for the capacitors to avoid ringing due to LC oscillations [11], [35]. In the MVPB, film capacitors are used due to their higher reliability over electrolytic capacitors

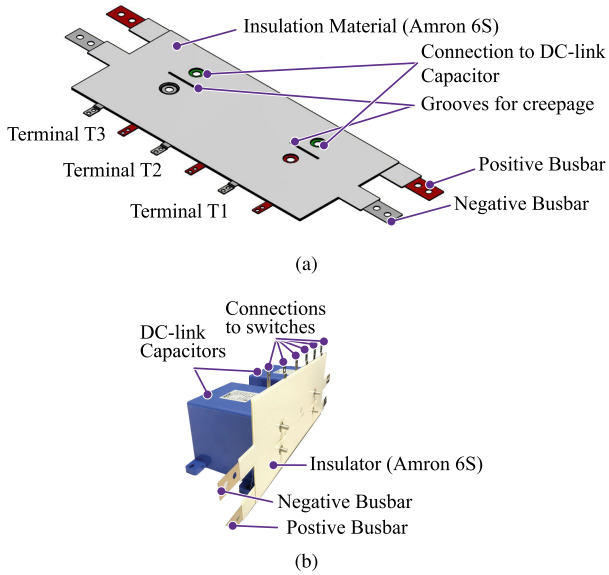


Fig. 5. (a) CAD diagram of the busbar used in the MV converter system. (b) Placement of the dc-link capacitors on the busbar along with the fingers for connecting it with the XHV power modules.

(which generally have a higher energy density). To accommodate a blocking voltage capability of 10 kV and to form the main dc-bus capacitor, two film capacitors from ICAR (5 kV; 50 μF; LNK-P4X-50-500) are connected in series.

Additional snubber capacitors are connected directly to the dc terminals. The instantaneous high-frequency switching current is supplied by these additional snubber capacitors (3300 pF; 6 kV; FKP1Y013305H00JSSD) and is not supplied from the main dc-bus capacitors, and therefore, the effect of the busbar commutation loop inductance is minimized. A series–parallel combination of these capacitors, where two capacitors are connected in series and four of the series-connected capacitors are connected in parallel, is selected to ensure the required voltage rating (12 kV) and the required snubber capacitance (6.6 nF). These capacitors have a dv/dt rating of 29 V/ns, individually, which corresponds to a maximum pulse current rating of 95 A per capacitor [36]. For the series–parallel combination, the effective current rating is $95\ \text{A}/2 \times 4 = 190$ A, which is adequate for the system. Hence, the same design can be used to further push the limits of the 10-kV SiC MOSFET modules in terms of higher dv/dt.

The 10-kV SiC MOSFET modules are connected through fingers on the busbars shown in Fig. 5(a), which increases the commutation loop inductance. Due to the vertical structure of the setup and the placement of the module terminations, it is not possible to construct the busbar without the fingers. Vertical design for the busbar is carried out, taking into account the design and placement of the heatsink, as explained later in this section.

A sandwiched busbar structure with Amron 6S insulation is manufactured and tested up to 17-kV dc across the terminals for a period of 30 min, and no leakage currents are observed proving the insulation considerations. Necessary clearance and creepage distances are provided between the dc terminals. The sandwich structure, as shown in Fig. 5(b), is used to minimize

TABLE IV
LOOP INDUCTANCE OF THE BUSBAR

Parameter	*Inductance*
Input to Terminal T1	84.71 nH
Input to Terminal T2	78.01 nH
Input to Terminal T3	81.73 nH
External Positive Finger	15.61 nH
External Negative Finger	15.69 nH

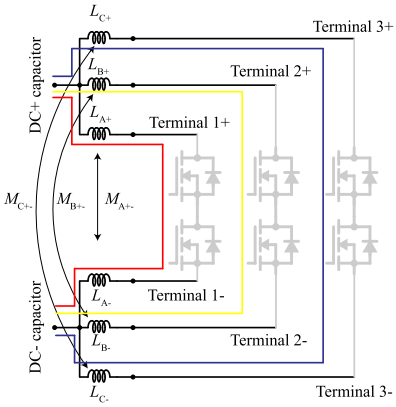


Fig. 6. Mutual inductances between the different phases, and the commutation loop paths for the three different phases.

the commutation loop inductance. The busbar conductor is constructed using aluminum, and the thickness of the conductor plate is kept at 1.5 mm for a current of 30 A, and some margin for mechanical stability. Necessary creepage distances between the capacitor terminals are also provided. Finite-element method (FEM) simulations are carried out in Ansys Q3D to estimate the commutation loop inductance, and the results are shown in Table IV. For estimating the commutation loop inductance, it should be noted that the mutual inductance between different phases does not affect the commutation loop inductance since the commutation path involves only a single phase, as shown in Fig. 6. As an example, it can be seen that the commutation loop inductance of Phase A is dependent only on L_{A+}, L_{A-}, and M_{A+-}, and not on the self/mutual inductances between other phases.

Temperature and current distribution through the busbar is also estimated, as shown in Fig. 7. The estimation is carried out at a single point of operation, where one of the phases (A-phase) experiences a full current of 20 A, and the other two phases (B-phase and C-phase) each carries half the current (10 A each). This estimation is carried out in COMSOL Multiphysics. It should be noted that the busbar experiences a minimal temperature rise on account of its large surface area, which minimizes the effective resistance.

C. Thermal Considerations

The MVPB employs an efficient thermal solution that uses a loop thermosyphon-based heatsink. The heat generated by the power semiconductor devices during operation causes the liquid inside the evaporator to change its phase, which, combined with the condensation of liquid in the condenser, generates a gravitational pressure imbalance that maintains the fluid circulation

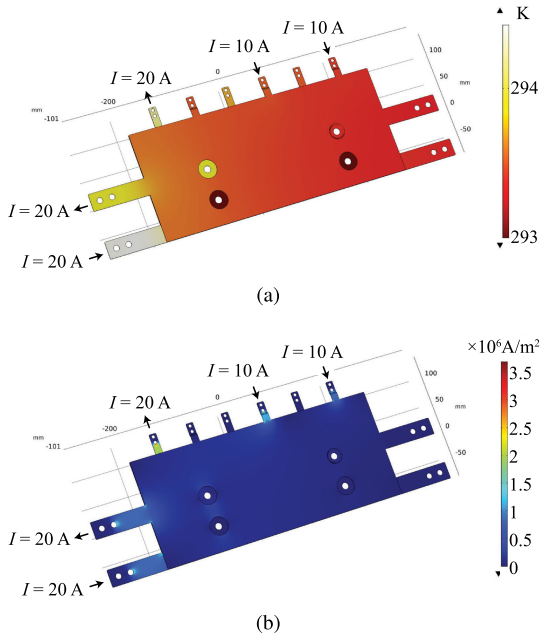


Fig. 7. (a) Temperature and (b) current distribution in the busbar with a current input of 20 A and natural air flow.

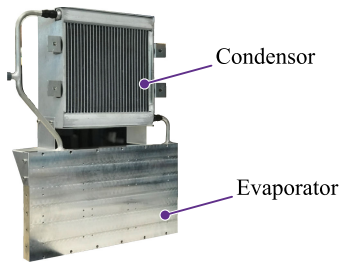


Fig. 8. Picture of the loop thermosyphon solution used for heat dissipation in the MV converter system. The evaporator is designed to dissipate up to 10 kW by just changing the condenser without any change in the total footprint.

between the condenser and the evaporator. A photograph of the loop thermosyphon solution is shown in Fig. 8. The thermal system design is carried out in collaboration with Advanced Cooling Technologies for manufacturing this heatsink [37]. One of the major advantages of the loop thermosyphon solution is the scalability of the system. The evaporator is designed to dissipate up to 10 kW by just changing the condenser (heat exchanger). This proves to be a big advantage when the system is scaled to higher power levels.

Considering the limits of the 10-kV 90-A SiC MOSFETs, a dc-link voltage of 7.2 kV and an RMS current of around 70 A is designed, which translates to a 500-kW inverter. Extrapolating the device loss curves, a rough estimation shows the total loss in all the devices is around 9 kW (1.5 kW per switch). Thus, the 10-kV 90-A SiC MOSFET modules and busbar structures can be used for up to 500 kW by just replacing of the heat exchanger section of the heatsink in the same footprint without any other changes to the power block. Fig. 9 shows an FEM simulation of the evaporator block, where the temperature of the evaporator

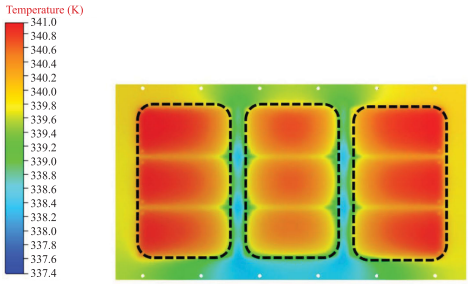


Fig. 9. FEM simulation of the loop thermosyphon solution.

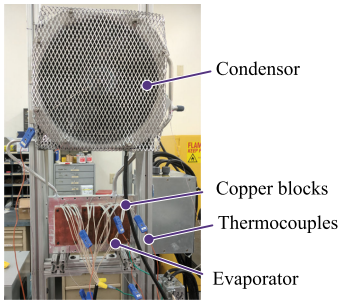


Fig. 10. Photograph for the setup for testing and validating the operation of the loop thermosyphon before using it in the MV converter system.

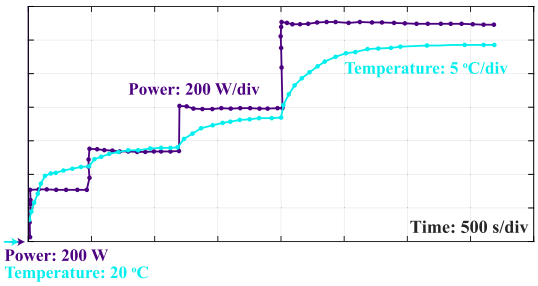


Fig. 11. Test data for the loop thermosyphon solution. The power is increased in steps, and the temperature at one particular point (close to the die position) is noted.

block is shown. An ambient temperature of 50 °C is assumed. The FEM simulation is based on two boundary conditions:

1) total power: 2000 W;
2) coolant temperature: 60 °C.

The maximum evaporator temperature is 68 °C. The power loss on the heatsinks is emulated by attaching copper blocks and heating them using a standard resistive heater cartridge. A photograph of the setup is shown in Fig. 10. Type T thermocouple probes are used to measure the temperature at different points on the heatsink. The loop thermosyphon solution is tested up to a power level of 1500 W, and the maximum temperature of the evaporator is noted. The thermal resistance and capacitance of the heatsink are measured by applying power step changes on the heatsink, as shown in Fig. 11. The thermal resistance of the heatsink is 0.026 °C/W, and the thermal capacitance is estimated as 793 J/°C. The calculation of the thermal resistance and thermal capacitance is carried out according to [38]. A thermal model is generated from the extracted data, as shown

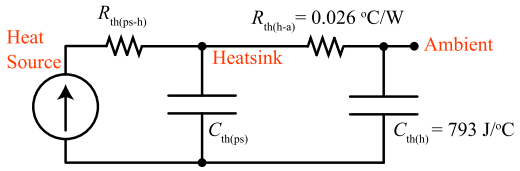


Fig. 12. Thermal network model of the loop thermosyphon solution.

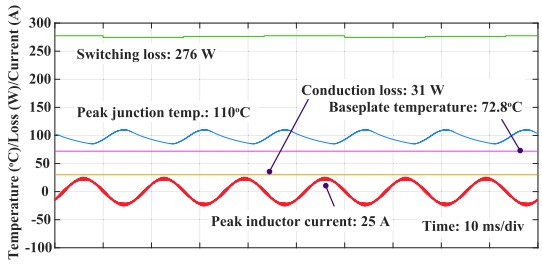


Fig. 13. Thermal simulation results carried out in PLECS for a 7.2-kV 100-kW operation from the parameters measured from the loop thermosyphon heatsink and the device thermal characteristics.

TABLE V
THERMAL SIMULATION RESULTS FOR THE SYSTEM AT RATED CONDITIONS OF 7.2 KV AND 100 KW

Parameter	*Value*
DC-link voltage	7.2 kV
Peak AC current	25.7 A
Rated power	100 kW
Switching loss (per device)	276 W
Conduction loss (per device)	31 W
Total loss (per device)	307 W
Total loss on one heatsink	1843 W
Maximum junction temperature	110°C (module is rated at 175°C)
Maximum heatsink temperature	73°C

in Fig. 12. $R_{th(ps-h)}$ and $C_{th(ps)}$ represents the effective thermal resistance and capacitance from the heat source (die) till the heatsink. A brief thermal simulation is carried out to validate the design of the loop thermosyphon system. The total losses for the system operating at 100 kW (at 7.2 kV dc-link voltage) are extracted from Fig. 3(b) and (d). The junction-to-case thermal resistance of the 10-kV SiC MOSFET module, along with the heatsink data, is fed into a PLECS model, and the result is shown in Fig. 13. An ambient temperature of 25 °C is taken. It can be seen that the total switching losses at rated conditions of 7.2 kV and 100 kW power transfer results in a single device switching loss of 276 W and the conduction losses of 31 W. This gives a total loss of 307 W per switch, thereby rendering a total power loss of 1843 W for one heatsink. A maximum junction temperature of 110 °C is seen, which is well within the maximum operating junction temperature of these devices and modules. This is tabulated in Table V.

D. Designing the Support Structure

A support structure is designed to hold the loop thermosyphon vertically to provide an effective cooling configuration of the

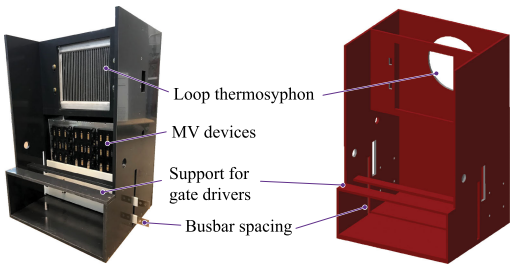


Fig. 14. CAD model and photograph of the support structure of the MV converter system.

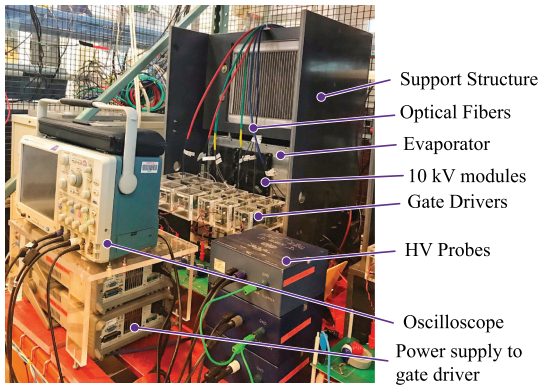


Fig. 15. Photograph of the MVPB.

evaporator plates. Moreover, the support structure should provide easy accessibility to the busbars, gate drivers, capacitors, and also the mounted sensors. The computer-aided design (CAD) diagram of the support structure and a picture of the support structure are shown in Fig. 14. The support structure provides an effective solution to placing all the different components on one structure, making it modular in nature. It is made up of PVC material and provides structural balance to the system.

E. Medium-Voltage Power Block

Taking into account all the design considerations, the MVPB is built, as shown in Fig. 15. In addition, thermocouples are connected to the baseplate of the module to estimate the baseplate temperature. The baseplate is painted black to estimate the evaporator temperature using a thermal camera.

Cost, volume, and weight division analyses of the MVPB are carried out. Since this power block is aimed at an MV-AFEC, the analysis takes the filter inductor into account. The cost/kW ($/kVA) of the laboratory prototype is $550/kW. The cost division of the MV-AFEC is carried out, as shown in Fig. 16(a). It should be noted that since these 10-kV SiC MOSFETs are at a nascent stage of development and are available only as custom-made modules, the percentage of the cost of the 10-kV SiC devices does not reflect the true operating cost of such a system in widespread field applications.

Similar to the cost division, a volume and weight division of the converter system is also carried out, as shown in Fig. 16(b) and (c). The dimensions of the MVPB is given by 520 mm × 490 mm × 820 mm. The weight of the power block

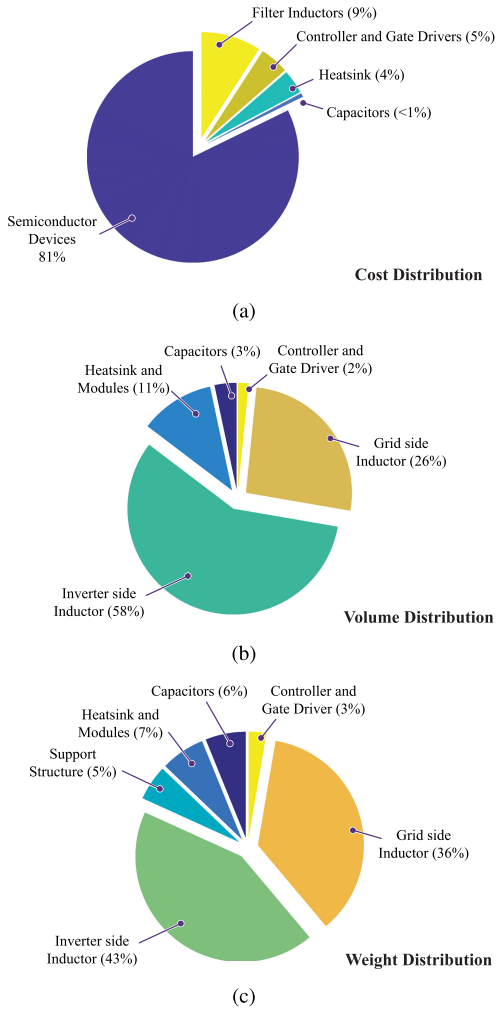


Fig. 16. (a) Cost, (b) volume, and (c) weight distribution of the components used in the MV-AFEC system.

TABLE VI
DESIGN ASPECTS OF THE MV-AFEC SYSTEM

Parameter	*Value*
Cost/kW	$550/kW
Weight/kW	3.6 lb./kW
Volume/kW	4.63 l/kW

is around 65 lb. In the system, the converter-side inductor is mounted on a small cart, and the total size of the inductor is around 500 mm × 700 mm × 500 mm, while the weight is approximately 160 lb. The grid-side inductor, which is built as a single three-phase inductor, has dimensions of 620 mm × 316 mm × 405 mm and weighs approximately 135 lb. Table VI presents the design aspect of the MV-AFEC system in terms of cost, volume, and weight per kilowatt for the MV-AFEC.

IV. HARDWARE CHALLENGES FOR DEVELOPING THE MV-AFEC SYSTEM

The MVPB is designed to provide a modular three-phase two-level system that can be used in any converter system. Apart from the hardware challenges mentioned in the previous section,

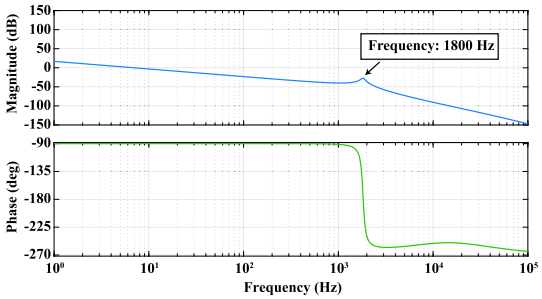


Fig. 17. Frequency response of the LCL filter.

designing an MV front-end converter requires careful design and implementation of additional components, such as current filters, voltage and current sensors, and a hardware controller system.

A. Filter Design Considerations

As mentioned earlier, an LCL filter with $R_{\rm d}$–$C_{\rm d}$ damping is used in the MV front-end converter system. The current through the filter capacitor is designed at 10% per unit (p.u.), which decides the values of the filter capacitors

$$C_{\rm f} + C_{\rm d} = \frac{0.1}{2 \times \pi \times 60 \times Z_{\rm p.u.}} \tag{1}$$

where $Z_{\rm p.u.}$ is the per-unit impedance of the converter system. $C_{\rm f}$ and $C_{\rm d}$ denotes the values of the filter capacitors. For the filter inductors, the total inductor drop at rated condition is considered at 5%. The effective resonance frequency ($\omega_{\rm res}$) is designed at 1.8 kHz, which is more than five times from the seventh harmonic frequency and lower than one-fifth of the switching frequency

$$\omega_{\rm res} = \sqrt{\frac{L_{\rm s} + L_{\rm g}}{L_{\rm s} \times L_{\rm g} \times (C_{\rm f} + C_{\rm d})}}. \tag{2}$$

The grid-side inductor and the converter-side inductor are 7.7 and 15.5 mH, respectively, and are calculated according to [39]. A passive damping technique is adopted in this design to suppress the resonance frequency components of current. The value of damping resistance is 20 Ω and is calculated according to [40]. The detailed design procedure to calculate the values of the filter parameters is provided in [21]. A frequency response of the designed LCL filter is shown in Fig. 17, where the designed corner frequency of 1.8 kHz can be seen. Physically, the converter-side inductor needs to be designed to withstand a switching frequency voltage component over the fundamental frequency component, as well as a switching current ripple. On the other hand, the grid-side inductor witnesses only the fundamental frequency component of current as the LCL filter provides higher order filtering. This further helps to smooth out the voltages across the grid-side inductors. This makes the physical design of the converter-side inductor to be more challenging as compared to the grid-side inductor.

Furthermore, the design of the converter-side MV filter inductors also needs careful design considerations with respect to the parasitic capacitance across them. This is due to the high dv/dt observed across them during the switching transitions [41]. The parasitic capacitance across the inductor is detrimental for the system on account of the fact that a differential mode (DM) current flows through the parasitic capacitance, which, in turn, flows through the switching device, creating additional switching losses, and thus decreasing the reliability of the system [32], [41]. To validate this, an experiment is conducted on the three-phase two-level inverter system, with an RL load. An external capacitance of 1000 pF is connected across the inductors to emulate the parasitic capacitance. A dc bus voltage of 2500 V is supplied, and a switching frequency of 20 kHz is used. An additional spike current of up to 10 A is observed, as shown in Fig. 18. The additional current is the effect of the high dv/dt of these devices and the effective parasitic capacitance across the differential current path.

In the MV front-end converter system, for the converter-side inductors, a series of LV inductors is connected to achieve the required MV level, as shown in Fig. 19(a).

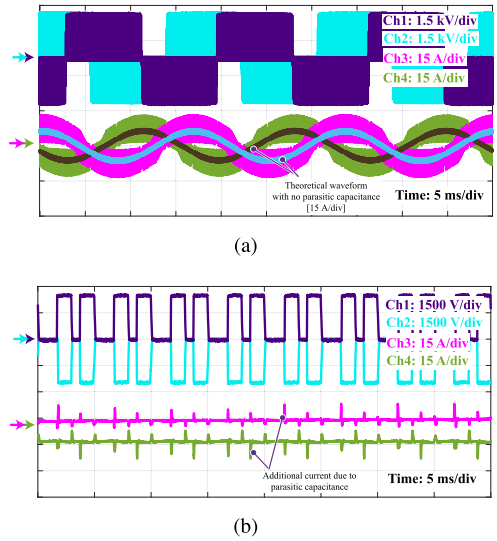


Fig. 18. (a) Experimental results of the three-phase inverter with an input voltage of 2500 V. (c) Zoomed-in version where a spike is observed in the current due to the high dv/dt across the 10-kV SiC MOSFET and the parasitic capacitance across the filter inductors. (Ch1: Line-to-line voltage across R-phase; Ch2: Line-to-line voltage across Y-phase; Ch3: R-phase current; Ch4: Y-phase current) [32].

Fig. 19. Photograph of the (a) converter-side inductors and (b) grid-side inductors. A single-phase of the converter-side inductors is shown.

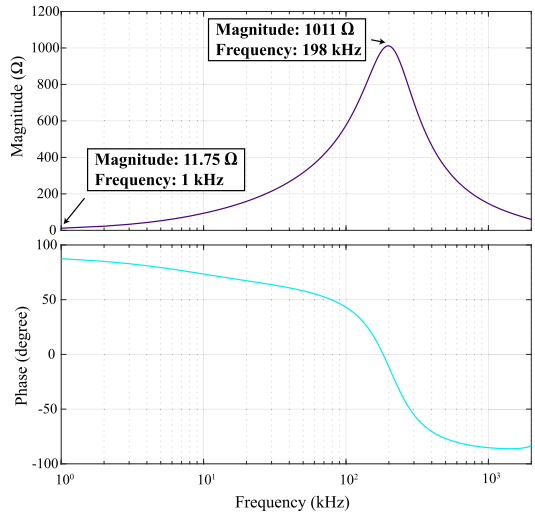


Fig. 20. Impedance plot of a single LV inductor.

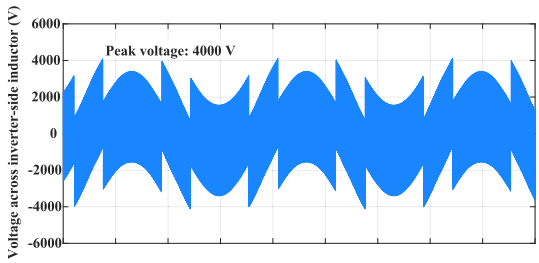


Fig. 21. Voltage across the series-connected converter-side inductor for demonstrating the peak voltage across the series-connected structure.

A frequency characterization is carried out to measure the inductance and capacitance of the inductors. From the frequency characterization of a single inductor (see Fig. 20), the inductance value at 10 kHz is 1.75 mH as compared with 2.25 mH at 60 Hz. Since the inductance requirement for the converter-side filter is 15.5 mH (see Section IV-A), nine inductors in series yield 9×1.75 mH $= 15.75$ mH. The converter-side inductor experiences a maximum voltage of nearly 4 kV, as shown in Fig. 21, for a grid voltage of 4.16 kV and a dc-link voltage of 7.2 kV. In the system, nine inductors are connected in series, each having a recommended voltage rating of 600 V [42].

A voltage rating of 600 V for an individual inductor leads to an effective voltage rating of 9×600 V $= 5.4$ kV. Since the maximum voltage experienced by the inductors is 4 kV, the converter-side inductors are able to handle the voltage sufficiently.

A brief analysis of the parasitic capacitance of these inductors is carried out to ensure a low DM current. Since these are commercially LV inductors, a high parasitic capacitance of these inductors is expected. The parasitic capacitance of the inductor is evaluated from the frequency characterization curve. With the resonance frequency at 198 kHz and inductance of 1.8 mH, a parasitic capacitance of 0.36 nF is expected. Nine of these inductors are connected in series to reduce the effect of this parasitic capacitance, as well as to achieve the required voltage rating. Under the assumption of all the nine inductors being exactly identical, the equivalent inductance and the equivalent capacitance is

$$L_{\text{eq}} = 9 \times L_{\text{ind}} = 9 \times 1.8 \text{ mH} = 15.75 \text{ mH} \tag{3}$$

$$C_{\text{p(eq)}} = \frac{1}{9} \times C_{\text{p(ind)}} = \frac{1}{9} \times 0.36 \text{ nF} = 0.04 \text{ nF}. \tag{4}$$

Measurements of the parasitic capacitance and the inductance of different inductors are carried out, and the variation is found to be minimal ensuring the correctness of the assumption of the equality of the nine inductors.

The series connection of LV inductors offers a multitude of advantages. The series connection of these inductors helps in reducing the effective parasitic capacitance across the filter inductors. Since these are series-connected structures, it offers a level of modularity while scaling up MV converter systems. The grid-side inductor does not need any special consideration and is built as a single three-phase inductor, as shown in Fig. 19(b).

B. Voltage and Current Sensing

The voltage sensing for the MV converter system is carried out using a commercially available sensor LEM DV4200/SP4, which can measure voltages up to 4000 V, with a bandwidth of 6.5 kHz. Half the dc-link voltage is measured using the sensor since the sensor has a maximum rating of 4000 V. A total measurement error of 1% is expected for this voltage sensor. This generates a maximum voltage measurement error of 36 V for the dc-link voltage measurement. The grid voltage measurements are carried out using commercially available LEM LV100-4000/SP2V voltage sensors.

The current sensing is carried out by off-the-shelf components. Current sensors, LEM LA-55P, are used in the MV converter systems since the total measured current is low. Four turns of wires are put in each current sensor, thus measuring four times the current, which helps in improving the accuracy of current sensing.

Due to the presence of high dv/dt in the system, a lot of noise is seen at the sensing output, which leads to incorrect feedback sensing and, thus, controller instability. To avoid this, a shield is provided on the sensing wiring and is directly connected to the earth. The presence of the shield reduces the noise at the sensing output since most of the CM currents, which travel through the sensing wires, get diverted to the earth terminal directly instead of the ground of the sensing board. This also ensures that the whole system is tied to a common point of reference. For additional precautions, CM chokes are placed on the power supply for the sensing board. A schematic of the sensing mechanism is shown in Fig. 22.

C. Controller Implementation and Protection-Feedback Board

The controller implementation is carried out using an NI CRIO-9024 in a Labview environment, as shown in Fig. 23(a). In this setup, the NI system is used over a more widely used DSP+FGPA interface keeping in mind that it is an industrial-grade controller meeting the necessary EMC standard EN61326 (IEC 61326) and can work with an operational humidity of 10% RH to 90% RH, noncondensing (IEC 60068-2-56) and

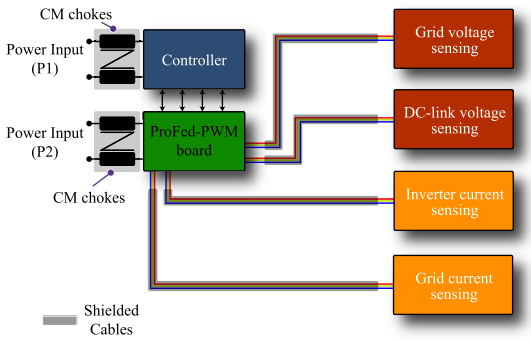


Fig. 22. Schematic of the voltage and current sensing mechanism.

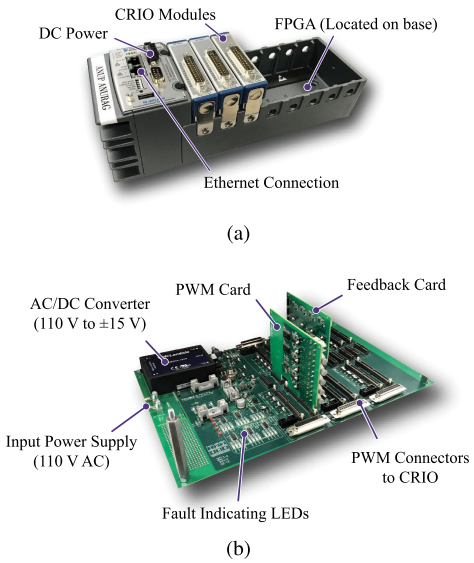


Fig. 23. Photograph of (a) NI CRIO-9024 controller used to control the MV converter system and (b) ProFed-PWM board used to interface the MV front-end converter system with the controller.

a pollution degree of 2 (IEC 60664) [43]. This is necessary since the system is aimed at implementation in the real field and commercialization. In addition, the modularity of the NI system relating to the choice of installed modules makes it the ideal choice for controller implementation.

A protection-feedback-PWM (ProFed-PWM) board is used for interfacing the controller to the system and is shown in Fig. 23(b). The ProFed-PWM board has three essential functions.

1) It provides optical PWM pulses to the gate drivers.
2) It converts current sense signals from the voltage and current sensors to voltage signals to interface with the controller.
3) It provides a level of hardware protection to the system by disabling the PWM pulses and informing the controller system when the sense voltages/currents exceed predetermined values.

TABLE VII
CONTROLLER PARAMETERS

Parameter	*Value*
Current controller bandwidth	1 kHz
Voltage controller bandwidth	100 Hz
$K_{\text{p\_cc}}$, $K_{\text{i\_cc}}/f_{\text{sw}}$	63, 0.6
$K_{\text{p\_vc}}$, $K_{\text{i\_vc}}/f_{\text{sw}}$	-0.00124, -1.2×10^{-6}

V. CONTROL DESIGN OF THE MV-AFEC SYSTEM

The control strategy for the MV-AFEC is aimed at maintaining the dc-link voltage at a set value. A closed-loop voltage-oriented current control based on a synchronous dq frame is used to control the MV-AFEC system. Fig. 24 gives the control strategy of the MV-AFEC system. A three-phase synchronous phase-locked loop is used for synchronizing the inverter voltage with the grid voltage. The dc-link voltage controller generates the current reference for the d-axis (i^*_{sd}) current controller, and the current reference for the q-axis is user controlled. A proportional–integral (PI) controller is used in the inner current control loop. Necessary feedforward terms are also added to the control path. The bandwidth of the inner current controller is designed to be ten times less than the switching frequency. Depending on these criteria, the controller parameters $K_{\text{p\_cc}}$ and $K_{\text{i\_cc}}$ are determined. Fig. 25 shows the transfer function between the grid current and the inverter voltage, with and without the PI controller. An outer voltage control loop is implemented to regulate the dc-bus voltage. This controller generates the d-axis current reference as the active power transfer between the dc and ac sides affects the dc-bus dynamics. The bandwidth of the dc-bus controller is designed to be ten times slower than the inner current loop to make sure that the controllers do not interact with each other. Fig. 24 gives the block diagram of the controller system. Additional information regarding different delays is provided in Appendix A. Table VII gives the parameters of the controller system. Furthermore, the effect of the sensor discretization has been taken into account while designing the controller parameters to achieve better dynamic performance. It is found that the effect of the sensor delays is negligible for designing the controller for the frequency range under consideration. The voltage controller is designed to achieve a target gain crossover frequency of 100 Hz (one-tenth of the current controller bandwidth). Fig. 26 presents the transfer function between the dc-bus voltage to the d-axis current with and without the PI controller. Additional information showing the derivation of the transfer functions for the controller is provided in Appendix A.

VI. EXPERIMENTAL TESTING OF THE MV CONVERTER SYSTEM

With the limited availability and high cost of the 10-kV SiC MOSFETs, simple tests, involving double-pulse tests, buck and boost converter tests, buck–boost converter tests, full-bridge tests, etc., are carried out at different voltage levels to evaluate the XHV modules [34]. The operations of the gate driver, heatsink, and the XHV modules are verified in these tests. A 10-kV dc power source from Magna Power is built by paralleling six

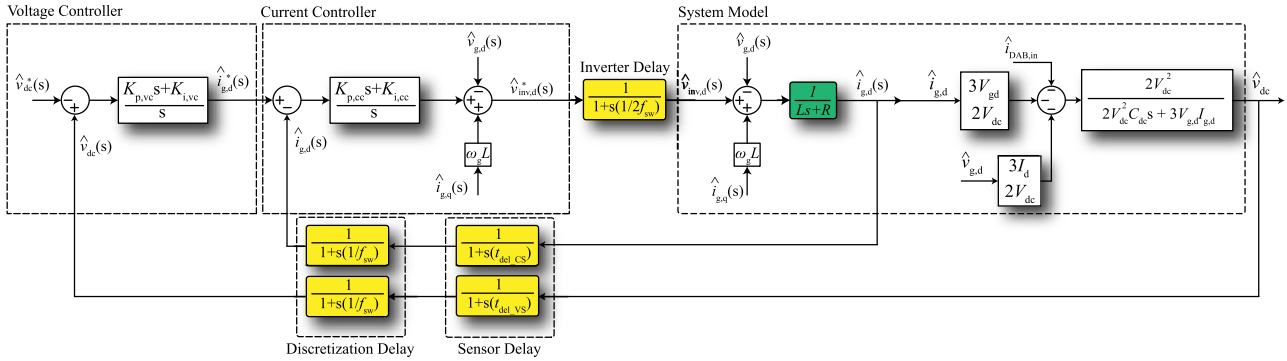


Fig. 24. *d*-axis current controller and the dc-bus voltage controller showing all the delays in the real system. The *q*-axis current controller is similar to the *d*-axis current controller with a small change in the input and the feedforward terms.

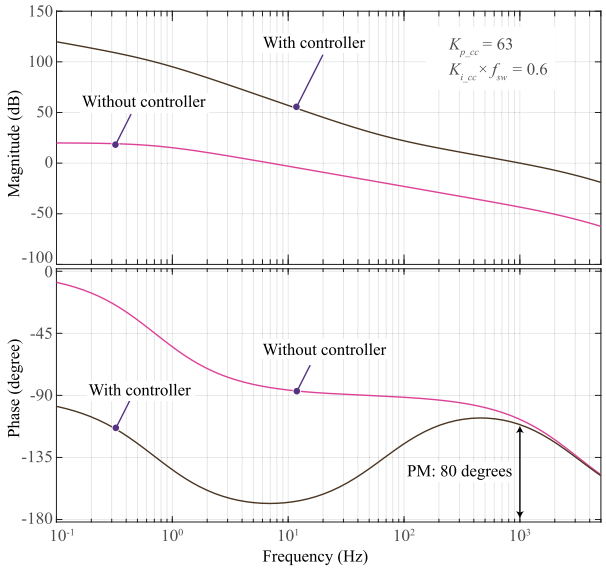


Fig. 25. Current controller design showing the system bode plot with and without the PI controller (PM: phase margin).

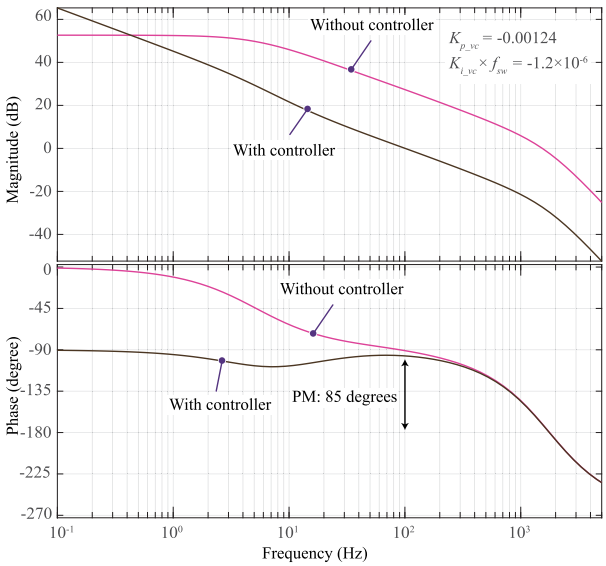


Fig. 26. Voltage controller design showing the system bode plot with and without the PI controller (PM: phase margin).

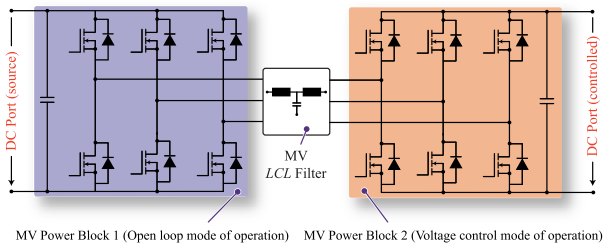


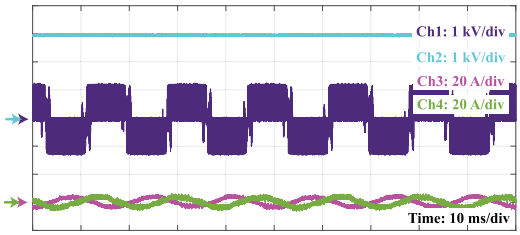
Fig. 27. Schematic of a back-to-back three-phase inverter test setup for testing the voltage control.

units of Magna Power XR10000-0.8/480 and is used for testing purposes.

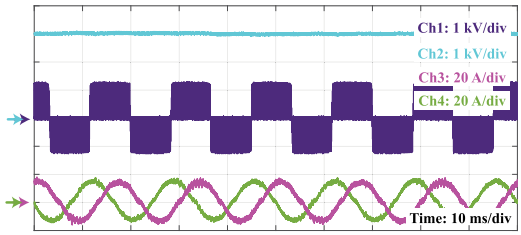
Initial testing of the MV converter system, including the voltage control, is carried out using a back-to-back system, as shown in Fig. 27. MVPB#1 provides the required three-phase ac voltage signal, which acts as the grid voltage, for MVPB#2. This testing closely resembles the operation of a grid-connected three-phase inverter system since MVPB#2 runs in the voltage control mode of operation with its ac port connected to a three-phase ac voltage source. This is safer than a grid-connected operation on account of the fact that the dc–ac conversion stage (MVPB#1) is controllable. The dc power supply has in-built protection functions, which turn OFF the input voltage during abnormal situations.

Various experimental tests are carried out to validate the operation of these devices in an MV-AFEC system. Experimental test results at a 3000-V dc-link voltage for MVPB#2 for an active current of 5 A and a reactive current of 0 and 10 A are shown in Fig. 28(a) and (b), respectively. MVPB#1 is operated in open loop at a dc-link voltage of 1200 V and a modulation index of 0.8.

Experimental testing at a dc-link voltage of 3500 V is carried out for an active current of 7 A and a reactive current of 5 A, as shown in Fig. 29, to ensure the operation of the MV-AFEC system at that dc-link voltage. The dc voltage of MVPB#1 is kept at 2000 V while keeping the modulation index at 0.8. It should be noted that the emulated grid voltage for MVPB#2 is not a sinusoidal voltage waveform but a switched waveform with a 60-Hz sinusoidal frequency and a peak fundamental phase voltage of 800 V (output pole voltage of MVPB#1). With the successful operation of the MV converter in a back-to-back



(a)



(b)

Fig. 28. Experimental results for the back-to-back testing of voltage control at a dc-link voltage of 3000 V for an active current of 5 A and a reactive current of (a) 0 A and (b) 10 A. (Ch1: Pole voltage ($V_{RY,OL}$); Ch2: MV dc-link voltage (V_{DC}); Ch3: Current through R-phase (I_R); Ch4: Current through Y-phase (I_Y).

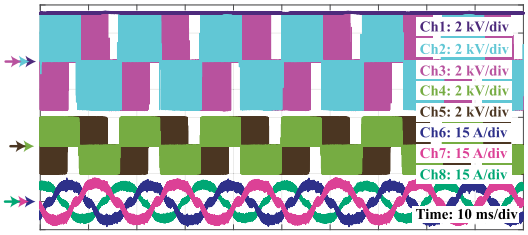
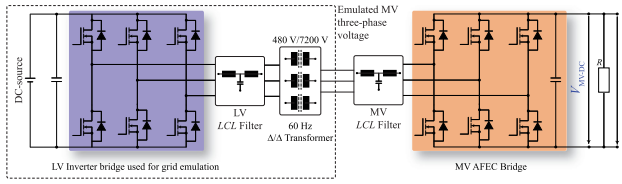


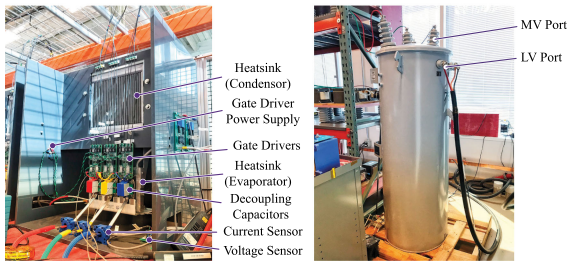
Fig. 29. Experimental results for the back to back testing with voltage control at 3500 V. (Ch1: DC-bus voltage (V_{DC}); Ch2: Closed-loop inverter Y-B line–line voltage ($V_{YB,CL}$); Ch3: Closed-loop inverter ($V_{RY,CL}$); Ch4: Open-loop inverter $V_{YB,OL}$; Ch5: Open-loop inverter $V_{RY,OL}$; Ch6: R-phase current (I_R); Ch7: Y-phase current (I_Y); Ch8: B-phase current (I_B).)

system, testing is carried out to ensure the operation of MVPB#2 with a sinusoidal three-phase input at the ac port. An LV inverter, along with a 60-Hz step-up transformer (480 V/7200 V), is used to generate the required three-phase ac voltage, as shown in Fig. 30. Tests are conducted to validate the operation in this scenario for various dc-link voltages, as shown in Fig. 31. The frequency spectrum of the inverter current and the grid current is measured for Fig. 31(b) and is shown in Fig. 31(c). The total harmonic distortion (THD) of the inverter current is measured according to the IEEE 519-2014 standard [44] and is 2.75%.

The operation of the MV converter system is further validated by loading the system using a resistive load. A resistive load of 490 Ω is connected across the dc link to achieve a power transfer of 25 kW. Fig. 32 shows the operation of the MV converter system at different values of voltage and power levels. It is seen that the currents are almost sinusoidal in nature. The frequency spectrum of the inverter current and the grid current is measured for Fig. 32(b) and is shown in Fig. 33. The THD of the inverter current and the grid current is 2.67% and 2.31%, respectively.

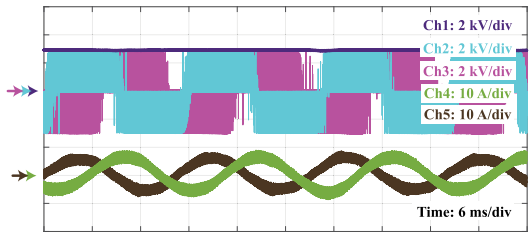


(a)

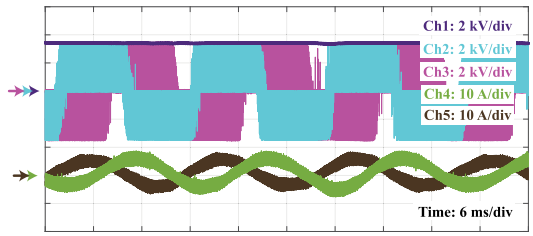


(b) (c)

Fig. 30. (a) Emulated grid-connected operation of the MV-AFEC system. Photograph of (b) the LV inverter used for grid emulation and (c) 60-Hz step-up transformer with a 1:15 turns ratio.



(a)



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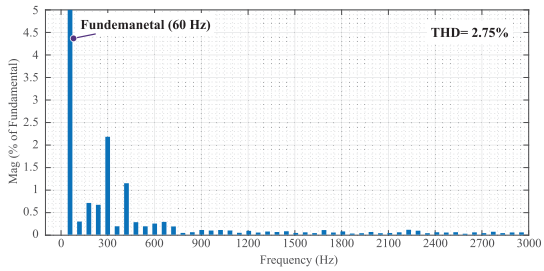
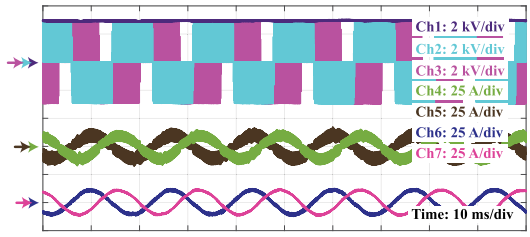
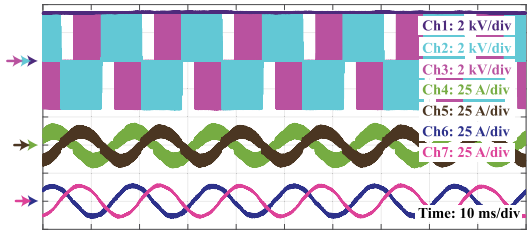


(c)

Fig. 31. Experimental results for the MV-AFEC testing at (a) 3000 V and (b) 3500 V dc link with an active current of 5 A and a reactive current injection of 3 A. (Ch1: DC-link voltage (V_{DC}); Ch2: Pole voltage ($V_{RY,CL}$); Ch3: Pole voltage ($V_{YB,CL}$); Ch4: Inverter current through R-phase ($I_{R,INV}$); Ch5: Inverter current through Y-phase ($I_{Y,INV}$).) (c) Frequency spectrum of the inverter current of Fig. 31(b) for a frequency range up to 3 kHz (RMS of fundamental frequency: 7.3 A).

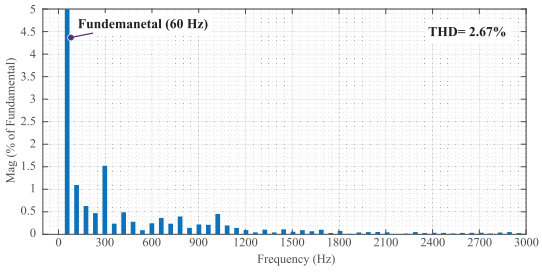


(a)

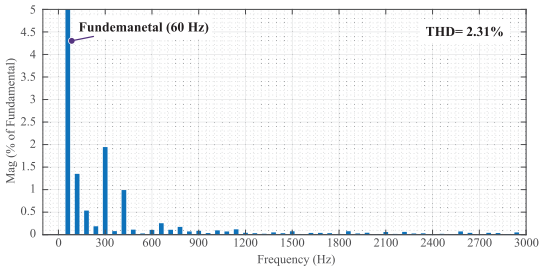


(b)

Fig. 32. Experimental results for the MV-AFEC system with active loading at (a) 3000 V and (b) 3500 V. A resistive load of 490 Ω is connected at the dc link, and thus, an active power of 18.5 and 25 kW, respectively, is transferred. (Ch1: DC-link voltage (V_{DC}); Ch2: Pole voltage ($V_{RY,CL}$); Ch3: Pole voltage ($V_{YB,CL}$); Ch4: Inverter current through R-phase ($I_{R,INV}$); Ch5: Inverter current through Y-phase ($I_{Y,INV}$); Ch6: Grid current through R-phase ($I_{R,GRID}$); Ch7: Grid current through Y-phase ($I_{Y,GRID}$).)



(a)

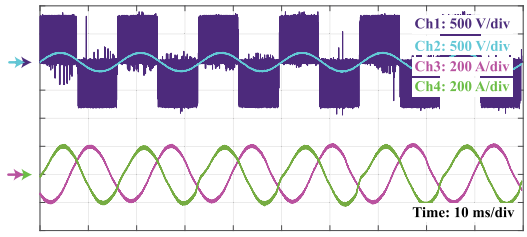


(b)

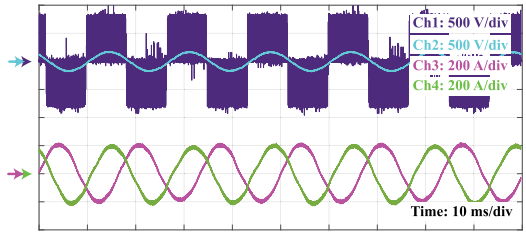
Fig. 33. (a) Frequency spectrum of the inverter current for a frequency range up to 3 kHz (RMS of fundamental frequency: 13.48 A). (b) Frequency spectrum of the grid current for a frequency range up to 3 kHz (RMS of fundamental frequency: 12.64 A).

The THD is well within the IEEE limits of 5% THD and 3% THD component for individual harmonics. Fig. 34 gives the voltage and current waveforms for the LV inverter system used for grid emulation.

With successful operation of the 10-kV SiC MOSFETs at a voltage level of 3500 V, experimental results demonstrating

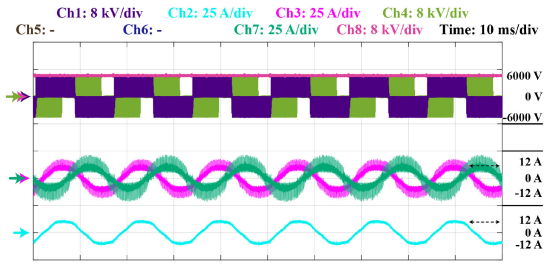


(a)

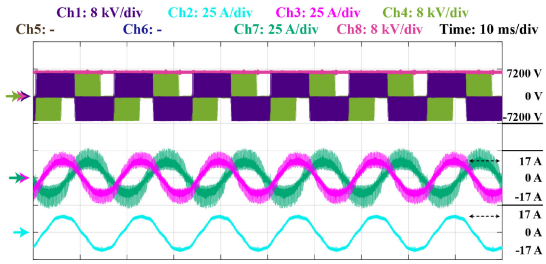


(b)

Fig. 34. Experimental results for the LV grid emulator driving the MV-AFEC system with active loading at (a) 3000 V and (b) 3500 V. An active power of 18.5 and 25 kW, respectively, is transferred in the two cases. (Ch1: Pole voltage across R-phase and Y-phase; Ch2: Voltage across filter capacitor of the LCL filter; Ch3: Current through LV R-phase; Ch4: Current through LV Y-phase.)



(a)



(b)

Fig. 35. Experimental results showing the operation of the MV-AFEC system at a dc-link voltage of (a) 6 kV and (b) 7.2 kV. (Ch1/Ch4: MV pole voltage ($v_{RY\text{-}MV}/v_{YB\text{-}MV}$); Ch2: Grid current through R-phase; Ch3/Ch7: Inverter current through MV R/Y-phase; Ch8: MV DC-link voltage ($v_{dc\text{-}MV}$).)

the operation of the MV-AFEC at higher voltage levels are demonstrated. Fig. 35 shows the operation of the MV-AFEC at a dc-link voltage of 6 and 7.2 kV and a peak current of 12 and 17 A, respectively. Fig. 36 shows the thermal measurement result during continuous operation of the MV-AFEC system after 30 min of operation. Since the MV converter system is aimed at an SST application, the final validation of the operation of the converter, including the controller, is carried out by using an

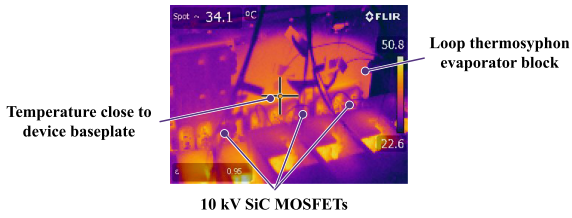


Fig. 36. Thermal measurement result during continuous operation of the MV-AFEC system after 30 min of operation.

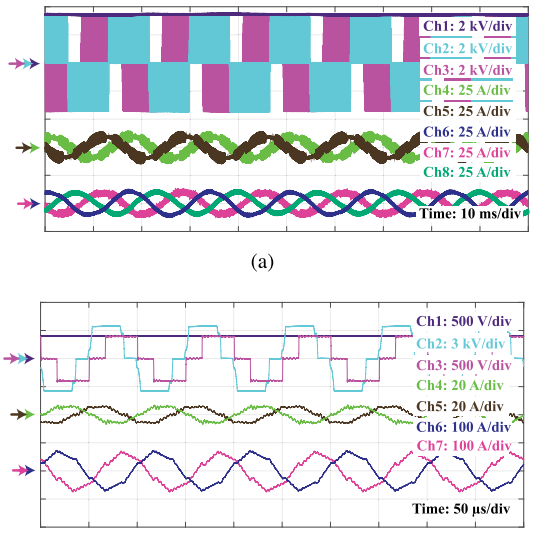


Fig. 37. Experimental results showing the cascaded operation of the MV-AFEC system with the DAB converter system (a) MV-AFEC. (Ch1: MV dc-link voltage ($v_{\text{dc-MV}}$); Ch2/Ch3: MV pole voltage ($v_{\text{RY-MV}}/v_{\text{YB-MV}}$); Ch4/Ch5: Inverter current through MV R/Y-phase; Ch6/Ch7/Ch8: Grid current through MV R/Y/B-phase), and (b) DAB system (Ch1: LV dc-link voltage ($v_{\text{dc-LV}}$); Ch2: MV pole voltage ($v_{\text{RY-MV}}$); Ch3: LV pole voltage ($v_{\text{RY-LV}}$); Ch4/Ch5: Current through MV R/Y-phase; Ch6/Ch7: Current through LV R/Y-phase.)

active load (i.e., the DAB converter). Since the DAB forms an active load, the stability of the system is affected differently as compared to the previous cases. A stability analysis is carried out to ensure proper operation of the MV-AFEC system for an SST application and is shown in Appendix B. Experimental results showing the operation of the MV-AFEC system in cascade with the dc–dc stage (DAB converter system) are shown in Fig. 37. Operation of the DAB converter at a dc-link voltage of 7.2 kV is also demonstrated in Fig. 38 validating the design and development of the MV power converter system. The entire system is successfully operated and demonstrated in a mobile container, installed at the naval base at Port Hueneme, CA, USA, as shown in Fig. 39. The results demonstrate the successful continuous operation of the system in the laboratory as well as the mobile container.

VII. Efficiency Analysis of the MVPB

An efficiency estimation and measurement of the MVPB is carried out. With the data obtained from the static and dynamic characterization, device loss models are developed in PLECS

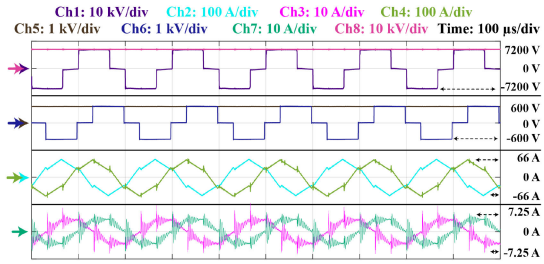


Fig. 38. Experimental results demonstrating the operation of the DAB system of the MUSE-SST at a dc-link voltage of 7.2 kV and an active power transfer of 30 kW. (Ch1/Ch6: MV/LV pole voltage ($v_{\text{RY-MV}}/v_{\text{RY-LV}}$); Ch2/Ch4: Current through the LV R/Y-phase; Ch3/Ch8: Current through the MV R/Y-phase; Ch5/Ch7: LV/MV dc-link voltage ($v_{\text{dc-LV}}/v_{\text{dc-MV}}$).)

Fig. 39. Photograph of the entire SST system in a mobile container (a) outside the mobile container and (b) inside the mobile container.

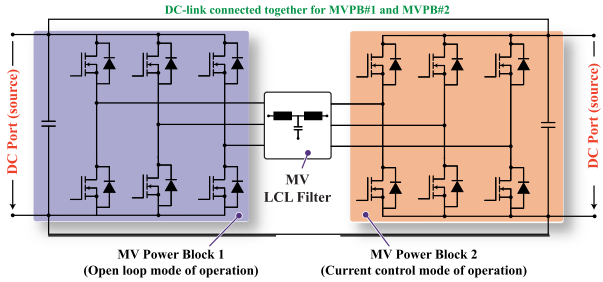


Fig. 40. Schematic of a back-to-back three-phase inverter test setup for estimating the efficiency of the power blocks. The dc links of both the power blocks are shorted and the ac link is connected via MV inductors.

to estimate the efficiency of the power block. This is verified experimentally using the back-to-back test, similar to [45], with the dc link of the individual power blocks connected together, and the ac link connected via a three-phase inductor, as shown in Fig. 40. In the back-to-back test, one power block (MVPB#1) regulates the ac-link voltage with a certain modulation index, and the other power block (MVPB#2) controls the power circulating between them. The input dc power supply only provides the system losses, and thus, the efficiency of the power blocks can be estimated at different operating conditions. Fig. 41 shows the simulated and measured efficiency of the MVPB for various values of power transferred. Fig. 42 shows the breakdown of the switching and conduction losses for each of the cases at a transferred power of 2500 W and 35 kW. It is observed that the majority of losses are observed as switching losses, and only a small fraction of the total power loss is due to the conduction loss.

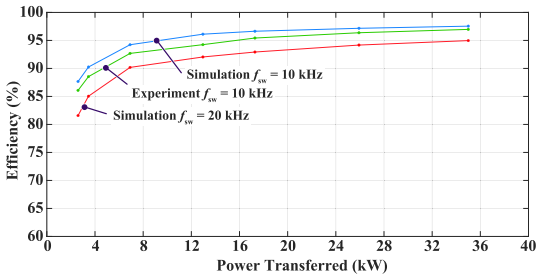


Fig. 41. Measured and simulated efficiency of the MVPB at a dc-link voltage of 7200 V.

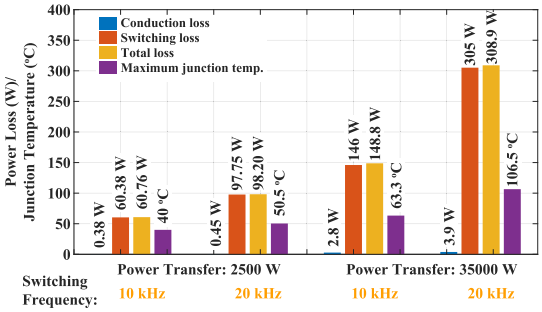


Fig. 42. Measured loss breakdown of a single device in the MVPB for different operating frequency and power transfer.

This is expected since the switching energy losses of the 10-kV SiC MOSFETs in the order of tens of millijoules (20–100 mJ). However, the percentage of conduction losses increases with the increase in power transferred across the converter due to the increase in current through the devices. It should also be noted that the total losses, and consequently, the efficiency, decrease by a significant amount for a switching frequency of 20 kHz. Peak efficiency of 95.5% at a power transfer of 35 kW is seen based on the measurements. It can be seen that the experimental efficiencies are slightly lower than the once obtained via simulations. This is attributed to the fact that the losses in the inductor are not considered in the simulation results. The additional losses in the inductor decrease the experimental efficiencies.

VIII. Conclusion

This article demonstrates the continuous operation of Gen3 10-kV SiC MOSFET modules in a three-phase AFEC system at a dc-link voltage of 7.2 kV for the first time in the literature. The design challenges associated with the successful operation of these 10-kV SiC devices are also discussed in detail. It is identified that the reduction in the CM current through the gate drivers and in the DM current through the filter inductors proves to be the most critical design challenge for operating the 10-kV SiC MOSFET modules continuously and reliably. These major issues are attributed directly to the high dv/dt of the 10-kV SiC MOSFETs and are not typically present in LV systems. Solutions to mitigate the effect of dv/dt on the operation of the converter system are proposed. A compact thermal solution based on a loop thermosyphon solution is presented, taking into account its scalability for higher power designs. Based on measured losses, the thermal management can provide a solution for up to 500 kVA system with the same footprint and by just changing the condenser. A test methodology and experimental results of the 10-kV SiC MOSFET modules are provided, which validates the reliable operation of these 10-kV SiC devices and the correctness of the design considerations. Operation of the AFEC in cascade with the DAB system is also shown, which demonstrates the validity of the development of the MVPB. The efficiency of the designed MVPB is also measured, and a peak efficiency of 95.5% is seen. The design considerations and consequent experimental testing are aimed at serving a standardized procedure for designing and implementing MV converter systems. It is envisaged that the successful operation of these MV SiC devices would pave the way for their deployment in real-field operation, as demonstrated by the operation at the naval base at Port Hueneme, CA, USA.

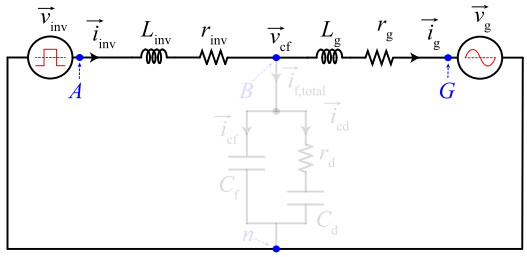


Fig. 43. Schematic representation of the per-phase equivalent circuit showing a simplified model of the LCL filter, which is essentially an L filter.

Appendix A
Converter Transfer Functions

Since the considered system is a balanced three-phase system, a per-phase equivalent circuit is sufficient to model the system. The filter capacitors in the LCL filter are designed to carry 5% of the rated current, and hence, the current through the capacitor, $i_{\text{f, total}}$ is very low compared to the grid current. The system can, thus, be simplified to a circuit, as shown in Fig. 43. For simplification, the following relations are defined:

$$\vec{i}_{\text{inv}} = \vec{i}_{\text{g}} \tag{5}$$

$$L = L_{\text{inv}} + L_{\text{g}} \tag{6}$$

$$r = r_{\text{inv}} + r_{\text{g}}. \tag{7}$$

Applying Kirchhoff's voltage law in Fig. 43, and transforming into the grid voltage vector rotating reference frame, we obtain

$$\vec{v}_{\text{inv,}}dq = r\vec{i}_{\text{g,}}dq + L\frac{d\vec{i}_{\text{g,}}dq}{dt} + \omega_{\text{g}}L\vec{i}_{\text{g,}}qd + \vec{v}_{\text{g,}}dq \tag{8}$$

where ω_{g} represents the grid frequency. Equation (8) can be transformed into the Laplace domain and represented in block diagrams for both the d-axis and q-axis, as shown in Fig. 44. Fig. 44 represents the dynamic relationship between the inverter voltage, $v_{\text{inv,dq}}$, and the grid current, $i_{\text{inv,dq}}$.

For the dc voltage dynamics, assuming that the inverter and the LCL filter have zero power losses, the dc current i_{dc} can be

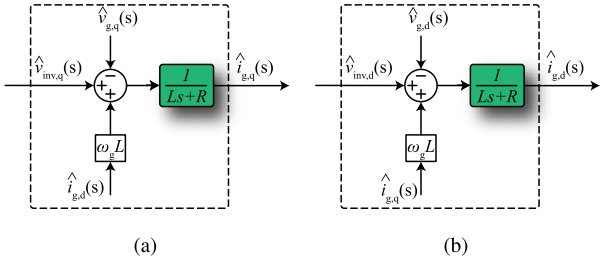


Fig. 44. (a) q-axis and (b) d-axis representation of the simplified model of the LCL filter.

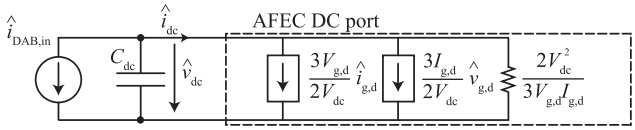


Fig. 45. Small-signal model of the dc port.

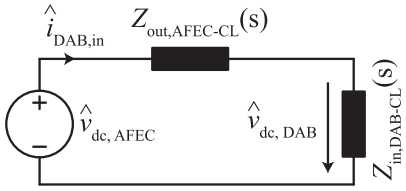


Fig. 46. Simplified representation of the MV dc-link port showing the closed-loop output impedance of the AFEC and the closed-loop input impedance of the DAB system.

derived by analyzing the power balance equation presented in (9). Furthermore, as the converter system is balanced and three phase in nature, the instantaneous ac power is constant

$$i_{\mathrm{dc}}(t) = f(v_{\mathrm{g,}d}(t), i_{\mathrm{g,}d}(t), v_{\mathrm{dc}}(t)) = \frac{3v_{\mathrm{g,}d}(t)i_{\mathrm{g,}d}(t)}{2v_{\mathrm{dc}}(t)}. \quad (9)$$

The AFEC dc port small-signal model can be obtained by perturbing and linearizing (9) around any operating point; the following relations can be derived:

$$I_{\mathrm{dc}} = \frac{3V_{\mathrm{g,}d}I_{\mathrm{g,}d}}{2V_{\mathrm{dc}}} \quad (10)$$

$$\hat{i}_{\mathrm{dc}}(t) = \frac{3I_{\mathrm{g,}d}}{2V_{\mathrm{dc}}}\hat{v}_{\mathrm{g,}d} + \frac{3V_{\mathrm{g,}d}}{2V_{\mathrm{dc}}}\hat{i}_{\mathrm{g,}d} + \frac{3V_{\mathrm{g,}d}I_{\mathrm{g,}d}}{2V_{\mathrm{dc}}^2}\hat{v}_{\mathrm{dc}} \quad (11)$$

where X and $\hat{x}$ give the operating point and perturbation of the parameter, respectively. The small-signal representation of the dc port of an unterminated AFEC system is shown in Fig. 45. From Fig. 45, the relation between the d-axis grid current, $\hat{i}_{\mathrm{gd}}$, and $\hat{v}_{\mathrm{dc}}$ can be derived as

$$\frac{\hat{v}_{\mathrm{dc}}}{\hat{i}_{\mathrm{gd}}} = -\frac{3V_{\mathrm{gd}}}{2V_{\mathrm{dc}}} \times \frac{2\,V_{\mathrm{dc}}^2}{2\,V_{\mathrm{dc}}^2 C_{\mathrm{dc}}s + 3V_{\mathrm{gd}}I_{\mathrm{gd}}}. \quad (12)$$

From the ac current dynamics and the dc voltage dynamics, the complete controller system can be designed. Furthermore, the effect of discretization is taken into account while designing

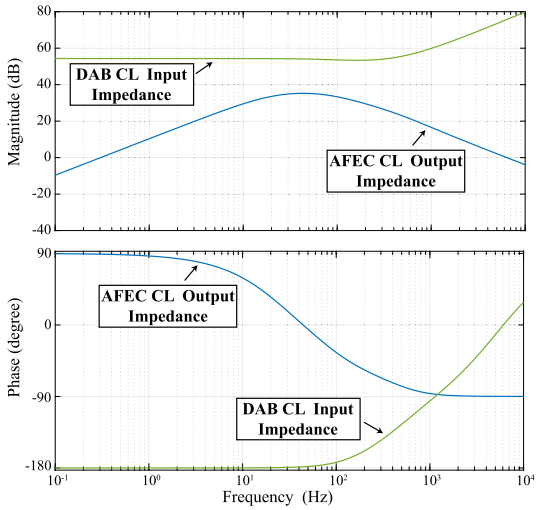


Fig. 47. Closed-loop output and input impedances of the AFEC and the DAB, respectively.

the controller. A zero-order-hold transfer function is incorporated in the feedback path to emulate the effect of the discretization of the digital controller

$$\mathrm{Delay}_{\mathrm{ZOH}} = \frac{1}{1 + \frac{s}{f_{\mathrm{sw}}}}. \quad (13)$$

In addition to the inherent delay caused by the discretization, the sensor delay, t_{del}, should also be taken into account and can be represented as

$$\mathrm{Delay}_{\mathrm{del}} = \frac{1}{1 + st_{\mathrm{del}}}. \quad (14)$$

In addition to these delays, the transfer function of the inverter is also taken into account, which can be represented by the following first-order transfer function:

$$\mathrm{Delay}_{\mathrm{INVERTER}} = \frac{1}{1 + \frac{s}{2f_{\mathrm{sw}}}}. \quad (15)$$

This delay is present inherently and arises from the delay between the inverter reference voltage (v^*) and the actual output voltage of the inverter system. Fig. 24 shows the entire control system, including all the delays. For the controller design, it is observed that the effect of the sensor delays is negligible for the frequency range under consideration. However, the effect of the discretization delay and the PWM delay has been taken into consideration while designing the control system. The bode plots for the system are shown in Figs. 25 and 26, where a phase margin of 80° and 85° shows the stability of the system.

Appendix B
Stability of the Converter System With an Active Load

The MV-AFEC, when interconnected with an active load, DAB, with a common dc link, can be represented, as shown in Fig. 46. The cascaded system stability can be determined by analyzing these closed-loop impedances. From Fig. 46, the dc

voltage seen by the DAB $\hat{v}_{\text{dc,DAB}}$ can be determined as

$$\hat{v}_{\text{dc,DAB}} = \hat{v}_{\text{dc,AFEC}} \frac{Z_{\text{in,DAB-CL}}(\text{s})}{Z_{\text{out,AFEC-CL}}(\text{s}) + Z_{\text{in,DAB-CL}}(\text{s})} = \hat{v}_{\text{dc,AFEC}} \frac{1}{1 + Z_{\text{out,AFEC-CL}}(\text{s})/Z_{\text{in,DAB-CL}}(\text{s})} \quad (16)$$

where $\hat{v}_{\text{dc,AFEC}}$ is the unterminated output dc voltage of the AFEC system. Thus, for $\hat{v}_{\text{dc,DAB}}$ to be stable and equal to $\hat{v}_{\text{dc,AFEC}}$, the following condition needs to be met:

$$\|Z_{\text{out,AFEC-CL}}(\text{s})\| \ll \|Z_{\text{in,DAB-CL}}(s)\|. \quad (17)$$

This is a sufficient condition for the DAB converter stage to be decoupled from the AFEC system [46]. Fig. 47 shows the closed-loop input impedance of the DAB converter and the closed-loop output impedance of the MV-AFEC. A detailed study of the stability analysis of the MV converter system with an active load is carried out in [35].

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