A Multi-Load Capacitive Power Transfer System With Load-Independent Characteristic for Reefer Container Application

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***Abstract*—In order to supply power wirelessly to reefer containers without constructing an extra power tower, this article proposed a novel multiload capacitive power transfer (CPT) system with an SP-CL isolation compensation topology. Unlike the traditional multiload CPT system, where receivers function solely as power consumers, in the proposed system, each receiver not only supplies power to the connected load but transfers power wirelessly to the next receivers. The coupler model with the cross-coupling of metal containers is established for reefer container application. Then, the SP-CL isolation compensation topology analysis based on the single circuit is carried out to achieve the load-independent characteristics with constant output voltage. The output characteristics and efficiency of the proposed CPT system are analyzed, considering the impact of the parasitic resistance. Besides, the voltage stress of passive components is optimized to design the experiment system. A 1.8-kW prototype with three loads is built to validate the effectiveness of the proposed CPT system. The equal power distribution (600 W and 600 W and 600 W) is achieved, and the system efficiency can reach 83.7%.**

***Index Terms*—Capacitive power transfer (CPT), load-independent, multiload, reefer container.**

I. Introduction

REEFER containers play an essential role in the cold-chain transportation industry. Nowadays, the reefer containers are powered by plug-in/out-based power supply systems, as shown in Fig. 1(a), which suffer three main drawbacks. First, the physical plug-in connection is labor-intensive and time-consuming, and undesirable unplugging occurs when containers are moved, leading to equipment damage. Second, such systems are unsuitable for extreme weather conditions, such as rain and snow, etc. Third, power towers are required to establish plug-in/out-based power supply systems, increasing land and construction costs.

Wireless power transfer (WPT) technology as an emerging power supply method without a direct electrical connection is a potential solution to alleviate the above drawbacks [1]–[5]. Inductive power transfer (IPT) and capacitive power transfer (CPT) are the two mainstream approaches in WPT technology [6], [7], wherein IPT utilizing the alternating magnetic fields to transfer power have been applied for reefer containers charging application in [8]. Whereas the containers are mainly made of aluminum alloy or other metal materials, the alternating magnetic fields generated in the IPT system will inevitably cause large eddy current losses in the metal environment, leading to significant system performance degradation [9]. Hence, using electric fields to transfer power instead of magnetic fields, CPT technology with low eddy current loss is a better solution for reefer container charging.

CPT technology is becoming a research hotspot in the WPT field with the advantages of low costs, lightweight, and low eddy current losses in metal surroundings [10]–[16]. Most studies concentrate on single-input and single-output (SISO) CPT systems [17]–[24]. Lu *et al.* proposed the single input and single output CPT system with the compensation topology of double-side *LCLC, LCL*, and *LC* compensation topologies to realize the constant voltage or constant current output. Nevertheless, to power multiple loads in reefer container application, a power tower is required to install the SISO system, leading to extra costs of lands and constructions for the power tower. As consideration of economy, the SISO CPT system is not a commendable scheme and the single-input and multiple-output (SIMO) CPT systems [25]–[27] may be a potential solution in reefer container application. There are a few research works on SIMO CPT systems. Su *et al.* proposed a mixed-resonant topology for multiple pickups. The transmitter is an array of aluminum subplates insulating with each other. Each receiver consists of two plates placed horizontally on the transmitter [25]. In [26], a multiload CPT system was proposed for low-power battery charging applications. The transmitter consisting of a pair of conductive plates transfers power to several pairs of

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receiver plates. However, as the receiver side of those CPT systems functions solely as power consumers, a bulky transmitter is needed to power multiple receivers, which is unsuitable for applying in stacked placed reefer containers with high land costs.

In this article, a novel multiload CPT system with SP-CL compensation topology is proposed to power the multiple reefer containers simultaneously, as shown in Fig. 1(b). The coupler plates are installed between each adjacent container, each container receives power from the previous container and transfers energy to the next container, hence the energy can be transferred through the ground to the top container. There are three innovative contributions in this article.

First, the coupler structure considering the cross-coupling with metal containers are simplified into the T-type and Π-type model. Different from the traditional four-plates or six-plates, the proposed coupler can be regarded as five-plates. To eliminate the undesirable loop current through multiple couplers. The electrical isolation circuit is introduced and the contrastive analysis of the proposed CPT system with and without isolation is expressed particularly in this article.

Second, the circuit analysis of the proposed multiload CPT system based on the single circuit is carried out to achieve load-independent output voltage property. Then, the impact of the parasitic resistance and the variation of system parameters is analyzed, which reveals that the mutual inductance and the equivalent coupling capacitance are significant in system parameters design.

Third, the system parameter design methodology based on voltage optimization is proposed, and an experimental prototype with three loads is implemented to verify the theoretical analysis. The experimental results of output characteristics agree with the set value, and the disconnection of the latter load would not affect the others.

The rest of this article is organized as follows. Section II presents the analysis based on a single circuit. Section III analyzes the impact of parasitic resistance and Section IV provides the system parameters design method based on voltage stress optimization. Section V validates the proposed system by experiment. Finally, Section VI concludes this article.

II. Proposed Topology

A. System Structure

As shown in Fig. 2, the proposed CPT system mainly consists of a dc voltage source, an inverter, a transmitter TX_0, multiple repeaters RT_1, RT_2, …, RT_N (N is the total number of the loads in the CPT system) serving as receivers as well. TX_0 consists of primary coupler plates and an isolation compensation topology formed by two loosely coupled inductors L_{P1}, L_1 with a mutual inductance M_1 and two compensated capacitors C_{P1}, C_1. Each RT_i ($1 \le i \le N$) contains secondary coupler plates, a rectifier, a load R_{Li}, and an SP-CL compensation topology consisting of three compensated inductor $L_{P(i+1)}$, L_{i+1}, L_{Si}, and three compensated capacitors $C_{P(i+1)}$, C_{i+1}, $C_{\mathrm{S}i}$. For container application, TX_0 is installed on the ground, RT_i ($1 \le i \le N$) is located on the ith container. Four metal plates provide a power flow loop between each adjacent container. The receiver container is powered by the previous container and transfers the power to the next adjacent container simultaneously, creating a power flow loop from TX_0 to RT_N. As the reefer containers are contacted, an undesirable energy flow may occur through the containers, leading to an unnecessary power loss. Therefore, to eliminate the impact of extra energy flow, two loosely coupled inductors L_i and L_{Pi} are introduced as electric isolation shown in Fig. 2, which are analyzed specifically in Section II-C.

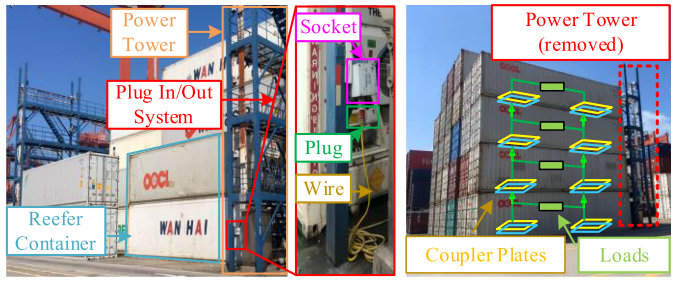


Fig. 1. (a) Reefer containers and power tower. (b) Installation of the proposed CPT system.

B. Coupler Structure

To transfer power wirelessly from the previous container to the next container, a four-plate coupler structure is placed in the gap between the containers shown in Fig. 3. As the adjacent containers are stacked on each other, two contacted aluminum plates P_5, P_6 represent the bottom of the upper container and the top of the container below. Four aluminum plates P_1, P_2, P_3, P_4 represent the coupler structure. Every two plates can form a coupling capacitor, and an equivalent circuit of the capacitive coupling structure is illustrated in Fig. 4(a).

For the application scenarios of reefer containers, a few misalignments in containers are likely to cause container collapse. Hence there is almost no misalignment between each container. Furthermore, the coupler structure in Fig. 3 is designed to be symmetrical, and the equivalent circuit in Fig. 4(a) can also be regarded as symmetric. So, there is no difference in potential between P_5 and P_6, which means there is no current through P_5 and P_6 in ideal conditions. In addition, if there is a single system ground point in the proposed system, the current earth I_x is zero. Obviously, P_5 or P_6 is the only ground point for one load application, and the full-capacitor model in Fig. 4(a) can be simplified to the Π-type circuit as shown in Fig. 4(d) through the simplification process of Fig. 4(b) and (c), where C_M, C_{e1}, C_{e2} can be expressed as

$$\begin{cases} C_M = \frac{C_{13}C_{24}-C_{14}C_{23}}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_{e1} = C_{12} + \frac{(C_{15}+C_{16})(C_{25}+C_{26})}{C_{15}+C_{16}+C_{25}+C_{26}} \\ \qquad\quad + \frac{(C_{13}+C_{14})(C_{23}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} - C_M \\ C_{e2} = C_{34} + \frac{(C_{35}+C_{36})(C_{45}+C_{46})}{C_{35}+C_{36}+C_{45}+C_{46}} \\ \qquad\quad + \frac{(C_{13}+C_{23})(C_{14}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} - C_M. \end{cases} \tag{1}$$

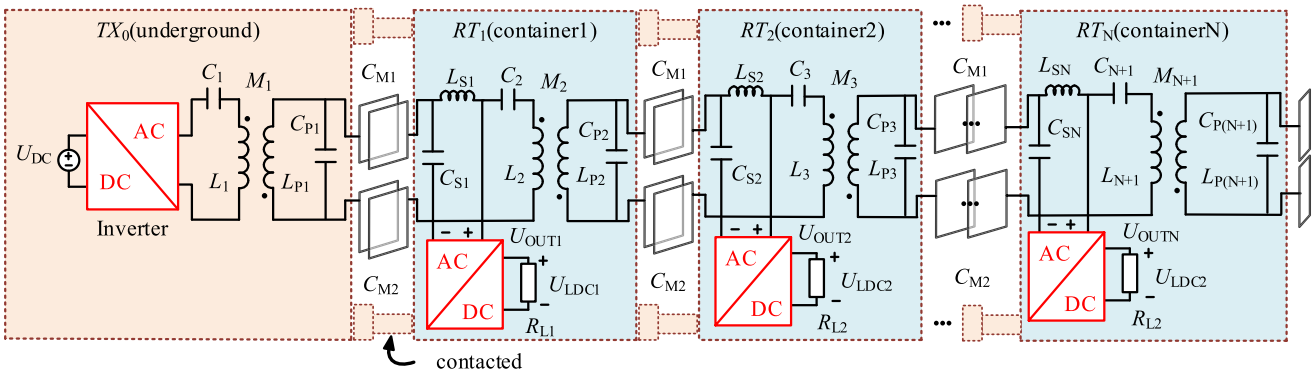


Fig. 2. SP-CL compensation topology in the proposed CPT system for reefer containers.

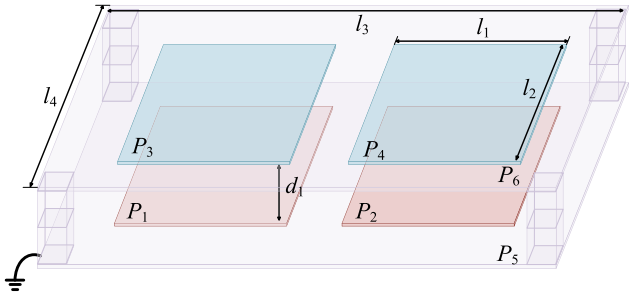


Fig. 3. Structure of the coupler plates in reefer container.

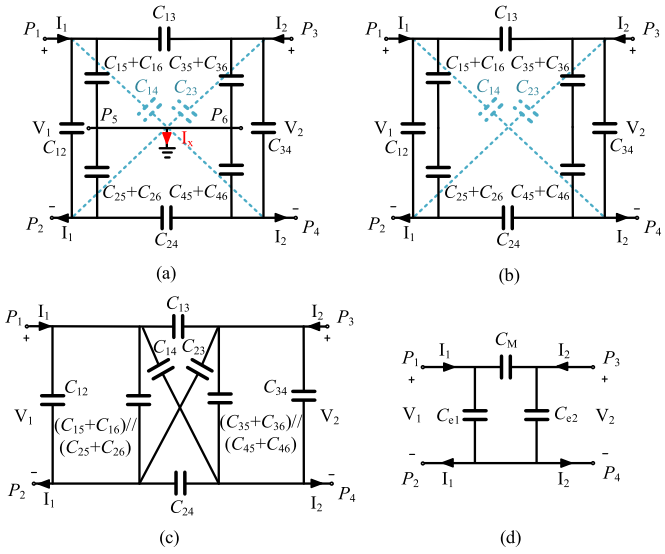


Fig. 4. Simplification process of capacitor model. (a) Full-capacitor model. (b) Simplified model without grounding points. (c) Combine parallel capacitors. (d) Π-type equivalent circuit.

C. Isolation Structure

In practical application, due to parasitic resistance, there is inevitably a difference in potential between P_{5i} and P_{6i}. Fig. 5 illustrates the schematic diagram of the CPT system without isolation for multiple containers (only container N, container (N-1), and container 1 are presented for simplicity). P_{5i} and P_{6i} represent the top and bottom of the RT_i ($1 \le i \le N$). Containers made of metal materials can be regarded as electric conductors with low resistance R_{xi}. The current through P_{5i} and P_{6i} expressed as I_{xi} ($1 \le i \le N$) can be calculated as follows:

$$I_{Xi} = \frac{|\varphi_{5\_i} - \varphi_{6\_i}|}{R_{xi}}. \tag{2}$$

It can be seen that with low resistance R_{xi} and potential difference between P_{5i} and P_{6i}, a large undesirable current may occur through the container, leading to undesirable energy dissipation affecting output characteristics.

The simulation model with three loads of the CPT system in Fig. 5 was built under the MATLAB/Simulink, where the compensation topology without isolation replaced equivalently the two loosely coupled inductors L_{Pi}, L_i in Fig. 2 with LCL circuit. The simulation model adopted the parameters given in Tables I and II, and the output voltage gains are set to 1. Fig. 7(a) shows the output ac voltages of the rectifier. It can be seen that without isolation, the output voltage of R_{L1}, R_{L2}, and R_{L3} shown

TABLE I
PARAMETERS FOR THEORETICAL ANALYSIS

Symbol	Value	Symbol	Value	Symbol	Value
f	500kHz	U_{Li}, U_{IN}	300V	R_{Li}	150Ω
C_M	31.2pF	C_{e1}	20.4pF	C_{e2}	20.9pF

TABLE II
COMPENSATION PARAMETERS OF EXPERIMENTAL SETUP

Symbol	Value	Symbol	Value	Symbol	Value
C_1	3.85nF	C_2	2.56nF	C_3	2.41nF
C_{P1}	347pF	C_{P2}	324pF	C_{P3}	307pF
C_{S1}	347pF	C_{S2}	324pF	C_{S3}	307pF
L_1	28.3μH	L_2	39.5μH	L_3	42.1μH
L_{P1}	256μH	L_{P2}	271μH	L_{P3}	285μH
L_{S1}	256μH	L_{S2}	271μH	L_{S3}	285μH
M_1	20.1μH	M_2	22.6μH	M_3	24.7μH

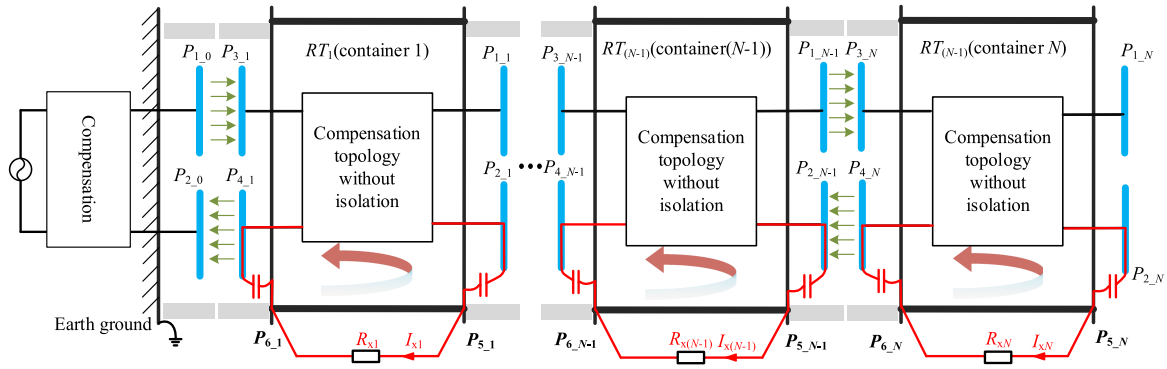


Fig. 5. Schematic diagram of CPT system without isolation compensation topology.

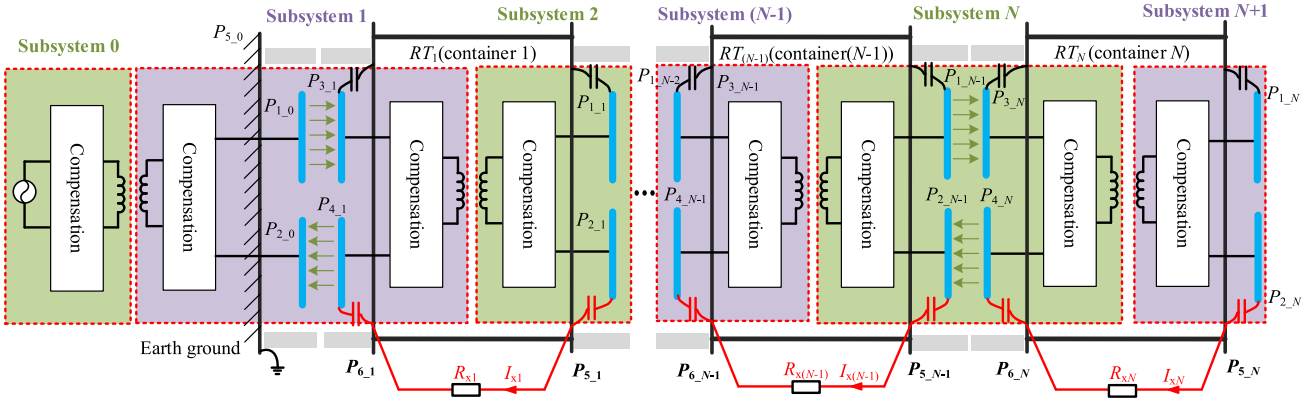


Fig. 6. Schematic diagram of CPT system with isolation compensation topology.

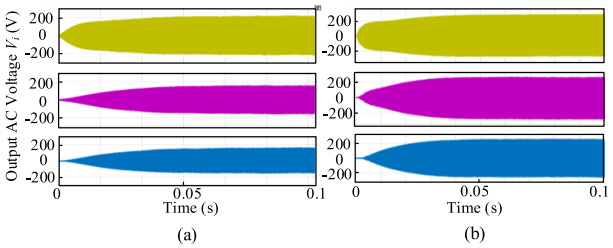


Fig. 7. Simulated waveforms of ac output voltage. (a) Without isolation. (b) With isolation.

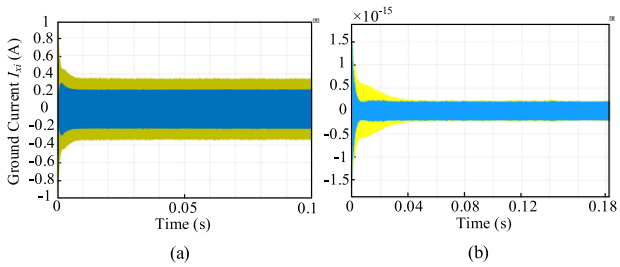


Fig. 8. Simulated waveforms of branch current I_x. (a) Without isolation. (b) With isolation.

in Fig. 7(a) has dropped almost half compared to Fig. 7(b), which is due to the existence of the extra current path between containers. Fig. 8(a) shows the simulated waveforms of current I_{xi}, which can be seen that the current I_{xi} has reached 0.6 A in the system without isolation. When utilizing the compensation topology with isolation shown in Fig. 8(b), the current pass through each container is almost zero.

To eliminate the impact of the extra current path, the isolation circuit with two loosely coupled inductors L_{Pi}, L_i is introduced in compensation topology shown in Fig. 6. The same as the circuit in Fig. 5, there is the current path between P_{5_i} and P_{6_i}. However, by inducing the isolation structure, the multiloads CPT system can be divided into multiple subsystems, which are marked in green and purple boxes. The adjacent subsystems are connected by the branch of I_{xi} ($1 \le i \le N$). For subsystem (N+1), it is connected to subsystem N only through the branch of I_{xN}. According to Kirchhoff's law, the current I_{xN} is zero. Similarly, for subsystem N, the branch current connected to other subsystems satisfy the expression as follows:

$$I_{x(N-1)} + I_{xN} = 0. \tag{3}$$

Since I_{xN} is zero, $I_{x(N\text{-}1)}$ is also equal to zero. A similar derivation can be applied to subsystem i, and it can be concluded I_{xi} ($1 \le i \le N$) is equal to zero either. That means, with isolation compensation, each subsystem is independent of the other. The

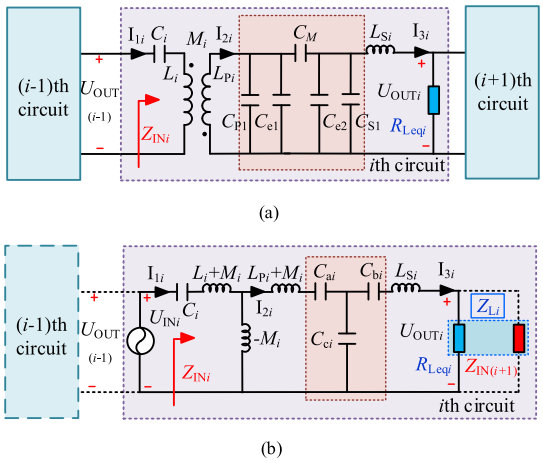


Fig. 9. Simplified circuit model of the *i*th load.

simulated results of isolation models are illustrated in Figs. 7(b) and 8(b). The output voltage gains are set to 1. From the Ac output voltage curves shown in Fig. 7(b), it can be seen that the output voltage gains of the three loads are almost the same and equal to the set value.

Therefore, the isolation structure functions as the electrical isolation to eliminate the undesirable loop current between the coupler, avoiding the reduction of the system output performance. On the other hand, the isolation structure as a part of compensation topology plays a critical role in system parameters design and output characteristics control, which will be discussed in the following section.

D. Working Principle

The misalignment of coupler plates can be neglected for reefer containers, and thus the equivalent circuit of each coupler can be regarded as the same. With the Π-type equivalent coupler circuit, the proposed system can be simplified in Fig. 9(a). Different from the subsystem mentioned in Section II-C, the whole system can be divided into *N* circuits. The proposed CPT system with *N* loads can be analyzed based on the topology of *i*th ($1 \le i \le N$) load shown in Fig. 9(b). The purple box represents the *i*th circuit which includes the *i*th compensation topology, *i*th equivalent resistance combined with *i*th rectifier and *i*th load. $U_{\mathrm{OUT}\,i}$ is the output voltage of the *i*th load. $Z_{\mathrm{IN}\,i}$ is the input impedance of the *i*th circuit. The influence of the parasitic resistances is neglected in this section

$$\begin{cases} C_{ai} = C_M + C_{Pi} + C_{e1} + \frac{C_M(C_{Pi}+C_{e1})}{C_{Si}+C_{e2}} \\ C_{bi} = C_M + C_{Si} + C_{e2} + \frac{C_M(C_{Si}+C_{e2})}{C_{Pi}+C_{e1}} \\ C_{ci} = (C_{Pi} + C_{e1}) + (C_{Si} + C_{e2}) + \frac{(C_{Pi}+C_{e1})(C_{Si}+C_{e2})}{C_M}. \end{cases} \tag{4}$$

The fundamental harmonics approximation method is applied to analyze the proposed CPT system. In Fig. 9(b), $U_{\mathrm{IN}\,i}$ represents the equivalent input voltage source of the *i*th circuit, which is equal to the output voltage of $(i-1)$ th circuit. The output and input voltage of each circuit satisfied the relationships expressed as

$$\begin{cases} U_{INi} = \frac{2\sqrt{2}}{\pi} U_{DC}, i = 1 \\ \dot{U}_{INi} = \dot{U}_{OUT(i-1)}, (2 \le i \le N). \end{cases} \tag{5}$$

The equivalent load impedance of *i*th circuit Z_{Li} can be expressed as

$$\begin{cases} Z_{Li} = R_{Leqi} // Z_{IN(i+1)} \\ R_{Leqi} = \frac{8}{\pi^2} R_{Li} \end{cases} \tag{6}$$

where $R_{Leq\,i}$ is the equivalent ac load resistor of the combination of the rectifier and R_{Li}, and $Z_{\mathrm{IN}(i+1)}$ represents the input impedance of the $(i+1)$th circuit.

The system is designed to be resonant at the operating angular frequency ω_{s}, which satisfied that

$$\omega_s = \frac{1}{L_i C_i} = \frac{1}{L_{Pi}} \left(\frac{1}{C_{ci}} + \frac{1}{C_{ai}} \right) = \frac{1}{L_{Si}} \left(\frac{1}{C_{ci}} + \frac{1}{C_{bi}} \right). \tag{7}$$

According to Kirchhoff's law, the currents of each loop in the *i*th circuit are calculated as shown in

$$\begin{cases} I_{1i} = \frac{U_{\mathrm{IN}i}}{C_{ci}^2 Z_{Li} M_i^2 \omega_s^4} \\ I_{2i} = -j \frac{U_{\mathrm{IN}i}}{M_i \omega_s} \\ I_{3i} = -\frac{U_{\mathrm{IN}i}}{C_{ci} Z_{Li} M_i \omega_s^2} \end{cases} \tag{8}$$

the output voltage in Fig. 9(b) can be expressed as

$$\dot{U}_{OUTi} = -\dot{U}_{INi} \frac{X_{Cci}}{X_{Mi}} = (-1)^i \dot{U}_{IN} \left(\frac{\prod_{k=1}^{i} X_{Cck}}{\prod_{k=0}^{i} X_{Mk}} \right) \tag{9}$$

where $X_{Cck} = 1/(\omega_{\mathrm{s}} C_{ck})$ and $X_{Mk} = \omega_{\mathrm{s}} M_k$.

The output voltage gain $G_{\mathrm{V}\,i}$ of the *i*th circuit is defined as the ratio of the output voltage $U_{\mathrm{OUT}\,i}$ to the output voltage $U_{\mathrm{OUT}(i\text{-}1)}$ expressed as follows:

$$G_{Vi} = \frac{|U_{\mathrm{OUT}i}|}{|U_{\mathrm{OUT}(i-1)}|} = \frac{X_{Cci}}{X_{Mi}}. \tag{10}$$

The input impedance $Z_{\mathrm{IN}\,i}$ is expressed as

$$Z_{\mathrm{IN}i} = \frac{X_{Mi}^2 Z_{Li}^2}{X_{Cci}^2}. \tag{11}$$

From (10), the output voltage is only related to the input voltage and the ratio of X_{Cci} and X_{Mi}, but not to the load resistance $R_{Leq\,i}$. Therefore, the output voltages remain constant regardless of the load variations. The amplitudes of each output voltage are identical when the following condition is satisfied:

$$X_{Cci} = X_{Mi} (i = 0, 1, 2, \ldots, N). \tag{12}$$

III. Impact of Parasitic Resistance

A. Impact of Parasitic Resistances on the Output Voltage

In practical application, due to parasitic resistances, the actual output properties tend to be different from the set value. Fig. 10 illustrates the *i*th circuit with the parasitic resistance of compensation inductors. It should be mentioned that the resistance

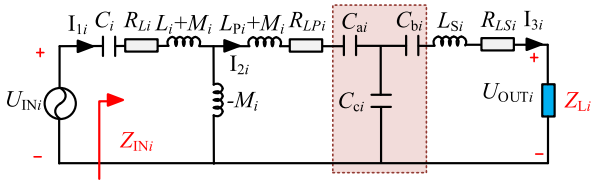


Fig. 10. *i*th circuit with parasitic resistances.

of capacitors and the power loss in the coupler structure is neglected for simplification. Assume that the parasitic resistance of inductors is expressed as R_{Li}, R_{LPi}, R_{LSi}, the definitions of the quality factors and the resistances are expressed as

$$\begin{cases} R_{Li} = \omega L_i / Q_{Li} \\ R_{LPi} = \omega L_{Pi} / Q_{LPi} \\ R_{LSi} = \omega L_{Si} / Q_{LSi}. \end{cases} , 1 \le i \le N \tag{13}$$

According to the above analysis, the loop current in Fig. 10 can be calculated as shown in

$$\begin{cases} I_{1i} = \dfrac{U_{\mathrm{IN}i}\left(1+\frac{R_{LPi}}{X_{Cci}^2} Z'_{Li}\right)}{R_{Li}+\frac{Z'_{Li}}{X_{Cci}^2}(X_{Mi}^2+R_{Li}R_{LPi})} \\ I_{2i} = j\dfrac{U_{\mathrm{IN}i}\frac{X_{Mi}}{X_{Cci}^2} Z'_{Li}}{R_{Li}+\frac{Z'_{Li}}{X_{Cci}^2}(X_{Mi}^2+R_{Li}R_{LPi})} \\ I_{3i} = \dfrac{U_{\mathrm{IN}i}\frac{X_{Mi}}{X_{Cci}}}{R_{Li}+\frac{Z'_{Li}}{X_{Cci}^2}(X_{Mi}^2+R_{Li}R_{LPi})} \end{cases} \tag{14}$$

where $Z'_{Li} = Z_{Li} + R_{LSi}$, the expression of Z_{Li} is given in (6). Similarly, the expression of the output voltage $U_{\mathrm{OUT}i}$ is expressed in (15), and the input impedance of *i*th circuit $Z_{\mathrm{IN}i}$ is expressed in (16). From (16), it could be concluded that the input impedances of *i*th circuit are resistive, which means the zero-phase angle of the whole system can be achieved

$$U_{\mathrm{OUT}i} = I_{3i} Z_{Li} = \frac{U_{\mathrm{IN}i}\frac{X_{Mi}}{X_{Cci}}}{R_{Li}+\frac{Z'_{Li}}{X_{Cci}^2}(X_{Mi}^2+R_{Li}R_{LPi})} Z_{Li} \tag{15}$$

$$Z_{\mathrm{IN}i} = \frac{U_{\mathrm{IN}i}}{I_{1i}} = \frac{R_{Li}+\frac{Z'_{Li}}{X_{Cci}^2}(X_{Mi}^2+R_{Li}R_{LPi})}{1+\frac{R_{LPi}}{X_{Cci}^2} Z'_{Li}}. \tag{16}$$

In reality, the relationship of X_{Mi}, R_{Li}, R_{LPi} satisfies $X_{Mi}^2 \gg R_{Li}R_{LPi}$, and generally, the parasitic resistance R_{LSi} is far small than the load resistance Z_{Li}. Therefore, the output voltage can be simplified as

$$U_{\mathrm{OUT}i} = \frac{U_{INi} Z_{Li}}{R_{Li}\frac{X_{Cci}}{X_{Mi}} + \frac{X_{Mi}}{X_{Cci}} Z_{Li}} = \prod_{j=1}^{N} \frac{U_{\mathrm{IN}} Z_{Lj}}{R_{Lj}\frac{X_{Ccj}}{X_{Mj}} + \frac{X_{Mj}}{X_{Ccj}} Z_{Lj}}. \tag{17}$$

From (16), it could be concluded that when the system input voltage U_{IN} and the parasitic resistance R_{Li} are fixed, the output voltage $U_{\mathrm{OUT}i}$ of *i*th load is related as the value of Z_{Li}, X_{Cci}, X_{Mi}. Compared with the conclusion from (10), the variation of the load impedance Z_{Li} will affect the output voltage under the impact of the parasitic resistance. To explicitly reveal the

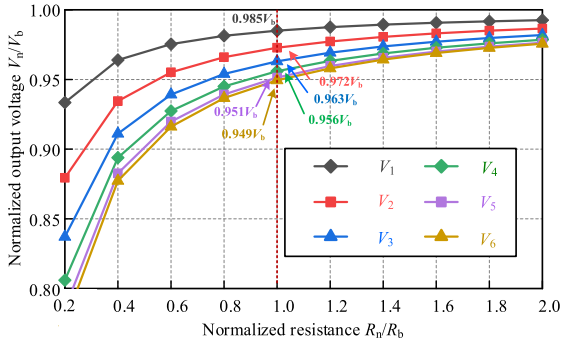


Fig. 11. Output voltage versus load resistance.

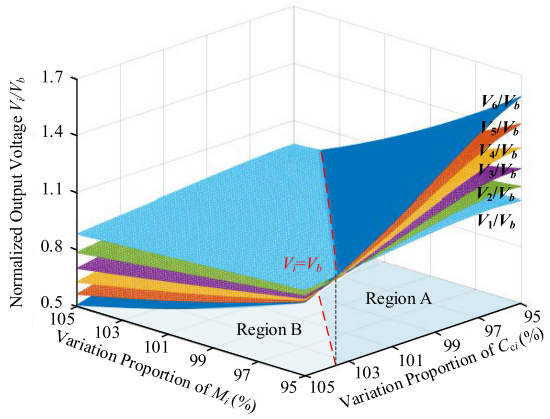


Fig. 12. Output voltage versus the variation of the compensation parameters.

impact of the parasitic resistance, Figs. 11 and 12 illustrate the relationships of the output voltage against the load resistance and the variation of circuit parameters C_{ci}, M_i with different load numbers when the quality factor $Q = 600$.

For simplicity, the parameters of each circuit are set to identical, which means that $L_1 = L_2 = L_3 = \cdots = L_N$, $L_{P1} = L_{P2} = L_{P3} = \cdots = L_{PN}$, $L_{S1} = L_{S2} = L_{S3} = \cdots = L_{SN}$, $R_{L1} = R_{L2} = \cdots = R_{LN}$.

To normalize the voltage and the resistance, the based values are defined as

$$V_b = U_{\mathrm{IN}}, R_b = X_{Cc1}. \tag{18}$$

It can be seen from Fig. 11 that the voltage drop of each load has increased with the decrease of the load resistance when considering parasitic resistance. The loop current through the parasitic resistance has been increased, leading to a larger voltage drop in the compensation topology. Therefore, increasing the value of load resistance could help to reduce the voltage drop induced by the parasitic resistance. In addition, under the constant load resistance, increasing the load number N will increase the output voltage drop, which is due to the equivalent load resistance Z_{Li} decreases with the increase of the load number N.

Fig. 12 illustrates the output voltage against the variation of the mutual inductance M_i and capacitance C_{ci}. It can be concluded that decreasing the value of M_i and C_{ci} will enhance

the output voltage, which is consistent with the analysis of (10). In region A, the output voltages V_i are higher than V_b, and $V_6>V_5>V_4>V_3>V_2>V_1$. While in region B where the output voltage $V_i/V_b<1$, the output voltages V_i have decreased with the increase of i. In addition, when the M_i and C_{ci} varied by $\pm5\%$, the output voltage changed from 0.53 to 1.62. Therefore, it is significant to assure the fixation of M_i and C_{ci}, and the proposed system is appropriate for the usage scenario with no or minor misalignment.

B. System Efficiency

The impact of the parasitic resistances on the system efficiency is analyzed in this section. The power loss of the CPT system includes inverter loss, rectifier loss, passive elements loss and coupler loss. It should be mentioned that the coupler loss is not considered in theoretical analysis.

1) Inverter:

$$\begin{aligned} P_{\text{inverter}} &= P_{\text{Cond}} + P_{\text{SW}} \\ &= 2I_1^2 r_m + 4\sqrt{2}V_{\text{dc}} I_1 \left|\sin\theta\right| \left(\frac{E_{\text{off}}+E_{\text{on}}}{V_{DD}I_D} + \frac{Q_{\text{DD}}}{I_{R\_D}}\right) f \end{aligned} \tag{19}$$

where P_{SW} represents the MOSFETs' switching loss, E_{off} and E_{on} are the turn-ON and turn-OFF loss of MOSFETs, respectively. V_{DD} and I_D are, respectively, the reference drain–source voltage and source current of MOSFETs. Q_{DD} is the reverse recovery charge and $I_{R\cdot D}$ is the reference current of the diode [28], [29].

2) Rectifier: The power loss of rectifier j $(1 \le j \le N)$ is expressed as follows:

$$\begin{aligned} P_{\text{rectifier}j} &= \tfrac{4}{\pi}\int_{\theta}^{\theta+\pi} (V_f + r_d i_{sj}) i_{sj} d(\omega t) \\ &= \tfrac{4\sqrt{2}}{\pi} V_f I_{Sj} + 2r_d I_{Sj}^2, 1 \le j \le N \end{aligned} \tag{20}$$

where V_f is the diode forward voltage and r_d is the equivalent ON-state resistance of the anti-parallel diodes [28], [29]. The total power loss of rectifiers is expressed as follows

$$\begin{aligned} P_{\text{rectifier}} &= \sum_{j=1}^{N} P_{\text{rectifier}j} \\ &= \tfrac{4\sqrt{2}}{\pi} V_f \sum_{j=1}^{N} I_{Sj} + 2r_d \sum_{j=1}^{N} I_{Sj}^2. \end{aligned} \tag{21}$$

3) Passive Elements Loss: According to the ith loop current given in (14), the power loss of the compensation topology in ith circuit is calculated as follows:

$$P_{\text{LOSS\_}i} = \frac{U_{\text{IN}i}^2 \left[\frac{X_{Mi}^2}{X_{Cci}^2}\left(\frac{R_{LPi}}{X_{Cci}^2}Z' + R_{LSi}\right) + R_{Li}\left(\frac{R_{LPi}}{X_{Cci}^2}Z' + 1\right)^2\right]}{\left[R_{Li} + \frac{Z'_{Li}}{X_{Cci}^2}(X_{Mi}^2 + R_{Li}R_{LPi})\right]^2}. \tag{22}$$

From (22), it could be concluded that when the system frequency f, the impedance X_{Cci}, X_{Mi} and parasitic resistance R_{Li}, R_{LPi}, R_{LSi} are fixed, the power loss in ith circuit is only related to the input voltage $U_{\text{IN}i}$ (equal to $U_{\text{OUT}(i\text{-}1)}$) and the load resistance Z_{Li}. Therefore, the variation trend of the power loss is the same as the output voltage analyzed above. The power loss of the circuit far from the TX_0 is less than those of the circuit nearby TX_0, which is due to the loop current in ith circuit decreasing with the increase of i. The loop current in TX_0 is the maximum current of the system, leading to maximum power loss compared to another circuit. The system efficiency can be calculated by

$$\eta_s = \frac{\sum_{i=1}^{N} P_{\text{OUT}i}}{P_{\text{inverter}} + P_{\text{rectifer}} + \sum_{i=1}^{N}(P_{\text{OUT}i} + P_{\text{LOSS\_}i})}. \tag{23}$$

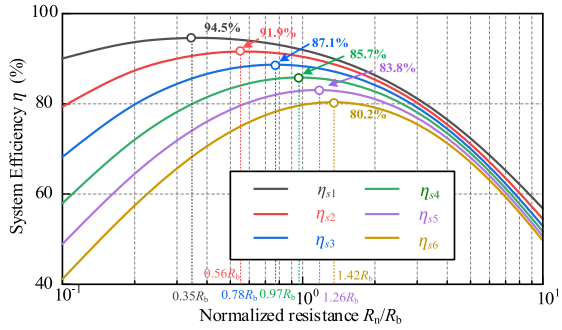


Fig. 13. System efficiency against the load resistance ($Q=600$ and $k=0.236$).

Based on the analysis above, Fig. 13 shows the curves of the system efficiency η_{si} $(1 \le i \le 6)$ against the load resistance with different load numbers when $Q = 600$. It clearly shows that, for the system efficiency η_{si} with different load numbers, there are different optimal load resistances with the maximum system efficiency. The value of optimal load resistance increases with the addition of load numbers. Moreover, it is obvious that increasing the load numbers would reduce the system efficiency, so the optimization of system efficiency could consider increasing the load resistance with multiple loads.

The coupling coefficient k_i of inductor L_i and L_{Pi} is expressed as

$$k_i = \frac{M_i}{\sqrt{L_i L_{Pi}}}. \tag{24}$$

The ac–ac efficiency of each circuit η_i $(1 \le i \le N)$, defined as the ratio of the input power of $U_{\text{IN}i}$ to the output power of Z_{Li}, can be calculated as follows:

$$\begin{aligned} \eta_i &= \frac{Z_{Li}}{\frac{2Z'_{Li}}{k_i^2 Q_{Li}Q_{LPi}} + Z'_{Li} + \frac{X_{Li}}{Q_{Li}} + \frac{{Z'_{Li}}^2(1+k_i^2 Q_{Li}Q_{LPi})}{k_i^4 Q_{Li}Q_{LPi}^2 X_{Li}}} \\ &\le \frac{Z_{Li}}{\frac{2Z'_{Li}}{k_i^2 Q_{Li}Q_{LPi}} + Z'_{Li} + 2\frac{Z'_{Li}\sqrt{(1+k_i^2 Q_{Li}Q_{LPi})}}{k_i^2 Q_{Li}Q_{LPi}}}. \end{aligned} \tag{25}$$

When the value of X_{Li} satisfy the equation in (26), the maximum efficiency η_i $(1 \le i \le N)$ derived in inequation of (25) can be achieved

$$X_{Li} = \frac{Z'_{Li}\sqrt{1 + k_i^2 Q_{Li}Q_{LPi}}}{k_i^2 Q_{LPi}}. \tag{26}$$

According to (26), the system efficiency can be optimized by selecting the appropriate value of L_i, the optimized efficiency of each circuit is shown in (25). To further optimize system efficiency, the relationships between the system efficiency and

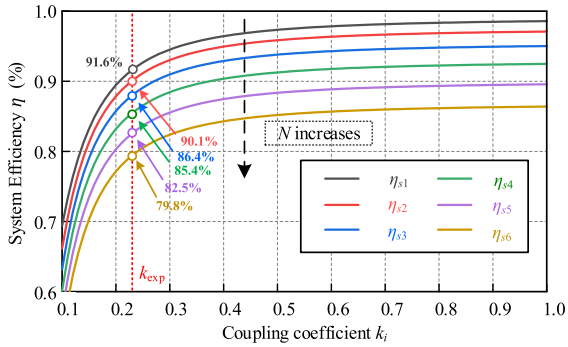


Fig. 14. System efficiency against the coupling coefficients ($Q = 600$ and $R = R_b$).

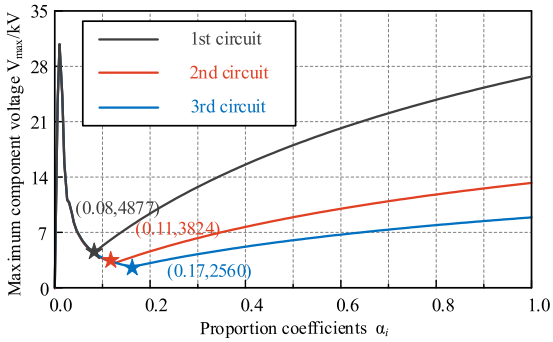


Fig. 15. Maximum voltage stress of compensation components against α_i.

the variation of the coupling coefficient k_i ($1 \le i \le 6$) are illustrated in Fig. 14. The calculation result shows that the enhancement of the k_i ($1 \le i \le 6$) will improve the system efficiency, while the system efficiency will reduce with the addition of load numbers. When the isolation structure utilizes the tightly coupled transformer, which means $k_i = 1$, the system efficiency is the highest. However, the magnetic loss might increase as a result of the high-frequency current, reducing the system efficiency. Therefore, the loosely coupled transformer can also be adopted, as long as the system efficiency meets the requirement.

IV. Multiload CPT System Design

To satisfy the power requirement for reefer container application, apart from increasing the mutual capacitor C_M and the operation frequency f, increasing the voltage applied on the coupler structure is the primary method. At the same time, the high voltage on compensation components and coupler structure will improve the system costs. Therefore, a system parameter design method based on the passive components voltage optimization is introduced in this section.

The relationships between the coupling capacitance C_M and parallel capacitance are denoted by

$$C_M = \alpha_i C_{Pi} = \alpha_i C_{Si} (i = 1, 2, 3) \tag{27}$$

where α_i are the proportion coefficients of C_{Pi} and C_{Si} to C_M in a range between 0 and 1.

The voltage stress of each compensation component can be calculated with the system parameters given in Table I. The curves of the maximum component voltage in the ith circuit against α_i are plotted in Fig. 15. It can be seen that the voltage stress in compensation components can be optimized with a proper selection of C_{Pi} and C_{Si}. The system design process of the proposed multiload CPT system to optimize the voltage stress is shown in Fig. 16. Substituting the selected C_{Pi} and C_{Si} into (4), the system parameters are calculated as given in Table II. It should be noted that the value of L_1 is designed to be slightly larger to achieve the ZVS operation of MOSFET.

The EMC performance is a significant factor to be considered in the CPT system design. According to [30], the electric field in this article should be smaller than 614 V/mm. The electric field

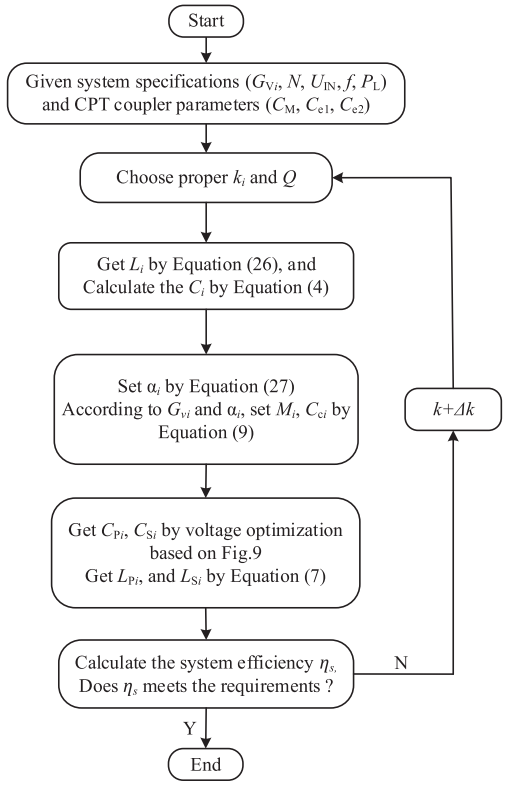


Fig. 16. Design flowchart of the multiload CPT system.

emissions of the coupler structure in the first circuit are simulated in Maxwell as shown in Fig. 17. According to Tables I and II, the maximum potential difference on coupler structure can be calculated as 6.9 kV, and P_5, P_6 are floated as simulations of the metal wall of reefer containers. It can be seen from Fig. 17(a) that the electric field strength of the red region is higher than 614 V/mm, while the maximum field strength between P_1-P_4 can reach 210 kV/m. As the shielding effect of P_5 and P_6, the electric field above and below the coupler structure has been significantly reduced, while there is still a small field leaking out to the surroundings in the experimental coupler. For reefer container application, as shown in Fig. 17(b), the electric fields can be suppressed between the containers, and the EMC safety

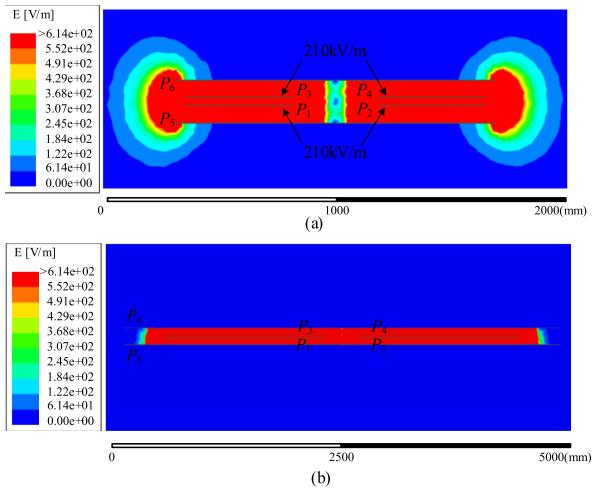


Fig. 17. Electric field emissions of coupler structure by Maxwell. (a) Experimental coupler. (b) Reefer container.

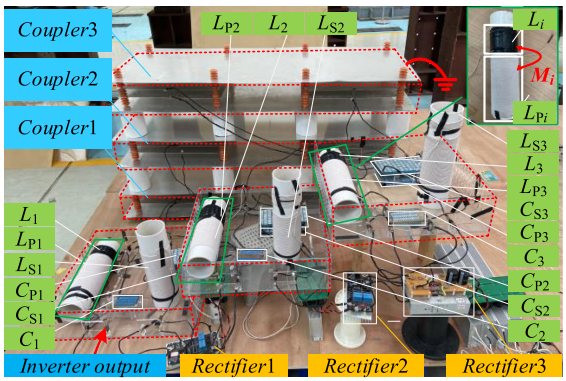


Fig. 18. Experimental prototype of the proposed CPT system.

of reefer containers can be guaranteed due to the shielding effect of the metal wall.

V. Experiment

A. Experimental Prototype

A 1.8-kW experiment prototype with three loads was constructed to verify the theoretical analysis, as shown in Fig. 18. The system parameters are given in Table II. Coupler plates are made of aluminum materials with the size of 500 mm × 500 mm × 2 mm. As the gap between reefer containers is measured as 200 mm, which means d_2 in Fig. 3 is 200 mm, the transmitting distance is set to 40 mm. Two rectangular grounded aluminum plates with the size of 1500 mm × 600 mm × 2 mm are placed at the top and bottom of the coupler plates as an imitation of the reefer container. The loosely coupled inductor L_i and L_{Pi} are two coils winded in a PVC pipe with mutual inductance M_i. Actually, L_i and L_{Pi} can be integrated into the tightly coupled transformer in practical application, while here adopted the simplest method to avoid the magnetic loss.

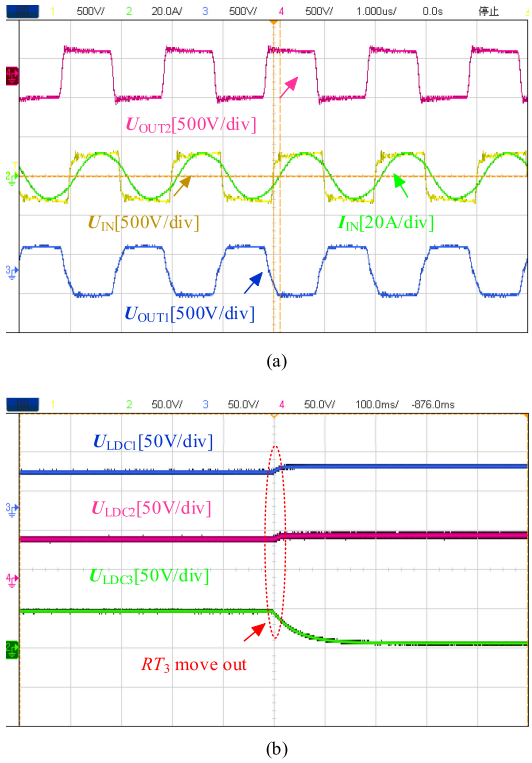


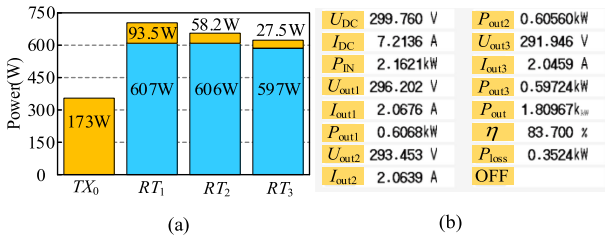
Fig. 19. Experimental results. (a) Experimental waveforms of U_{IN}, I_{IN}, U_{OUT1}, and U_{OUT2}. (b) Waveforms of U_{LDC1}, U_{LDC2}, and U_{LDC3} when RT_3 disconnected.

B. Experimental Results

Fig. 19(a) shows the waveforms of the U_{IN}, I_{IN}, U_{OUT1}, and U_{OUT2} when $U_{DC} = 300$V and $P_{OUT1} = P_{OUT2} = P_{OUT3} = 600$ W. The voltage gain is set to 1. It is observed that U_{OUT1} lags U_{IN} 180° and U_{OUT2} lags U_{OUT1} 180°, which satisfied the phase shift expressed in (9), and ZVS turn-ON operation is achieved in the inverter. The output dc voltage obtained in Fig. 11(d) can reach 296.2, 293.4, and 291.9 V, which is conformed to the design value.

Fig. 19(b) shows the waveforms of U_{LDC1}, U_{LDC2}, and U_{LDC3} when RT_3 moves out. For safety concerns, the validation experiment was carried out when $U_{DC} = 50$V. It can be seen that when RT_3 moves out, the load voltage U_{LDC1} changes from 50.8 to 57.5 V, U_{LDC2} changes from 50.5 to 56.3 V. When RT_3 moves out, the equivalent load resistance Z_{L1}, Z_{L2} have increased, reducing the loop current in RT_2, RT_1, and TX_0. That means the voltage drop in the parasitic resistance has decreased either, increasing the output voltage when RT_3 moves out.

Fig. 20(a) illustrates the power distribution among receivers when load resistances are 150 Ω. The blue part represents the output power in each receiver, and the yellow part represents each receiver's power loss. The power loss in RT_1 to RT_3 accounted for 54.0%, 33.6%, and 15.9%, respectively. As the same analysis given before, the loop current value decided the power loss in each circuit. While the loop current in TX_0 is the largest, leading to the highest power loss compared to other parts. Fig. 20(b) shows the result of the power analyzer. It can be seen



(a) (b)

Fig. 20. Experimental results when $U_{\mathrm{DC}} = 300$ V, $R_{Leq1} = R_{Leq2} = R_{Leq3} = 150\ \Omega$. (a) Power distribution among receivers. (b) Measured efficiency and output power.

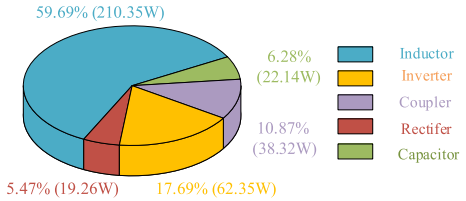


Fig. 21. Power loss distribution among circuit components when $N = 3$.

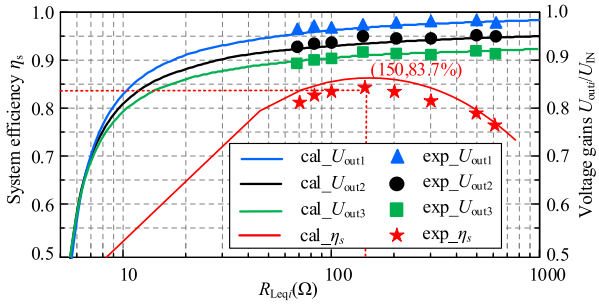


Fig. 22. System efficiency η_s and voltage gain versus R_{Leqi}.

that the system efficiency is 83.7%, and the TX_0 generates the highest power loss for the largest current flowing in the circuit among other receivers.

The power loss distribution among the circuit components is evaluated and shown in Fig. 21. The power loss in inverter, rectifier, and compensation elements can be calculated by their inner resistances according to the datasheets and experimental results [18]. The rest of the losses are assumed to be in the coupler plates. The power loss in compensation inductors accounts for approximately 60% of the total losses, which can be reduced by adopting high quality factors inductors. Moreover, larger coupling coefficients of loosely coupled inductors can enhance the system performance either.

Fig. 22 shows the calculation curves and experimental results of the voltage gain and system efficiency η_s versus load resistance R_{Leqi}. The curve of η_s is plotted at $R_{Leq1} = R_{Leq2} = 150\,\Omega$ while R_{Leq3} varied from 0 to 1000 Ω. Fig. 22 demonstrates that the output voltage fluctuation is within 7.68% when the load changes from 70 to 600 Ω. Moreover, due to the impact of parasitic resistance, the output voltage will decrease slightly as the load resistance decreases. The system efficiency increases first and then decreases with the increase of the R_{Leq3}. Thus, a proper design of system parameters can optimize system efficiency in future research.

TABLE III
EXPERIMENTAL RESULTS AND SIMULATED RESULTS

Symbol	Experiment Value	Simulated Value with isolation	Simulated Value without isolation
U_{OUT1}	296V	300V	226V
U_{OUT2}	293V	300V	189V
U_{OUT3}	291V	300V	175V

TABLE IV
RMS OF THE VOLTAGE STRESS

Symbol	Value	Symbol	Value	Symbol	Value
V_{CP1}	3.88kV	V_{CP2}	3.62kV	V_{CP3}	3.41kV
V_{CS1}	4.86kV	V_{CS2}	3.41kV	V_{CS3}	1.78kV
V_{LP1}	3.88kV	V_{LP2}	3.62kV	V_{LP3}	3.41kV
V_{LS1}	4.78kV	V_{LS2}	3.36kV	V_{LS3}	1.75kV

The simulated results and experimental results of the output voltage in the proposed system with/without isolation structure are given in Table III. The simulation is carried out in MATLAB/Simulink without considering the parasitic resistance, which highlights the impact of loop current between the coupler. As given in Table III, the experimental value is close to the simulated value with isolation structure, while the output voltage dropped a lot in the simulated value without isolation. It verified the proposed theory, and the isolation structure is necessary to maintain the output properties.

When $\alpha_1 = 0.09$, $\alpha_2 = 0.12$, and $\alpha_3 = 0.16$, RMS of the voltage stress on L_{Pi}, L_{Si}, C_{Pi}, C_{Si} are measured as given in Table IV (the voltages of L_i and C_i are far less than that of others, so they are not listed here). It could be found that the first circuit suffers from the most extensive voltage stress, the second circuit is the next, the third circuit is the smallest. That is due to the TX_0 transferring the largest power to the following receiver. Therefore, it is crucial to add extra insulation to the first circuit.

When considering the contact resistance, or out of contact due to insulation problem between P_5 and P_6, the potential difference between P_5 and P_6 against the misalignment are evaluated by calculation and experiments as shown in Fig. 23. When P_5 and P_6 are connected by the resistance of 10 Ω, 50 Ω and 100 Ω, the calculation and experimental results are illustrated in Fig. 23(a). When the misalignment of *X*-axis is 250 mm (half of the coupler length), the potential difference between P_5 and P_6 is 5.34 V, while the misalignment of *Y*-axis has almost no effect on $|\varphi_{P5}\text{-}\varphi_{P6}|$. Moreover, the potential difference between P_5 and P_6 enhances with the increase of contact resistance. Fig. 23(b) presents the curves when P_5 and P_6 are connected by capacitors of 0.5, 1, and 2 nF. It can be concluded that with a larger contact capacitor between P_5 and P_6, the potential difference of container is higher with misalignment of *X*-axis. As the same with Fig. 23(a), the misalignment of *Y*-axis has little effect on $|\varphi_{P5} - \varphi_{P6}|$. For reefer container application, the misalignment of *X*-axis and *Y*-axis are generally 0–100 mm,

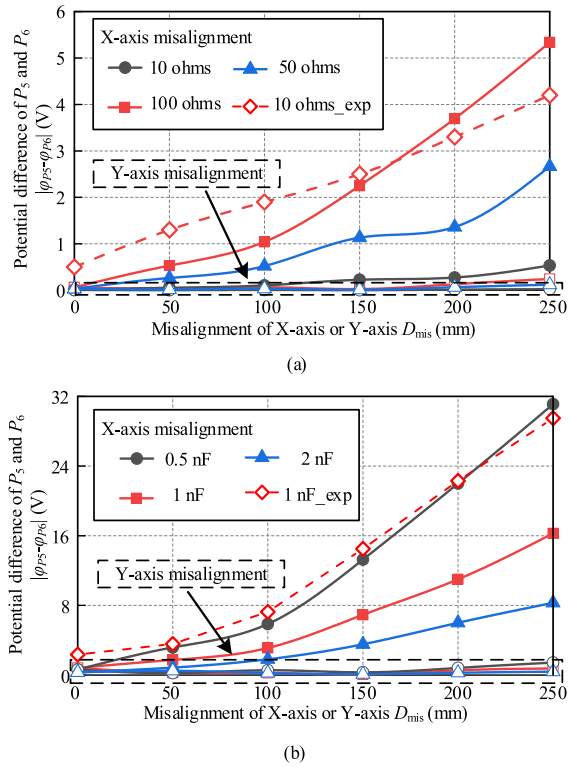


Fig. 23. Potential difference of P_5 and P_6 against misalignment. (a) Contact resistance. (b) Contact capacitors.

which is extremely small compared to the reefer container size of 5.42 m × 2.26 m × 2.24 m. Therefore, there is almost no difference in potential between containers for reefer container application.

VI. Conclusion

In this article, a novel multiload CPT system was proposed for the reefer container charging system. Each container functions not only as a receiver, but a repeater to powering the next container. The SP-CL compensation topology with an isolation structure was proposed to achieve the constant voltage output. The isolation structure eliminates the undesirable loop current of cross-coupling and functioned as a compensation circuit either. The impact of parasitic resistance was analyzed to show the practical performance of the output voltage and the system efficiency. A parameters design method based on voltage stress optimization was given, and the experimental results of a 1.8-kW prototype system had validated the effectiveness of the proposed theory. The fluctuation of the output voltage was within 7.68% when the load changes from 70 to 600 Ω. The power loss in RT_1 to RT_3 accounted for 54.0%, 33.6%, and 15.9%, respectively. The maximum efficiency can reach 83.7%, and the voltage stress was reduced by parameter optimization. Future work may consider the different compensation topologies of the multiload CPT system for other output characteristics.

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