A Generalized Real-Time Computation Method With Dual-Sampling Mode to Eliminate the Computation Delay in Digitally Controlled Inverters

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***Abstract*—Digital control has been widely adopted in grid-connected inverters, thanks to easy implementation of complicated control algorithms. However, the digital control delay deteriorates the performance of the inverter and tends to cause system instability. In this article, the generating mechanism of the digital control delay, including computation delay and pulsewidth modulation delay, is analyzed. Then, a generalized real-time computation method with a dual-sampling mode is derived to directly eliminate the computation delay, based on two- and multilevel phase-legs. On this basis, the operation principle of the method for three- and single-phase inverters with two- and multilevel topologies is elaborated. Finally, the experimental and simulation results from three- and single-phase *LCL*-type grid-connected inverters are provided to verify the effectiveness of the proposed method.**

***Index Terms*—Computation delay, digital control delay, dual-sampling mode, inverter, real-time computation.**

I. Introduction

A DISTRIBUTED power generation system (DPGS) is an effective way to utilize the renewable energy, such as wind and solar energy, to alleviate the problems of energy shortage and environmental pollution. As the power conversion interface between the DPGS and the utility grid, the grid-connected inverter plays an important role in injecting high-quality current into the grid [1].

Digital control has been widely adopted in grid-connected inverters thanks to simple hardware circuit, high disturbance- rejection ability, and easy implementation of complicated control [2]. However, digital control introduces control delay, including the computation delay and pulsewidth modulation (PWM) delay [3], resulting in reduced bandwidth of the control loop [4]. Furthermore, when active damping is adopted [5], right-half-plane (RHP) poles could be generated and the real part of the output impedance may be negative, which deteriorates the system stability [5]–[8]. Therefore, it is significant to reduce the impact of digital control delay, and the approaches can be classified into two kinds.

One approach is to compensate the digital control delay by adding a phase-lead unit [9]–[12] or adopting prediction control [13]–[15]. The compensation unit $G(z) = 1/(1+z^{-1})$ is proposed in [9], which is essentially an infinite impulse response filter and has positive phase below the Nyquist frequency. Nevertheless, the gain of the compensation unit becomes infinity around the Nyquist frequency, which will amplify high-frequency noise. This problem can be solved by introducing a weighting coefficient λ, and the compensation unit is changed to $G'(z) = 1/[\lambda+(1-\lambda)z^{-1}]$ [10]. However, the frequency range with effective phase compensation is narrowed. In order to compensate the phase delay in a wider frequency range, the compensation unit is modified as $G''(z) = [(1+\alpha+\beta)-nz^{-1}]/(1+\alpha z^{-1})$ by using the interpolation method [11]. In [12], the polynomial is used to fit a prediction component with the Taylor formula to counteract the digital control delay, and a low-pass filter is cascaded to avoid high-frequency noise amplification. Nevertheless, the above methods cannot completely compensate the digital control delay. For the predictive control schemes, such as linear prediction [13], Smith prediction [14], and Kalman prediction [15], the predictive accuracy depends on the accuracy of the system model, and the parameters variation, estimation, and sampling in practical circuit will influence the performance and stability of the system [16]. Although the predictive error can be reduced by the extended state observer, it cannot be totally eliminated [17].

The other approach is to directly reduce the computation delay by adjusting the sampling instant or the modulation wave update instant. Instead of locating the sampling instants at the peak and/or valley of the carrier in the synchronous sampling mode, the sampling instants are shifted toward the modulation wave update instants to reduce the computation delay [4], [5], [18]. However, the sampled signal is not the average value per switching period and contains aliasing components. Meanwhile,

Manuscript received April 25, 2021; revised August 27, 2021 and October 7, 2021; accepted November 12, 2021. Date of publication November 18, 2021; date of current version January 19, 2022. This work was supported in part by the National Natural Science Foundation of China under Award 52077101, in part by the Jiangsu Province 333 Program for Excellent Talents under Award BRA2020039, and in part by the Postgraduate Research and Practice Innovation Program of Jiangsu Province under Award KYCX20_0199. Recommended for publication by Associate Editor J. A. Cobos. *(Corresponding author: Xinbo Ruan.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3129069.

Digital Object Identifier 10.1109/TPEL.2021.3129069

the sampling instant may be close to the switching action instant, resulting in switching noise in the sampled results [5]. A multisampling method is proposed in [19], where the sampled signals and modulation wave are updated multiple times in one carrier period, and thus, both the computation and PWM delays are reduced. However, the sampled results are also influenced by the aliasing and switching noise. In [20], a real-time computation method is proposed, where the sampling instants are located at the peak and/or valley of the carrier, and the modulation wave is updated immediately once the computation is completed. If the modulation wave is computed out and updated before it intersects the carrier, the computation delay can be eliminated. This method requires enough time for computation. Although advanced and high-performance digital signal processors (DSPs) have fast computation speed, the computation time is still not short enough when the switching frequency is quite high with GaN and SiC power devices. In [21], a dual-sampling mode is proposed to achieve real-time computation for single-phase full-bridge inverter, and the allowed computation time is one-eighth carrier period.

Combining the aforementioned two kinds of approaches together, a hybrid PWM update method for a three-phase ac drives is proposed in [22]. In a sampling period, the modulation wave is first updated at the beginning of each sampling period according to predictive control with the last-period sampled results. Once the real-time computation of the present-period sampled results is completed, the modulation wave is immediately updated again. In this way, the computation delay can also be eliminated. However, the modulation wave should be computed out and updated multiple times in one sampling period, and the system performance depends on the predictive accuracy.

This article aims to directly eliminate the computation delay by choosing suitable sampling instant and adjusting the modulation wave update instant, and a generalized real-time computation method with a dual-sampling mode is derived for three- and single-phase inverters with two- and multilevel topologies.

The rest of this article is organized as follows. In Section II, the generating mechanism of the digital control delay is presented. In Section III, to directly eliminate the computation delay, the generalized real-time computation method with a dual-sampling mode is derived based on the two- and multilevel phase-legs. In Section IV, the working principles of the generalized real-time computation method with the dual-sampling mode for three- and single-phase grid-connected inverters are illustrated. In Section V, the improved current control performance with reduced control delay is demonstrated. In Section VI, experimental and simulation results are provided to verify the effectiveness of the proposed generalized real-time computation method with the dual-sampling mode. Finally, Section VII concludes this article.

II. Generating Mechanism of Digital Control Delay

In this section, the three-phase two-level *LCL*-type grid-connected inverter, as shown in Fig. 1, is selected to illustrate the generating mechanism of the digital control delay. $V_{\rm in}$ is the input dc voltage, v_{xo} ($x = a$, b, or c) is the phase-leg voltage and $v_{\rm g}$ is the grid voltage. Three pairs of the inverter-side inductors L_1, filter capacitors C, and grid-side inductors L_2 form the three-phase *LCL* filter. The injected grid currents $i_{\rm g\_}abc$ and the capacitor currents $i_{\rm C\_}abc$ are sampled for computing the modulation waves, $v_{\rm M\_}abc$, which are sent to the sinusoidal pulsewidth modulator (SPWM) to generate the drive signals for the power switches.

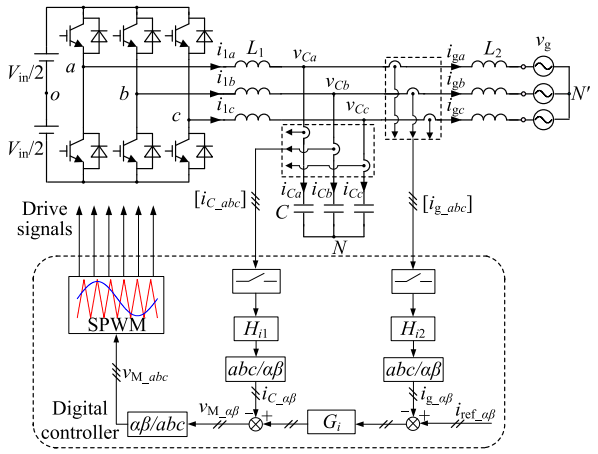

Fig. 1. Main circuits and control diagrams of the three-phase two-level *LCL*-type grid-connected inverter.

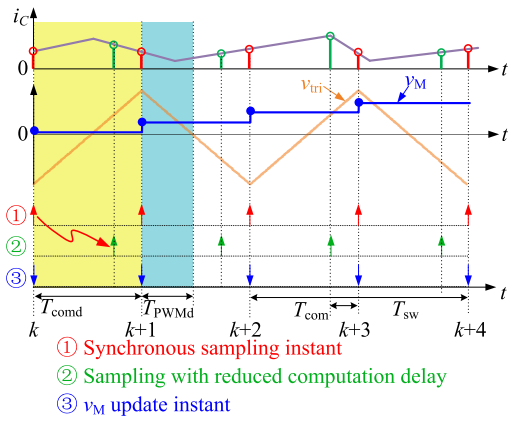

Fig. 2. Key waveforms of signals sampling and digital SPWM.

Taking phase a as an example, Fig. 2 shows the key waveforms of sampling i_C and digital bipolar SPWM, where $T_{\rm sw}$ is the switching period. In the synchronous sampling mode, i_C is sampled twice in a switching period, and the sampling instants ① are located at the peak and the valley of the carrier, respectively. Thus, the average value per switching period (the fundamental component) of i_C is obtained. At the kth time step, the sampled current is used to compute $v_{\rm M}$. In order to avoid the unwanted intermediate PWM transitions, $v_{\rm M}$ is updated at the $(k+1)$th time step. Thus, the computation delay $T_{\rm comd} = 0.5T_{\rm sw}$ is introduced.

After being updated, the modulation wave is held on for $0.5T_{\rm sw}$ and compared with the triangular carrier to generate the drive signals for the power switches. This behavior can be

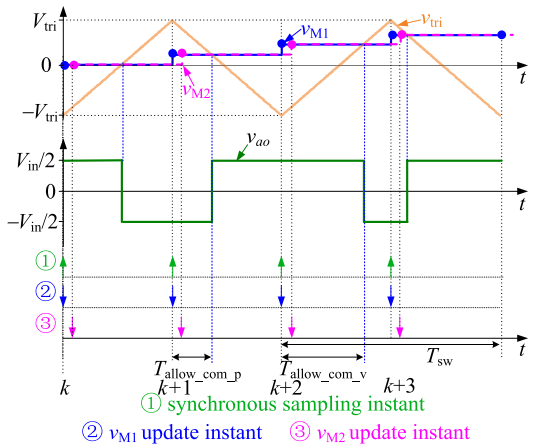

Fig. 3. SPWM scheme of a real-time computation method for a two-level phase-leg.

modeled by the zero-order holder (ZOH), expressed as

$$G_{\mathrm{h}}(s)=\frac{1-e^{-0.5sT_{\mathrm{sw}}}}{s}\approx T_{\mathrm{sam}}e^{-0.25sT_{\mathrm{sw}}}. \tag{1}$$

As seen from (1), the ZOH introduces a delay of half hold-on time of the modulation wave, which is called the PWM delay, expressed as $T_{\mathrm{PWMd}}=0.25T_{\mathrm{sw}}$.

III. Generalized Real-Time Computation Method With the Dual-Sampling Mode

A. Real-Time Computation Method With the Dual-Sampling Mode for the Two-Level Phase-Leg

As discussed in Section II, the PWM delay is always half hold-on time of the modulation wave. Therefore, reducing or even eliminating the computation delay is crucial to reducing the digital control delay. To attain this, the sampling instant or the modulation wave update instant can be adjusted to make them closer.

As observed in Fig. 2, by shifting the sampling instant (denoted as ②) toward the modulation wave update instant with the interval of the computation time T_{com}, the computation delay is reduced to T_{com}. However, the sampled results are not the average value per switching period and contain low-order aliased harmonic components. Moreover, the sampled results might be distorted by the switching noise if the sampling instant is close to the switching instance. Thus, shifting the sampling instant is not a good choice.

In Fig. 3, the sampling instant is still located at the valley or peak of the carrier, and the modulation wave is updated immediately after it is computed out, which is named as real-time computation method. As seen, v_{M1} is the ideal modulation wave obtained at the very instant of sampling and updated without any delay. The actual modulation wave v_{M2} is obtained with an inevitable computation delay T_{com}. If v_{M2} can be computed out and updated before it intersects v_{tri}, the output voltage of phase-leg v_{ao}, generated by v_{M2} is exactly the same as that generated by v_{M1}. As a result, the computation delay is totally eliminated. To realize this, when the sampling instant is located at the peak of the carrier, which is the peak-value sampling mode, the allowed computation time is

$$T_{\mathrm{allow\_com\_p}}=\frac{V_{\mathrm{tri}}-v_{\mathrm{M2}}}{2V_{\mathrm{tri}}}\frac{T_{\mathrm{sw}}}{2} \tag{2}$$

where V_{tri} is the amplitude of the carrier, and $-V_{\mathrm{tri}}<v_{\mathrm{M2}}<V_{\mathrm{tri}}$.

When the sampling instant is located at the valley of the carrier, which is the valley-value sampling mode, the allowed computation time is

$$T_{\mathrm{allow\_com\_v}}=\frac{v_{\mathrm{M2}}+V_{\mathrm{tri}}}{2V_{\mathrm{tri}}}\frac{T_{\mathrm{sw}}}{2}. \tag{3}$$

According to (2) and (3), the allowed computation time in respect of v_{M2} for the valley- and peak-sampling modes are depicted, as shown in Fig. 4. As seen, the allowed computation time decreases with v_{M2} when using the peak-value sampling mode, and increases with v_{M2} when using the valley-value sampling mode. Obviously, when v_{M2} is close to V_{tri} or $-V_{\mathrm{tri}}$, the allowed computation time is extremely short.

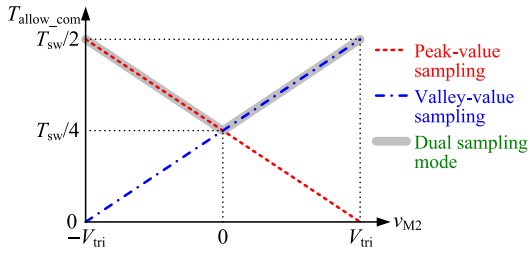

Fig. 4. Allowed computation time versus the modulation wave.

For the sake of the longer allowed computation time, it is natural to combine the two sampling modes and only implement sampling behavior once in a switching period. When $-V_{\mathrm{tri}}\le v_{\mathrm{M2}}\le 0$, the peak-value sampling mode is chosen, while when $0\le v_{\mathrm{M2}}\le V_{\mathrm{tri}}$, the valley-value sampling mode is chosen. Thus, the allowed computation time is shown in Fig. 4 with the heavy solid line, and the minimum allowed computation time is $T_{\mathrm{sw}}/4$. This sampling method is named as dual-sampling mode, and Fig. 5 shows the key waveforms of the real-time computation method with the dual-sampling mode for the two-level phase-leg.

To better observe the performance of the synchronous sampling mode, the real-time computation method, and the real-time computation method with the dual-sampling mode, Table I gives the comparison among these methods in terms of the computation delay, PWM delay, total delay, and minimum allowed computation time.

B. Real-Time Computation Method With the Dual-Sampling Mode for the Multilevel Phase-Leg

First, the real-time computation method with the dual-sampling mode is extended for a three-level phase-leg, as shown in Fig. 6. Fig. 7 shows the key waveforms of the level-shifted carrier SPWM scheme, where two carriers with the amplitude of $V_{\mathrm{tri}}/2$ are used. As seen, in the negative half-cycle, $v_{\mathrm{M2}}<v_{\mathrm{tri1}}$, Q_1 is turned OFF and Q_4 is turned ON. Therefore, when $v_{\mathrm{M2}}>$

TABLE I
COMPARISONS AMONG SPWM SCHEMES OF DIFFERENT METHODS FOR ONE PHASE-LEG

Phase-leg	SPWM scheme	Sampling and modulation wave update method	Implementing times of sampling in a switching period	Computation delay	PWM delay	Total delay	Minimum allowed computation time
Two-level	Bipolar SPWM	Synchronous sampling mode	2	$T_{sw}/2$	$T_{sw}/4$	$(3T_{sw})/4$	$T_{sw}/2$
		Real-time computation	2	0	$T_{sw}/4$	$T_{sw}/4$	Extremely short
		Real-time computation with dual-sampling mode	1	0	$T_{sw}/2$	$T_{sw}/2$	$T_{sw}/4$
(n+1)-level	Carrier level-shifted SWPM	Real-time computation with dual-sampling mode	1	0	$T_{sw}/2$	$T_{sw}/2$	$T_{sw}/4$
	Carrier phase-shifted SWPM		n	0	$T_{sw}/(2n)$	$T_{sw}/(2n)$	$T_{sw}/(4n)$

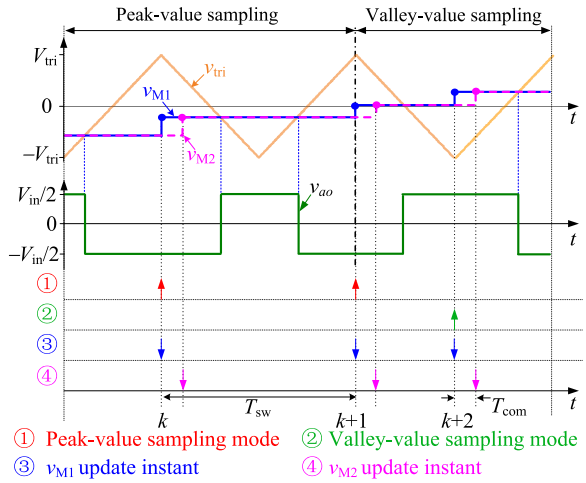

Fig. 5. SPWM scheme of the real-time computation method with the dual-sampling mode.

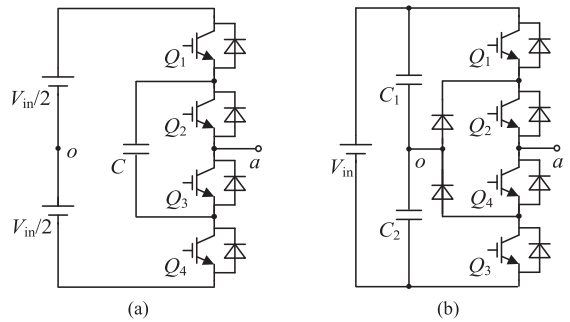

Fig. 6. Topologies of the three-level phase-leg. (a) Capacitor-clamped. (b) Diode-clamped.

v_{tri2}, Q_2 is turned ON and Q_3 is turned OFF, resulting in $v_{ao} = 0$, and when $v_{M2} < v_{tri2}$, Q_2 is turned OFF and Q_3 is turned ON, resulting in $v_{ao} = -V_{in}/2$. Similarly, in the positive half-cycle, v_{ao} has two voltage steps, i.e., 0 and $V_{in}/2$. Other three-level topologies, e.g., T-type topology [23], can also generate the same phase-leg voltage v_{ao} with the same SPWM scheme, so they are not discussed here.

When adopting the real-time computation method with the dual-sampling mode, as seen in Fig. 7, during one switching period, the sampling behavior takes place once and the sampling

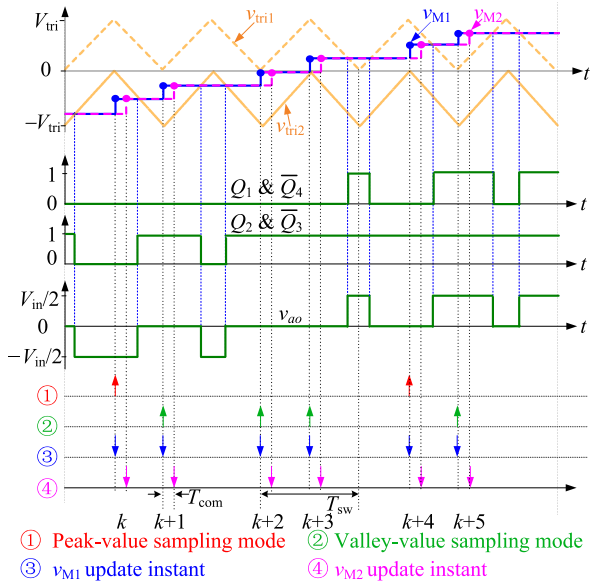

Fig. 7. Level-shifted-carrier SPWM scheme of the real-time computation method with the dual-sampling mode for a three-level phase-leg.

mode depends on v_{m2}, just as Fig. 5. Generally, for an $(n+1)$-level phase-leg [24], n carriers are used and their amplitudes are all V_{tri}/n, with the level-shifted carrier SPWM scheme. In a switching period, the sampling behavior still takes place once, and the modulation wave is also computed out and updated once time. Therefore, the PWM delay is $T_{sw}/2$, and the minimum allowed computation time is $T_{sw}/4$.

Besides, for the capacitor-clamped three-level phase-leg [25], the phase-shifted carrier SPWM can also be adopted, as shown in Fig. 8, where two carriers are 180°-phase-shifted. In the negative or positive half-cycle, regarding the two carriers v_{tri_1} and v_{tri_2} with shadow as one carrier, the waveforms of the modulation wave and the carrier are similar to those in Fig. 5, only the equivalent switching frequency is doubled. Therefore, when using the real-time computation method with the dual-sampling mode, the sampling behavior is implemented twice during one switching period, and the sampling modes are also decided by v_{M2}. Generally, for an $(n+1)$-level phase-leg with the phase-shifted carrier SPWM scheme, n carriers are used with $360°/n$ shifted phase. In a switching period, the sampling behavior is carried out n times, and the modulation wave will be computed

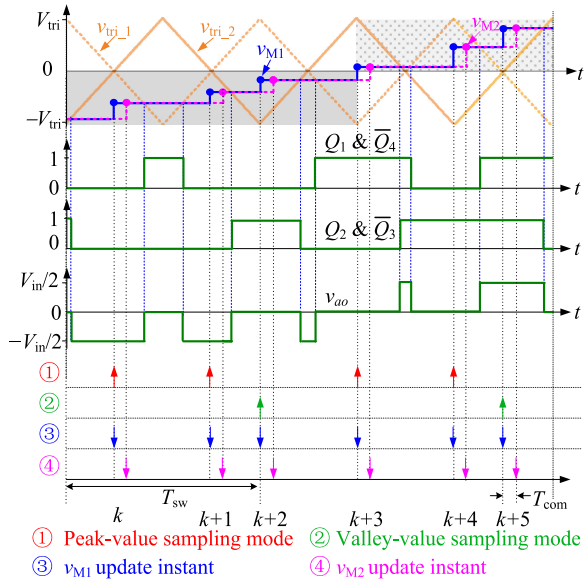

Fig. 8. Phase-shifted-carrier SPWM scheme of the real-time computation method with the dual-sampling mode for a three-level capacitor-clamped phase-leg.

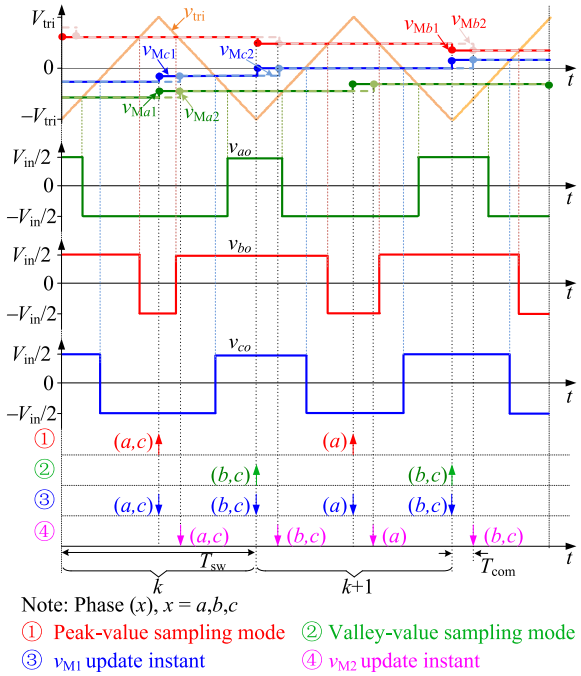

Fig. 9. SPWM of the real-time computation method with the dual-sampling mode for the two-level three-phase inverter.

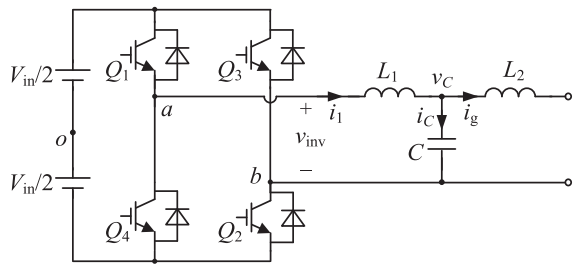

Fig. 10. Topology of the two-level full-bridge single-phase inverter.

out and updated n times. In this case, $T_{\mathrm{PWMd}} = T_{\mathrm{sw}}/(2n)$ and $T_{\mathrm{allow\_com}} = T_{\mathrm{sw}}/(4n)$.

The comparison of the real-time computation method with the dual-sampling mode for an $(n+1)$-level phase-leg with level-shifted carrier SPWM and phase-shifted SPWM is also given in Table I. As seen, with the phase-shifted carrier SPWM, the PWM delay is reduced to $T_{\mathrm{sw}}/(2n)$. This is because the sampling behavior is implemented n times in a carrier period and the hold-on time of the modulation wave becomes T_{sw}/n. However, the minimum allowed computation delay is reduced to $T_{\mathrm{sw}}/(4n)$.

IV. Applications of the Generalized Real-Time Computation Method With the Dual-Sampling Mode for Three- and Single-Phase Inverters

Based on the operating principle of the generalized real-time computation method for one phase-leg, this section elaborates the applications of the method for three- and single-phase grid-connected inverters.

A. Real-Time Computation Method With the Dual-Sampling Mode for the Three-Phase Inverter

Recalling Fig. 1, in the SPWM modulator for the three-phase two-level grid-connected inverter, one carrier and three 120°-phase-shifted modulation waves are used. To ensure that each phase modulation wave can be updated within the minimum allowed computation time, the sampling mode for each phase-leg is determined independently, as discussed in Section III-A, and then, the SPWM scheme of the real-time computation method with the dual-sampling mode for the two-level three-phase inverter can be obtained, as shown in Fig. 9.

As seen, three-phase modulation waves are independently computed out and updated once in a switching period with different sampling modes. For example, during the kth period, phases a and c adopt the peak-value sampling mode, while phase b adopts the valley-value sampling mode. In this way, the computation delay is eliminated, and the PWM delay and the allowed computation are the same as those of one phase-leg, i.e., $T_{\mathrm{PWMd}} = T_{\mathrm{sw}}/2$ and $T_{\mathrm{allow\_com}} = T_{\mathrm{sw}}/4$.

When adopting the real-time computation method with the dual-sampling mode in a multilevel three-phase inverter, the SPWM scheme can also be considered as a combination of that for three independent multilevel phase-legs. Therefore, the detailed operation principle is not repeated here.

B. Real-Time Computation Method With the Dual-Sampling Mode for the Single-Phase Inverter

In a single-phase full-bridge inverter, there are two phase-legs. For the two-level phase-legs, as shown in Fig. 10, the bipoloar SPWM can be used. Just as Fig. 5, when $v_{\mathrm{M2}} > v_{\mathrm{tri}}$, Q_1 and Q_2 are turned ON and Q_3 and Q_4 are turned OFF, resulting in $v_{\mathrm{inv}} = V_{\mathrm{in}}/2$, when $v_{\mathrm{M2}} < v_{\mathrm{tri}}$, Q_1 and Q_2 are turned OFF and Q_3 and Q_4 are turned ON, resulting in $v_{\mathrm{inv}} = -V_{\mathrm{in}}/2$. However, the harmonic components in v_{inv} is quite large. Acutally, the popular modulation scheme for a single-phase inverter is the unipolar and double-frequency SPWM scheme, whose working

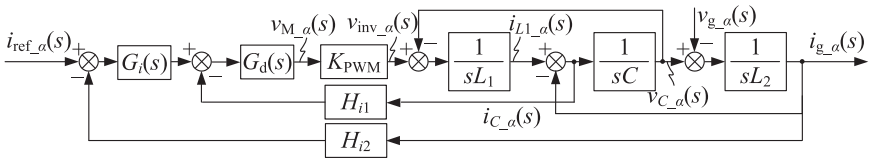

Fig. 11. Mathematical model of the *LCL*-type grid-connected inverter at the α-axis.

principle can also be illustrated by Fig. 8. When using the real-time compuatation method with a dual-sampling mode, the modulation wave is computated out and updated twice in a switching period. Therefore, the PWM delay is $T_{\rm sw}$/4, and the minimum allowed computation is $T_{\rm sw}$/8.

It is worth mentioning that the real-time computation method with a dual-sampling mode for the two-level single-phase inverter with the unipolar and double-frequency SPWM scheme is exactly the method proposed in [21].

As for the multilevel phase-legs, the real-time computation method with the dual-sampling mode can be adopted similarly according to the SPWM scheme for one phase-leg since it is still only one modulation wave used in the SPWM scheme. The PWM delay and the minimum allowed computation delay can be obtained according to Table I.

V. Improvements of Current Control Performance With Reduced Control Delay

When the real-time computation method with the dual-sampling mode is adopted, the control delay can be reduced. In this section, the current control performance of the three-phase *LCL*-type grid-connected inverter is analyzed to demonstrate the improvements brought by the reduced control delay.

A. Modeling the LCL-Type Grid-Connected Inverter

The main circuits and control diagrams of the three-phase *LCL*-type grid-connected inverter are given in Fig. 1, where the *LCL* filter can be designed with the method given in [26]. i_{g_abc} are sampled with the sensor gain of H_{i2} and transferred to $i_{g\_\alpha\beta}$ with *abc*/$\alpha\beta$ transformation. Then, $i_{g\_\alpha\beta}$ are compared with the current reference $i_{ref\_\alpha\beta}$, and the errors are sent to the current regulator $G_i(s)$. The capacitor currents are fed back with the coefficient of H_{i1} to damp the *LCL* filter resonance [5]. Subtracting $i_{C\_\alpha\beta}$ from the output of $G_i(s)$ yields the modulation waves $v_{M\_\alpha\beta}$. On this basis, the mathematical model of the *LCL*-type grid-connected inverter under the $\alpha\beta$ frame can be obtained. Since the mathematical models of the α-axis component and the β-axis component are the same and decoupled, Fig. 11 only gives the mathematical model of the α-axis component, where $G_d(s) = e^{-sTd}$ represents the digital control delay, $K_{PWM} = V_{in}/(2V_{tri})$ is the transfer function from v_{M_α} to v_{inv_α}, and V_{tri} is the amplitude of the triangular carrier.

According to Fig. 11 and using the equivalent transformations presented in [6], the current loop gain $T(s)$ can be obtained as

$$T(s) = \frac{K_{\rm PWM}G_i(s)G_{\rm d}(s)H_{i2}}{s^3L_1L_2C + s^2L_2CH_{i1}K_{\rm PWM}G_{\rm d}(s) + s(L_1+L_2)}. \tag{4}$$

To guarantee the zero-error tracking performance, the proportional–resonance (PR) regulator is adopted here, expressed as [27]

$$G_i(s) = K_{\rm p} + \frac{2\pi K_{\rm r}s}{s^2+\omega_{\rm o}^2} \tag{5}$$

where $K_{\rm p}$ is the proportional coefficient, $K_{\rm r}$ is the resonant coefficient, and $\omega_{\rm o}$ is the fundamental angular frequency.

In order to guarantee system stability, the crossover frequency $f_{\rm c}$ is usually designed much lower than the resonant frequency of the *LCL* filter, $f_{\rm r}$ [28]. Therefore, at $f_{\rm c}$ and the frequencies lower than $f_{\rm c}$, the *LCL* filter can be regarded as an *L* filter. Thus, the magnitude of $T(s)$ is simplified as

$$|T(s)| \approx \left|\frac{H_{i2}K_{\rm PWM}G_i(s)G_{\rm d}(s)}{s(L_1+L_2)}\right| = \left|\frac{H_{i2}K_{\rm PWM}G_i(s)}{s(L_1+L_2)}\right|. \tag{6}$$

Meanwhile, the PR regulator can be reduced to a proportional gain at $f_{\rm c}$, and thus, we have $|G_i(s)| \approx K_{\rm p}$. Letting $|T(j2\pi f_c)| = 1$ yields

$$K_{\rm p} \approx \frac{2\pi(L_1+L_2)}{K_{\rm PWM}H_{i2}}f_{\rm c}. \tag{7}$$

B. Current Control Performances With Different Reduced Control Delay

The performance of current control can be judged from following indices: 1) the loop gain at $f_{\rm o}\pm0.5$ Hz, denoted as $T_{\rm fo\pm0.5}$, which is usually designed larger than 75 dB to ensure that the steady-state error of the grid current is less than 1% when the grid frequency fluctuates from $f_{\rm o}-0.5$ Hz to $f_{\rm o}+0.5$ Hz; 2) the phase margin (PM), which is usually designed larger than 45° to preserve good dynamic performance; and 3) the gain margin (GM), which is usually designed larger than 3 dB to ensure the system robustness.

Substituting $s = j2\pi(f_{\rm o}\pm0.5)$ into (5), we have

$$G_i(2\pi(f_{\rm o}\pm0.5)) = K_{\rm p} \mp \frac{jK_{\rm r}(f_{\rm o}\pm0.5)}{0.5(2f_{\rm o}\pm0.5)}. \tag{8}$$

Since $f_{\rm o} >> 0.5$Hz, (8) can be approximated as

$$G_i(2\pi(f_{\rm o}\pm0.5)) \approx K_{\rm p} \mp jK_{\rm r}. \tag{9}$$

Substituting (9) into (6) leads to

$$\begin{aligned} T_{f{\rm o}\pm0.5} &= 20\lg|T(j2\pi f_{\rm o\pm0.5})| \\ &= 20\lg\left|\frac{H_{i2}K_{\rm PWM}(K_{\rm p}\pm jK_{\rm r})}{j2\pi(f_{\rm o}\pm0.5)(L_1+L_2)}\right|. \end{aligned} \tag{10}$$

Substituting (7) into (10) and manipulating, K_r constrained by $T_{fo\pm0.5}$ is obtained as

$$K_{r\_Tfo\pm0.5}=\sqrt{10^{\frac{T_{fo\pm0.5}}{10}}\left(f_o\pm0.5\right)-f_c}\frac{2\pi\left(L_1+L_2\right)}{H_{i2}K_{PWM}}. \tag{11}$$

According to $G_d(s)=e^{-sTd}$, the phase-leg introduced by the digital control delay $G_d(s)$ is expressed as

$$\angle G_d\left(j2\pi f\right)=-360^\circ\cdot T_d f. \tag{12}$$

Substituting $G_d(j2\pi f_x)=-90^\circ$ into (12), the frequency f_x, where $G_d(s)$ introduces a 90° phase-leg, can be derived as

$$f_x=1/(4T_d). \tag{13}$$

When $f_r<f_x$, the phase of $T(s)$ always crosses over -180° at f_r, so the resonance peak at f_r should be damped below 0 dB to ensure system stability. When $f_r>f_x$, the phase-leg introduced by $G_d(s)$ makes the phase plot of $T(s)$ crossover -180° at f_x in advance. Therefore, GM is expressed as

$$GM=\begin{cases}-20\lg\left|T\left(j2\pi f_r\right)\right|, & f_r\le f_x\\ -20\lg\left|T\left(j2\pi f_x\right)\right|, & f_r>f_x.\end{cases} \tag{14}$$

Substituting (4) into (14), the boundary of H_{i1} with respect to f_c under the constraint GM can be derived as

$$H_{i1\_GM}\left(f_c\right)=\begin{cases}\frac{2\pi f_c L_1}{K_{PWM}}10^{\frac{GM}{20}}, & f_r\le f_x\\ \frac{2\pi f_c L_1}{K_{PWM}}\left[10^{\frac{GM}{20}}\left(\frac{f_r}{f_x}\right)^2 f_c+\frac{f_r^2-f_x^2}{f_x}\right], & f_r>f_x.\end{cases} \tag{15}$$

Substituting $s=j2\pi f_c$ into (4), PM can be expressed as

$$PM=\frac{\pi}{2}-2\pi f_c T_d-\arctan\frac{K_r\omega_i}{\pi f_c K_p}-\arctan\frac{H_{i1}K_{PWM}f_c\cos\left(2\pi f_c T_d\right)}{2\pi\left(f_r^2-f_c^2\right)L_1+H_{i1}K_{PWM}f_c\sin\left(2\pi f_c T_d\right)}. \tag{16}$$

Since H_{i1} should meet both PM and GM constraints, H_{i1} in (16) should be substituted by H_{i1_GM}. Then, substituting (7) and (15) into (16), the boundary of K_r with respect to f_c under both the PM and GM constraints can be derived as (17), shown at the bottom of next page.

Substituting the constraint of $T_{fo\pm0.5}>75$ dB, GM >3 dB, PM $>45^\circ$, and the parameters listed in Table II given in Section VI into (11) and (17), the satisfactory regions of K_r and f_c for different T_d are depicted, as shown in Fig. 12. As seen, the satisfactory region becomes larger as T_d reduces, and larger K_r and f_c can be selected to improve the steady-state and dynamic performance.

Here, we choose $f_c=750$ Hz and $K_r=50$, corresponding to point A in Fig. 12, as a design example. Then, $K_p=0.312$ and $H_{i1}=0.7$ can be, respectively, obtained according to (7) and (15). According to (4) and the parameters given in Table II, the Bode plots of the current control loop of the three-phase grid-connected inverter, $T_{3p}(s)$, with $T_d=0.75T_{sw}$ and $T_d=0.5T_{sw}$ can be depicted, respectively, as shown in Fig. 13 . As seen, when $T_d=0.75T_{sw}$, $T_{3p}(s)$ has a pair of RHP poles, yet it has no positive or negative crossing. According to the Nyquist criterion, the system is unstable. When $T_d=0.5T_{sw}$, $T_{3p}(s)$ has no RHP pole and positive or negative crossing. Therefore, the system is stable, and PM $=46^\circ$ and GM $=8.2$ dB. Agreeing with Fig. 12, the system is stable when $T_d=0.5T_{sw}$, while it is unstable when $T_d=0.75T_{sw}$.

Similarly, the current-loop parameters of the two-level single-phase grid-connected inverter can also be designed, as listed in

TABLE II
PARAMETERS OF THE THREE-PHASE TWO-LEVEL GRID-CONNECTED INVERTER

Parameter	Symbol	Value	Parameter	Symbol	Value
Input voltage	V_{in}	700 V	Grid-side inductor	L_2	1.4 mH
Rated power	S	6 kVA	Resonant frequency of LCL filter	f_r	1613 Hz
Grid voltage	V_g	220 Vrms	Amplitude of the triangular carrier	V_{tri}	4.578 V
Fundamental Frequency	f_o	50 Hz	Proportional coefficient of $G_i(s)$	K_p	0.312
Switching frequency	f_{sw}	10 kHz	Resonant coefficient of $G_i(s)$	K_r	50
Inverter-side inductor	L_1	3.2 mH	Feedback coefficient of capacitor-current	H_{i1}	0.7
Filter capacitor	C	10 μF	Grid current senor gain	H_{i2}	1

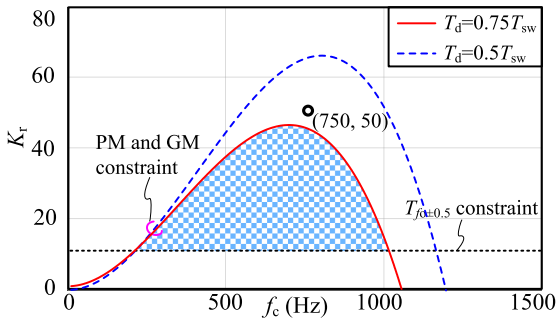

Fig. 12. Satisfactory regions of K_r and f_c constrained by T_{fo}, PM, and GM.

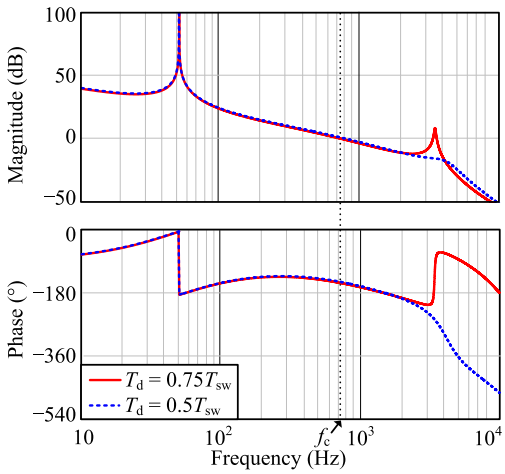

Fig. 13. Bode plots of the current control loop gain $T_{3p}(s)$ with different control delay.

TABLE III
PARAMETERS OF THE SINGLE-PHASE TWO-LEVEL GRID-CONNECTED INVERTER

Parameters	Symbol	Value	Parameters	Symbol	Value
Input voltage	V_{in}	380 V	Grid-side inductor	L_2	230 μH
Rated power	S	6 kVA	Resonant frequency of LCL filter	f_r	3811 Hz
Grid voltage	V_g	220 Vrms	Carrier amplitude	V_{tri}	4.578V
Fundamental frequency	f_o	50 Hz	Proportional coefficient of $G_i(s)$	K_p	0.08
Switching frequency	f_{sw}	10 kHz	Resonant coefficient of $G_i(s)$	K_r	20
Inverter-side inductor	L_1	720 μH	Feedback coefficient of capacitor-current	H_{i1}	0.1
Filter capacitor	C	10 μF	Grid current senor gain	H_{i2}	1

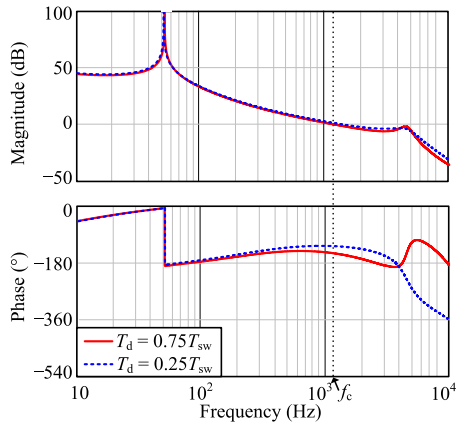

Fig. 14. Bode plots of the current control loop gain $T_{1p}(s)$ with different control delay.

Table III. According to (4) and the parameters given in Table III, the Bode plots of the current control loop of the single-phase grid-connected inverter, $T_{1p}(s)$, with $T_d = 0.75T_{sw}$ and $T_d = 0.25T_{sw}$ can be depicted, respectively, as shown in Fig. 14. As seen, when $T_d = 0.75T_{sw}$, $T_{1p}(s)$ has a pair of RHP poles, yet it has no positive or negative crossing. Thus, the system is unstable according to the Nyquist criterion. When $T_d = 0.25T_{sw}$, the system is also stable, with PM = 59° and GM = 5.2 dB.

VI. EXPERIMENTAL VERIFICATION

A. Experimental Results

The prototypes of a 6-kW three-phase two-level *LCL*-type grid-connected inverter and a 6-kW single-phase full-bridge *LCL*-type grid-connected inverter are fabricated in the laboratory, as shown in Fig. 15. The main parameters of these two inverters are listed in Tables II and III. Both of them

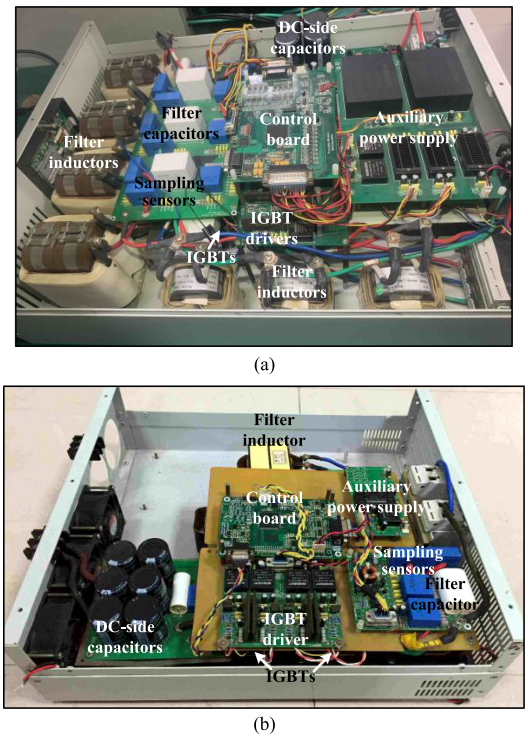

Fig. 15. Photographs of the prototypes of (a) three-phase grid-connected inverter and (b) single-phase grid-connected inverter.

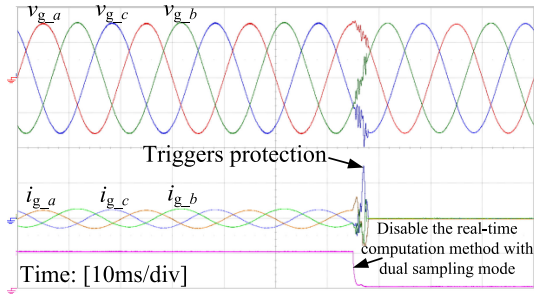

Fig. 16. Experimental waveforms of the three-phase grid-connected inverter with unipolar and double-frequency SPWM. v_{g_x}: 200 V/div and i_{g_x}: 50 A/div.

are implemented with insulated-gate bipolar transistor modules (CM100DY-24NF), which are driven by M57962L. The grid voltages are sensed by voltage halls (LV25-P). The filter capacitor currents and the grid currents are sensed by current halls (LA55-P). All the signals are sampled by 14-bit A/D converters (MAX1324-ECM), and the proposed control scheme is performed in a DSP (TMS320F2812). Meanwhile, a programmable ac source (Chroma 6590) is used to simulate the grid.

Fig. 16 shows the experimental waveforms of the three-phase grid-connected inverter. As observed, when the real-time computation method with the dual-sampling mode is enabled, the control delay is $0.5T_{sw}$ and the grid current is stable. Once

$$K_{r\_SM}(f_c) = \frac{2\pi^2 f_c^2 (L_1 + L_2)}{\omega_i H_{i2} K_{PWM}} \frac{2\pi L_1 (f_r^2 - f_c^2) \cos(PM + 2\pi f_c T_d) - K_{PWM} H_{i1\_GM}(f_c) \sin(PM) f_c}{2\pi L_1 (f_r^2 - f_c^2) \sin(PM + 2\pi f_c T_d) + K_{PWM} H_{i1\_GM}(f_c) \cos(PM) f_c} \quad (17)$$

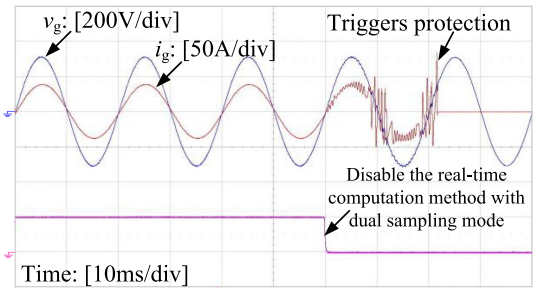

Fig. 17. Experimental waveforms of the single-phase grid-connected inverter with unipolar and double-frequency SPWM.

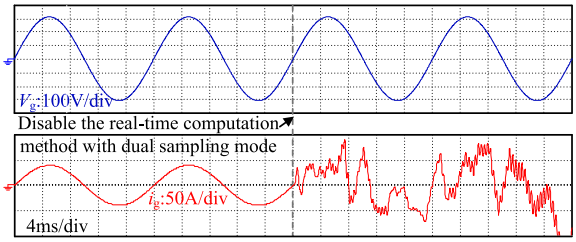

Fig. 18. Simulation waveforms of the capacitor-clamped three-level grid-connected inverter with level-shifted SPWM.

TABLE IV
PARAMETERS OF THE SINGLE-PHASE THREE-LEVEL GRID-CONNECTED INVERTER

Parameters	Symbol	Value	Parameters	Symbol	Value
Input voltage	V_{in}	380 V	Grid-side inductor	L_2	60 μH
Rated power	S	6 kVA	Resonant frequency of LCL filter	f_r	7502 Hz
Grid voltage	V_g	220 Vrms	Carrier amplitude	V_{tri}	4.578V
Fundamental frequency	f_o	50 Hz	Proportional coefficient of $G_i(s)$	K_p	0.0675
Switching frequency	f_{sw}	10 kHz	Resonant coefficient of $G_i(s)$	K_r	9
Inverter-side inductor	L_1	180 μH	Feedback coefficient of capacitor-current	H_{i1}	0.08
Filter capacitor	C	10 μF	Grid current senor gain	H_{i2}	1

the sampling mode is changed to the synchronous sampling method, the control delay increases to $0.75T_{sw}$ and the system becomes unstable. Fig. 17 shows the experimental waveforms of the single-phase grid-connected inverter. As seen, once the real-time computation method with the dual-sampling mode is disabled, the grid current oscillates soon and triggers protection. The experimental results shown in Figs. 16 and 17 agree with the stability analysis in Section V and verify the effectiveness of the proposed method.

B. Simulation Results of the Multilevel Grid-Connected Inverters

Simulation is performed with MATLAB/Simulink using a capacitor-clamped three-level inverter grid-connected inverter. The main parameters are given in Table IV; nevertheless, the detailed design procedure is not given due to page limits.

Fig. 18 shows the simulation results. The inverter is connected to a stiff grid, and the grid voltage remains sinusoidal. As seen, the grid current oscillates immediately once the real-time computation method with the dual-sampling mode is disabled. The simulation results verify the effectiveness of the proposed method in multilevel grid-connected inverters.

VII. CONCLUSION

This article first illustrated the generating mechanism of control delay, including computation delay and PWM delay, in a digitally controlled grid-connected inverter. By choosing suitable sampling mode and adjusting the modulation wave update instant, a generalized real-time computation method with the dual-sampling mode was derived to directly eliminate the computation delay, based on an $(n+1)$-level phase-leg. Then, the operation principles of this method for the three- and single-phase inverters with two- and multilevel topologies were elaborated. Besides, this article analyzed the improvements of current control performance with reduced control delay. Finally, the theoretical analysis and the effectiveness of the proposed method were verified by the experimental and simulation results.

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