

Systematic Design of a 100-W 6.78-MHz Wireless Charging Station Covering Multiple Devices and a Large Charging Area

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Abstract—This article details the systematic design of a 100-W multiload wireless charging station. The station provides positional flexibility for the receivers, exhibits limited cross-channel disturbance, and has high efficiency. The positional flexibility is achieved using a transmitter coil design approach, which uses interleaved windings and controlled coil geometry to shape the magnetic field. The limited cross-channel disturbance is realized with an impedance network, which maintains a constant transmitter coil current. A holistic system-level modeling and design method is proposed to design the entire system for maximum efficiency. The first step is decoupling each stages using parameterized source and/or load of adjacent stages, and optimize internally for minimum loss, which leads to a reduced design space. The second step is system-wide optimization, which addresses power loss interdependence. A 100-W, 6.78-MHz experimental system with a $0.5 \times 0.5 \text{ m}^2$ transmitter coil is demonstrated. The measured magnetic field variation on the charging surface is 15.9%. And the system shows no cross-channel disturbance when charging two 50-W receivers. The measured dc-to-dc efficiency is 92.8%.

Index Terms—Constant coil current, multiload, systematic design, uniform magnetic field, wireless power transfer (WPT).

I. INTRODUCTION

FOR consumer electronics, inductive wireless power transfer (WPT) is revolutionizing the way users interact with their devices. Prolific, seamless charging is promising to reduce onboard battery storage requirements and untether mobile devices from periodic wired charging requirements. At present, commercial implementations of WPT operating at 20–200 kHz range are largely limited to a charging pad where each device must be well-aligned to a dedicated position. Designing spatial freedom and thought-free ubiquitous charging platform covering multiple devices is still challenging.

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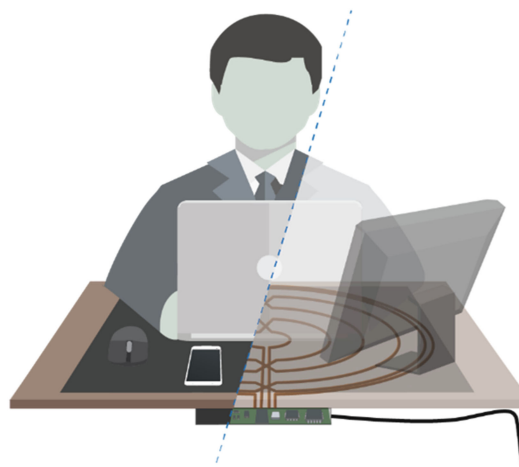


Fig. 1. Schematic of the target application, where the transmitter coil is placed on the bottom side of a large table.

A schematic of the target application is shown in Fig. 1. This arrangement models applications, such as a wireless charging desk or table. In the application, multiple electronic devices with built-in receiver coils may be placed arbitrarily on a planar charging surface parallel to the transmitter coil but a fixed distance away. Due to the physical extents of the electronic device, the built-in receiver coil sizes are substantially smaller than the transmitter coil, therefore exhibiting low coupling. Additionally, nearby metals in the receiver cases or foreign objects may exhibit significant eddy current heating at low frequencies [1].

General requirements for the multiload platform include charging flexibility and high efficiency. To achieve the desired flexibility, the WPT system must be designed with limited impact from spatial positioning of the receivers and exhibit limited cross-channel disturbance. In one possible design approach, these requirements are met when the following design constraints are satisfied.

- 1) The transmitter coil design results in a constant flux coupled to the receiver independent of spatial positioning.
- 2) The transmitter power stage design achieves a constant coil current amplitude independent of load impedance.

Previous research efforts achieving the first constraint are classified into two categories: new transmitter coil structures [2], [3] and optimizing the geometric construction of conventional

coils [4]. In [2] and [3], coil arrays are used to achieve magnetic field uniformity. The overall magnetic field is shaped by controlling the amplitude and phase of the current in each small coil using digitally controlled converters. This method, however, requires multiple converters and a complicated control strategy. In [4], geometric optimization is applied to shape the magnetic field distribution, eliminating the need for coil current control. However, this method increases the number of turns in the coil to reduce magnetic field variation, leading to a wire length that potentially approaches one-fourth wavelength at the system operating frequency, causing radiation and low-efficiency problems [5]. To achieve small flux variation with limited wire length, Kim *et al.* [6] report a coil with parallel turns to allow variable currents in each turn. The small flux variation is achieved through designing the geometric positions and current ratio of each turn simultaneously. The wire length is constrained through paralleling of adjacent turns. However, it is not reported how to design the coil, e.g., the coil geometry, inductance, or the magnetic field, in a WPT system.

To achieve the second design constraint, constant coil current can be achieved utilizing a closed-loop-controlled power stage to regulate the coil current [7], which requires complex sensing, communication, and controller design. Alternately, Jiang and Costinett [8] use an immittance network [9], which significantly reduces the variation in coil current resulting from changing loads without any additional sensing or control. However, previous literature has not examined constant-current impedance matching network (IMN) design in the context of a complete system optimization, including the interdependence between IMN parameters, inverter soft switching, transmitter coil magnetic field, receiver-induced voltage, and rectifier design.

Besides charging flexibility, high system-level efficiency is another key requirement of a WPT system. The overall power loss in a WPT system consists of converter power loss and coil conduction loss. The converter switching loss is significantly reduced using soft switching techniques [7], [10], [11], leaving the conduction loss as the dominant component of the total WPT system loss [11], [12]. In this case, the maximum achievable efficiency η_{\max} of a WPT system is determined by the coil quality factor Q and coupling coefficient k , $\eta_{\max} \approx 1 - 2/(kQ)$ [7], [12], [13]. Thereby, the traditional WPT system design methods use a sequential design approach that first iterates coil geometries to achieve the highest coil quality factor and coupling, then controls converters to an operating point, which presents an optimal loading to the coils to maximize efficiency [7], [10], [11]. This approach neglects the impact of power converter losses, and is not easily adaptable to the multireceiver design goals in this application. Reviewing the literature, although functional performance of individual stages is reported in isolation, no systematic approach has been presented that codesigns all stages as a complete multiload charging station, to achieve the desired flexibility and high efficiency. Therefore, this article focuses on the systematic design method to achieve the desired charging flexibility and high power conversion efficiency.

The rest of this article is organized as follows. In Section II, the multiload WPT system structure is presented. Due to the complexity, direct iteration design of the entire system, including

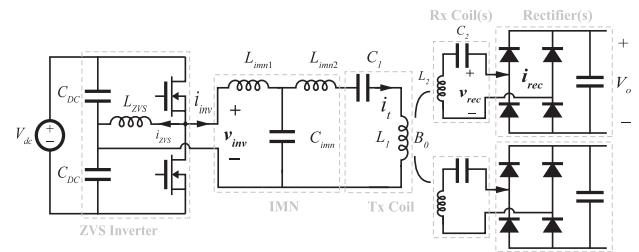


Fig. 2. Circuit schematic of the multiload WPT system, including inverter, IMN, transmitter and receiver coils, rectifiers, and dc load.

coil physical geometries, may be infeasible. Thus, each stage of the WPT system is first decoupled from adjacent stages to form subsystem models, parameterized using sources and/or loads. Sections III–VII model and locally optimize the parameterized subsystems. Then, the subsystem models are combined into system-wide optimization in Section VIII, which addresses power loss interdependence. An example 100-W, 6.78-MHz multiload wireless charging system is designed and prototyped in Section IX. Finally, Section X concludes this article.

II. SYSTEM STRUCTURE AND MODELING

The equivalent circuit of the multiload application is shown in Fig. 2, operating from a dc supply to two identical receivers. The transmitter (Tx) side consists of a high-frequency ZVS Class-D inverter, a passive IMN, and a transmitter coil with a uniform magnetic field and series resonant compensation. The receiver (Rx) side consists of a diode rectifier, a receiver coil, and a resonant capacitor that compensates the Rx side reactance. The transmitter and the receivers are coupled through the B -field. Diode rectifiers are used as opposed to synchronous rectifiers, which potentially reduce diode loss at the cost of size and control complexity [14].

The specifications of the multiload charging station include the total output power $P_{o,all}$ needed to charge the devices, the table thickness h across which the power is transmitted, and the geometrical size for the transmitter and receiver coils. In the application, the table thickness is measured to be 1.7 cm. The size of receivers is designed to fit the base of a computer monitor with a size of 8.5×5 in². To offer positional charging flexibility, the B -field must have minimal variation over the charging area for a near-constant induced voltage independent of receiver position. The system operates at 6.78-MHz frequency. The maximum B -field above the table is limited to $27 \mu\text{T}$ according to ICNIRP 2010 [15]. In this article, the input dc voltage is assumed to be 200 V to work with a front-end PFC [16]. The Rx side maximum output ac voltage is 40 V for the two 50-W receivers. This corresponds to a dc voltage limit of $V_o < (\frac{\pi}{4})40 = 31.5$, which is left variable for the system optimization, assuming the receivers have subsequent power conversion stages that can accommodate a variable dc voltage. The specifications of an example wireless charging station, which will be used for the analysis and design in this article, are given in Table I.

Before proceeding to the system-level design, each of the stages, corresponding to the dashed lines in Fig. 2, are examined

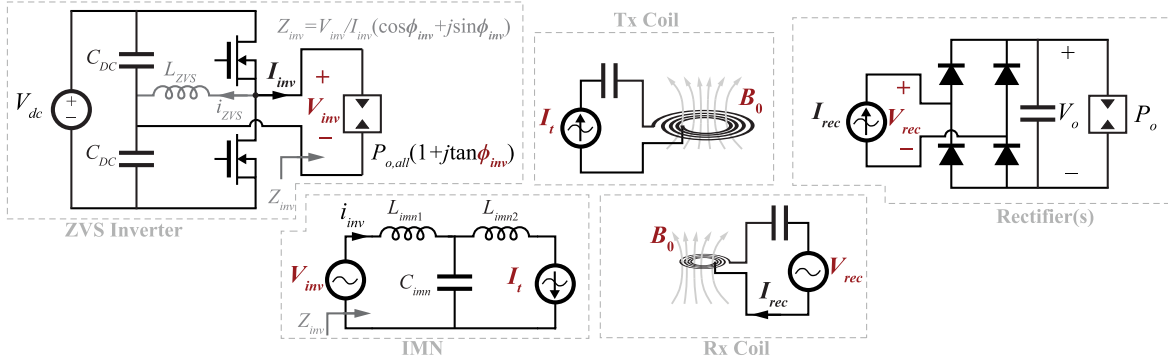


Fig. 3. Decoupled circuit model showing the parameters that couple adjacent stages and the parameters inside an individual stage.

 TABLE I
 SPECIFICATIONS OF THE DESIRED WPT STATION

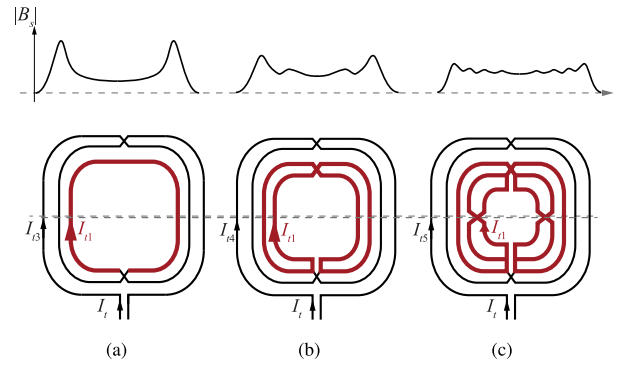
| Parameters | Variable | Value |
|--------------------------|-------------|---------------------------|
| Total output power | $P_{o,all}$ | 100 W |
| Table thickness | h | 1.7 cm |
| Size of Tx coil | - | 50x50 cm ² |
| Size of Rx coils | - | 21.6x12.7 cm ² |
| Magnetic field variation | κ | 30 % |
| System frequency | f_s | 6.78 MHz |
| Input voltage | V_{dc} | 200 V |
| Output voltage limit | V_o | 31.5 V |

individually, as shown by the equivalent circuit in Fig. 3. Fundamental harmonic analysis is used when analyzing the circuit. In the design process, the load of each stage equals the total output power assuming the system exhibits high efficiency. Although each stage is now able to be analyzed individually, the operation of each is coupled through the highlighted input/output variables in Fig. 3. Thus, e.g., the transmitter coil can be optimized for a given combination of coil current and average flux density, $[I_t, B_0]$, the final selection of these two parameters requires system-level consideration as they affect the performance of adjacent stages.

Each stage is designed first in isolation, resulting in an optimized design that is parameterized by the highlighted coupling variables of Fig. 3. Then, each of these parameterized designs is combined in a system-level optimization to select the optimal value of the coupling variables for the system-level performance, as detailed in Section VIII.

III. TRANSMITTER COIL MODELING

The large, 50×50 cm² area, transmitter coil is desired for positional flexibility. Due to the large area of the coil and high, 6.78-MHz frequency, large-reactance, and therefore high- Q coil designs are possible. However, the large area also constrains the design. The outer perimeter of the Tx coil is 2 m, which is comparable to the 11-m quarter-wavelength at 6.78 MHz. To meet design goals while maintaining negligible radiation, the main principle of the transmitter coil design is to use paralleled windings to increase the coverage of the winding area without requiring a higher number of turns, as illustrated in Fig. 4. Fig. 4(a) shows a conventional three-turn, symmetric coil with


 Fig. 4. Conventional three-turn coil (a) with innermost turn highlighted; (b) modified three-turn coil with two parallel windings for the innermost turn; and (c) modified three-turn coil where the innermost parallel winding has been further split into two parallel windings. Above each coil is a qualitative depiction of the B -field produced by the coil along the dashed line, some distance above the coil.

the innermost turn highlighted. The current in each of the three turns is identical and equal to the input current amplitude I_t , $i_t = [1, 1, 1]I_t$. In Fig. 4(b), this innermost turn has been split into two parallel windings. To facilitate equal current sharing in each parallel turn, the length and impedance of each turn are equalized by swapping the turns at their halfway point, shown at the top of the figure. If the impedances are perfectly balanced, the currents in each turn are now $i_t = [0.5, 0.5, 1, 1]I_t$, from innermost to outermost. In Fig. 4(c), the innermost paralleled turn from Fig. 4(b) is further split into two parallel and impedance-balanced turns. If the impact of the crossover points is negligible, the resulting coil magnetic field is equivalent to a five-turn coil, with currents $i_t = [0.25, 0.25, 0.5, 1, 1]I_t$ in each turn, but each complete current loop through the coil encompasses only three turns. This coil is described as having $n = 5$ physical turns and $N_{eq} = 3$ effective turns.

The qualitative B -field depiction of each coil at a receiver surface a distance h above the transmitter coil is shown at the top of Fig. 4. As winding effective turns are split into a higher number of physical turns covering the coil area, the field can be designed with greater uniformity.

To model the interleaved coil, both the geometric parameters and current distribution are necessary. The half-length, i.e., the radius of the maximal circle that can be circumscribed within

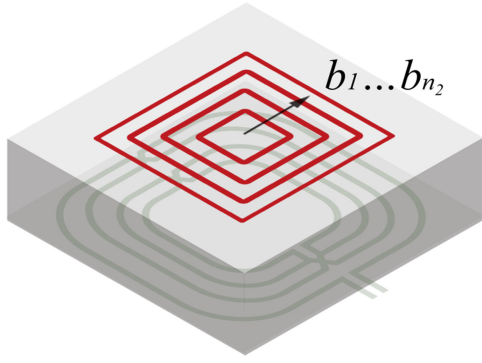


Fig. 5. Schematic showing the transmitter coil and the centrally located square on the charging surface for evaluating mutual inductance.

the square turn, is $a_{tx} = [a_1, \dots, a_n]$, where a_i is the half-length of (i)th turn. The current ratio, which describes the interleaving method, is $\lambda = [I_{t1}, \dots, I_{tn}]/I_t$, where λ_i is the ratio of (i)th turn.

A. Magnetic Field Analysis

The target charging surface has a distance h above from the transmitter and covers 90% of the extents of the transmitter coil. The calculated B -field is used to assess the field uniformity of each candidate coil design. As shown in Fig. 5, n_2 centrally located square loop with half-length of b_1, \dots, b_{n_2} is evenly distributed over the charging surface. b_i is the half-length of (i)th turn. The magnetic flux in the (i)th loop is

$$\Phi_i = \sum_{j=1}^n \lambda_j M_{j,i} I_t \quad (1)$$

where $M_{j,i}$ is the mutual inductance between the (i)th loop and the j th turn of the transmitter coil [17]

$$\begin{aligned} M_{j,i} = & \frac{\mu_0}{2\pi} \left[2\sqrt{(a_j + b_i)^2 + (a_j + b_i)^2 + h^2} \right. \\ & - 2\sqrt{(a_j + b_i)^2 + (a_j - b_i)^2 + h^2} \\ & - (a_j + b_i) \arctan \left(\frac{a_j + b_i}{\sqrt{(a_j + b_i)^2 + (a_j + b_i)^2 + h^2}} \right) \\ & + (a_j - b_i) \arctan \left(\frac{a_j - b_i}{\sqrt{(a_j + b_i)^2 + (a_j - b_i)^2 + h^2}} \right) \\ & + (a_j + b_i) \arctan \left(\frac{a_j + b_i}{\sqrt{(a_j + b_i)^2 + (a_j - b_i)^2 + h^2}} \right) \\ & \left. - (a_j - b_i) \arctan \left(\frac{a_j - b_i}{\sqrt{(a_j - b_i)^2 + (a_j - b_i)^2 + h^2}} \right) \right] \quad (2) \end{aligned}$$

The averaged B -field in the charging region is calculated by the flux in the outermost loop over its area

$$B_0 = \frac{\Phi_i}{4b_{n_2}^2} = \frac{I_t}{4b_{n_2}^2} \sum_{j=1}^n \lambda_j M_{j,n_2}. \quad (3)$$

The averaged B -field per unit input current is

$$\psi_0 = \frac{B_0}{I_t} = \frac{1}{4b_{n_2}^2} \sum_{j=1}^n \lambda_j M_{j,n_2}. \quad (4)$$

The magnetic flux in the strip region between (i)th and ($i+1$)th loop is $\Phi_{\text{strip},i} = \Phi_{i+1} - \Phi_i$. The averaged B -field in the strip region is

$$B_{\text{strip},i} = \frac{\Phi_{i+1} - \Phi_i}{4(b_{i+1}^2 - b_i^2)}. \quad (5)$$

When $(b_{i+1} - b_i)$ is small, $B_{\text{strip},i}$ is approximately equal to the point-by-point B -field along the arrow shown in Fig. 5. The qualitative B -field variation is

$$\kappa = \frac{\max_i (B_{\text{strip},i}) - \min_i (B_{\text{strip},i})}{\frac{1}{n_2} \sum_i B_{\text{strip},i}}. \quad (6)$$

B. Electric Field Compensation

In addition to a uniform magnetic field at the receiver surface, it is desirable to have minimal electric field generated by the coil. The electric field has the potential to generate an additional dielectric loss in the material that the coil is mounted within (e.g., a desk or table surface), and may cause EMI or safety concerns for objects placed on the charging surface. The electric field is generated due to the longitudinal voltage drop across the coil and may be reduced through distributing the series compensation capacitor into multiple discrete parts over the length of the coil [18]. Although the total longitudinal voltage drop is unchanged, the electric potential between any point on the coil and an external reference (e.g., a dc rail of the transmitter voltage supply) is reduced over the length of the coil.

In this section, it is assumed that adding two discrete capacitors for each equivalent turn is sufficient to compensate for the electric field. One capacitor is placed at the middle of the equivalent turn to compensate for the first half of the longitudinal voltage drop and the one is placed at the end to compensate for the other half. An impedance-based method is used to calculate the voltage drop of each effective turn and the discrete capacitance value, which fully compensates the voltage drop. It should be noted that within one interleaved pair, there is minimal electric field between adjacent turns due to the near-identical impedance and longitudinal voltage change.

When the (i)th effective turn has no subturns, its longitudinal voltage is

$$V_{t,i} = \omega_s I_t L_{mm} \quad (7)$$

where ω_s is the angular switching frequency. L_{mm} is the self-inductance of the m th physical turn in the (i)th effective turn, calculated by [19]

$$L_{mm} = 0.002 l_m \left(\ln \left(\frac{l_m}{r_0} \right) - 1 + 0.25\mu_0 + \frac{r_0}{l_m} \right) \quad (8)$$

where l_m is the perimeter of the m th physical turn in the (i)th effective turn and r_0 is the wire radius.

When the (i)th effective turn has interleaved subturns, including the $s_1^{\text{th}}, \dots, s_n^{\text{th}}$ physical turns, the voltage of (i)th effective turn is

$$V_{t,i} = \omega_s I_t \sum_{m=s_1}^{s_n} \left(\lambda_m^2 L_{mm} + \sum_{j=1, j \neq m}^n \lambda_j \lambda_m M_{jm} \right) \quad (9)$$

where M_{jm} is the mutual inductance between the m th and j th physical turn. M_{jm} is calculated from (2), replacing b_i with a_m .

To fully compensate for the longitudinal voltage change of (i)th equivalent turn, the capacitance value of the two identical discrete capacitors is

$$C_{t,i} = \frac{2I_t}{V_{t,i}\omega_s}. \quad (10)$$

The equivalent capacitance of all the distributed compensation capacitors is

$$C_1 = \frac{1}{2 \sum_{i=1}^{N_{eq}} \frac{1}{C_{t,i}}}. \quad (11)$$

C. Transmitter Coil Loss Model

With electric field compensation, the power loss in the dielectric base is assumed to be nearly zero. The remaining power loss in the transmitter coil consists of copper loss and compensation capacitor loss. The copper ESR is determined by both coil geometry and the interleaving method

$$R_{tx,copper} = \sum_{i=1}^n \frac{8\lambda_i^2 \rho a_i}{\pi (r_0^2 - (r_0 - \delta)^2)} \quad (12)$$

where ρ is the copper resistivity, and $\delta = 1/\sqrt{\mu_0 \rho f_s} \ll r_0$ is the skin depth at switching frequency f_s .

The total compensation capacitors' ESR is estimated by

$$R_{tx,cap} = 2 \sum_{i=1}^{N_{eq}} \frac{t_g}{\omega_s C_{t,i}} \quad (13)$$

where t_g is the loss tangent of the capacitor dielectric material indicated in the datasheets by the manufacturer [20]. In high-frequency applications, NP0 capacitors are used for stable capacitance and small ESR.

Combining copper and compensation capacitor ESR, the total ESR is $R_1 = R_{tx,copper} + R_{tx,cap}$. And the power loss in the transmitter coil is

$$P_{loss,tx} = 0.5 I_t^2 \left(\sum_{i=1}^n \frac{8\lambda_i^2 \rho a_i}{\pi (r_0^2 - (r_0 - \delta)^2)} + 2 \sum_{i=1}^{N_{eq}} \frac{t_g}{\omega_s C_{t,i}} \right). \quad (14)$$

D. Transmitter Coil Design

To design the coil, the number of turns N_{eq} is swept from 2 to 4; each effective turn is allowed to be implemented as a single turn, $\lambda = [1]$, two parallel turns, $\lambda = [0.5, 0.5]$, or three turns with $\lambda = [0.25, 0.25, 0.5]$; and the possible position for each turn a_i ranges from 1 to 25 cm with a 0.5-cm step, except

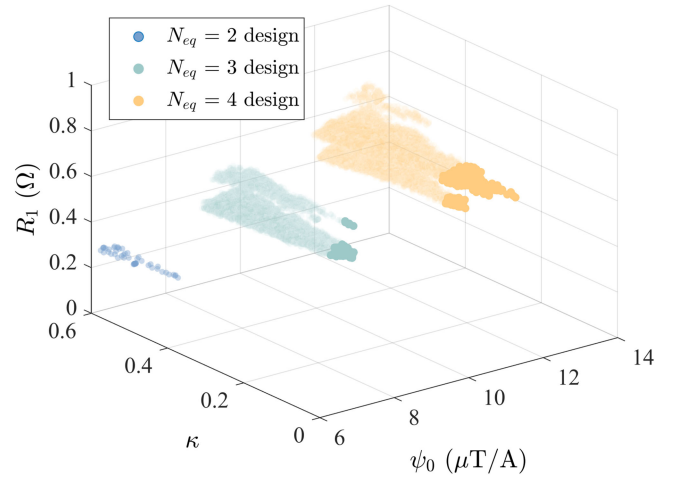


Fig. 6. Transmitter coil characteristics after iteration. For each N_{eq} , designs shown with lighter color exceed κ limit.

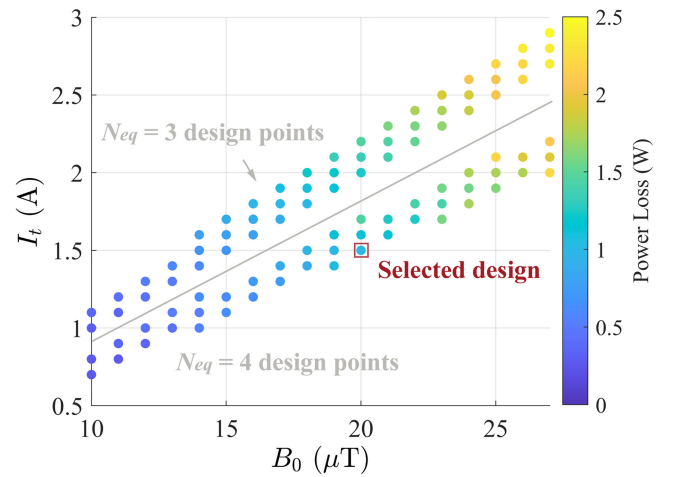


Fig. 7. Transmitter coil power loss, including the wire conduction loss and compensation capacitors loss.

for the outermost turn, which is fixed at 25 cm. At 6.78 MHz, the skin depth of copper is 25 μm ; Litz wire with sufficiently small strand gauge for this frequency has limited availability and is expensive [21]. AWG 12 solid copper wire is used in the design as it was found to exhibit sufficiently low resistance while still being small enough to be easily bent to the designed shape. As N_{eq} , a_{tx} , and λ are simultaneously swept, the resulting candidate coil performance (κ , ψ_0 , and R_1) are shown in Fig. 6.

Designs with κ larger than application requirements are discarded. For the remaining designs, the required I_t needed to generate a target B_0 is calculated using (3) and (4), and $P_{loss,tx}$ is calculated afterward using (14). Only designs with minimum power loss at any point are saved. The resulting candidate coil designs are shown in Fig. 7. The optimized designs form two strips for $N_{eq} = 3$ and $N_{eq} = 4$.

The final selection of B_0 and I_t , and therefore the coil geometry, is determined during the system-level optimization to capture the dependence of adjacent stages on B_0 and I_t . The final design, selected in Section VIII, is marked in Fig. 6.

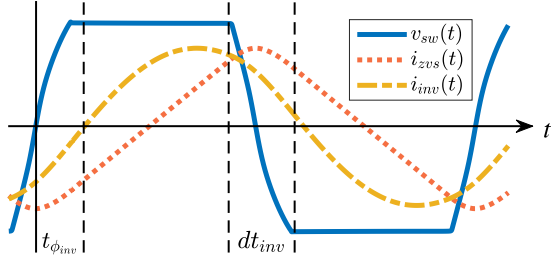


Fig. 8. Waveform of the ZVS inverter showing the output voltage and current.

Note that the selected design is not the minimum power loss transmitter coil, but is the transmitter coil that will result in minimum system-wide power loss. The model-based, geometric and current distribution optimization leads to the low loss coil design.

IV. ZVS INVERTER MODELING

The inverter schematic is shown in Fig. 3. At 6.78 MHz, it is critical to ensure the ZVS of inverter devices for safe operation. An auxiliary inductor L_{ZVS} may be added to the output for designs where the load current is not sufficient to obtain ZVS. The inductance is designed so the inverter achieves ZVS via the combination of i_{inv} and i_{zvs} .

Typical ZVS inverter waveforms are shown in Fig. 8, where dt_{inv} is the deadtime, ϕ_{inv} is the phase angle between the fundamental components of v_{inv} and i_{inv} , and $t_{\phi_{inv}} = \phi_{inv}(\frac{T_s}{2\pi})$.

v_{inv} is approximately trapezoidal

$$v_{inv}(t) = \begin{cases} V_{dc} \left(\mp 1 \pm \frac{2t}{dt_{inv}} \right) & , (0 \leq t \leq dt_{inv}) \\ \pm V_{dc} & , (dt_{inv} \leq t \leq T_s/2). \end{cases} \quad (15)$$

The fundamental component V_{inv} is extracted from v_{inv} using Fourier analysis

$$V_{inv} = \frac{2}{T_s} \sqrt{\left(\int_0^{T_s} v_{inv} \sin(\omega_s t) dt \right)^2 + \left(\int_0^{T_s} v_{inv} \cos(\omega_s t) dt \right)^2}. \quad (16)$$

During the ZVS transition, both i_{zvs} and i_{inv} flow through the output capacitors of the transistors simultaneously. When the auxiliary inductor is designed to achieve ZVS without diode conduction, the transition is described by

$$Q_{oss,inv} = \int_0^{dt_{inv}} (i_{zvs}(t) + i_{inv}(t)) dt \quad (17)$$

where $Q_{oss,inv}$ is the output charge of one phase leg when blocking V_{dc} , and $C_{oss,inv} = Q_{oss,inv}/V_{dc}$ is the equivalent output capacitance calculated from the nonlinear, voltage-dependent capacitance [22] from the device datasheet

$$C_{oss,inv} = \int_0^{V_{dc}} C_{oss}(V) dV. \quad (18)$$

During the ZVS transition, i_{zvs} is given by (19). where $\omega_z = 1/\sqrt{L_{ZVS}C_{oss,inv}}$, $\beta = dt_{inv}f_s\pi$ is half of the transient time in radians, and I_{inv} is amplitude of i_{inv} . The solutions for

$I_0 = i_{zvs}(0)$ is given by (20)

$$\begin{aligned} i_{zvs}(t) = & I_0 \cos\left(\omega_z t + \frac{\omega_z}{\omega_s}(\beta - \phi_{inv})\right) \\ & + C_{oss,inv} V_{dc} \omega_z \sin\left(\omega_z t + \frac{\omega_z}{\omega_s}(\beta - \phi_{inv})\right) \\ & + \frac{I_t}{\left(\frac{\omega_s^2}{\omega_z^2} - 1\right)} \left[\cos\left(\omega_z t + \frac{\omega_z}{\omega_s}(\beta - \phi_{inv})\right) \sin(\phi_{inv} - \beta) \right. \\ & \left. + \frac{\omega_s}{\omega_z} \sin\left(\omega_z t + \frac{\omega_z}{\omega_s}(\beta - \phi_{inv})\right) \right] \quad (19) \\ I_0 = & \frac{1}{1 + \cos(\omega_z dt_{inv})} \left[\frac{V_{dc}}{2L_{ZVS}} \left(\frac{T_s}{2} - dt_{inv} \right) \right. \\ & - \frac{V_{dc}}{2} \sqrt{\frac{C_{oss,inv}}{L_{ZVS}}} \sin(\omega_z dt_{inv}) + \frac{I_{inv}}{L_{ZVS}C_{oss,inv}\omega_s^2 - 1} \\ & (\sin(\omega_s dt_{inv} + \phi_{inv} - \beta) - \cos(\omega_z dt_{inv}) \sin(\phi_{inv} - \beta) \\ & \left. - \frac{\omega_s}{\omega_z} \sin(\omega_z dt_{inv}) \cos(\phi_{inv} - \beta) \right] \quad (20) \end{aligned}$$

A. Inverter Loss Model

The inverter is designed for full ZVS with no reverse conduction. The inverter power loss consists of three parts: the conduction loss on the switches P_{ds} , the output capacitance hysteresis loss under ZVS condition $P_{ZVS,Coss}$ [23], and the auxiliary inductor loss P_{tank}

$$P_{loss,inv} = P_{ds} + P_{ZVS,Coss} + P_{tank}. \quad (21)$$

The conduction loss in the transistors is

$$P_{ds} \approx I_{m,rms}^2 R_{ds} \quad (22)$$

where R_{ds} is the ON-resistance of one transistor and $I_{m,rms}$ is the rms value of $(i_{inv} + i_{zvs})$. $P_{ZVS,Coss}$ is [24]

$$P_{ZVS,Coss} = 4.5 \times 10^{-11} \frac{C_{oss}}{C_{ref}} \left(\frac{V_{dc}}{650} \right)^{1.6} f_s^{1.6} \quad (23)$$

where C_{ref} is the output capacitance of the reference device in [24]. The remaining loss mechanism P_{tank} is determined by the physical inductor design.

B. Inductor Design and Loss Model

P_{tank} consists of copper loss P_{wire} and core loss P_{core} , which are calculated under specified L_{ZVS} . In this article, a T-68 iron powder toroid core [25] is used to fit in the target application. Iron powder is commonly used in RF applications and has low core loss.

To achieve a specified L_{ZVS} , the number of turns N_z is [25]

$$N_z = \sqrt{\frac{L_{ZVS}}{k_z}} \quad (24)$$

where k_z is an empirical coefficient provided by the manufacturer datasheet.

The length of wire l_{zw} is

$$l_{zw} = \text{MLT} \cdot N_z \quad (25)$$

where MLT is the mean length per turn of the core.

Considering the operating frequency, solid copper wire is used [21] with an outer radius $r_{z,0}$. The effective conduction area A_{ac} is, assuming $r_{z,0} \gg \delta$

$$A_{ac} = (r_{z,0}^2 - (r_{z,0} - \delta)^2). \quad (26)$$

Combining l_{zw} and A_{ac} , the copper ESR is

$$R_{ZVS,wire} = \frac{\text{MLT} \rho_{cu} \sqrt{\frac{L_{ZVS}}{k_z}}}{(r_{z,0}^2 - (r_{z,0} - \delta)^2)}. \quad (27)$$

The wire ESR decreases when $r_{z,0}$ increases. Thus, for each L_{ZVS} , the thickest wire is preferred for minimum ESR. When the gap between adjacent wire is l_{gap} , the maximum wire radius is

$$r_{z,m} = \frac{2\pi r_{z,in} - N_z l_{gap}}{2(N_z + \pi)} \quad (28)$$

where $r_{z,in}$ is the inner radius of the T-68 core provided by the manufacture datasheet.

The final selection of $r_{z,0}$ depends on $r_{z,m}$ and the closest available AWG diameter.

The inductor current i_{ZVS} is approximated as a triangular wave when calculating the copper loss, which is valid for $dt_{inv} \ll \frac{T_s}{2}$ [11]. The peak value of i_{ZVS} is

$$I_{ZVS,pk} = \frac{V_{dc}}{8L_{ZVS}f_s}. \quad (29)$$

Combining (27) and (29), the power loss in the wire is

$$P_{wire} = \frac{1}{3} \cdot \left(\frac{V_{dc}}{8L_{ZVS}f_s} \right)^2 \frac{\rho_{cu} \text{MLT} \sqrt{\frac{L_{ZVS}}{k_z}}}{\pi (r_{z,0}^2 - (r_{z,0} - \delta)^2)}. \quad (30)$$

The core loss is calculated using the empirical equation provided by the manufacturer [25]

$$P_{core} = \left(\frac{f}{\frac{4 \times 10^9}{B^3} + \frac{3 \times 10^8}{B^{2.3}} + \frac{2.7 \times 10^6}{B^{1.65}}} + 3 \times 10^{-15} f^2 B^2 \right) V_e \quad (31)$$

where $B = I_{ZVS,pk} L_{ZVS} \cdot 10^8 / (A_e N_z f_s)$ is the magnetic flux density inside the core, A_e is the effective magnetic cross section, and V_e is the core volume.

C. ZVS Inverter Design

The selection of the inverter output voltage V_{inv} and load phase ϕ_{inv} is decided by the system optimization. Thus, the inverter design iterates over the possible transistor selection, dt_{inv} , L_{ZVS} , and inductor implementation to obtain the lowest power loss for any combination of $[V_{inv}, \phi_{inv}]$.

In the example design, dt_{inv} is iterated from 10 to 35 ns. When operating from a 200-V PFC supply [16], V_{inv} ranges from 116 to 126 V. ϕ_{inv} is iterated from resistive load to 60° inductive load. At each point, $[V_{inv}, \phi_{inv}]$, only the design which minimizes power loss is retained. Three GaN transistors with different R_{ds} are

TABLE II
SPECIFICATIONS OF THE GAN SWITCHES

| Part number | R_{ds} (mΩ) | $C_{oss,inv}$ @ V_{dc} (pF) |
|-------------|---------------|-------------------------------|
| GS66506T | 67 | 372 |
| GS66504B | 100 | 211 |
| GS065011 | 150 | 172 |

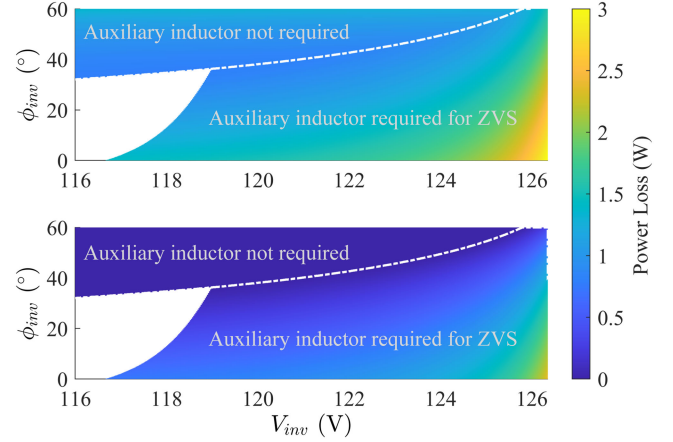


Fig. 9. Inverter power loss design result for GS065011. Top figure is the total inverter loss, and the bottom figure is the auxiliary inductor loss.

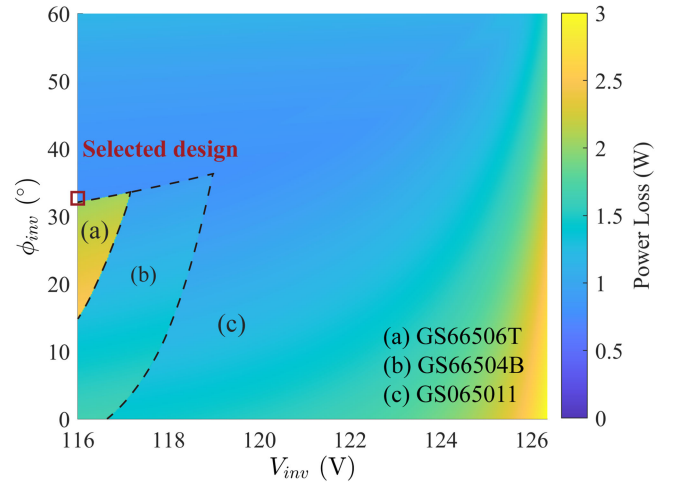


Fig. 10. Optimized inverter power loss with all iterated devices.

analyzed. The characteristics of the transistors are summarized in Table II.

The inverter power loss using GS065011 is shown in Fig. 9. The photograph on the left side is the total loss in the switches and the inductor. The photograph on the right side shows the inductor loss. With more inductive load current, the required auxiliary current and P_{tank} decrease. However, because I_{inv} increases with ϕ_{inv} , P_{ds} may increase, which limits the maximum ϕ_{inv} . The blank region is where the inverter cannot achieve ZVS with the corresponding dt_{inv} .

Combining the three devices, the minimum inverter loss design is shown in Fig. 10. The blank region of the GS065011 plots in Fig. 9 is filled by other devices with larger capacitance.

The final inverter design, resulting from system optimization in Section VIII, is marked by the red box, which minimizes system-wide power loss.

V. IMN MODELING

The IMN and associated parameters are shown in Fig. 3. To achieve a constant magnitude transmitter coil current, L_{imn1} is [8]

$$L_{\text{imn1}} = \frac{V_{\text{inv}}}{I_t}. \quad (32)$$

C_{imn} is designed to compensate L_{imn1}

$$C_{\text{imn}} = \frac{1}{\omega_s^2 L_{\text{imn1}}}. \quad (33)$$

The inverter output impedance is

$$Z_{\text{inv}} = \frac{V_{\text{inv}}}{I_{\text{inv}}} (\cos(\phi_{\text{inv}}) + j \sin(\phi_{\text{inv}})). \quad (34)$$

The reflected load from the receivers is $R_r = 2P_{o,\text{all}} I_t^{-2}$, which typically is much greater than R_1 in a high-efficiency system. Solving the equivalent circuit, the impedance of Z_{imn2} is

$$Z_{\text{imn2}} = \frac{(Z_{\text{inv}} - j\omega_s L_{\text{imn1}})}{1 - (Z_{\text{inv}} - j\omega_s L_{\text{imn1}})(j\omega_s C_{\text{imn}})} - R_r. \quad (35)$$

The imaginary part of Z_{imn2} may range from negative to positive, and thus may be physically implemented as either an inductance or capacitance.

The current in C_{imn} is

$$i_c = -\frac{V_{\text{inv}}(R_{l1} + R_r + Z_{\text{imn2}})}{Z_{\text{inv}} \cdot j\omega_s L_{\text{imn1}}}. \quad (36)$$

A. IMN Design

The IMN couples to both the inverter and transmitter coil design, and is thus dependent on design decisions made in both of the previous sections. Thus, the coupling parameters $[V_{\text{inv}}, \phi_{\text{inv}}, I_t]$ are swept over the same range as in the previous inverter and Tx coil designs. The resulting IMN design space is shown in Fig. 11. In this figure, multiple surfaces for varying V_{inv} are nearly completely overlapped, which indicates that the IMN design is insensitive to the minimal variations in V_{inv} from the inverter design.

To better understand the power loss distribution, a detailed loss breakdown is given in Fig. 12 for an example design with $I_t = 1.5$ A, $\phi_{\text{inv}} = 32^\circ$, and $V_{\text{inv}} = 116$ V. Because L_{imn1} decreases when I_t increases, and I_{inv} remains constant for a given ϕ_{inv} , the power loss in L_{imn1} decreases with I_t . When I_t is greater than 1 A, Z_{imn2} is implemented with an inductor and has an increased power loss. The final selection of IMN design is marked in both figures, resulted from Section VIII. The selected design is not the minimum power loss IMN design but is the design that will result in minimum system-wide power loss.

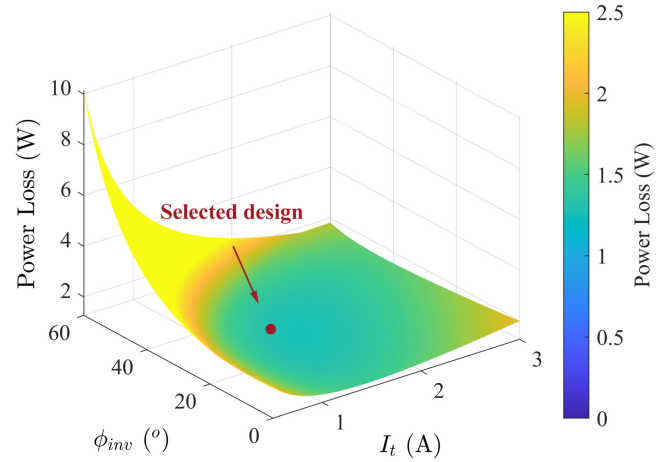


Fig. 11. IMN power loss result. Surfaces with various V_{inv} are shown, but almost fully overlapped.

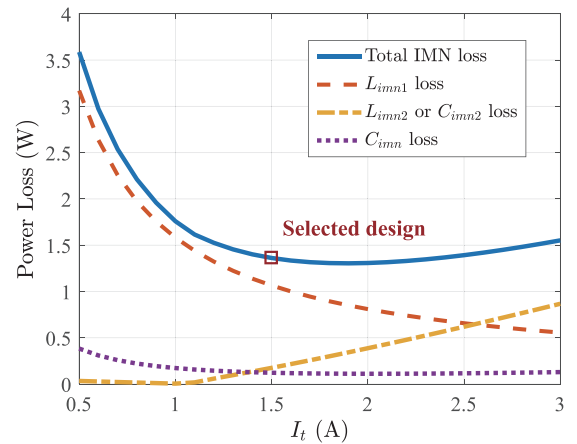


Fig. 12. IMN power loss breakdown at the proposed working point.

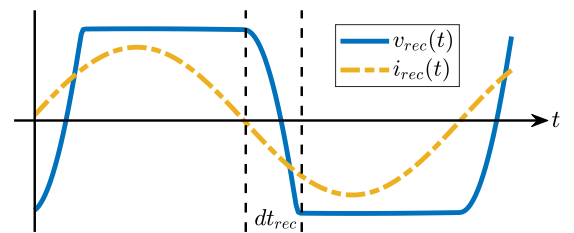


Fig. 13. Waveform of the diode rectifier showing the input voltage and current.

VI. RECTIFIER MODELING

At 6.78 MHz, the transition of the diode rectifier constitutes a significant portion of the overall period and needs to be included in the rectifier model. Typical waveforms of a 6.78-MHz diode rectifier are shown in Fig. 13. i_{rec} is approximated as sinusoidal assuming the series resonance formed by L_2 and C_2 is tuned near the system switching frequency.

One symmetric half-period of operation is divided into two intervals: the switching transition interval and the power delivery interval. During the transition interval, i_{rec} flows through the

parallel capacitances of the reverse-biased diodes

$$Q_{oss,rec} = \int_0^{dt_{rec}} I_{rec} \sin(\omega_s t) dt \quad (37)$$

where dt_{rec} is the transient time, I_{rec} is the amplitude of i_{rec} , and $Q_{oss,rec} = C_{oss,rec} V_o$ is two times the charge stored by a single diode capacitance when blocking V_o . $C_{oss,rec}$ is the equivalent output capacitance at V_o , which is calculated in the same manner as (18).

During the power delivery interval, i_{rec} flows through the forward-biased diodes to the output, delivering an average power

$$P_o = \frac{2}{T_s} \int_{dt_{rec}}^{T_s/2} V_o I_{rec} \sin(\omega_s t) dt \quad (38)$$

with power loss

$$P_{loss,rec} = \frac{4}{T_s} \int_{dt_{rec}}^{T_s/2} V_f I_{rec} \sin(\omega_s t) dt \quad (39)$$

where V_f is the forward voltage drop on each diode. V_f is modeled as the forward voltage v_o and resistance R_d , $V_f(t) = v_o + R_d i_{rec}(t)$. The total input power is the sum of output power and power loss $P_{rec,in} = P_{loss,rec} + P_o$.

Combining (37) and (38)

$$I_{rec} = \frac{\pi P_o + V_o \omega_s Q_{oss,rec}}{2V_o} \quad (40)$$

and

$$v_{rec}(t) = \begin{cases} \mp V_o + 2 \int_0^t \frac{I_{rec} \sin(\omega_s t)}{C_{oss,rec}} dt & , 0 \leq t \leq dt_{rec} \\ \pm V_o \pm 2(v_o + R_d \cdot I_{rec} \sin(\omega_s t)) & , dt_{rec} \leq t \leq \frac{T_s}{2} \end{cases} \quad (41)$$

where the terms with varying signs take on alternating polarity in subsequent half-periods. The fundamental component of v_{rec} is

$$V_{rec} = \frac{2}{T_s} \sqrt{\left(\int_0^{T_s} v_{rec} \sin(\omega_s t) dt \right)^2 + \left(\int_0^{T_s} v_{rec} \cos(\omega_s t) dt \right)^2} \quad (42)$$

The input phase is

$$\phi_{rec} = \arccos \left(\frac{P_{rec,in}}{I_{rec} V_{rec}} \right). \quad (43)$$

Thus, the equivalent impedance of the rectifier Z_{rec} with any specified output is

$$Z_{rec} = \frac{2(P_o + P_{rec})}{I_{rec}^2} \cdot (1 - j \tan(\phi_{rec})). \quad (44)$$

A. Rectifier Design

Because the output power and frequency are constrained by the design specifications, only the output voltage and device selection affect the rectifier design.

B340LB 3-A, 40-V Schottky diodes [26] are selected to implement the two rectifiers. In the rectifier design, V_o is iterated from 10 to 31.5 V according to the application requirement, with a step of 0.5 V. The rectifier characteristics, i.e., I_{rec} , Z_{rec} , and V_{rec} , are calculated for each V_o under nominal load of 50 W. The

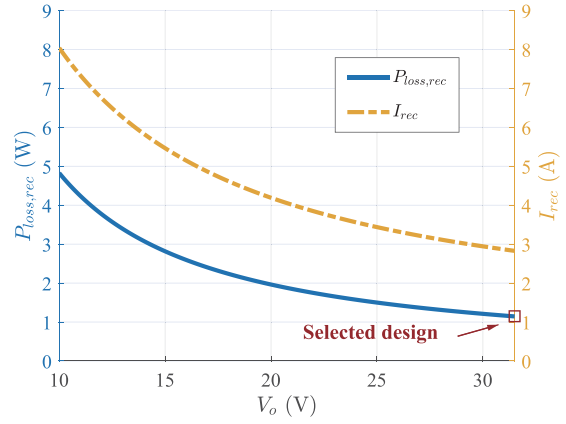


Fig. 14. Rectifier power loss and the required input current when the output power is 50 W.

calculated power loss and the required I_{rec} are plotted in Fig. 14. The calculated Z_{rec} for each voltage will be used in the receiver coil design for reactance compensation.

The rectifier has lower loss at high voltage and small current. The maximum V_o , however, is usually limited by the application, and the benefit from high values may be lost when latter dc–dc conversion stages are considered. In this case, additional loss modeling of any required dc–dc converter can be combined with the rectifier loss modeling to inform the selection of V_o without alteration to the overall system design method. The optimal design is marked by the red box in Fig. 14. Because the rectifier is one of the largest loss mechanisms, the individual-stage optimal corresponds to the system optimal.

VII. RECEIVER COIL MODELING

The receiver coil is designed as a conventional rectangular coil implemented using AWG 14 solid copper wire. The coil half-length and half-width are $a_{rx} = [a_{r1}, \dots, a_{rN_r}]$ and $b_{rx} = [b_{r1}, \dots, b_{rN_r}]$, where a_{ri} and b_{ri} are the half-length and half-width of (i)th turn. The number of turns is N_r and the wire radius is $r_{r,0}$.

When placed on the charging surface with an averaged flux density B_0 , the induced voltage is

$$V_{ind} = 4\omega_s B_0 \sum_{i=1}^{N_r} a_{ri} \cdot b_{ri}. \quad (45)$$

The coil inductance L_2 and ESR $R_{rx,wire}$ are calculated using the same modeling presented in Section III, replacing λ with 1. Note that after compensation the Rx side will have no circulating current. Thus, $V_{ind} \approx V_{rec}$ as the coil ESR is typically much smaller than the equivalent impedance of the rectifier. Since each V_{rec} is associated with a unique Z_{rec} and I_{rec} , the compensation capacitance is

$$C_2 = \frac{1}{\omega_s^2 L_2 + \omega_s \text{Im} \{Z_{rec}\}}. \quad (46)$$

The capacitor ESR $R_{rx,cap}$ is calculated according to (13). The total ESR of the Rx coil, including the compensation capacitor,

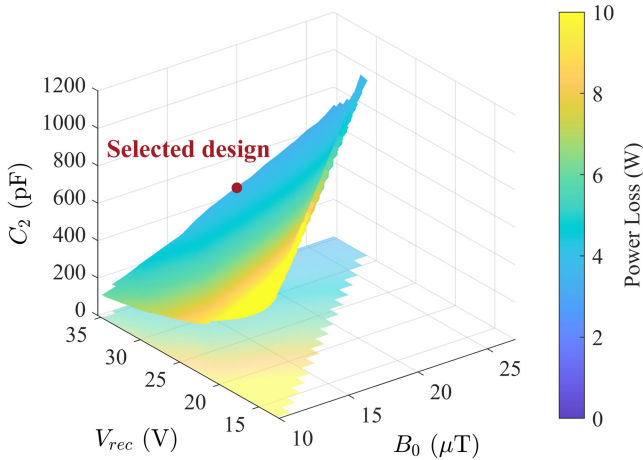


Fig. 15. Receiver coil power loss and the required compensation for a selection of B_0 and V_{rec} .

is $R_2 = R_{rx,wire} + R_{rx,cap}$. The power loss in the Rx coil is $P_{loss,rxcoil} = 0.5I_{rec}^2 R_2$.

A. Receiver Coil Design

To design the receiver coil, N_r is iterated from 2 to 4. The possible position for each turn ranges from 1 cm to maximum a_{rx} or b_{rx} with a 0.2-cm step. B_0 and V_{ind} use the same range as defined in the Tx coil and rectifier design, respectively. The design results are given in Fig. 15. For each B_0 , a minimum V_{ind} exists, which corresponds to the one-turn Rx coil design. V_{rec} values smaller than the minimum value cannot be designed, resulting in the blank region of the plot. The Rx coil, such as the rectifier, generally exhibits lower loss at higher voltage because I_{rec} decreases rapidly with V_{rec} . The maximum V_{rec} is limited to 35.4 V, which is determined by the rectifier V_o constraint. The final selection, determined in Section VIII, is marked in Fig. 15. Note that the selected design is not the minimum power loss coil design, but the design that will result in minimum system-wide power loss.

VIII. SYSTEM-LEVEL DESIGN

The WPT charging station consists of the five individual stages modeled in Sections III–VII. The goal of the WPT system-level design is optimizing all stages simultaneously to achieve high end-to-end efficiency while transferring full power. The additional design goals for multireceiver operation are incorporated into the individual stage design methods through the design of the IMN and the constraint on κ , resulting in the designed field uniformity across spatial and power variations.

Because each stage has been reduced to, at most, two parameters by the decoupled design, system-level optimization can be completed simply by an exhaustive search over the points of the parameterized subsystems: Inverter (see Fig. 10), IMN (see Fig. 11), Tx coil (see Fig. 7), Rx coil (see Fig. 15), and rectifier (see Fig. 14). Each of these figures shows the system-level optimized design selected by the exhaustive search. The remaining design choices are all coupling parameters; thus, any choice of

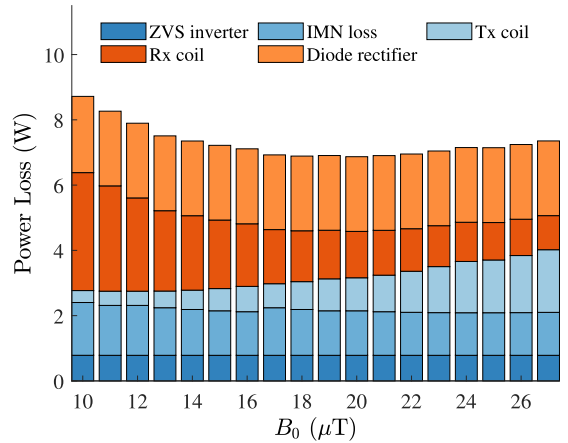


Fig. 16. Power loss of the entire system.

TABLE III
COMPARISON OF THE MEASURED AND CALCULATED CIRCUIT PARAMETERS

| Parameter | Variable | Design | Measurement |
|--|------------|--------|--------------|
| Tx coil inductance (μH) | L_1 | 12.3 | 12.6 (+2.4%) |
| Tx coil compensation (pF) | C_1 | 44.8 | 44 (-1.8%) |
| Tx coil ESR (Ω) | R_1 | 1.07 | 1 (-6.5%) |
| 1 st Rx coil inductance (μH) | $L_{2,1}$ | 1.65 | 1.66 (+0.6%) |
| 1 st Rx coil compensation (pF) | $C_{2,1}$ | 356 | 350 (-1.7%) |
| 1 st Rx coil ESR (Ω) | $R_{2,1}$ | 0.17 | 0.18 (+6%) |
| 2 nd Rx coil inductance (μH) | $L_{2,2}$ | 1.65 | 1.67 (+1.2%) |
| 2 nd Rx coil compensation (pF) | $C_{2,2}$ | 356 | 350 (-1.7%) |
| 2 nd Rx coil ESR (Ω) | $R_{2,2}$ | 0.17 | 0.18 (+6%) |
| IMN 1 st inductor (μH) | L_{imn1} | 1.82 | 1.85 (+1.6%) |
| IMN capacitor (pF) | C_{imn} | 303 | 300 (-1%) |
| IMN 2 nd inductor (μH) | L_{imn2} | 0.5 | 0.48 (-4%) |

a parameter on one stage constrains the selections that can be made in other stages.

Considering all stages simultaneously, the system-level power loss is shown in Fig. 16, where B_0 is retained as a parameter for the plot. For each B_0 , multiple systems exist but only the system with minimum loss is presented. The optimal system design occurs at a magnetic field $B_0 = 20 \mu\text{T}$ and exhibits a power loss of 6.9 W. Because each individual stage has been locally optimized for minimum power loss and the final step is an exhaustive search of all combinations of individual stage parameters, the selected design is the highest efficiency design predicted by the model. The optimized circuit parameters are summarized in Table III.

IX. EXPERIMENTAL VERIFICATION

To verify the WPT system modeling and design method, a 100-W, 6.78-MHz prototype WPT charging station is constructed using the optimized parameters of every stage. A photograph of the prototype is given in Fig. 17. The inverter and IMN together with auxiliary power supplies and front end line-frequency PFC rectifier [16] are implemented into a small box with a volume of $7.36 \times 5.26 \times 1.68 \text{ cm}^3$ for 25 W/in^3 power density. Only passive cooling is used in the experiments due to the high efficiency. Each receiver is connected to a BK8610

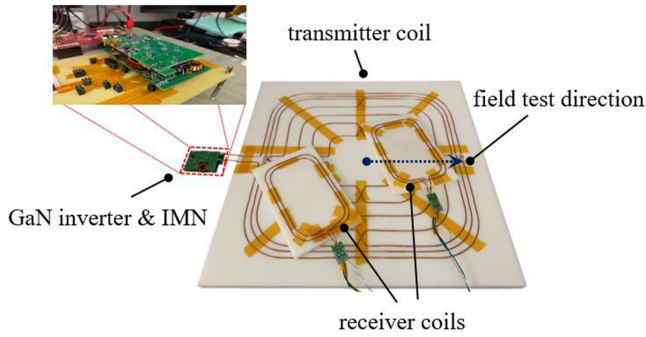


Fig. 17. Photograph of the prototype.

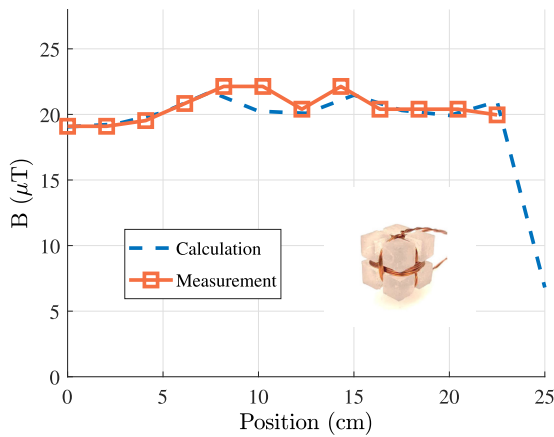


Fig. 18. Comparison of the designed and measured magnetic field.

electronic load. The transmitter and receiver coils are both shown upside-down so the windings are visible.

To precisely control the transmitter and receiver coils, their winding geometries are engraved into sheets of 1.7-cm HDPE dielectric using a CNC mill.

An Agilent 4294-A impedance analyzer is used to measure resistance and inductance of the coils. The measurement results are summarized in Table III and compared with the designed parameters, proving the accuracy of the modeling.

To verify the uniformity of the transmitter coil magnetic field, a field probe [12] is used to test the magnetic field when the system works with the nominal input voltage and no load is present. The field is measured along a line from the center to the middle of the edge, as shown by the arrow in Fig. 17. The measurement step is 2.25 cm and the position of the last measurement is 22.5 cm from the center, which covers 90% of the coil. The measurements are shown in Fig. 18 together with the model prediction showing that a near-uniform magnetic field is achieved. The measured $B_0 = 20.5 \mu\text{T}$ and field variation $\kappa = 15.9\%$, which is close to the calculated value of 15%. A photograph of the field probe [12] is also included in Fig. 18.

To verify the constant surface magnetic field and limited cross-channel disturbance, the prototype is measured under dynamically varying loading conditions. The load of the charging station is increased from 0 to 100 W and then decreased back to

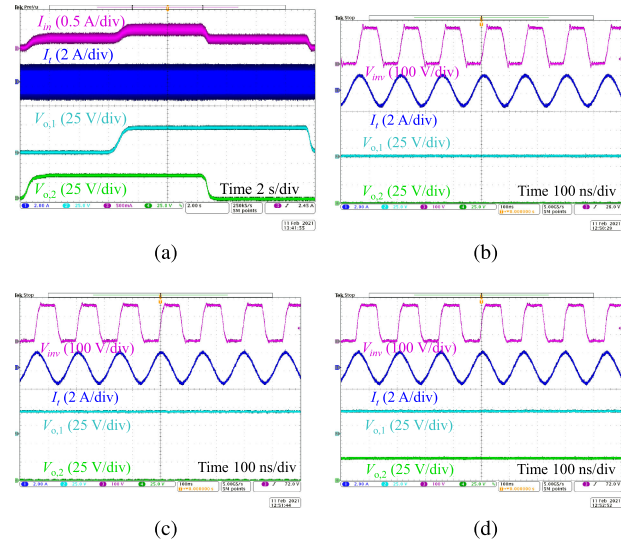


Fig. 19. Working waveform showing limited cross-channel disturbance and constant field with changing load (a) overall waveform with changing load, (b) zoom-in waveform of open load operation, (c) zoom-in waveform of 50-W operation, and (d) zoom-in waveform of 100 W operation.

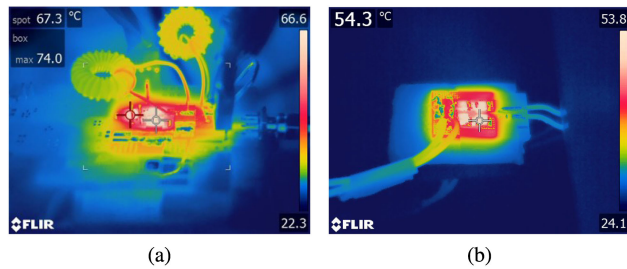


Fig. 20. Thermal photographs of the inverter and rectifier working at full power (a) inverter thermal photograph and (b) one diode rectifier thermal photograph.

zero. The load is changed through physically adding or removing two 50-W receivers to the field. Experimental waveforms are shown in Fig. 19(a). Measurements show that I_t remains constant as the power level varies, and the two rectifier output voltages are free from disturbance as the alternate receiver is added to or removed from the system.

Zoom-in waveforms of zero load, 50-W, and 100-W operation are shown in Fig. 19(b), (c), and (d), respectively.

Thermal photographs of the inverter and one diode rectifier working at full power are shown in Fig. 20, with passive cooling. It should be noted that the inverter is finally packed with PFC [16], auxiliary supply, and sensor board to form a small box, as shown in Fig. 17.

The system efficiency is defined as the total dc output power from all receivers divided by the transmitter side dc input power. Measured dc voltages and powers at the full load operating point are given in Table IV, together with a comparison to the model predictions, proving the accuracy of the system modeling and design. The measured dc–dc system efficiency is 92.8%. The modeled loss breakdown at this operating point is shown in Fig. 21. The measured efficiency, including the front-end PFC, is 90.3% [16].

TABLE IV
COMPARISON OF MEASURED AND CALCULATED CIRCUIT PARAMETERS

| Parameter | Variable | Design | Measurement |
|---------------------------------|-----------|--------|-----------------|
| Transmitter input voltage (V) | V_{dc} | 200 | 200 (+0%) |
| Transmitter input power (W) | P_{in} | 106.9 | 108.04 (+1.06%) |
| 1st receiver output voltage (V) | $V_{o,1}$ | 31.5 | 31.72 (+0.7%) |
| 1st receiver output power (W) | $P_{o,1}$ | 50 | 50.31 (+0.6%) |
| 2nd receiver output voltage (V) | $V_{o,2}$ | 31.5 | 31.61 (+0.3%) |
| 2nd receiver output power (W) | $P_{o,2}$ | 50 | 49.96 (-0.1%) |

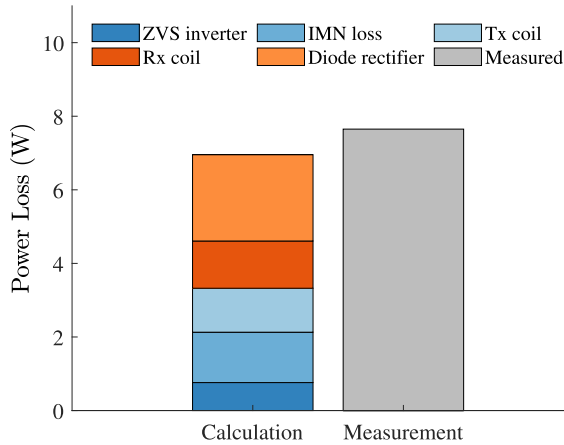


Fig. 21. Calculated loss components contributing to the total conversion losses of the prototype system at near 100-W output power.

TABLE V
COMPARISON OF 6.78-MHz SYSTEMS FOR PLANAR APPLICATION

| Ref. | Size [cm] | k | P_o [W] | N_{rec} | η_{all} [%] |
|-----------|-----------|------|-----------|-----------|------------------|
| [27] | Dia. 11.3 | 0.18 | 10 | 1 | 80 |
| [28] | Dia. 17.5 | 0.11 | 50 | 1 | 88 |
| [29] | Dia. 20 | 0.09 | 24 | 3 | 78 |
| [30] | 20 x 10 | - | 20 | 3 | 67 |
| [31] | 26 x 12 | - | 40 | 3 | 81.4 |
| This work | Dia. 50 | 0.11 | 100 | 2 | 92.8 |

A comparison to the state-of-the-art 6.78-MHz systems in the literature is given in Table V. The key parameters, including Tx coil size, coupling coefficient k , output power P_o , number of receivers N_{rec} , and peak overall efficiency η_{all} are reviewed. The proposed system exhibits high efficiency, as well as the desired charging flexibility.

X. CONCLUSION

This article presents the systematic modeling and design of a 100-W multiload wireless charging station to achieve the desired flexibility and high efficiency. The station includes a ZVS inverter, IMN, uniform-field Tx coil, Rx coils, and rectifiers. The systematic design decouples and parameterizes each stage using the source and/or load of adjacent stages and optimizes them internally to the greatest extent possible. Then, system-level optimization is performed on the reduced-order parameterized models of each stage.

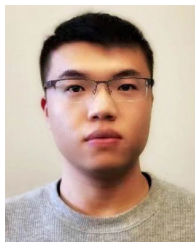
From the results of the systematic design considering every stage simultaneously, a system that achieves minimum power loss is selected for experimental verification of the modeling and design method. Measurements demonstrate the accuracy

of the used model and design method. The 100-W, 6.78-MHz experimental system with a 0.5×0.5 m² transmitter coil and two receivers achieves near-uniform magnetic field, limited cross-channel disturbance, and 92.8% end-to-end conversion efficiency.

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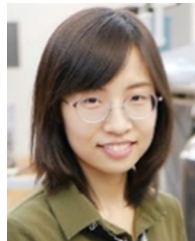
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