Letters

Proper Pulsewidth Setting to Avoid Underestimated Switching Loss in HV-IGBT Characterization

Kun Tan, *Member, IEEE*, and Lee Coulbeck

***Abstract*—This letter highlights the importance of appropriate pulsewidth duration of the double-pulse test for the high-voltage insulated gate bipolar transistor modules, in order to obtain the correct switching characterization and avoid underestimation in losses. Otherwise, it might cause improper design in power converters, especially in their thermal management. It demonstrates how the first ON-state pulsewidth during the test needs to be set long enough to characterize the switching-OFF of devices correctly. IGBT modules made by the leading European, Japanese, and Chinese manufacturers with voltage ratings spanning 3.3, 4.5, and 6.5 kV are tested for validation and guidance purposes. Moreover, the mechanism and impact factors of this pulsewidth effect are also investigated.**

***Index Terms*—Insulated gate bipolar transistors, loss measurement, reliability, semiconductor device testing.**

I. Introduction

LOSS characterization of power semiconductor devices is vital for their applications in power converters. Losses correspond to the energy conversion efficiency of converters and contribute to the thermal behavior of devices, so they need to be estimated and considered in the converter design phase. An accurate loss characterization benefits the prediction of heating and the design of heatsink, as well as the estimation of aging in devices and system reliability [1]. The losses of power devices are mainly from the switching and conduction losses, with OFF-state losses due to leakage current neglected. The conduction loss is generated due to the ON-state voltage of device. Typically, a curve tracer is used to characterize the ON-state voltage at different current and temperature conditions. The switching losses, consisting of the turn-ON and the turn-OFF, are commonly extracted during the double-pulse test (DPT).

The DPT circuit is shown in Fig. 1. Two high-voltage (HV) insulated gate bipolar transistor (IGBT) modules are connected in a half-bridge configuration, and a load inductor L connected in parallel with the upper module. The upper module is held in the OFF-state and operates as the free-wheeling diode. The lower module is regarded as the device under test (DUT) and is switched ON and OFF for characterization. Gate resistors $R_{\mathrm{G,ON}}$ and $R_{\mathrm{G,OFF}}$ are utilized on the gate driver to control the turn-ON and turn-OFF separately. Moreover, the external capacitor $C_{\mathrm{GE \cdot ex}}$ is applied to some modules when recommended by manufacturers, which can set the switching dv_{ce}/dt and di_{C}/dt separately to optimized transient behaviors. The energy required for the DPT is supplied by that stored in the capacitor bank C_{bus}, which is charged by the voltage source V_{dc}.

Ideal testing waveforms of the DUT in the DPT are depicted in Fig. 2, including the gate-emitter voltage V_{GE}, the collector current I_{C}, and the collector-emitter voltage V_{CE}. The gate driver applies two on pulses to the gate of the DUT, then its turn-OFF and turn-ON transitions can be characterized at the time of t_1 and t_2, respectively. The test initiates at time t_0, where C_{bus} has been charged to V_{dc}, and the DUT is OFF, so no current is flowing through L and the DUT. Then, during the first pulsewidth T_{ON}, the DUT is kept in the ON-state, hence L is charged by the bus voltage. Its current increases with a speed of di_{L}/dt and flows via the DUT. When I_{C} reaches the desired test condition of I_{Load}, the DUT is turned OFF at the end of T_{ON}. Meanwhile, V_{CE} might show a drop to the testing voltage condition of V_{Load}. After a period of OFF-time T_{OFF}, the DUT is switched ON at t_2. The testing conditions are nearly identical to that of t_1, owing to the small losses during the load current free-wheeling. Finally, the DUT is ultimately turned OFF at t_3 to finish the test.

Researchers [2], more than two decades ago, tested medium-voltage (1.2 kV) IGBT chips with both non-punch-through (NPT) and punch-through (PT) structures. It was found that the turn-OFF loss of the PT-IGBT does not depend on T_{ON}, but that of the NPT-IGBT increases with the increasing T_{ON} and will become saturated when T_{ON} is longer than several tens of microseconds. The authors claimed the characteristic strongly depends on the n-drift layer thickness, thus the NPT structure presents the effect, whereas the PT structure do not.

However, this finding did not draw much attention, as this T_{ON} effect is still rarely mentioned nowadays in research papers, international standards, device datasheets, and application notes. There is little guidance for T_{ON} requirement in the DPT or in service. Hence, it is all too easy to use an unsuitable pulse duration, especially for HV parts, as a larger capacitor is required to prolong the pulse. Moreover, the NPT and PT techniques are no longer adopted in current HV-IGBT modules. This evolution

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The authors are with Dynex Semiconductor Ltd., LN6 3LF Lincoln, U.K. (e-mail: k.tan.pe@outlook.com; lee.coulbeck@dynexsemi.com).

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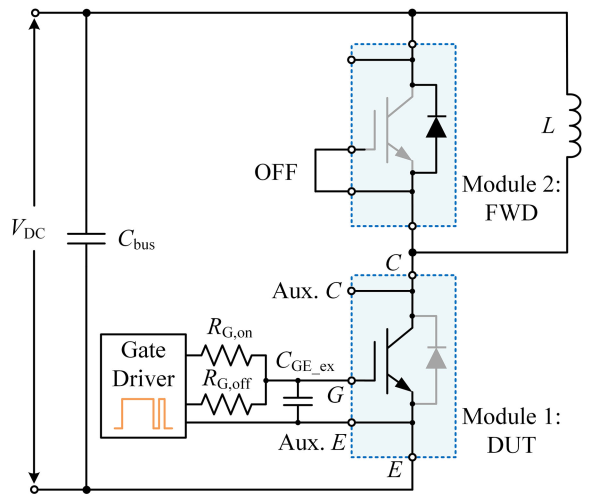

Fig. 1. Schematic of the DPT circuit for power semiconductor devices.

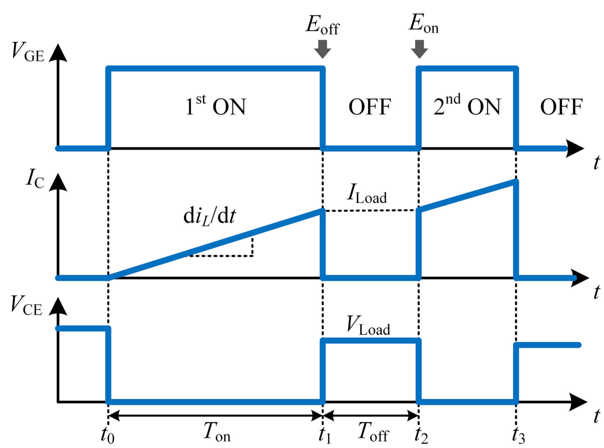

Fig. 2. Typical voltage and current waveforms in a DPT.

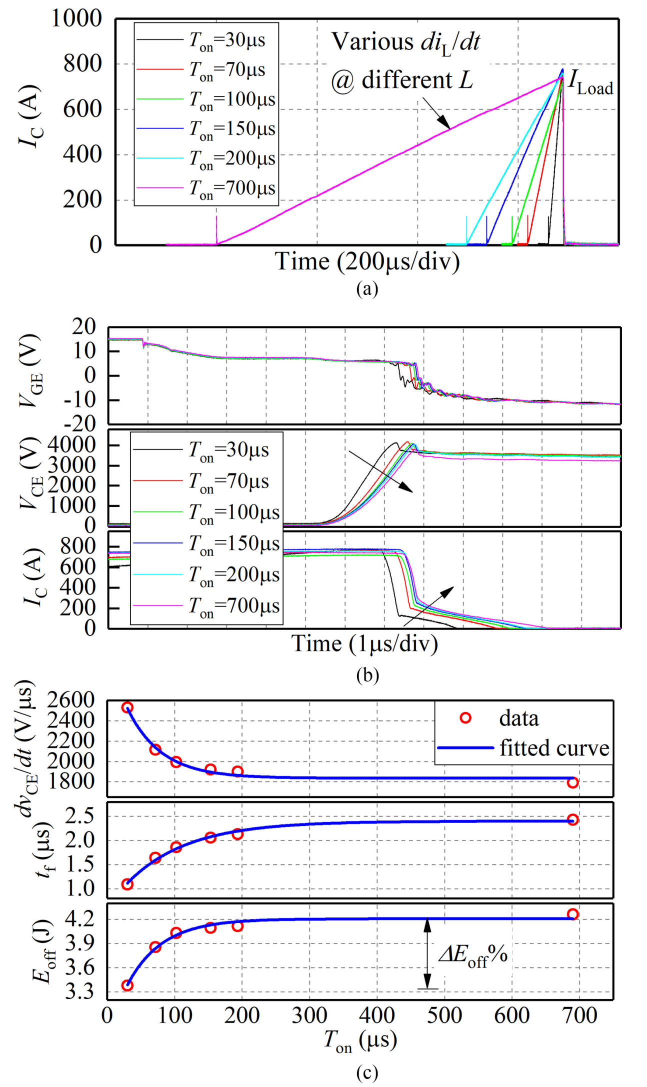

Fig. 3. Test waveforms and results of a 6.5 kV IGBT module under various T_{ON} as an example. (a) Reaching the desired load current with various di_{L}/dt. (b) Turn-OFF transient waveforms zoom-in. (c) Extracted parameters against T_{on}.

in chip structures, plus the pursuit of higher voltage devices (i.e., thicker drift layer), could exaggerate the T_{ON} effect and lead to larger characterization errors. Therefore, it is crucial to investigate this effect in the state-of-the-art HV-IGBTs, and to provide testing guidance accordingly. This letter will address these issues based on the experimental and simulation results.

II. Experimental Tests and Results

The detailed switching waveforms and parameters of a 6.5 kV IGBT module are shown in Fig. 3, as an example to illustrate the impact of various T_{ON}. The operating voltage and current conditions have been set to 3600 V/750 A, and T_{j} is 125 °C, all according to datasheet recommendations. Measured waveforms are aligned to the start of turn-OFF switching, i.e., t_1 in Fig. 2, for comparison purposes. As shown in Fig. 3(a), the $I_{\mathrm{Load}} = 750$ A test condition can be reached with various di_{L}/dt by changing L, hence the T_{on} required during testing varies between 30 to 700 μs. Turn-OFF transient waveforms are zoomed in, as shown in Fig. 3(b), which show that the positive dv_{ce}/dt, the negative di_{C}/dt and the tail current all present a significant dependence upon T_{on}. Both dv_{ce}/dt and di_{C}/dt are slowing down with the increasing T_{ON}, while the current tail is getting larger. The DUT's critical turn-OFF characteristics and their relationship to T_{ON} can be extracted including dv_{ce}/dt, the I_{C} fall time t_{f}, and the turn-OFF loss E_{off}, as illustrated in Fig. 3(c). With the increase of T_{ON} from 30 to 700 μs, dv_{ce}/dt decreases exponentially from ~2500 V/ μs to ~1800 V/ μs, whereas t_{f} and E_{off} show an exponential rise from 1.1 to 2.4 μs and from 3.4 to 4.3 J, respectively. Therefore, the impact of T_{on} on DUT's turn-OFF characteristics cannot be ignored, unless it is long enough for the DUT to saturate.

To evaluate the time taken to reach saturation for E_{off}, the time constant τ in the curve fitting (1) is adopted

$$y_{(x)} = y_0 + Ae^{-(x-x_0)/\tau}. \tag{1}$$

The percentage error $\Delta E_{\mathrm{off}}\%$ between $E_{\mathrm{off,max}}$ and $E_{\mathrm{off,min}}$ within the tested T_{ON} range, as illustrated in Fig. 3(c), is calculated by (2), which indicates to what extent the switching loss can be underestimated compared with the saturated value

$$\Delta E_{\mathrm{off}}\% = \frac{E_{\mathrm{off,max}} - E_{\mathrm{off,min}}}{E_{\mathrm{off,max}}} \times 100\%. \tag{2}$$

TABLE I
SUMMARY OF EXPERIMENTALLY TESTED HV-IGBT MODULES

Rating	Manufacturer	Part Number	Testing Conditions Based on Datasheet					Experimental Results		
			V_{Load} / I_{Load} (V / A)	$R_{G,on}$ (Ω)	$R_{G,off}$ (Ω)	C_{GE_ex} (nF)	T_j (°C)	T_{on} Test Range (μs)	τ for E_{off} (μs)	ΔE_{off}%
3.3kV	Dynex	DIM1500ESM33-TS	1800 / 1500	1.65	1.5	330	125	20 ~ 700	31.06	22%
	A	*	1800 / 1500	*	*	*	125	20 ~ 700	2.34	4%
	B	*	1800 / 1500	*	*	*	125	20 ~ 700	19.50	13%
	C	*	1800 / 1200	*	*	*	125	15 ~ 560	38.19	24%
4.5kV	Dynex	DIM1200ASM45-TL	2800 / 1200	2.4	2.7	220	125	30 ~ 400	38.21	29%
	Dynex	DIM1200ASM45-TF	2800 / 1200	2.4	2.7	220	125	30 ~ 400	30.16	27%
	A	*	2800 / 1200	*	*	*	125	30 ~ 400	34.21	14%
	D	*	2800 / 1200	*	*	*	125	30 ~ 400	49.20	35%
6.5kV	Dynex	DIM750ASM65-TS	3600 / 750	1.5	6.8	330	125	30 ~ 700	76.76	51%
	Dynex	DIM750ASM65-TL	3600 / 750	1.5	6.8	330	125	30 ~ 700	69.78	50%
	A	*	3600 / 750	*	*	*	125	30 ~ 700	51.68	20%
	E	*	3600 / 750	*	*	*	125	30 ~ 700	66.08	47%
	B	*	3600 / 750	*	*	*	125	30 ~ 700	76.97	45%

The HV-IGBT modules from the leading European, Japanese, and Chinese manufacturers are characterized using the datasheet specified conditions for V_{Load}, I_{Load}, R_{G}, $C_{\text{GE}\cdot\text{ex}}$, and T_{j}. Specifications and testing results are summarized in Table I. Note that the 3.3 kV device from Manufacturer-C has a different 1200 A current rating compared to others' 1500 A, hence, its T_{ON} test range is slightly narrower under the same L used but still long enough to eliminate the impact on the calculated τ. As can be seen from the results of τ for E_{off} and $\Delta E_{\text{off}}\%$, the T_{ON}'s impact on the loss characterization can be observed in all the HV-IGBT modules tested. It takes up to several hundred microseconds (5 times τ) time for the DUT to reach the final saturated E_{OFF}. It is noticeable that the 3.3 kV device from Manufacturer-A has a short time constant compared with the other modules, which could be caused by short lifetime as discussed in Section III-C.

Moreover, the percentage error $\Delta E_{\text{OFF}}\%$ caused by improper T_{ON} setting becomes more severe in the modules with higher voltage ratings. In the worst cases of 6.5 kV modules, the characterized E_{OFF} could be around 50% less than the actual value, if the T_{ON} used in characterization is too short. This significant underestimation may mislead application engineers during converter design and cause issues. Considering the significant amount of stored energy required for a long T_{on} to avoid the underestimation, it is recommended to set T_{ON} larger than 2.5 times τ. This will ensure the measured E_{OFF} is much closer ($\geq$ 92%) to the true value, hence compromising the stringent testing energy and equipment requirements.

III. MECHANISM AND CONTROL FACTORS INVESTIGATION

To further investigate the mechanism and control factors of the T_{on} effect observed in the previous section, simulations in Silvaco ATLAS are performed to gain an insight into the charge carrier behavior inside the IGBT. Allowing an estimate of the total charge carriers stored in the drift region at the end of T_{on}, as it will impact the following turn-OFF switching transient. All

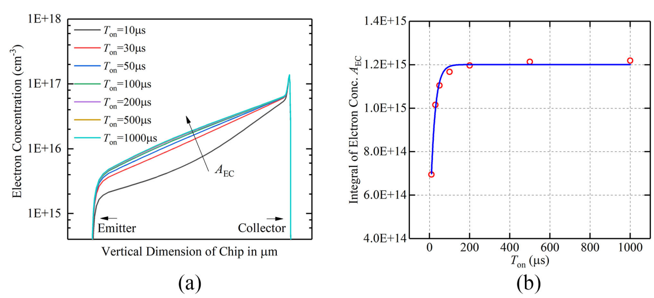

Fig. 4. Simulated electron concentration inside the IGBT at the end of T_{ON} pulse under the inductive load.

stored carriers need to be removed during turn-OFF, and the detailed physical model describing the process is given in [3].

A. Charge Carrier Concentration Under Various T_{on}

Simulation result of a 4.5 kV IGBT model is shown in Fig. 4(a). The electron concentration inside an IGBT is captured at 1200 A at the end of T_{ON} pulse. With increasing T_{on} applied, there are more electrons accumulated in the drift region at the end of T_{ON} as shown. The total electron concentration within the device is calculated, and it can be seen in Fig. 4(b) that the total electrons stored A_{EC} increases exponentially with T_{ON}. As more carriers are stored in the drift region, the device should present lower ON-state resistance and hence, a lower $V_{\text{CE(on)}}$ at the same collector current as shown in Fig. 5(a).

To experimentally validate the above simulations, the ON-state saturation voltage $V_{\text{CE(on)}}$ during the DPT needs to be measured. To overcome the wide voltage swing of V_{CE} between on-state and off-state, a diode clamping circuit has been utilized for the high-resolution $V_{\text{CE(on)}}$ measurement [4]. Note that the forward voltage drop of the clamping diode is included in the measurement due to the probing position in the circuit. The 4.5 kV IGBT module DIM1200ASM45-TF is tested at same conditions

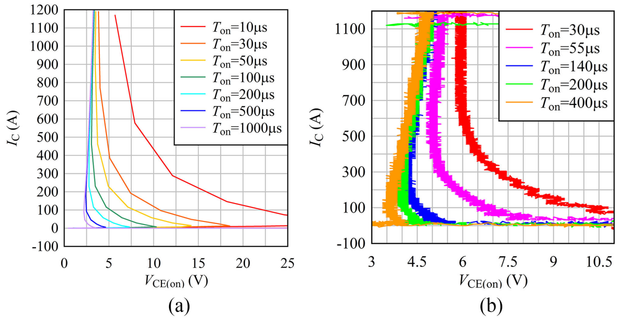

Fig. 5. Plots of I_C against $V_{CE(on)}$ at various T_{on} pulsewidth. (a) Simulation of the 4.5 kV model. (b) Experimental results of the module DIM1200ASM45-TF.

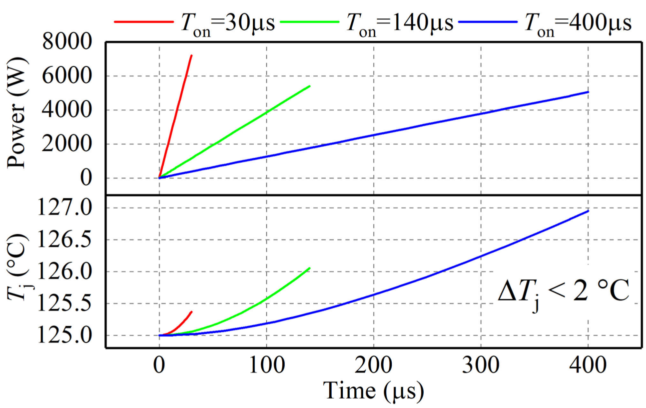

Fig. 6. Thermal network simulation results of junction temperature rise in DIM1200ASM45-TF during various T_{ON}.

in Table I. The experimentally measured I_C against $V_{CE(on)}$ waveforms are plotted in Fig. 5(b), which confirm that lower $V_{CE(on)}$ can be reached during the longer T_{ON}.

Therefore, the simulation and experimental results are consistent with the theory that, within a range of T_{ON}, the amount of conductivity modulation in the drift region is proportional to T_{ON}. That leads to changing switching speeds of both V_{CE} and I_C, including the higher current tail, as demonstrated in Fig. 3(b). Thus, E_{off} is impacted by T_{ON}.

B. Consideration of the ΔT_j During Test

It is necessary to examine and exclude that this effect is due simply to a rise of T_j during the DPT. Losses during the first pulse T_{on}, generated by the product of I_C and $V_{CE(on)}$, will heat up the DUT. The longer the T_{on}, the more losses and the higher the T_j reached. Another interesting point is that, for a shorter T_{on}, the $V_{CE(on)}$ for any current is higher as shown in Fig. 5, this too needs to be considered.

A fourth-order Foster thermal network as given in datasheet of the DIM1200ASM45-TF *(low switching loss variant, for worst case)* is built in LTspice in order to simulate the variation in T_j during the various T_{on}. The results in Fig. 6 show that the rise in T_j is small and less than 2 °C during the longest pulse. Hence, the change of T_j during T_{on} in the DPT is negligible.

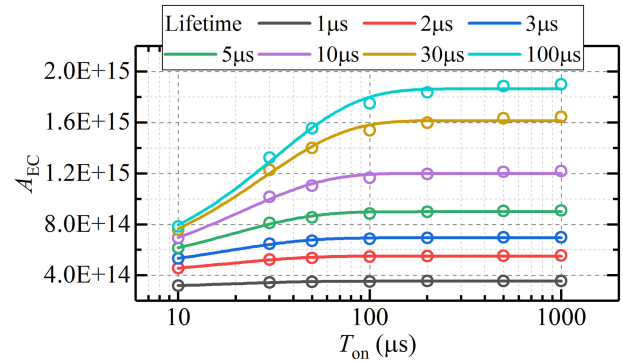

Fig. 7. Simulation of the impact of carrier lifetime on the T_{ON} effect.

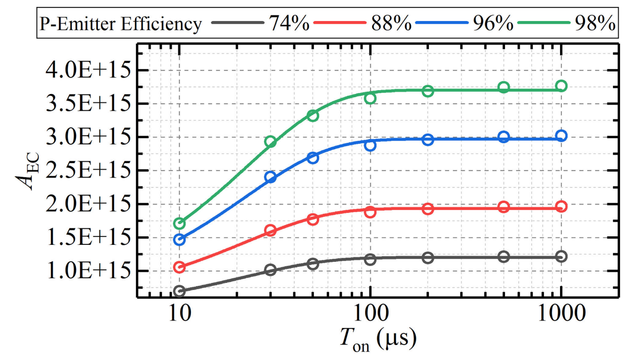

Fig. 8. Simulation of the impact of injection efficiency on the T_{ON} effect.

C. Investigating Possible Control Factors on the T_{on} Effect

Fig. 7 illustrates the simulated impact of the minority carrier lifetime, varying between 1 and 100 μs. It can be seen that the T_{on} effect becomes more apparent when the carrier lifetime is longer, and it requires a longer T_{on} for A_{EC} to reach the saturated value.

Results shown in Fig. 8 investigate the impact of the PNP transistor injection efficiency of the IGBT by varying the p-type emitter efficiency. It shows that the T_{on} effect is not really affected by the bipolar PNP emitter efficiency as all cases simulated show a very similar τ.

Finally, IGBT models of various voltage ratings, and hence different chip thickness and doping of the drift layer, are simulated under the commonly used voltage and current testing conditions, as those in Table I. Results in Fig. 9 support [2] suggesting that these HV-IGBTs are all presenting the T_{on} effect, with an increasing time constant in the higher voltage-level devices. This finding is consistent with the experimental results in Table I.

IV. Conclusion

This letter highlights that the first ON-state pulse duration during the DPT needs to be set long enough to characterize modern HV-IGBT modules correctly. This effect is caused by different total charge carriers stored in the drift region at the end of T_{on}, which are relating to the minority carrier lifetime, the injection efficiency, and dimensions of IGBT chip.

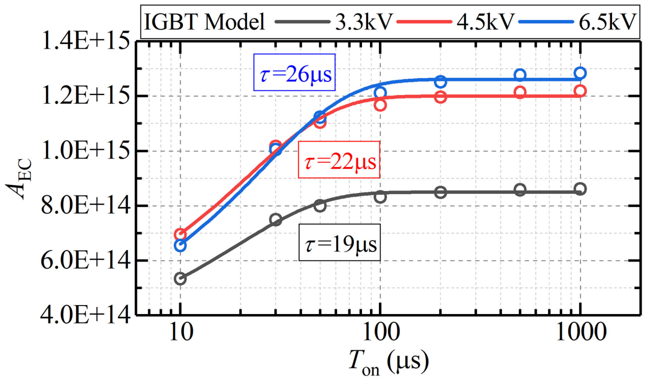

Fig. 9. Simulation of the impact of device voltage-class on the T_{ON} effect.

It is recommended, for a specific DUT, to set $T_{\mathrm{on}} \geq 2.5$ times τ, ensuring E_{off} is much closer ($\geq 92\%$) to the equilibrium value while providing a compromise with the capacitor size required for the long duration and high line voltage testing.

For simplicity, a general guidance for all HV-IGBT modules:

1) for 3.3 kV modules (τ is around 30 μs), to use $T_{\mathrm{on}} \geq 75$ μs;
2) for 4.5 kV modules (τ is around 40 μs), to use $T_{\mathrm{on}} \geq 100$ μs;
3) for 6.5 kV modules (τ is around 70 μs), to use $T_{\mathrm{on}} \geq 175$ μs.

When the HV-IGBT modules are used with the ON-state duration less than requirements above, trading off conduction losses against turn-OFF losses is noteworthy for users.

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