Online Efficiency Optimization of a Closed-Loop Controlled SiC-Based Bidirectional Boost Converter

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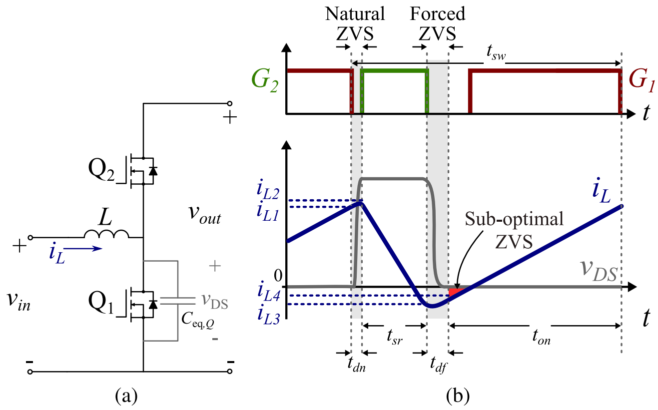
***Abstract*—This article presents an online efficiency optimization strategy for a digitally controlled, wide operating range silicon carbide based boost converter with bidirectional power flow. The proposed strategy minimizes switching losses at any given operating point by adjusting the converter switching frequency and dead times to optimally set the peak synchronous rectifier turn-OFF current. This results in the converter achieving zero-voltage switching quasi-square wave (ZVS-QSW) operation with minimum inductor current ripple. The optimal timing parameters are determined online by fit functions based on sensed input/output voltages and inductor current, and applied to the converter in a low-bandwidth feed-forward loop operating in conjunction with closed-loop regulation of the converter output voltage. The fit functions are developed from multivariate curve fitting of the analytical solutions of the minimum-conduction ZVS-QSW state plane over the complete range of operation. The proposed approach enables bidirectional operation with efficiencies greater than 97.5% for input voltages ranging from 200 to 400 V, step-up conversion ratios up to 2.5, and power levels between 2 and 8 kW. The converter also achieves efficiencies greater than 99% over wide power levels at boost conversion ratios lower than 2.**

***Index Terms*—Curve fitting, digital control, feedforward, nonlinear capacitance, optimization, quasi-square wave, silicon carbide, zero-voltage switching.**

I. INTRODUCTION

FREQUENCY-DEPENDENT switching losses present a significant impediment to realizing high-frequency compact switched-mode power converters [1]. Of principal concern are the turn-ON switching losses that are primarily dependent on the device parasitic output capacitances and the reverse recovery of the rectifier body diodes. Particularly with fast turn-OFF wide-bandgap devices, the turn-ON losses tend to be the dominant loss mechanism in high-frequency hard-switched converters [2]–[5]. Reducing the turn-ON losses is the key to achieving higher efficiencies, especially for wide operating range converters, such as PFC rectifiers [6]–[9], inverters [10], [11], and bidirectional dc–dc converters in electric vehicle powertrain applications [12]–[15].



(a) (b)

Fig. 1. (a) Boost converter switching cell. (b) ZVS-QSW operating waveforms wherein the converter achieves ZVS with a higher conduction loss penalty.

Zero-voltage switching quasi-square wave (ZVS-QSW) operation of pulsewidth-modulated dc–dc converters, introduced in [16] and analyzed in detail in [6], [17], and [18], is a well-known approach for mitigating the turn-ON switching losses. This approach increases the inductor current ripple such that a sufficiently negative excursion of the current results in a soft zero-voltage transition between the turn-OFF of the synchronous rectifier (SR) switch and the turn-ON of the main switch. The amount of negative current required depends on the converter input and output voltages. The ZVS-QSW operation is illustrated in Fig. 1 for a boost converter switching cell shown in Fig. 1(a). The individual device parasitic output capacitances are lumped into a single equivalent capacitance ($C_{\mathrm{eq},Q}$). Fig. 1(b) shows the ZVS-QSW waveforms with the inductor current forced negative during t_{sr}. The main switch Q_1 can turn ON anytime after the "forced" ZVS resonant interval (t_{df}) ends. SR switch Q_2 always turns ON with zero voltage after the "natural" resonant interval (t_{dn}). As seen in Fig. 1(b), an excessive negative current at Q_2 turn-OFF results in additional circulating currents (highlighted in red), which in turn require higher peak currents to deliver the same average inductor current increasing conduction losses. These losses can be minimized by optimally setting the negative current during t_{sr} resulting in minimum-conduction ZVS-QSW operation seen in Fig. 2(a). Operation in this mode enables ZVS transitions with the lowest

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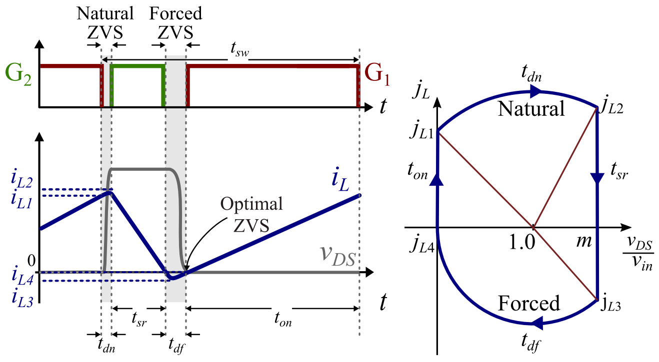


(a) (b)

Fig. 2. Minimum-conduction ZVS-QSW (a) operating waveforms and (b) normalized state-plane diagram.

possible negative current, thus reducing conduction losses [18]–[20], but it requires precise adjustment of the timing parameters, particularly the switching period (t_{sw}), and the forced ZVS dead time interval (t_{df}). In response to changing operating conditions, these timing parameters must be adjusted online to maintain minimum-conduction ZVS-QSW operation, consequently optimizing converter efficiency over its full operating range.

Online efficiency optimization strategies that vary converter timing parameters have been extensively adopted for both conventional silicon-based [21]–[27] and wide-bandgap converters [5], [7]–[11], [23], [28]–[32]. Generally, two distinct approaches have been pursued. The first approach employs external analog circuitry to detect zero crossings of either inductor current [7]–[9], [24], [29] or switch-node voltage [23], [31] and adjusts timing parameters based on this information. This approach typically leads to implementation complexity with sensitivity to noise and delays. Moreover, it also suffers from a lack of flexibility since most converters considered have only unidirectional power flow. Shahzad *et al.* [9] demonstrate optimization for both inductor current polarities with two comparator circuits and flipping the edge-trigger logic based on polarity.

The second class of online-optimization approaches relies entirely on digital implementation. For example, in [22] and [21], the converter timing parameters are perturbed over a range and values that maximize efficiency are applied. This strategy requires long convergence times for wide operating ranges and may not achieve maximal efficiency since only one of the timing parameters is swept. Lookup-table-based approaches that adjust switching frequencies and operational modes based on theoretical or empirically determined table entries for a given operating condition are adopted in [11] and [27]. In applications where both the input/output voltages and converter power levels must vary, the table dimensions grow, increasing storage requirements and complexity. Approaches that directly compute the timing parameters are presented in [5], [10], [25], [26], [28], and [30]. These approaches reduce the computational complexity by fixing one parameter, such as peak SR turn-OFF current [10], [25], [26], dead times [5], [28], or frequency [30] and online adjusting the remaining parameter. This results in either hard-switched or suboptimal ZVS operation over specific ranges. A hybrid modulation strategy combining the discontinuous conduction and ZVS-QSW mode by introducing additional switching intervals is proposed in [32]. Generally speaking, few previously presented approaches achieve minimum-conduction ZVS-QSW operation over wide ranges since most of them can vary only a single timing parameter. While it may theoretically be possible to extend some of these approaches to both frequency and dead times, the resulting increase in complexity could end up being prohibitive in practical implementation.

The optimization strategy proposed in this article achieves wide-range minimum-conduction ZVS-QSW operation by online adjusting both the converter switching frequency and the forced ZVS dead time. The direct computation of the optimal timing parameters is achieved through multivariate polynomial functions that are developed offline from surface-fitting the analytical solutions and are easily implemented in the controller. A low-bandwidth feed-forward loop operating concurrently with the feedback loop evaluates the polynomial functions that generate the optimal timing parameters for sensed input/output voltages and average inductor current.

This article is organized as follows. Section II provides a broad overview of the proposed control scheme. Section III illustrates the variation in optimal timing parameters with operating conditions and develops comprehensive analytical models that capture this variation across the converter's entire operating range. In Section IV, multivariate polynomial curve fitting approaches are developed for these analytical models, and implementation details are discussed. Experimental results in Section V validate the proposed online-optimization approach for bidirectional power flow as well as in transient operation. Additionally, efficiencies achieved under varying operating conditions with this strategy are compared with conventional fixed frequency/dead time operation and single-parameter optimization approaches. Finally, Section VI concludes this article.

II. OVERVIEW OF THE CONTROL ARCHITECTURE FOR ONLINE EFFICIENCY OPTIMIZATION

Calculation of the optimal switching frequency and dead times requires a solution of the minimum-conduction ZVS-QSW state-plane representation shown in Fig. 2(b) that plots the normalized inductor current j_L as a function of the normalized switch-node voltage. The current normalization factor i_B is defined as v_{IN}/R_0, where R_0 is the characteristic impedance $\sqrt{L/C_{\text{eq},Q}}$. Although the timing parameters calculated from the minimum-conduction ZVS-QSW state plane are unique for a given combination of input voltage v_{IN}, conversion ratio m, and processed power (average inductor current), the state-plane equations governing the converter's operation in this mode do not have straightforward closed-form expressions. They must be numerically solved to obtain the timing parameters. Since such a numerical computation is not suitable for direct implementation on a controller platform, a twofold approach to simplifying online optimization is adopted in this article. As a first step, analytical models for optimal timing parameters, f_{sw} and t_{df}, are developed offline through numerical solution

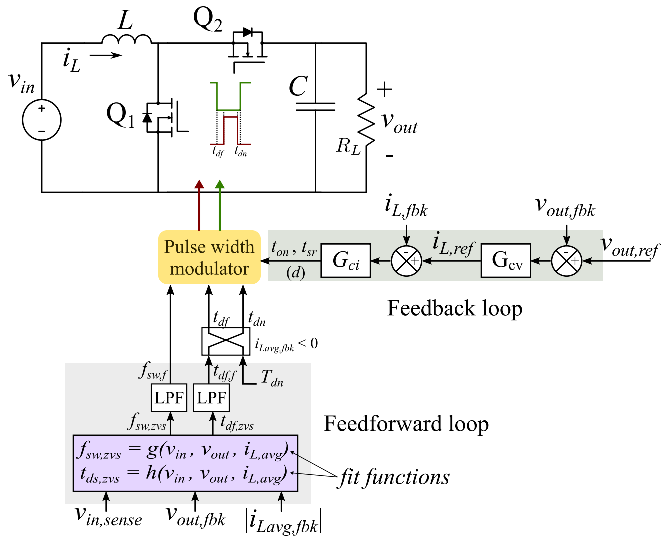


Fig. 3. Controller architecture includes a feedback loop responsible for the output voltage regulation and a feed-forward loop that implements the online efficiency optimization.

of the minimum-conduction ZVS-QSW state plane for the entire region of converter operation. A multivariate polynomial function is then fit to these theoretical models using a standard curve fitting toolbox [33]. This approach, first introduced in [34], simplifies the online optimization to evaluating polynomial functions (fit functions) that yield the optimal timing parameters for given operating conditions. The fit functions are then easily implemented on a microcontroller platform and evaluated in a low-bandwidth feed-forward loop operating in conjunction with the feedback loop.

Fig. 3 presents the resulting control architecture. The feedback loop responsible for the output voltage regulation contains an outer voltage loop followed by an inner average current-mode control loop. The current and voltage compensators designed using standard frequency domain techniques are implemented in discrete time with a sampling rate equal to the switching frequency [35]. The online efficiency optimization, implemented in the feed-forward path, senses the input voltage (v_{IN}), output voltage (v_{OUT}), and the average input current ($i_{L,\text{avg}}$) to compute the optimal switching frequency (f_{sw}), and dead time (t_{df}) using the fit functions g and h. It should be noted that the dead time optimization applies only to the turn-ON transition of the main switch (Q_1). The SR Q_2 turn-ON transition, which achieves ZVS naturally, operates with a constant dead time. The predicted optimal timing parameters are applied to the pulsewidth modulator (PWM) through low-pass filters to ensure smooth transitions as the operating conditions change. The converter eventually settles at timing parameters that achieve minimum-conduction ZVS for a given operating point. Given that operating conditions are changing relatively slowly in the considered application, the feed-forward adjustment operates at a much slower rate than the voltage regulation loop. Furthermore, as discussed further in Section IV-B, the proposed online-optimization strategy is easily extended to bidirectional power flow by utilizing the absolute value of the sensed average inductor current.

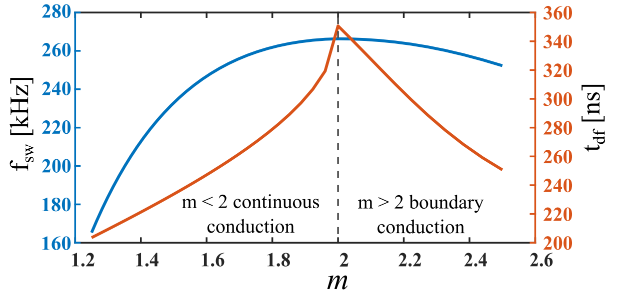
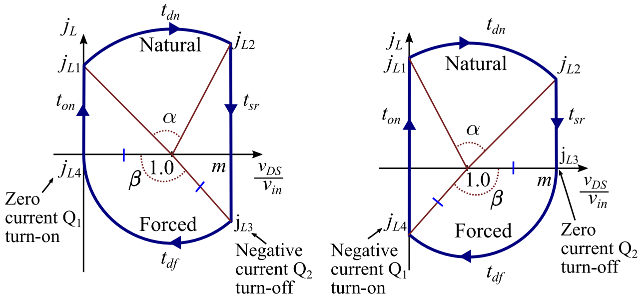


Fig. 4. Optimal f_{sw} and t_{df} as functions of the conversion ratio m for fixed $v_{\text{OUT}} = 500$V and $i_{L,\text{avg}} = 25$A, and v_{IN} varying from 200 to 400V.



(a) (b)

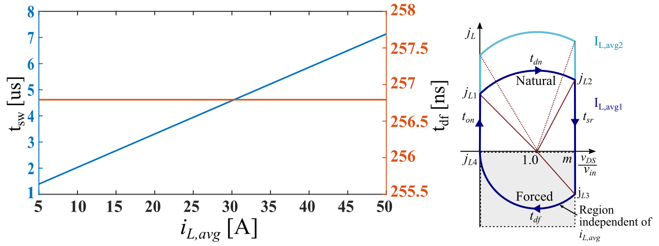
Fig. 5. State-plane diagrams for converter operation in (a) $m < 2$ continuous conduction mode and (b) $m > 2$ boundary conduction mode.

III. TIMING PARAMETERS FOR MINIMUM-CONDUCTION ZVS-QSW OPERATION

A systematic approach to numerically solving a boost converter minimum-conduction state plane for the optimal timing parameters over the full operating range is shown in the Appendix. Before developing the analytical models and the resulting fit-functions from the solutions, it is helpful to inspect the trajectory of the optimal timing parameters for variation in each of the converter operating conditions (m, $i_{L,\text{avg}}$, v_{IN}). This step yields insight into the converter operation in minimum-conduction ZVS-QSW mode as well as the curve fitting process.

A. *Variation With Conversion Ratio m*

Fig. 4 shows the optimal switching frequency (f_{sw}) and forced ZVS dead time (t_{df}) as functions of the conversion ratio m defined as $m = v_{\text{OUT}}/v_{\text{IN}}$. The plot is generated from the analytical solutions by fixing the converter output voltage at 500V (thereby fixing the equivalent switch node capacitance) and the average inductor current at 25A, and by varying the input voltage from 200 to 400V to vary m from 1.25 to 2.5. The optimal f_{sw} shows a parabolic dependence on m, with maxima at $m = 2$, whereas the optimal t_{df} splits into two curves across $m = 2$ conversion line. The converter operation in minimum-conduction ZVS-QSW mode can be divided into two distinct regions of operation, as illustrated in the state-plane diagrams of Fig. 5. $m < 2$ continuous conduction mode of Fig. 5(a) requires a negative current j_{L3} at the SR Q_2 turn-OFF instant to satisfy the forced ZVS condition $j_{L3}^2 + (m-1)^2 \geq 1$. Setting the two terms equal results in minimum-conduction ZVS operation with



(a) (b)

Fig. 6. (a) Optimal switching period t_{sw} and forced dead time interval t_{df} as functions of $i_{L,\mathrm{avg}}$ varying from 5 to 50A for fixed $v_{\mathrm{IN}} = 300\mathrm{V}$ and $v_{\mathrm{OUT}} = 500\mathrm{V}$, and (b) state-plane diagrams for two different average inductor currents.

j_{L3} set optimally and the main switch Q_1 turning ON at strictly zero current and zero voltage.

Increasing m shifts the point $(1.0, 0)$ on the state-plane horizontal axis inward toward $(0, 0)$. The optimal j_{L3} decreases (less negative), resulting in smaller rectifier turn-ON time t_{sr}, thereby increasing f_{sw}. The normalized angle β becomes larger, increasing t_{df}. At $m = 2$, the point where 1 and $m - 1$ segments on the state plane are equal, both Q_2 turn-OFF and Q_1 turn-ON occur at zero current with optimal f_{sw} and t_{df} reaching their maximum values. Angle β traverses an angle of π with $t_{df} = \pi\sqrt{LC_{oss,Q}}$. Increasing m further results in $m > 2$ boundary conduction mode shown in Fig. 5(b). Turning OFF Q_2 at strictly zero current results in minimum-conduction ZVS with Q_1 now turning ON with optimal negative current j_{L4}. Optimal j_{L4} follows the equation $j_{L4}^2 + 1 = (m-1)^2$. Both the optimal f_{sw} and t_{df} decrease with increasing m in the boundary conduction mode. Even though a negative current is not required in the boundary conduction mode since the converter "naturally" achieves ZVS turn-ON for Q_1, precise timing parameter adjustments are still required to ensure the rectifier switch turn OFF at zero current (to avoid body diode conduction) in order to achieve the minimum-conduction ZVS-QSW operation.

The optimal timing parameters are strongly dependent on the conversion ratio m. A curve fitting approach for optimal f_{sw} requires a higher order fit with respect to m. Optimal t_{df} requires two independent fits across the $m = 2$ conversion boundary.

B. Variation With Average Inductor Current $i_{L,avg}$

Fig. 6(a) plots the optimal switching period and forced dead time interval as functions of the average inductor current ($i_{L,\mathrm{avg}}$) from 5–50A with v_{IN} fixed at 300 and 500V, respectively. As evident from the state-plane diagram of Fig. 6(b), the $j_L < 0$ region (negative vertical axis) is independent of $i_{L,\mathrm{avg}}$, implying that the Q_2 turn-OFF and Q_1 turn-ON currents (j_{L3} and j_{L4}), and the forced ZVS interval t_{df} depend only on the input and output voltages of the converter. Optimal t_{df}, therefore, remains constant for a given v_{IN} and v_{OUT}, whereas optimal t_{sw} linearly increases with $i_{L,\mathrm{avg}}$ to accommodate the increasing values of t_{on} and t_{sr}, thereby implying an inverse dependence of the optimal f_{sw} on $i_{L,\mathrm{avg}}$.

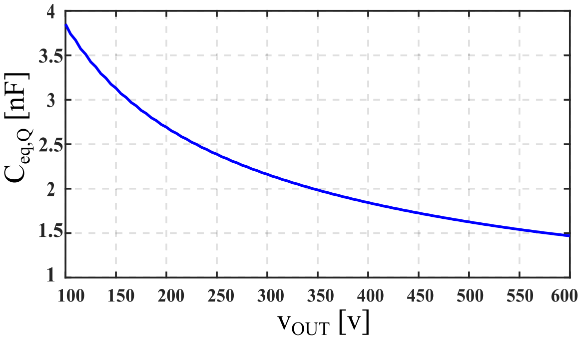


Fig. 7. Charge-equivalent switch node capacitance $C_{\mathrm{eq},Q}$ of the half-bridge module as a function of the dc output voltage.

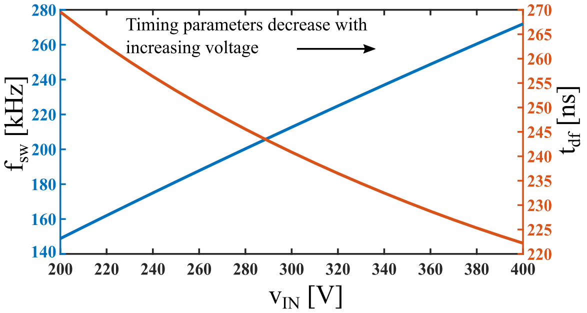


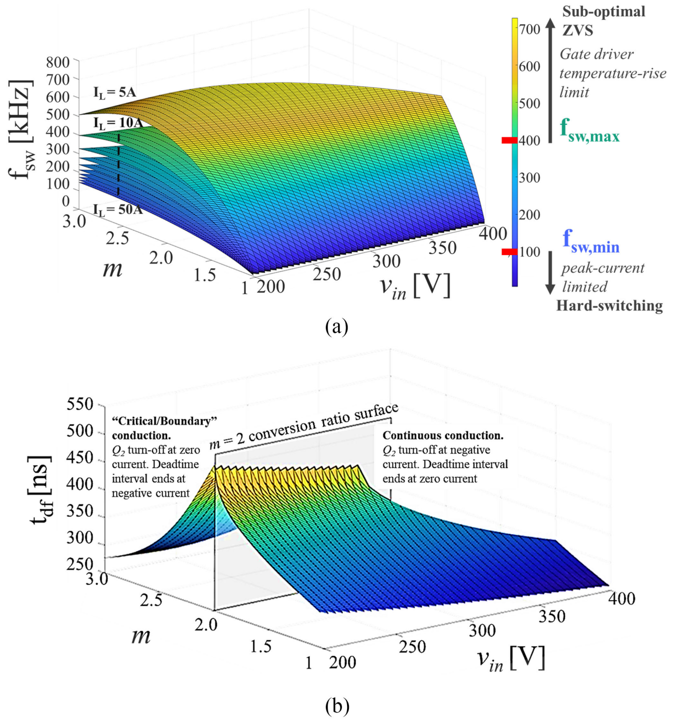
Fig. 8. Optimal f_{sw} and t_{df} as functions of v_{IN} varying from 200 to 400V for fixed $m = 1.5$ and $i_{L,\mathrm{avg}} = 25\mathrm{A}$. v_{OUT} consequently varies from 300 to 600V effectively varying $C_{\mathrm{eq},Q}$ from 4 to 1.5nF.

C. Effect of Varying Switch Node Capacitance

The device parasitic output capacitance C_{oss} exhibits a highly nonlinear drain-source voltage dependence. An analytical approach for taking the equivalent half-bridge switch node capacitance $C_{\mathrm{eq},Q}$ [of Fig. 1(a)] into account is described in [36] and [37] and requires calculating the charge-equivalent capacitance $C_{\mathrm{eq},Q}$ as per

$$C_{\mathrm{eq},Q} = \frac{1}{V_{\mathrm{out}}} \int_0^{V_{\mathrm{out}}} \left(C_{oss}(v) + C_{oss}(V_{\mathrm{out}} - v) \right) \mathrm{d}v. \tag{1}$$

The charge-equivalent capacitance for the half-bridge semiconductor module employed in the boost converter under consideration is plotted in Fig. 7 as a function of the output voltage. The impact of the varying switch node capacitance on the optimal timing parameters can be evaluated by fixing m and $i_{L,\mathrm{avg}}$ at 1.5 and 25A, respectively, and by varying v_{IN} from 200 to 400V. The converter output voltage consequently varies from 300 to 600V, effectively varying the equivalent switch node capacitance from 4.5 to 3nF. The resulting trajectory of the optimal timing parameters captured in Fig. 8 shows a near-linear decrease with increasing input voltage. Each operating point on the plot represents a distinct state plane with a different switch node capacitance and, therefore, a unique resonant frequency and characteristic impedance. With a near-linear trajectory, a lower order curve-fit polynomial is sufficient to accurately capture the variation with v_{IN}.



(a)

(b)

Fig. 9. Minimum-conduction ZVS-QSW (a) optimal f_{sw} for different $i_{L,\text{avg}}$ values, and (b) optimal t_{df}, both plotted as functions of v_{IN} and m.

D. Comprehensive Analytical Models

The trajectories of optimal timing parameters indicate that the minimum-conduction ZVS switching frequency is a function of three parameters: m, $i_{L,\text{avg}}$, and v_{IN}, whereas the forced ZVS dead time interval depends only on m and v_{IN}. The switching frequency analytical model can be constructed from multiple surfaces wherein each surface represents the optimal f_{sw} for the variation in v_{IN} and m for a given $i_{L,\text{avg}}$. Analytical model for the optimal t_{df} consists of two surfaces split across the $m = 2$ conversion ratio plane. The comprehensive analytical models for optimal timing parameters over the converter's full operating range are developed in Fig. 9. The steps involved in developing and plotting the models are detailed in the Appendix. Input voltage v_{IN} is varied from 200 to 400V and v_{OUT} from v_{IN} to 600V, both in steps of 5V, representing a theoretical variation of 1.0 to 3.0 in the converter's conversion ratio m. The average inductor $i_{L,\text{avg}}$ across the optimal f_{sw} surfaces varies from 5 to 50A in steps of 5A. The analytical models account for the varying $C_{\text{eq},Q}$ and follow the optimal timing parameter trends presented earlier. Although the frequency models indicate a wide variation in optimal f_{sw} (from less than 100 to 800kHz), not all switching frequency values are attainable in the hardware implementation. The converter is constrained to operate within the limits $f_{\text{sw,min}}$ and $f_{\text{sw,max}}$. Gate-driver ratings set the maximum switching frequency threshold $f_{\text{sw,max}}$ while peak currents on the magnetics set the lower limit $f_{\text{sw,min}}$. Within these limits, the converter achieves minimum-conduction ZVS-QSW at all operating points. At operating points that require optimal f_{sw} beyond $f_{\text{sw,max}}$, the converter operates with suboptimal ZVS switching frequency clamped to $f_{\max}$. Likewise, the converter hard switches with f_{sw} fixed to $f_{\text{sw,min}}$ at operating points requiring optimal frequencies below $f_{\text{sw,min}}$.

IV. ONLINE EFFICIENCY OPTIMIZATION USING MULTIVARIATE POLYNOMIAL CURVE FITTING

This section addresses implementation issues related to the online efficiency optimization strategy where the converter switching frequency and the forced ZVS dead time are adjusted in response to operating conditions. Computation of the optimal timing parameters is achieved through multivariate polynomial functions that are developed from surface fitting the analytical solutions developed in Section III.

A. Multivariate Polynomial Curve Fitting

Based on the dependencies observed in Section III, the analytical-model surfaces employ a *poly25* polynomial fit with a second-degree polynomial in input voltage v_{IN} and a fifth-degree in conversion ratio m. The *poly25* polynomial comprises 15 coefficients and is given by

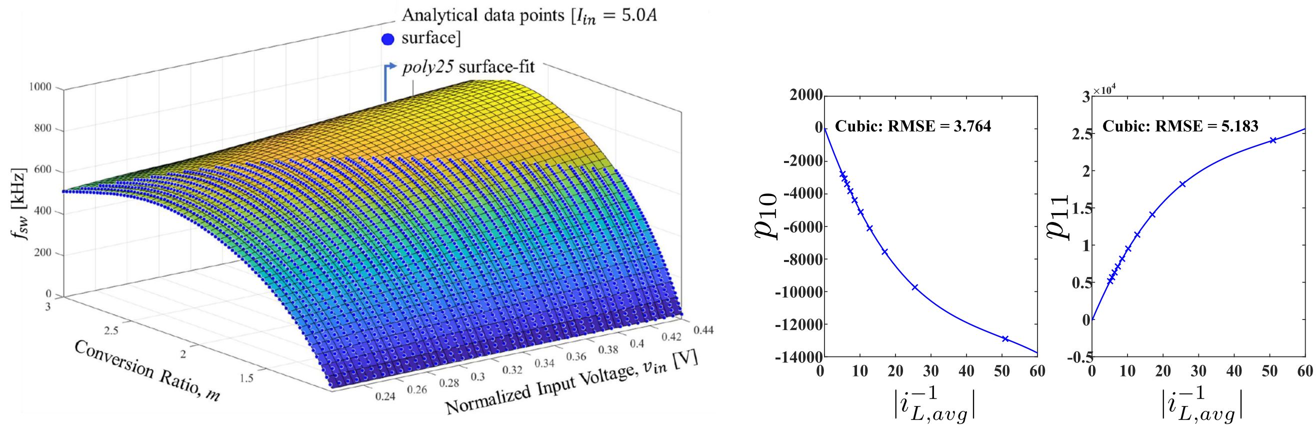
$$\begin{aligned} y(v_{\text{in}}, m) = p_{00} &+ p_{10}.v_{\text{in}} + p_{01}.m \\ &+ p_{20}.v_{\text{in}}^2 + p_{11}.v_{\text{in}}.m + p_{02}.m^2 \\ &+ p_{21}.v_{\text{in}}^2.m + p_{12}.v_{\text{in}}.m^2 + p_{03}.m^3 \\ &+ p_{22}.v_{\text{in}}^2.m^2 + p_{13}.v_{\text{in}}.m^3 + p_{04}.m^4 \\ &+ p_{23}.v_{\text{in}}^2.m^3 + p_{14}.v_{\text{in}}.m^4 + p_{05}.m^5 \qquad (2) \end{aligned}$$

where y is the optimal timing parameter (f_{sw} or t_{df}), and $p_{i,j}$ are the curve-fit coefficients.

The multivariate polynomial fitting of the optimal f_{sw} demonstrated in Fig. 10 involves two steps. First, independent *poly25* surfaces corresponding to distinct $i_{L,\text{avg}}$ values uniquely fit each analytical surface from the model. This step results in ten different $poly25$ surfaces

$$f_{\text{sw}}\big|_{I_{L,\text{avg}}=I_k} = p_{00}\big|_{I_k} + p_{10}\big|_{I_k}.v_{\text{in}} + \cdots + p_{05}\big|_{I_k}.m^5 \qquad (k = 1, 2, \ldots, 10). \quad (3)$$

Fig. 10(a) illustrates this step for a single optimal f_{sw} surface with $i_{L,\text{avg}} = 5\text{A}$. To keep the *poly25* terms tractable, the v_{IN} axis is normalized with respect to the voltage sensor full-scale value before the fitting process. In the second step, the corresponding coefficients (e.g., $p_{00}\big|_{I_1}, p_{00}\big|_{I_2} \cdots p_{00}\big|_{I_{10}}$) across the ten *poly25* functions are curve-fit with $i_{L,\text{avg}}$. Due to an inverse dependence of the optimal f_{sw} on the average inductor current, curve fitting the *poly25* coefficients with $i_{L,\text{avg}}^{-1}$ results in a better fit. A common curve-fit order is employed across all coefficients to simplify implementation while adequately reducing the root-mean-square error (RMSE) for fit coefficients. Fig. 10(a) illustrates the fit along with computed RMSE for two coefficients p_{10}, and p_{11}. Each coefficient $p_{i,j}$ employs a



(a) (b)

Fig. 10. Two-step multivariate frequency fitting process: (a) *Step 1*: *poly25* surface fit to data points obtained from the analytical model for a distinct $i_{L,\text{avg}}$, and (b) *Step 2*: corresponding *poly25* coefficients as functions of $i^{-1}_{L,\text{avg}}$.

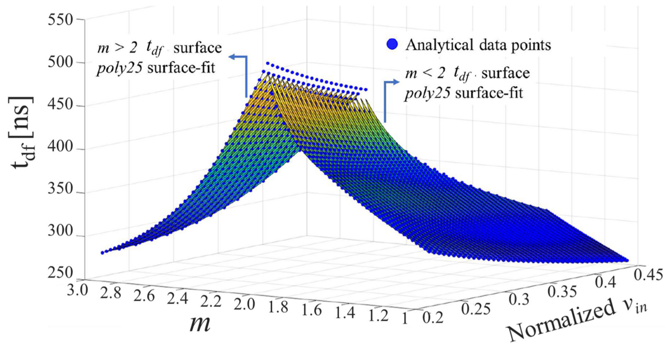
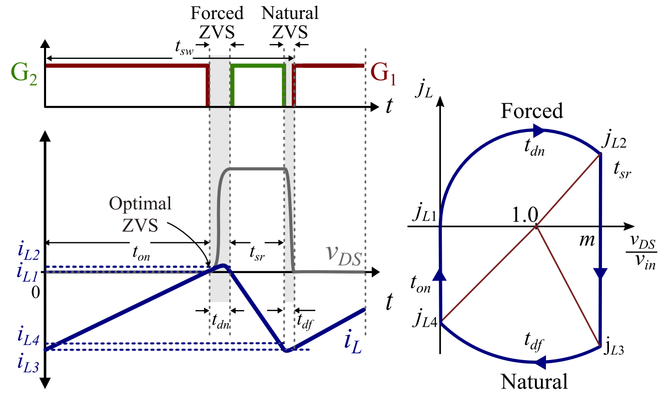


Fig. 11. Illustration of the forced ZVS dead time fitting approach.



(a) (b)

Fig. 12. Minimum-conduction ZVS-QSW for reverse power-flow: (a) operating waveforms and (b) normalized state-plane diagram.

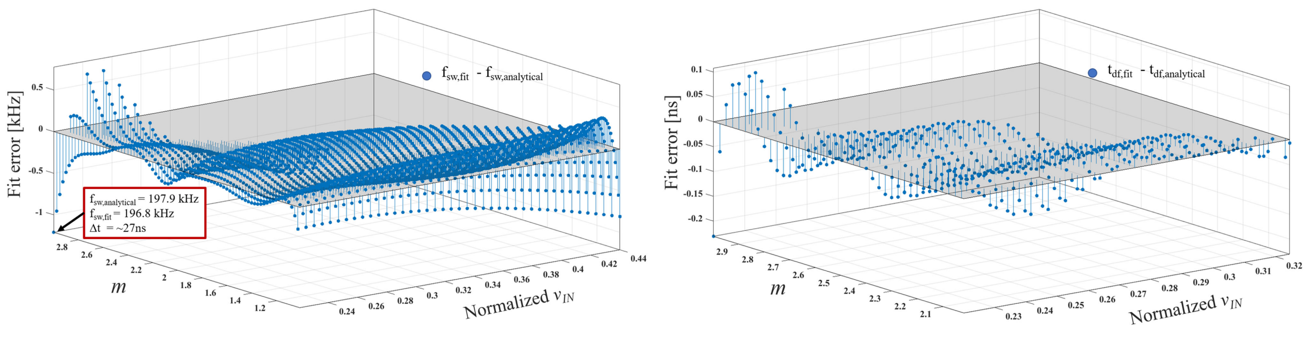
cubic-fit shown as

$$p_{ij} = a_{ij,1}\left(\frac{1}{I_{L,\text{avg}}}\right)^3 + a_{ij,2}\left(\frac{1}{I_{L,\text{avg}}}\right)^2 + a_{ij,3}\left(\frac{1}{I_{L,\text{avg}}}\right) + a_{ij,4}$$
$$(i = 0, 1, 2, \quad j = 0, 1, \ldots, 5 \quad i + j <= 5). \tag{4}$$

The forced ZVS dead time interval analytical models are fit using two *poly25* surfaces corresponding to the two conversion ratio ranges $m > 2$ and $m \leq 2$. The online optimization in the microcontroller implementation applies the appropriate fit during run-time depending on sensed input and output voltages and the corresponding conversion ratio m. Fig. 11 illustrates the t_{df} fit approach.

B. Extension to Bidirectional Power Flow

When the power flow reverses, the polarity of the average inductor current flips, and the converter operates in the buck mode. The converter operating waveforms and the minimum-conduction ZVS-QSW state-plane diagram of Fig. 2 are redrawn in Fig. 12 for reverse power flow. The converter processes the same power since the absolute value of i_{Lavg}, and the input/output voltages are equal in both cases. The waveforms indicate that a polarity reversal in the inductor current also flips the definitions of the main and the SR switch. Flipping the switch definitions implies that the natural and the forced ZVS transition intervals also flip. For an average negative polarity, the inductor current must now make a small positive excursion to ensure ZVS turn-ON for the switch Q_2. The corresponding state-plane representation for reverse power flow in Fig. 12(b) keeps the definitions of the time intervals and instantaneous current labels consistent with the forward power flow. The forced ZVS dead time interval flips to the $j_L > 0$ region of the plot and must be applied to the top switch Q_2. Further inspection of the state-plane diagram and the analytical solution for reverse power flow reveals that the optimal timing parameters are identical in both cases, given the same v_{IN}, v_{OUT}, and $|i_{L,\text{avg}}|$. The analytical models and the curve fitting approaches developed in the previous sections are therefore independent of the current polarity. It may also be observed that since the converter mode of operation is defined based on the magnitude of the current at the rectifier turn-OFF instant, the continuous and boundary conduction modes of operation also flip with the current polarity. Nevertheless, there is no impact on the optimal timing parameters since the definition of the



(a) (b)

Fig. 13. Residual plots for *poly25* fits against analytical models for (a) optimal f_{sw} with $i_{L,\mathrm{avg}} = 20A$ and (b) optimal t_{df} in $m > 2$ boundary conduction mode.

conversion ratio ($v_{\mathrm{OUT}}/v_{\mathrm{IN}}$ where $v_{\mathrm{OUT}} > v_{\mathrm{IN}}$) is consistent in both modes. As indicated in the control architecture of Fig. 3, the feed-forward loop operates with $|i_{L,\mathrm{avg}}|$, generates the optimal timing parameters, and applies t_{df} appropriately to the switch undergoing the forced ZVS transition.

C. Evaluation of the Curve-Fit Approach

Residual plots offer an insightful method to evaluate the fit performance and compare different fit models. Residuals are the differences between the analytical data and fit data. Fig. 13(a) plots the residuals from the *poly25* fitting of the analytical f_{sw} surface with $i_{L,\mathrm{avg}} = 20\mathrm{A}$, and Fig. 13(b) plots the dead time residuals for the $m > 2$ boundary conduction mode surface. In both plots, the residuals are scattered around zero without displaying a systematic pattern, demonstrating that the *poly25* model fits the analytical data well. Furthermore, the relatively low magnitude of the residuals indicates a high degree of accuracy between the fit and the analytically determined optimal timing parameters. To evaluate the impact of a frequency residual on converter operation, it is useful to consider the impact of the residual on the switching period. As an example, the highest residual of around 1kHz on the 20-A frequency model surface of Fig. 13(a) results in a difference of around 30ns in the switching period at the analytically calculated frequency of 197.9kHz. Compared to the optimal forced ZVS dead time intervals of $250 - 550ns$, 30ns differences in the switching period have a negligible impact on the ZVS transitions. The fitting errors of less than 1ns in the dead time are smaller than the controller's minimum adjustable dead time of 2.5ns. The residuals may also be converted to fixed percentage errors that are independent of the analytical timing parameters. The 1-kHz frequency residual, for example, represents an 0.55% error in the switching period.

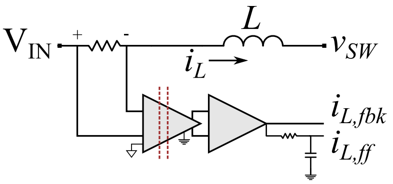


Fig. 14. Inductor current sensing strategy.

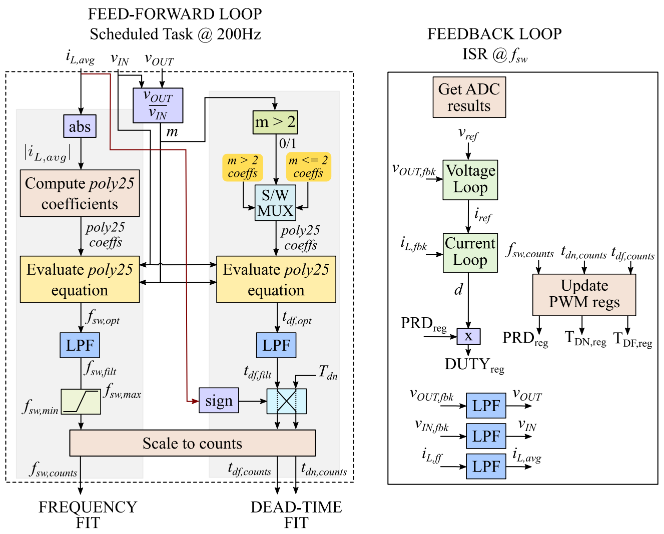


Fig. 15. Controller implementation flowchart.

D. Current Sensing and Microcontroller Implementation

Fig. 14 illustrates the inductor current sensing strategy. Both the feedback and the feed-forward loops utilize the output from a common sensing circuit. The sensing circuit consists of an isolated current-sense amplifier [38] followed by a differential amplifier stage. The isolated amplifier limits the circuit bandwidth to 950kHz. Due to the limited bandwidth of the sensing circuit, the feedback signal is subject to variable operating-point delays, which makes it more challenging to obtain a precise average value of the sensed inductor current. The low-pass filtered version of the sensed signal is therefore provided as a separate input to an independent ADC channel. The corner frequency of the analog filter is placed at around 1kHz. This signal is further filtered digitally to generate a digital representation of the average inductor current, which is then used as an input to the feed-forward loop, as shown in Figs. 3 and 15.

Fig. 15 shows a flowchart of the microcontroller implementation of the online-optimization approach. The high-bandwidth feedback loop is executed in an interrupt service routine (ISR) triggered at the controller sampling frequency, which equals the converter switching frequency. The sampling frequency varies as the converter switching frequency is adjusted. The ISR gets the ADC results, executes the voltage and the current loop compensator calculations, evaluates the duty cycle command, and updates the PWM duty-cycle register based on the PWM period register. Additionally, the ISR also applies digital low-pass filters on the sensed ADC values to provide the feed-forward optimization loop with average values of the sensed converter signals.

The low-bandwidth feed-forward loop can tolerate a certain amount of jitter between execution intervals and is therefore implemented outside the interrupt context in the main thread as a 200-Hz scheduled task. The task sequentially performs the frequency and dead time optimization steps. Online frequency optimization executes the frequency-fit steps of Section IV-A in reverse. The controller first computes the 15 *poly25* coefficients from cubic-fit functions of the sensed average inductor current's absolute value. Using these coefficients and the sensed input and output voltages, the controller determines the optimal switching frequency by evaluating the *poly25* surface-fit equation. The optimal forced ZVS dead time is then calculated by evaluating another *poly25* equation with the appropriate set of coefficients depending on the conversion ratio. The natural ZVS dead time is set to a constant value that ensures safe operation without shoot-through in all operating conditions. To ensure that the feed-forward timing parameters are modified smoothly through incremental changes, the optimal timing parameters are applied to the converter through digital low-pass filters with a conservatively designed corner frequency of approximately 6Hz to minimize the impact on the feedback loops while providing sufficiently fast updates to the timing parameters in response to changes in operating conditions. The variables for natural and forced ZVS dead times are updated based on the inductor current polarity. The PWM registers are updated inside the feedback loop interrupt right before the computation of the duty cycle counts to ensure integrity of the duty cycle with varying switching frequency.

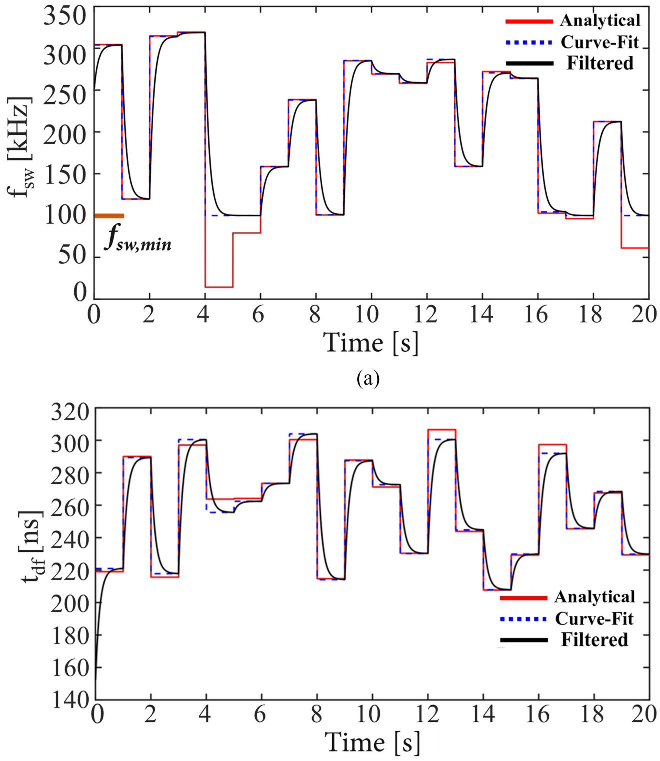
The online-optimization strategy collectively for the two parameters requires storing 90 floating-point coefficients (50 cubic-fit and 30 *poly25* coefficients) and computation of 17 curve-fit equations (15 cubic-fit and two *poly25*) in addition to evaluating exponents of the input parameters. These requirements are relatively small for modern microcontroller architectures [39]. The overall execution time of 20μ s for the optimization algorithm (with feedback interrupts disabled) measured on the utilized controller platform is only a small fraction of the period of the 200-Hz feed-forward loop execution rate. Additionally, a 200-MHz clock of the controller platform (see Table I) allows for a 5-ns resolution in period adjustment that is adequate for a 100 to 400kHz switching frequency range considered in this application.

E. Offline Validation of the Online-Optimization Strategy

Before implementing the optimization approach on the hardware prototype, an offline validation of the algorithm is performed by feeding the feed-forward optimization loop with a vector of arbitrarily generated signals representing input/output voltages and average inductor currents. The values received by the 200-Hz feed-forward loop are updated every second. The results for frequency and dead time offline validation are shown in Fig. 16(a) and (b), respectively. The curve-fit timing parameters represented by dashed lines closely match the analytical values shown in bold red. The low-pass filtered values of the timing

TABLE I
BOOST CONVERTER PARAMETERS

Parameter	Value\Specifications
Input voltage, v_{IN}	200 - 400 V
Output voltage, v_{OUT}	v_{IN} - 600 V
Conversion ratio, m	1.1 - 2.5
Output power (Bidirectional), p_{OUT}	1 - 8 kW
Average inductor current (Bidirectional), $\|i_{L,avg}\|$	5 - 30 A
Planar inductor	7.65 µH
Optimal f_{sw} variation	100 - 400 kHz
Optimal t_{df} variation	250 - 600 ns
Fixed T_{dn}	75 ns
Half-bridge module	Cree 900 V, 192 A CPM3-0900-0010A
Controller	TI Delfino TMS320F28379D



(a)

(b)

Fig. 16. Results of offline validation of feed-forward optimization algorithm with arbitrarily generated converter operating conditions for (a) switching frequency $f_{\rm sw}$ and (b) forced ZVS dead time t_{df}.

TABLE II
COMPARISON OF ANALYTICAL AND CURVE-FIT OPTIMAL FREQUENCIES AND DEAD TIMES, TOGETHER WITH MEASURED EFFICIENCIES AT THE STEADY-STATE OPERATING POINTS OF FIGS. 18 AND 19

Operating Point				Analytical values		Curve-fit values		Conduction Mode	Measured Efficiency
Fig.	V_{in}	m	$I_{L,avg}$	F_{sw}	T_{dr}	F_{sw}	T_{dr}		
18(a)	251.6 V	2.4	15.0 A	437.3 kHz	250 ns	400.9 kHz	240 ns	boundary	98.0 %
18(b)	299.1 V	2.0	21.2 A	354.4 kHz	325 ns	353.8 kHz	320 ns	boundary	98.6 %
18(c)	350.2 V	1.4	21.4 A	253.2 kHz	225 ns	253.2 kHz	230 ns	continuous	99.2 %
19	353.4 V	1.4	−21.3 A	252.8 kHz	225 ns	248.3 kHz	230 ns	boundary	99.0 %

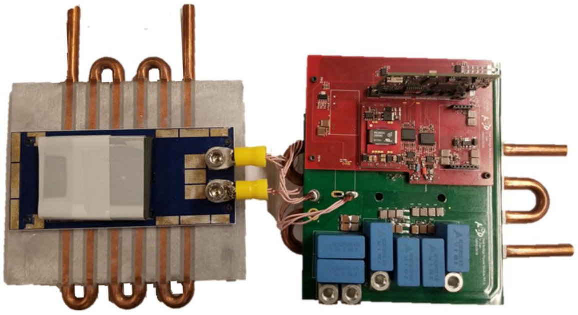


Fig. 17. SiC-based boost converter prototype with a planar inductor. Converter specifications are listed in Table I.

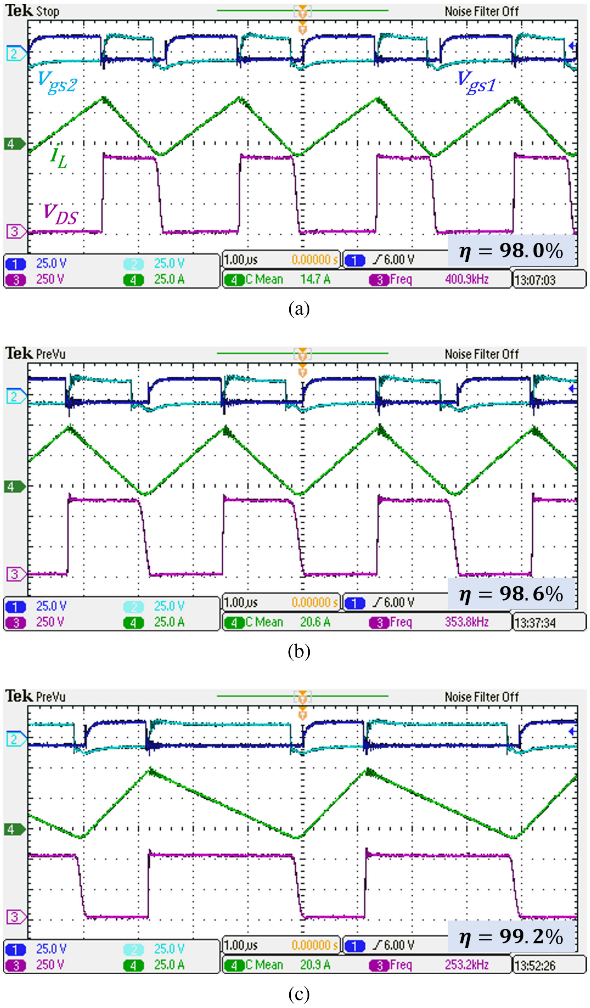
parameters applied in the converter controller are indicated by the black lines. The settling time of approximately one second allows the converter to gradually transition to the new timing parameters. Additionally, one may observe how the curve-fit frequency values are saturated to applicable frequency limits.

V. EXPERIMENTAL VALIDATION

The 8-kW SiC-based boost converter experimental prototype shown in Fig. 17 operates with the parameters and components listed in Table I.

A. *Steady-State Operation and Efficiency at Selected Operating Points*

The converter's closed-loop operation with online frequency and dead time adjustment is verified at different steady-state operating points. The operating points selected demonstrate minimum-conduction ZVS-QSW operation across a wide range of conversion ratios and power levels. Fig. 18(a) and (b) shows converter waveforms at $m > 2$ and $m = 2$ boundary conduction mode, and Fig. 18(c) at $m < 2$ continuous conduction mode. Bidirectional operation (with closed-loop regulation of the low-voltage bus) is validated in Fig. 19 with v_{IN}, v_{OUT}, and $|i_{L,\mathrm{avg}}|$ identical to the operating point of Fig. 18(c). Table II lists the specific operating points with the expected analytical and online-adjusted optimal timing parameters, along with the measured efficiency for each operating point. The online-adjusted curve-fit timing parameters closely match the optimal values predicted by the analytical models at all operating points. The only exception is the $250 - 600V$, 3.7kW point of Fig. 18(a), where the optimal switching frequency exceeds the 400-kHz ceiling. The switching frequency is clamped to 400 kHz resulting in a slightly suboptimal ZVS operation. At all other operating points, the converter achieves near-ideal minimum-conduction



(a)

(b)

(c)

Fig. 18. Converter operating waveforms with the online-optimization strategy at (a) 250–600V, 3.7kW, (b) 300–600V, 6.3kW, and (c) 350–500V, 8.0kW.

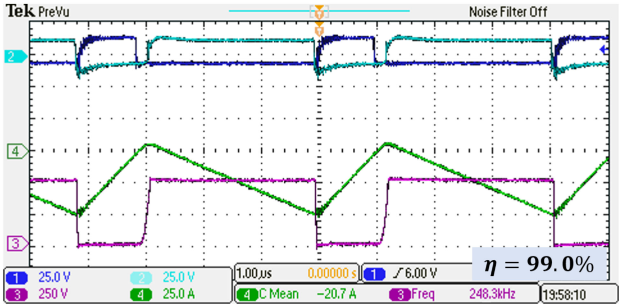
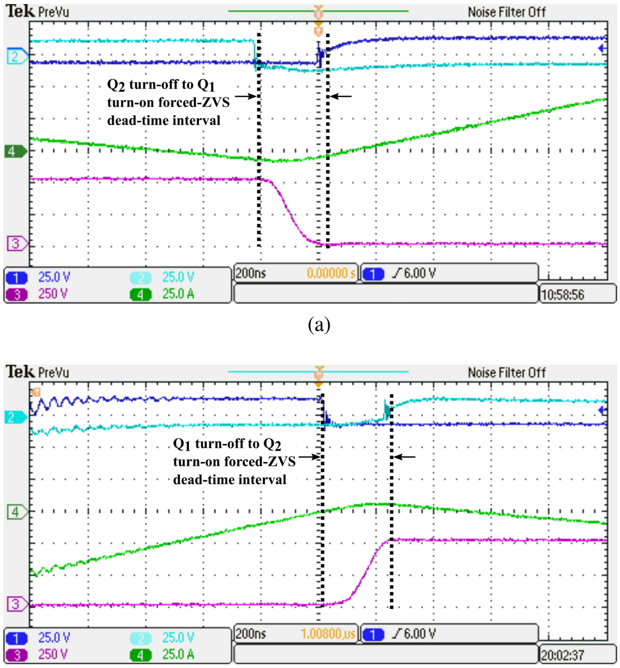


Fig. 19. Converter operational waveforms with the online-optimization strategy at 350–500V, -8.0kW.



(a)

(b)

Fig. 20. Magnified forced ZVS transitions at 350–500V, 8kW for (a) forward and (b) reverse power flow.

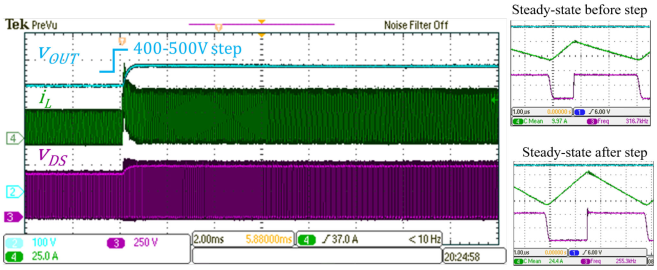


Fig. 21. Closed-loop transient response with feed-forward optimization for a voltage reference step from 400 to 500V.

ZVS-QSW operation. Fig. 20(a) and (b) magnifies the forced ZVS intervals in forward and reverse power flow, respectively. The switches undergoing forced ZVS intervals flip with the inductor-current polarity but operate with near-identical timing parameters, confirming applicability of the optimization strategy to bidirectional power flow. It is evident that online efficiency optimization control strategy enables high efficiency at all considered operating points.

B. Transient Operation With Online Optimization

Fig. 21 captures the converter's closed-loop transient response for a step change in the output voltage reference from 400 to 500V, with the input voltage fixed at 300V. This output voltage step results in a corresponding step in the output power from 3 to 7.5kW. The results confirm that voltage regulation is unaffected by the feed-forward optimization of timing parameters. The overshoot of about 25% in the inductor current results in a short settling time of about a millisecond for the output voltage. Before the transient is applied, the converter operates with optimal timing parameters of 316.7kHz and 230n s with a measured steady-state efficiency of 99.1%. Postapplication of the step-reference transient, the converter settles at the new optimal values of 255.3kHz and 255n s over around 100m s time interval to a new steady state with a measured efficiency of 98.9%. The waveform inserts in Fig. 21 that illustrate the steady-state operation before and after the transient confirm that the converter maintains minimum-conduction ZVS-QSW operation with changing operating conditions.

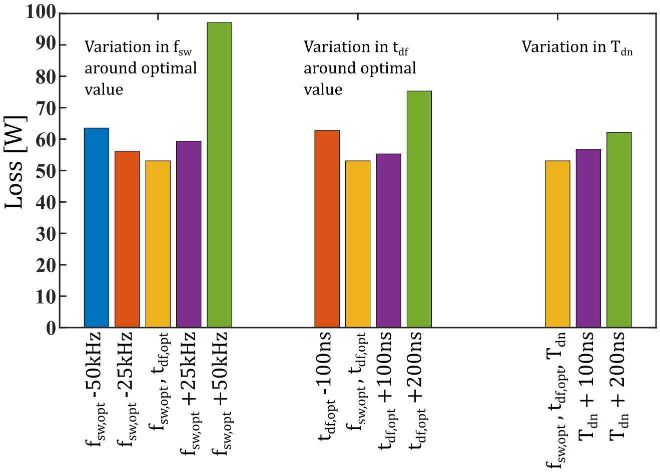


Fig. 22. Impact of varying each timing parameter (f_{sw}, t_{df}, and T_{dn}) from the minimum-conduction ZVS-QSW optimal values ($f_{\mathrm{sw,opt}} = 297.6$kHz, $t_{df,\mathrm{opt}} =$ 230n s) on measured converter losses. The losses are measured at the operating point $v_{\mathrm{IN}} = 350V$, $v_{\mathrm{OUT}} = 500V$, and $p_{\mathrm{OUT}} = 6kW$.

C. Impact of Online Optimization on Converter Losses

Fig. 22 illustrates the impact of varying the timing parameters (f_{sw}, t_{df}, and T_{dn}) away from the minimum-conduction ZVS-QSW optimal values on measured converter losses at a fixed operating point with v_{IN}, v_{OUT}, and p_{OUT} set to 350V, 500V, and 6kW, respectively. The first set of bar plots shows converter losses when the switching frequency is varied by ±25 and ±50kHz from the optimal value of $f_{\mathrm{sw,opt}} = 297.6kHz$. In the second set, the forced ZVS dead time is varied by ±100 and 200n s around the optimal value of 230n s. Both sets of experiments show that the converter losses increase as the timing parameters deviate from the optimal values. Operating at switching frequencies higher than $f_{\mathrm{sw,opt}}$ has a severe impact on efficiency due to turn-ON switching losses, whereas lower values of f_{sw} achieve ZVS at the cost of increased conduction losses. The converter hard-switches (either partially or fully) for both insufficient and excessive t_{df} values. The third set of bar plots vary the natural-ZVS dead time interval T_{dn}. Starting from a nominal value that prevents shoot-through conduction between the switches, large variations in this dead time interval results in relatively small increases in the losses that can be attributed to increased conduction times of the SR body diode. Given the high peak currents in this application, the optimal natural ZVS dead time intervals tend to lie in the relatively small range of 10 to 50n s. This parameter may therefore be fixed to a minimum value that

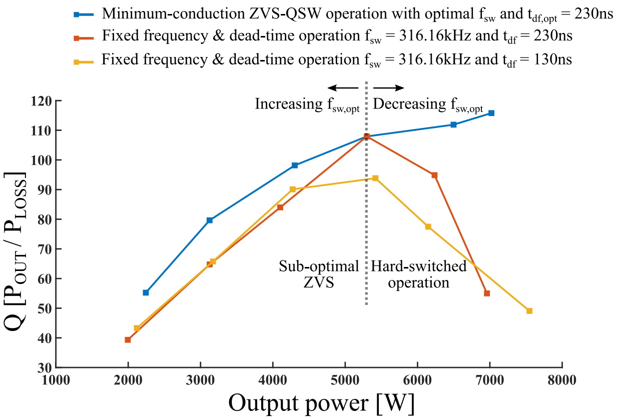


Fig. 23. Measured converter $Q = P_{\mathrm{OUT}}/P_{\mathrm{loss}}$ for online-optimized minimum-conduction ZVS-QSW operation in comparison with conventional fixed-frequency operation for $v_{\mathrm{IN}} = 350V$, $v_{\mathrm{OUT}} = 500V$ and converter power varied from 2 to 7kW.

ensures safe operation at all operating points. Fig. 22 indicates that for a converter to maintain high efficiency with varying operating conditions, online adjustment of both the switching frequency and the forced ZVS interval is vital.

Fig. 23 compares the measured converter Q, defined as

$$Q = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{loss}}} = \frac{\eta}{1-\eta} \tag{5}$$

where η is the converter efficiency, for the case when the converter is operating with optimal timing parameters and for the case when the converter is operated conventionally, with fixed frequency and dead time values. With the converter input and output voltages fixed at 350 and 500V, the output power levels are varied from 2 to 7kW. The optimal dead time (independent of power) is 230ns. The fixed frequency is set to 316kHz, which equals the optimal value at 5kW, and the fixed dead times are set to 230 and 130ns, respectively. The results in Fig. 23 reconfirm that achieving wide-range high efficiencies requires varying both the switching frequency and the forced ZVS dead time of the converter. Conventional fixed-frequency operation (even with dead time optimization, as in [21] and [30]) results in significantly lower Q at higher power operating points due to partial/full hard-switching. At lower power levels with higher optimal frequencies, the fixed frequency operation results in increased negative Q_2 turn-OFF currents with suboptimal ZVS and higher conduction losses. Consequently, optimization strategies that vary switching frequency by conservatively fixing the peak negative SR turn-OFF current [25], [26] result in increased conduction losses. These losses tend to be particularly significant for $m > 2$ boundary-conduction mode, where it is necessary to turn OFF Q_2 at zero current to achieve minimum-conduction ZVS operation. The plots of Fig. 23 also indicate the benefits of dead time optimization. At 5-kW power level, where the fixed and the optimal frequencies are equal, a shorter than optimal dead times results in a lower Q due to increased switching losses. This trend continues at higher power levels, where insufficient dead times lead to hard-switching of higher v_{DS} voltages.

TABLE III
COMPARISON OF EFFICIENCY PERFORMANCE

Reference	V_{IN} **[V]**	m	η **[%] at 50% Rated Power**	Q
This work	250	2.4	98.0	49.0
[15]	300	2.7	96.1	24.6

The converter achieves 99% efficiency for $m < 2$ conversion ratios over a wide power range, which compares well to the similarly high-efficiency results reported in [14] and [20] at relatively low step-up ratios. For higher step-up ratios ($m > 2$), as shown in Table III, a significantly higher efficiency and the converter Q increased by a factor of 2 are measured compared to the state-of-the-art boost converter described in[15].

VI. CONCLUSION

Minimum-conduction zero-voltage switching quasi-square wave (ZVS-QSW) mode of operation enables optimal zero-voltage switching maximizing efficiency at a given operating point but requires precise adjustment of both the converter switching frequency and dead times. This article presents an online efficiency optimization strategy that dynamically adjusts the switching frequency and forced ZVS dead times in a feed-forward manner to achieve minimum-conduction ZVS-QSW operation over wide ranges of input and output voltages, and power levels. This feed-forward optimization operating in conjunction with feedback regulation determines the optimal timing parameters through multivariate polynomial curve fitting of analytical models constructed from solutions of the minimum-conduction ZVS-QSW state planes. Taking into account the equivalent switch node capacitance at each operating point, the analytical models comprehensively capture the variation in optimal timing parameters over the complete region of converter operation. Multivariate curve fitting of these models yields easily implementable polynomial expressions that predict the optimal timing parameters as functions of input voltage, converter conversion ratio, and average inductor current with a straightforward extension to bidirectional power flow.

The proposed online-optimization approach is validated on a 8-kW SiC boost prototype. Minimum-conduction ZVS-QSW operation of the converter is verified at selected operating points with diverse input voltages, conversion ratios, and power levels in both directions. The online-adjusted timing parameters closely match the optimal values from the analytical models. The prototype demonstrates significant performance improvements over conventional fixed-frequency and dead time approaches, and achieves efficiencies greater than 97.5% for input voltages ranging from 200 to 400 V, step-up conversion ratios up to 2.5, and power levels between 2 and 8 kW. Furthermore, efficiencies greater than 99% are measured over wide power levels for conversion ratios less than 2. Examining the converter's transient response confirms that the feed-forward optimization has no impact on the closed-loop operation and achieves minimum-conduction ZVS-QSW operation under varying operating conditions.

The systematic approach to developing analytical models, the resulting curve fitting process, and the implementation techniques presented in this article can be applied to other converter topologies.

APPENDIX
ANALYTICAL MODELS FOR MINIMUM-CONDUCTION ZVS-QSW OPERATION

This section presents a step-by-step approach in MATLAB to developing the analytical models for minimum-conduction ZVS-QSW optimal timing parameters over the converter's full range of operation. The optimal timing parameters in the analytical models are obtained by numerically solving the minimum-conduction ZVS state-plane equations of the converter subject to operating point constraints (values of m, equivalent switch node capacitance, and average inductor current).

Step 1: Create the input parameter coordinate system

The vectors for input and output voltages and the average inductor current are set up as follows:

$$vin\_vec = 200, 205, \ldots, 400$$

$$vout\_vec = 200, 205, \ldots, 600$$

$$iL\_vec = 5, 10, \ldots, 50.$$

The input coordinate system $(v_{\text{IN}},\ v_{\text{OUT}},\ i_{L,\text{avg}})$ consisting of all combinations of the three operating-point variables can be created using the function

$$[v_{\text{IN}},\ v_{\text{OUT}},\ i_{L,\text{avg}}] = \text{meshgrid}(vin\_vec,\ vout\_vec,\ iL\_vec).$$

Each input variable is stored as a three-dimensional (*row*, *column*, *page*) matrix. The size of the each dimension is equal to the length of the corresponding vector. As an example, accessing each of the three matrices with an index $(31,\ 61,\ 4)$ results in an operating point with $v_{\text{IN}}, v_{\text{OUT}}$, and $i_{L,\text{avg}}$ equal to 350, 500, and 20A, respectively. Evaluating conversion ratio m at every output/input voltage combination transforms the original coordinate system to the $(v_{\text{IN}},\ m,\ i_{L,\text{avg}})$ system.

Step 2: Compute the charge-equivalent switch node capacitance

For a given output voltage in a boost converter, the charge equivalent switch node capacitance $C_{\text{eq},Q}$ follows from (1). The calculation of this capacitance, as detailed in [36], requires extracting the device capacitance as a function of drain-to-source voltage from the device datasheet, plotting the equivalent switch node capacitance curve, and numerically integrating this curve to evaluate the area under the curve. The charge-equivalent capacitance is computed for each value in the $vout\_vec$. For the devices in the experimental prototype, this capacitance is plotted as a function of the output voltage in Fig. 7.

Step 3: Solution using the state plane

The minimum-conduction ZVS-QSW state plane requires $v_{\text{IN}},\ v_{\text{OUT}},\ i_{L,\text{avg}},\ C_{\text{eq},Q}$, and the constant inductance value L. The state-plane diagram is solved numerically to obtain the optimal timing parameters f_{sw} and t_{df}. The voltage and current normalization factors i_B and v_B are shown in the $m < 2$ state plane of Fig. 24 as an example.

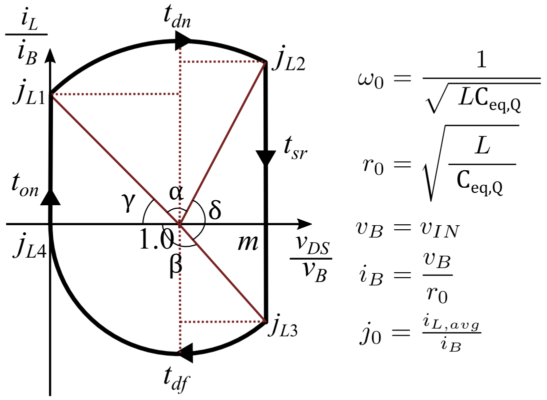


Fig. 24. State-plane diagram example for $m < 2$ continuous conduction mode, with state-plane angles and normalization factors shown.

The state-plane equations derived in [18] are rearranged in terms of the unknown quantities j_{L1}, j_{L2}, j_{L3}, j_{L4}, and $f_{\text{sw,opt}}$. The minimum-conduction ZVS requirement reduces the number of unknown quantities by imposing the mode-dependent constraints

$$j_{L4} = 0, \quad \text{for } m < 2$$

$$j_{L4}, j_{L3} = 0, \quad \text{for } m = 2$$

$$j_{L3} = 0, \quad \text{for } m > 2.$$

The function $vpasolve$ is used to numerically solve the system of equations for the specified unknown quantities. The unknown quantities in the state plane all lie in the interval $[0\ \infty]$ that may be specified as a search-range parameter to $vpasolve$. The numerical solver outputs the normalized inductor currents and the optimal frequency $f_{\text{sw,opt}}$. The forced ZVS dead time interval t_{df} is obtained by denormalizing the state-plane angle β found from the solutions for j_{L3} or j_{L4}. For the boost converter, β is given as

$$\beta = \begin{cases} \frac{\pi}{2} + \text{atan}(\frac{m-1}{j_{L3}}), & \text{for } m < 2 \\ \pi, & \text{for } m = 2 \\ \frac{\pi}{2} + \text{atan}(\frac{1}{j_{L4}}), & \text{for } m > 2 \end{cases}.$$

An important point to note is that the values of m passed to the solver may vary from 0.5 to 3 since v_{OUT} varies from 200 to 600V. Since the state-plane diagrams considered here are valid only for the boost mode of operation with $m > 1$, a precondition check is implemented before invoking the numerical solver.

Step 4: Trimming the data and plotting the model results

The optimal timing parameters $f_{\text{sw,opt}}$ and $t_{df,\text{opt}}$ are evaluated at every point in the coordinate system of the input variables. The invalid operating point $(m < 1)$ solutions are excluded from the solutions by replacing them with NaN. Points exceeding any other limitations, such as conversion ratio range, or power limits may be excluded similarly.

The model results are plotted using the *surf* function. Each surface corresponds to all valid analytical solutions on a specific page for a particular $i_{L,\mathrm{avg}}$ in $f_{\mathrm{sw,opt}}$ and $t_{df,\mathrm{opt}}$ matrices. Since all pages in the $t_{df,\mathrm{opt}}$ matrix are identical, only one needs plotting.

ACKNOWLEDGMENT

The views and opinions expressed in this article do not necessarily state or reflect those of the United States Government or any agency thereof. The work presented in this article is an extension of the approach introduced in [30]. A detailed treatment of analytical models and curve fitting approaches is presented here in addition to extending the approach for bidirectional power flow. Additional experimental results are provided that demonstrate efficiency improvements over conventional fixed-frequency approaches.

REFERENCES

[1] J. W. Kolar, J. Biela, and J. Minibock, “Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency vs. 7 kW/dm^3 power density,” in *Proc. IEEE 6th Int. Power Electron. Motion Control Conf.*, 2009, pp. 1–21.

[2] X. Li *et al.*, “Achieving zero switching loss in silicon carbide MOSFET,” *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12 193–12199, Dec. 2019.

[3] E. A. Jones, F. F. Wang, and D. Costinett, “Review of commercial GaN power devices and GaN-based converter design challenges,” *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[4] A. Anthon, J. C. Hernandez, Z. Zhang, and M. A. E. Andersen, “Switching investigations on a SiC MOSFET in a TO-247 package,” in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, 2014, pp. 1854–1860.

[5] B. Agrawal, L. Zhou, A. Emadi, and M. Preindl, “Variable-frequency critical soft-switching of wide-bandgap devices for efficient high-frequency nonisolated DC-DC converters,” *IEEE Trans. Veh. Technol.*, vol. 69, no. 6, pp. 6094–6106, Jun. 2020.

[6] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, “Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier,” *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

[7] Q. Huang, R. Yu, Q. Ma, and A. Q. Huang, “Predictive ZVS control with improved ZVS time margin and limited variable frequency range for a 99% efficient, 130-W/in^3 MHz GaN totem-pole PFC rectifier,” *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 7079–7091, Jul. 2019.

[8] X. Ren, Y. Wu, Z. Guo, Z. Zhang, and Q. Chen, “An online monitoring method of circuit parameters for variable on-time control in RM boost PFC converters,” *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1786–1797, Feb. 2019.

[9] D. Shahzad, S. Pervaiz, N. Zaffar, and K. K. Afridi, “Control of a GaN-based high-power-density single-phase online uninterruptible power supply,” in *Proc. 20th Workshop Control Model. Power Electron.*, 2019, pp. 1–6.

[10] Q. Huang and A. Q. Huang, “Variable frequency average current mode control for ZVS symmetrical dual-buck H-bridge all-GaN inverter,” *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4416–4427, Dec. 2020.

[11] D. Neumayr, D. Bortis, E. Hatipoglu, J. W. Kolar, and G. Deboy, “Novel efficiency-optimal frequency modulation for high power density DC/AC converter systems,” in *Proc. IEEE 3rd Int. Future Energy Electron. Conf. ECCE Asia*, 2017, pp. 834–839.

[12] H. Chen, H. Kim, R. Erickson, and D. Maksimović, “Electrified automotive powertrain architecture using composite DC-DC converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 98–116, Jan. 2017.

[13] Y. Gao, V. Sankaranarayanan, E. M. Dede, A. Ghosh, D. Maksimovic, and R. W. Erickson, “Drive-cycle optimized 99% efficient SiC boost converter using planar inductor with enhanced thermal management,” in *Proc. 20th Workshop Control Model. Power Electron.*, 2019, pp. 1–7.

[14] M. Pavlovský, G. Guidi, and A. Kawamura, “Assessment of coupled and independent phase designs of interleaved multiphase buck/boost dc-dc converter for EV power train,” *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2693–2704, Jun. 2014.

[15] S. Christian, R. A. Fantino, R. A. Gomez, Y. Zhao, and J. C. Balda, “High power density interleaved ZCS 80-kW boost converter for automotive applications,” *IEEE Trans. Emerg. Sel. Topics Power Electron.*, to be published, doi: 10.1109/JESTPE.2021.3099408.

[16] C. P. Henze, H. C. Martin, and D. W. Parsley, “Zero-voltage switching in high frequency power converters using pulse width modulation,” in *Proc. 3rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, 1988, pp. 33–40.

[17] K. D. T. Ngo, “Generalization of resonant switches and quasi-resonant DC-DC converters,” in *Proc. IEEE Power Electron. Specialists Conf.*, 1987, pp. 395-403.

[18] D. Maksimovic, “Design of the zero-voltage-switching quasi-square-wave resonant switch,” in *Proc. IEEE Power Electron. Specialist Conf.*, 1993, pp. 323–329.

[19] A. Rodriguez, A. Vazquez, M. R. Rogina, and F. Briz, “Synchronous boost converter with high efficiency at light load using QSW-ZVS and SiC mosfets,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 386–393, Jan. 2018.

[20] M. R. Rogina, A. Rodriguez, A. Vazquez, and D. G. Lamar, “Improving the efficiency of SiC-based synchronous boost converter under variable switching frequency TCM and different input/output voltage ratios,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7757–7764, Nov./Dec. 2019.

[21] V. Yousefzadeh and D. Maksimovic, “Sensorless optimization of dead times in DC-DC converters with synchronous rectifiers,” *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 994–1002, Jul. 2006.

[22] W. Al-Hoor, J. A. Abu-Qahouq, L. Huang, W. B. Mikhael, and I. Batarseh, “Adaptive digital controller and design considerations for a variable switching frequency voltage regulator,” *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2589–2602, Nov. 2009.

[23] K. Wang, H. Zhu, J. Wu, X. Yang, and L. Wang, “Adaptive driving scheme for ZVS and minimizing circulating current in MHz CRM converters,” *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3633–3637, Apr. 2021.

[24] Y. Panov and M. M. Jovanovic, “Adaptive off-time control for variable-frequency, soft-switched flyback converter at light loads,” *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 596–603, Jul. 2002.

[25] T. Konjedic, L. Korošec, M. Truntič, C. Restrepo, M. Rodič, and M. Milanovič, “DCM-based zero-voltage switching control of a bidirectional DC-DC converter with variable switching frequency,” *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3273–3288, Apr. 2016.

[26] J. Baek, W. Choi, and B. Cho, “Digital adaptive frequency modulation for bidirectional DC-DC converter,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5167–5176, Nov. 2013.

[27] S. H. Kang, D. Maksimović, and I. Cohen, “Efficiency optimization in digitally controlled flyback DC-DC converters over wide ranges of operating conditions,” *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3734–3748, Aug. 2012.

[28] Y.-C. Liu, Y.-L. Syu, N. A. Dung, C. Chen, K.-D. Chen, and K. A. Kim, “High-switching-frequency TCM digital control for bidirectional-interleaved buck converters without phase error for battery charging,” *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2111–2123, Sep. 2020.

[29] Y. Zhang, C. Chen, T. Liu, K. Xu, Y. Kang, and H. Peng, “A high efficiency model-based adaptive dead-time control method for GaN HEMTs considering nonlinear junction capacitors in triangular current mode operation,” *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 124–140, Mar. 2020.

[30] D. Lyu *et al.*, “Extended off-time control for CRM boost converter based on piecewise equivalent capacitance model,” *IEEE Access*, vol. 8, pp. 155 891–155901, 2020.

[31] Z. Zhang, H. Lu, D. J. Costinett, F. Wang, L. M. Tolbert, and B. J. Blalock, “Model-based dead time optimization for voltage-source converters utilizing silicon carbide semiconductors,” *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8833–8844, Nov. 2017.

[32] H. N. Le and J.-I. Itoh, “Wide-load-range efficiency improvement for high-frequency SiC-based boost converter with hybrid discontinuous current mode,” *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1843–1854, Feb. 2018.

[33] *Curve Fitting Toolbox User’s Guide*, *version 3.5.12*, The MathWorks, Inc., Natick, MA, USA, 2020.

[34] V. Sankaranarayanan, Y. Gao, R. W. Erickson, and D. Maksimovic, “Online efficiency optimization of a closed-loop controlled SiC-based boost converter,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 285–291.

[35] L. Corradini, D. Maksimovic, P. Mattavelli, and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*. Hoboken, NJ, USA: Wiley, 2015.

[36] D. Costinett, D. Maksimovic, and R. Zane, “Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies,” *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 985–995, Feb. 2015.

[37] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, “ZVS of power MOSFETs revisited,” *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[38] *Isolated Amplifier for Current Shunt Measurement*, Skyworks, 2021. [Online]. Available: https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/data-sheets/si8920-datasheet.pdf

[39] *TMS320F2837xD Dual-Core Microcontrollers*, Texas Instruments, 2019. [Online]. Available: https://www.ti.com/lit/gpn/tms320f28379 d

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