Measurement-Based Identification of DC-Link Capacitance of Single-Phase Power Electronic Devices for Grey-Box Modeling

Elias Kaufhold, *Student Member, IEEE*, Jan Meyer, *Senior Member, IEEE*, and Peter Schegner, *Senior Member, IEEE*

***Abstract*—This article presents a non-destructive measurement-based identification of the dc-link capacitance in single-phase power electronic devices for modeling purposes. These devices are typically found in public low voltage networks for low power applications. A large number of manufacturers of these devices with individual approaches to the design of the components of the power electronic devices challenges the modeling and thus the analysis of their interaction with other devices and the low voltage network. Since the manufacturers typically do not disclose their design, only little information based on the assumptions can be made with regard to an individual device. This article provides a new method to identify the dc-link capacitance of single-phase power electronic devices based on analyzing the ripple part of the dc-link voltage, which contributes to the present research activities toward realistic modeling of such devices for power systems studies. The analytical background is provided and a simulative validation is performed. Finally, a laboratory application to a commercially available single-phase inverter for photovoltaic systems is demonstrated in terms of real measurement.**

***Index Terms*—Converters, measurements, modeling, power electronics (PEs), power systems.**

NOMENCLATURE

Symbol	*Definition*
x	Real value.
$\hat{x}$	Amplitude value.
$\underline{x}$	Complex value.
X	Root-mean-square value/magnitude.
$y(x)$	Dependency of y on x.
$\|\mathrm{x}\|$	Absolute value.
$\boldsymbol{x}$	Column vector.
$\boldsymbol{X}$	Matrix.
$\underline{X}^{(\nu\mu)}$	Complex matrix element with the indices ν, μ.

Manuscript received February 18, 2021; revised June 12, 2021 and September 17, 2021; accepted November 2, 2021. Date of publication November 11, 2021; date of current version December 31, 2021. This work was supported by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation)–360497354. Recommended for publication by Associate Editor H. Wang. *(Corresponding author: Elias Kaufhold.)*

The authors are with the Institute of Electrical Power Systems and High Voltage Engineering, Technische Universitat Dresden, 01062 Dresden, Germany (e-mail: elias.kaufhold@tu-dresden.de; jan.meyer@tu-dresden.de; peter.schegner@tu-dresden.de).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3127241.

Digital Object Identifier 10.1109/TPEL.2021.3127241

I. INTRODUCTION

THE share of power electronic (PE) devices in low voltage (LV) networks has increased due to high requirements on the energy efficiency and the aim to fulfill the climate goals. The transition from a small number of centralized energy generators toward a large number of decentralized power generators results in a large variety of different devices. Furthermore, modern loads are increasingly designed with PE front-ends at the grid side. In this study, PE devices are referred to as converters (ac/ac conversion), inverters (dc/ac conversion), and rectifiers (ac/dc). It has become a major research topic to model and analyze the interactions between PE devices and the LV network, particular in the harmonic range [1]. The main reason for this new research field are observations of very high current emissions and the instable behavior of PE devices, namely converters and inverters in LV networks [2], [3] that have been reported first in the Swiss railway grid [4].

Present measurement-based models, i.e., black-box models, are often used for harmonic power flow studies or impedance-based stability assessments. However, they are typically restricted to a small-signal analysis, although they only represent the behavior of the PE device around a specific operating point, e.g., a specific power level or supply voltage distortion. To improve the reliability of power system studies, more detailed models are required that enable realistic conclusions toward current emissions and stability of PE devices in the power system. A promising approach is the use of grey-box models, which separates the device into its main components in terms of the envisaged study and identifies these components individually.

One of these main components of single-phase PE devices is the dc link capacitance, which is directly related to the amplitude of the voltage ripple in the dc link. This voltage ripple is the main cause of the frequency coupling components, which in turn are essential for accurate modeling of a PE device, especially for harmonic studies.

Consequently, the aim of this article is the identification of the dc-link capacitance in single-phase PE devices as one of the main components with the device stability and emission characteristics. Since only one point measurement on the circuit board of the voltage across the switches is required next to knowing the power level of the device, the proposed measurement-based

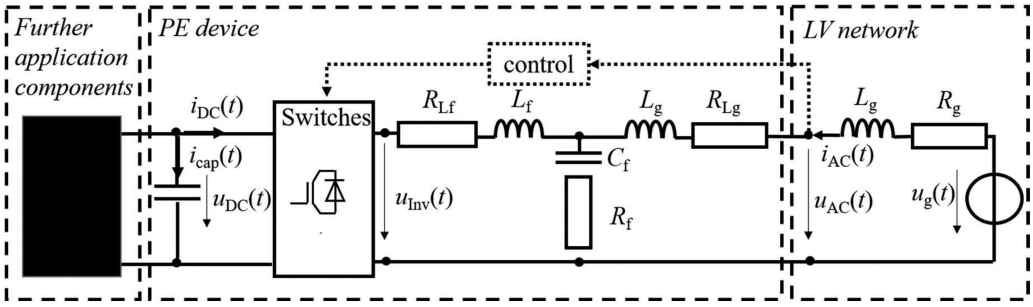

Fig. 1. Scheme of a PE device and the LV network.

identification can be applied in a non-destructive way to commercially available products.

The rest of this article is organized as follows. Section II provides a brief state of the art of modeling. Section III explains the new identification method in terms of its theory, shows simulative results, and demonstrates an application in the laboratory on a commercially available photovoltaic (PV) inverter. Section IV discusses the method. Finally, Section V concludes this article.

II. State-of-the-Art

A. System Model

The system model can be represented in two parts: the PE device and the LV network. As current state of the art, the LV network is often represented as a simple *RL*-circuit for the network impedance $\underline{Z}_g$ while the background distortion is considered in the background voltage in terms of u_g. In more advanced studies, resonances [5] as well as real LV networks have been considered, while in more generic studies, reference network impedances according to *IEC* standards, e.g., [6], [7], are typically chosen. For the individual PE devices, different modeling approaches can be applied based on the available knowledge.

B. Device Modeling Approaches

The choice of the modeling approach is related not only to the available knowledge but also to the required degree of detail of the study and the available computational resources.

1) White-Box Approach: The most detailed approach is the white-box approach. All significant pieces of information about the device are known and the implementation of each device component can be performed accurately. While this leads to very reliable results with a very high degree of detail, the implementation requires a lot of effort, though modular approaches, e.g., [8], have been proposed to reduce the implementation effort. Furthermore, because of the high degree of detail of the model, the time constants for solving white-box models can be tremendous, so that the right solver settings are essential [9].

Fig. 1 shows the scheme of a PE device and the LV network that is exemplarily depicted in terms of an *RL*-equivalent. In particular, the PE device consists typically of semiconductor switches, e.g., an H4 bridge, a grid-side filter, a dc-link capacitor, and a control. Furthermore, on the application side, there can be another converter for the back-to-back topology, e.g., for pulsewidth modulation (PWM) based electric vehicle (EV) chargers for ac connection, or the PE device is simply operated as an inverter on dc basis, e.g., for PV systems and battery storage systems.

2) Grey-Box Approach: Next to the detailed white-box approach, only partial knowledge is required for the grey-box approach. This can be information about the topology or individual parts of the model. Instead of a full detailed representation, individual components can be estimated by using classical control theory, e.g., the Kalman filter [10], [11], and more recently also by using neural networks [12]. An estimation method for the dc-link capacitance by voltage injection is described in [13]. A further methodology for three-phase voltage-source converters is proposed in [14]. It applies the ordinary least squares method to estimate the dc-link capacitance during the converter start-up requires access to the control, which is typically not possible for commercial devices. However, the existing methods are based on invasive procedures and consequently they are difficult to be applied to commercially available devices.

Furthermore, present methods are solely based on estimation models, which in turn require appropriate estimator settings. The authors have developed a non-invasive measurement-based method for the identification of the grid-side filter circuit in single-phase inverters [15]. This article aims to proceed with the grey-box approach by providing a measurement-based identification method for the dc-link capacitance as second out of the three future model elements, i.e., the control will represent the last part and is currently in the research focus, to enable enhanced models of commercially available single-phase inverters for time-domain studies, e.g., for harmonic stability simulations.

3) Black-Box Approach: For the black-box approach, no specific knowledge is required. Often, the pairs of input-output signals are considered, which can be represented by a decoupled Norton model. This model can be represented by the current $\underline{I}_{\mathrm{PED}}$ and the admittance $\underline{Y}_{\mathrm{PED}}$, with the LV network and its network impedance $\underline{Z}_g$ as well as its background voltage $\underline{U}_g$. Both parts interact by means of the voltage $\underline{U}_{\mathrm{AC}}$ and the current $\underline{I}_{\mathrm{AC}}$ at the point of coupling. The even more advanced coupled Norton model can additionally consider the so-called frequency couplings. Frequency coupling implies, that one voltage frequency component $\underline{U}_{\mathrm{AC}}(f)$ at the grid-side terminals leads

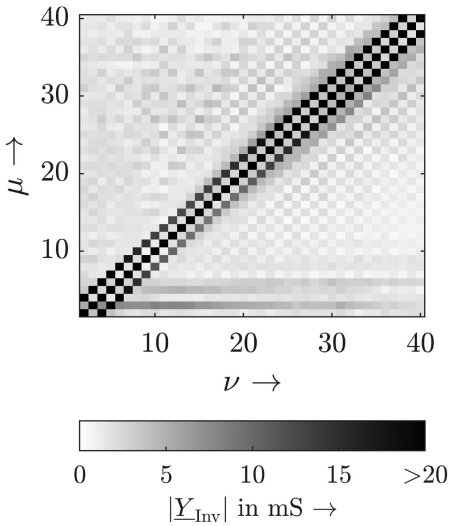

Fig. 2. FCM of a commercially available single-phase PV inverter.

to multiple current frequency components $\underline{I}_{\mathrm{AC}}(f)$. Usually, harmonics (multiples of the fundamental frequency) are chosen as frequencies *f* because modeling harmonic levels and harmonic propagation are the most common research objectives. If from the perspective of a chosen reference-point only one voltage harmonic component of order μ is changed during the *i*th measurement, its change can be related to the changes in the current at all harmonic orders ν and the frequency coupling matrix (FCM) $\underline{\boldsymbol{Y}}$ can be obtained.

To identify the frequency coupling components systematically, a frequency sweep has been proposed in [16] and been extended to also identify phase dependencies [17], [18]. For each measurement *i* (one voltage harmonic at one phase angle and magnitude), the individual matrix elements can be calculated according to

$$\underline{Y}^{(\nu\mu)} = \frac{\underline{I}^{(\nu)}_{\mathrm{ac}\,i} - \underline{I}^{(\nu)}_{\mathrm{ac\,ref}}}{\underline{U}^{(\mu)}_{\mathrm{ac}\,i} - \underline{U}^{(\mu)}_{\mathrm{ac\,ref}}}. \tag{1}$$

As an example, the FCM of the PE device (a PV inverter) that is considered for the later laboratory measurements is shown in Fig. 2. In case multiple values are obtained for a single frequency coupling element (e.g., by applying multiple phase angles and/or multiple magnitudes for one voltage harmonic), the respective frequency coupling element could be expressed, e.g., by a look-up table, an average complex value, a Tensor (e.g., [19]) or a functional relationship.

The decoupled and the coupled Norton model are used for harmonic power flow studies as well as for the formal stability analysis, e.g., following the impedance-based stability criterion. However, they are operating point-dependent and allow only a small-signal analysis. Therefore, a probabilistic approach has been proposed [20] for the formal stability analysis. An alternative modeling approach has been proposed by using the Hammerstein–Wiener model, e.g., [21], [22]. However, this has also only been studied for one operating point.

C. Condition Monitoring

To provide more general models that are also able to reflect the dynamic behavior of the devices, time-domain models are required. Component-based models provide a suitable approach to enable time-domain models for future studies but face the challenge of the device component identification as the present methods are not sufficient for the applicability on most commercially available device.

While the purpose of condition monitoring (CM) is not the component modeling, the measurement-based methods are possibly of use for the identification of the components and their physical values, e.g., the dc-link capacitance. There is a large number of different methods for CM that can be categorized into methods that make use of current sensors with and without current injection, into circuit-based methods, and into methods that are data based [23]. For the application on commercially available devices, non-invasive methods are required that are generally applicable. These non-invasive methods typically use the measurement of the current through the capacitor to identify the equivalent series resistance and the capacitance [24], [25].

In [26], a variable electrical network is developed to perform the CM during the shutdown of the inverter. For rectifiers, a trigger device prototype is developed to measure exactly at 0° and 90° point on wave of the voltage to identify the dc-link capacitance [27]. However, both methods require specific supplemental prototype devices to perform the CM without the measurements of the current through the capacitors while in addition, the self-commutated switching in the inverter will prevent the application of a reliable trigger device prototype as presented in [27] for line-commutated rectifiers.

III. DC-Link Capacitance Identification

The dc-link capacitance is important to buffer the intermittent power flow in single-phase devices between the ac- and the dc-side of a PE device. This accounts not only for inverters but also for converters, since the typical back-to-back topology that is found in low power applications is based on a dc-link consisting of a capacitance only. It should be noted that the proposed method is not intended to be applied to any other dc-link topologies, e.g., based on an inductance or a combination of inductance and capacitance. However, such topologies are usually used in three-phase applications of higher power and traction systems which are not in the scope of this article.

A. Theory

Single-phase inverters for low power applications are usually operated at a displacement factor of about 1. Consequently, the method is based on the assumption that only active power is generated. It should be noted that it can in principle also be extended to consider reactive power. However, this would make it more complex. The ac-side instantaneous power can be calculated with

$$p_{\mathrm{ac}}(t) = -u_{\mathrm{ac}}(t)\, i_{\mathrm{ac}}(t) \tag{2}$$

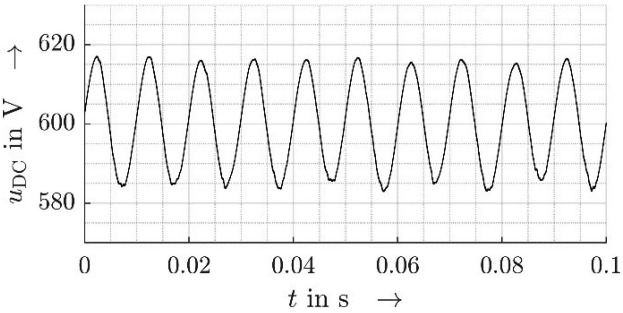

Fig. 3. Voltage across dc-link capacitance u_{dc} in steady-state.

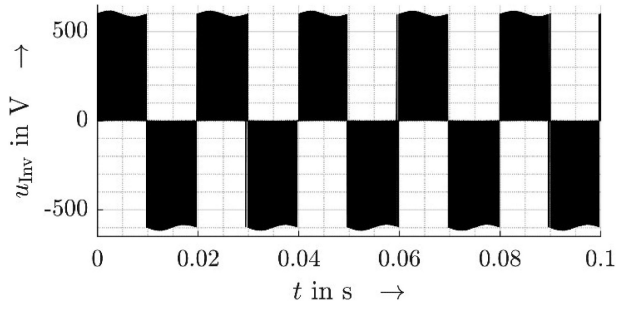

Fig. 4. Simulated voltage u_{Inv} across the semiconductor switches.

and

$$p_{\mathrm{ac}}(t) = -\hat{u}_{\mathrm{ac}}\sin(2\pi f_1 t)\hat{i}_{\mathrm{ac}}\sin(2\pi f_1 t) \tag{3}$$

to

$$p_{\mathrm{ac}}(t) = -\frac{\hat{u}_{\mathrm{ac}}\hat{i}_{\mathrm{ac}}}{2}\left(1-\cos(4\pi f_1 t)\right) \tag{4}$$

with the fundamental frequency f_1 that represents the power frequency of the LV network. This power consists of a steady component, that is provided by the respective application P_{app} (i.e., the PV module) and an alternating power component $p_{\mathrm{cap}}(t)$, which is contributed by the dc-link capacitance. The power balance between ac-side and dc-side

$$p_{\mathrm{dc}}(t) = -p_{\mathrm{ac}}(t) \tag{5}$$

requires

$$p_{\mathrm{dc}}(t) = u_{\mathrm{dc}}(t)\, i_{\mathrm{dc}}(t) = P_{\mathrm{app}} - p_{\mathrm{cap}}(t) \tag{6}$$

and can be reformulated to

$$p_{\mathrm{dc}}(t) = \frac{\hat{u}_{\mathrm{ac}}\hat{i}_{\mathrm{ac}}}{2} - \frac{\hat{u}_{\mathrm{ac}}\hat{i}_{\mathrm{ac}}}{2}\cos(4\pi f_1 t). \tag{7}$$

The alternating part $p_{\mathrm{cap}}(t)$ in the dc-side power requires in addition to a steady component also an alternating (ripple) component in the dc-link voltage $u_{\mathrm{dc}}(t)$, which can be formulated as follows:

$$u_{\mathrm{dc}}(t) = u_{\mathrm{dc\ avg}} + \hat{u}_{\mathrm{dc\ rip}}\sin(4\pi f_1 t) \tag{8}$$

and is depicted in Fig. 3.

The current through the capacitance is calculated as follows:

$$i_{\mathrm{cap}}(t) = C_{\mathrm{dc}}\frac{\mathrm{d}u_{\mathrm{dc}}(t)}{\mathrm{d}t} \tag{9}$$

or rather

$$i_{\mathrm{cap}}(t) = 4\pi f_{\mathrm{ac}} C_{\mathrm{dc}}\hat{u}_{\mathrm{dc\ rip}}\cos(4\pi f_1 t). \tag{10}$$

Taking into account the maximum buffered power of the dc-link capacitance and relate it to the power provided by the application

$$P_{\mathrm{app}} = \max\left(\frac{-\hat{u}_1\hat{i}_1}{2}\cos(4\pi f_1 t)\right) = \hat{p}_{\mathrm{cap}} \tag{11}$$

can be formulated according to (6) and (7). Consequently, it becomes possible to calculate the dc-link capacitance in terms of

$$C_{\mathrm{dc}} = \frac{P_{\mathrm{app}}}{4\pi\, f_1 u_{\mathrm{dc\ avg}}\hat{u}_{\mathrm{dc\ rip}}}. \tag{12}$$

For the calculation, only the measurement of the voltage across the dc-link capacitance or a voltage equivalent to it is needed, e.g., with point measurements on the circuit board. Current measurements that are typically not possible in commercial devices are not required. As the method is considered a measurement-based identification method, no device parameters are required to identify the capacity of the dc-link capacitors.

B. Simulation

After having derived the analytical solution, a white-box simulation is performed to measure the required signals and to verify the proposed method. Although accessible in simulations, in practice, a direct measurement of the dc-link voltage is often not possible, since the connections of the capacitors are isolated as practical experiences with commercial devices have shown by opening the cases. However, the voltage across the semiconductor switches, u_{Inv} in Fig. 1, is usually accessible. This voltage includes additional to the dc ripple voltage also the high-frequency components due to the semiconductor switching of the device.

Based on the double Fourier integral analysis in [28], the spectrum of a full-bridge topology can be calculated according to (15) with the modulation index m_{a}, the carrier frequency f_{car} of the PWM-based switching, the parameter m and the Bessel function of first kind J at order n. Due to the fast decay of the Bessel functions J in terms of

$$J_n(x) = \sum_{k=0}^{\infty}\frac{(n-1)^k\left(\frac{x}{2}\right)^{n+2k}}{k!\Gamma(n+k+1)} \tag{13}$$

with

$$\Gamma(x) = \int_0^{\infty} e^{-t}t^{x-1}\mathrm{d}t \tag{14}$$

the frequency coupling components in the modulation components around the power frequency, i.e., $2f_1$, are negligible. Yet, [28] neglects $u_{\mathrm{dc\ rip}}$ and only considers $U_{\mathrm{dc\ avg}}$ [cf. (8)], it can be seen in Fig. 5 that the ripple in u_{DC} and in u_{Inv} (cf. Figs. 3 and 5) are actually similar, since the losses and thus the voltage drop across the semiconductor switches in conducting state can be neglected. Consequently, also the measurement of u_{Inv} can

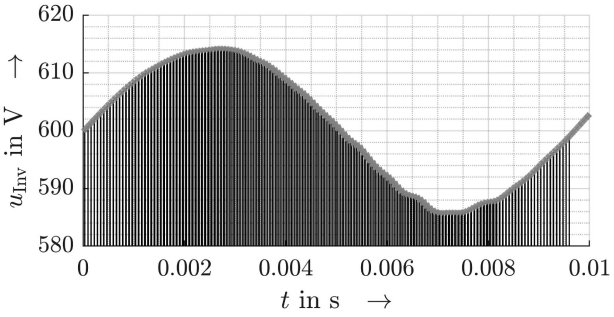

Fig. 5. Detail of simulated voltage u_{Inv} (black) and u_{DC} (gray envelope).

TABLE I
MODEL PARAMETER

Parameter	Value		Parameter	Value
LCL-filter				
L_f	0.04 mH		R_{Lf}	0.008 mΩ
L_g	0.02 mH		R_{Lg}	0.008 mΩ
C_f	5 µF		R_{Cf}	8.2 Ω
Switching frequency			*DC-link capacitance*	
T_{sw}	$\frac{1}{8000}$ s		C_{DC}	400 µF
DC-link voltage control				
$K_{\mathrm{P\,DC}}$	$0.12\frac{C_{\mathrm{DC}}}{T_{\mathrm{sw}}}$		$T_{\mathrm{N\,DC}}$	$17\,T_{\mathrm{sw}}$
$K_{\mathrm{I\,DC}}$	$\frac{K_{\mathrm{P\,DC}}}{T_{\mathrm{N\,DC}}}$			
AC-current control				
$K_{\mathrm{P\,AC}}$	$\frac{L_f+L_g}{3T_{\mathrm{sw}}}$		$K_{\mathrm{I\,AC}}$	$\frac{R_{Lf}+R_{Lg}}{3T_{\mathrm{sw}}}$
$T_{\mathrm{N\,AC}}$	$\frac{K_{\mathrm{P\,AC}}}{K_{\mathrm{I\,AC}}}$			
Phase locked loop (PLL)				
α	2.4		T_{PLL}	$\alpha^2 T_{\mathrm{sw}}$
K_{PLL}	$\frac{1}{\alpha\hat{u}_{\mathrm{AC}}T_{\mathrm{sw}}}$			

be used for the proposed identification method.

$$u_{\mathrm{Inv}}(t) = \frac{4U_{\mathrm{dc}}}{\pi}\sum_{n=1}^{\infty}\frac{J_n\left(n\frac{f_1}{f_{\mathrm{car}}}\frac{\pi}{2}m_{\mathrm{a}}\right)}{n\frac{f_1}{f_{\mathrm{car}}}}\sin\left(n\frac{\pi}{2}\right)\cos(2n\pi f_1 t) + \frac{4U_{\mathrm{dc}}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{q}J_{2n-1}\left(q\frac{\pi}{2}m_{\mathrm{a}}\right) \times\cos\left([m+1-n]\,\pi\right)\cos\left(4m\pi f_{\mathrm{car}}t+[2n-1]\,2\pi f_1\,t\right). \quad (15)$$

The simulation model is based on the parameters according to Table I and with regard to the circuit elements in Fig. 1.

While Figs. 4 and 5 are time-domain representations of u_{Inv}, the frequency spectrum of u_{DC} can also be studied by applying a discrete Fourier transform (DFT). The DFT of u_{DC} is shown in Fig. 6 and calculated based on a 100 ms (5 cycles at 50 Hz power frequency) measuring window, which has been used to identify all values according to (12).

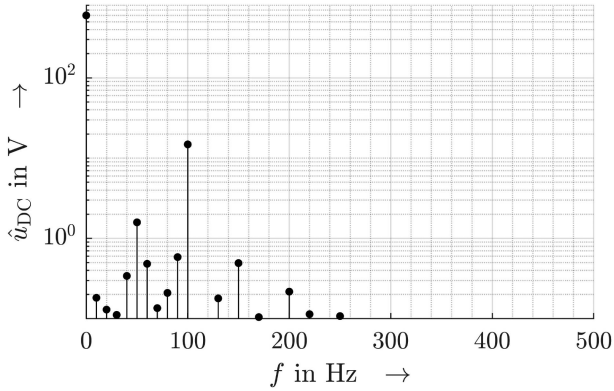

Fig. 6. Discrete Fourier transform of simulated voltage u_{DC} up to 500 Hz.

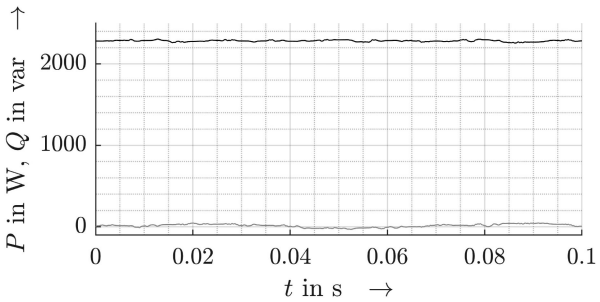

Fig. 7. Simulated active power (black) and reactive power (gray).

A frequency-domain study of $\underline{u}_{\mathrm{Inv}}$ will not lead to an correct the component $\underline{U}_{\mathrm{DC}}(2f_1)$, since the high frequency of the semiconductor switching will also affect the amplitude of the low-frequency components in the voltage spectrum $\underline{U}_{\mathrm{Inv}}(f)$. However, the amplitude $\hat{u}_{\mathrm{DC\ rip}}$ of the dominant $2f_1$ component can also be identified by reconstructing $u_{\mathrm{DC\ rip}}$ based on the envelope of u_{Inv} (see Fig. 5).

The dominant $2f_1$ component (i.e., 100 Hz) becomes present with about 14.91 V and is at least one decade larger than the other frequency components in the voltage besides the dc component. Following (14), the power P_{app} needs to be identified. Based on the current, and the voltage measurements at the inverter terminals, the resulting active and reactive power are depicted in Fig. 7. For the considered 100-ms-window the average P_{app} amounts 2280 W. $U_{\mathrm{DC\ avg}}$ equals 600.01 V. The power frequency of the LV network is set to exactly 50 Hz.

With (14), the dc-link capacitance can be identified by inserting the measured data and the respective values with

$$C_{\mathrm{dc\ sim1}} = \frac{2280\ \mathrm{W}}{4\pi 50\ \mathrm{Hz}\cdot 600.01\ \mathrm{V}\cdot 14.91\ \mathrm{V}} = 405.63\ \mu\mathrm{F}. \quad (16)$$

The simulation allows now to draw a comparison to the implemented value of the capacitance, which is set to exactly $400\ \mu$F. The deviation of about 1% originates mainly from small deviations in the power, e.g., Q is not zero. However, a deviation of 1% for the simulation seems appropriate to consider the theory as valid.

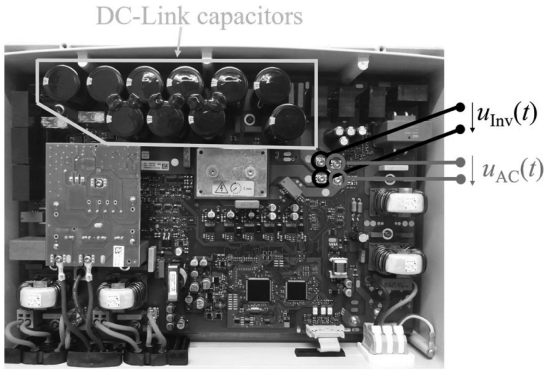

Fig. 8. Commercial inverter with open case.

Another simulation has been performed to study the impact of dc power level on the results. The dc power has been reduced by about 50% to 1100 W, which leads to a maximum dc-level voltage of 607 V and a minimum value of 592.8 V. Consequently, the capacitance value is identified with 410.96 μF. This is about 2% in relation to the implemented value and about another 1% compared to the value determined at nominal dc power. The authors recommend to apply the proposed method in the range of 90% - 100% of the rated inverter power.

A second simulative validation has been performed on another single-phase PV inverter, which is part of the MATLAB/Simulink library and operates at a power frequency of 60 Hz. The dc-link capacity has been implemented with 3 mF, while the measured data have resulted in

$$C_{\mathrm{dc\ sim2}} = \frac{2620\ \mathrm{W}}{4\pi 60\ \mathrm{Hz} \cdot 434.25\ \mathrm{V} \cdot 2.75\ \mathrm{V}} = 2.91\ \mathrm{mF}. \quad (17)$$

C. Laboratory Application

For demonstration purposes, the method is applied to a commercially available single-phase inverter for PV applications. The datasheet provides general information, e.g., about the topology, but no details about specific parameters, e.g., of the circuit, are disclosed. The inverter is shown in Fig. 8 with its open case. Although the dc-link capacitors are visible, their wiring is not identifiable and their capacitance values are not always visible. In addition, manufacturing tolerances can cause significant deviations from the rated capacitance.

1) Measurement Setup: For the laboratory setup, a grid-simulator is used that can emulate the background voltage u_{g}. In order to keep the voltage at the terminals of the inverter as undistorted as possible (as required by the method), a sinusoidal voltage is generated and no additional impedance is applied, i.e., $\underline{Z}_{\mathrm{g}}$ (see Fig. 1) is set to zero.

The sampling rate of the measurement device is 1 MHz. The overall uncertainty of the method is majorly determined by the error of the used measurement equipment. For this article, the uncertainty of the measurement device including all influence factors has been determined experimentally by using a reference calibrator. For u_1 and i_1 the uncertainty for the measured values is below 1%. As the same inputs are used for the dc-side measurements, their error for $u_{\mathrm{DC\ avg}}$ and $\hat{u}_{\mathrm{DC\ rip}}$ is also less than 1%. Based on the uncertainty assessment using Taylor approximation of first degree, P_{app} in (11) can be determined with an error of 2%. The value of C_{DC} is then determined by 4%. This error is much lower than the nameplate uncertainty, which is usually 20%. The impact of further influences, like power losses of inverter is discussed in Section IV.C.

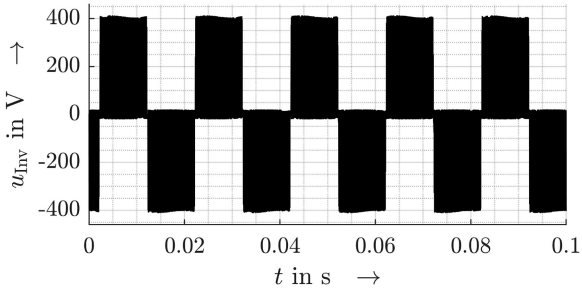

Fig. 9. Measured voltage u_{Inv} across the semiconductor switches.

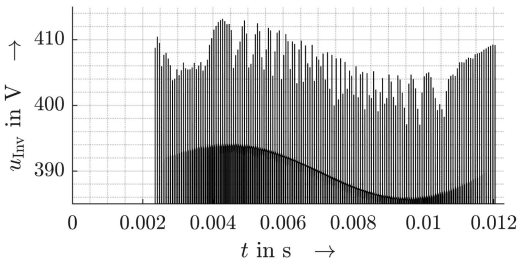

Fig. 10. Detail of the measured voltage u_{Inv}.

2) Measurement Results: As previously for the simulations, the voltage across the switches is measured and shown in Fig. 9. The detail of this voltage in Fig. 10 shows clearly the overvoltages due to the real behavior of the switches, which results from parasitic elements that have been neglected in the simulations.

Still, the underlying voltage with the ripple at $2f_1$ is clearly visible. A value of 4V can be identified for $\hat{u}_{\mathrm{dc\ rip}}$ from the time-domain data (see Fig. 10) and the maximum power point tracker (MPPT) has set the dc-reference such that $U_{\mathrm{dc\ avg}}$ is measured with 390 V (see Fig. 10). The power P_{app} has been set to 2300 W and has been generated by a programmable PV panel simulator. Inserting the measured values into (12) leads to

$$C_{\mathrm{dc\ meas}} = \frac{2300\ \mathrm{W}}{4\pi \cdot 50\ \mathrm{Hz} \cdot 390\ \mathrm{V} \cdot 4\ \mathrm{V}} = 2.347\ \mathrm{mF}. \quad (18)$$

The effect of the ambient temperature on the capacitance has not been studied further, though in literature, the deviation has been identified below 0.8%, e.g., [24].

IV. Discussion

A. Results for DC-Link Capacitance

As expected, the capacitance in the commercial inverter is more conservative than in the simulated inverter. Although the capacitances of both the simulative model and the commercially identified model are in a typical range for single-phase low power inverters. A larger dc-link capacitance will be more expensive but lead to a smaller ripple voltage amplitude $\hat{u}_{\mathrm{dc\ rip}}$. The

reduced ripple voltage amplitude will cause less stress on the dc-link capacitors and reduce the frequency coupling. In contrast, a smaller dc-link capacitance will demand a more dynamic control but at lower costs. Finally, an appropriate trade-off has to be made by the manufacturer.

B. Method Advantages

The proposed method is non-invasive, since it does not require any signal injection or modifications of control parameters. Consequently, the dc-link capacitance can be identified from a retro perspective, i.e., after the manufacturing process of the PE device has been completed. Besides the parameter identification for grey-box models as described in the article, the method can be used for quality control during the production process (e.g., to check the mechanical connection in terms of a parasitic and unwanted behavior) as well as to monitor possible aging of the dc-link capacitors during the operation time without taking the PE device apart. The non-invasive method simplifies the effort for the required measurements, so that next to devices for low power applications, also the dc-link capacitance in PE devices with high power ratings and high dc-voltage levels can be identified. For devices without the above proposed monitoring not being included, the method enables an in-situ identification of the dc-link capacitance while the PE device is in normal operation not requiring to be taken out of service or adding additional devices for the capacitance identification. The method does not require to remove any device component, which could cause the destruction of the device.

C. Impact of Inverter Losses

Next to the addressed measurement uncertainties in Section III-C1, the losses inside the inverter will affect the accuracy of the proposed method. The losses can be considered with P_{loss} by reformulating (12) in terms of

$$C_{\mathrm{dc}} = \frac{P_{\mathrm{app}} - P_{\mathrm{loss}}}{4\pi f_1 u_{\mathrm{dc\ avg}}\, \hat{u}_{\mathrm{dc\ rip}}}. \tag{19}$$

Based on the literature, the maximum losses inside grid-connected single-phase inverters are below 6% [29]. Since the inverter losses contribute directly to the accuracy, the effect of neglecting the inverter losses will also be below 6%.

D. Modeling and Stability Considerations

In many present studies based on white-box models, the dc-link capacitance is often neglected and the dc-link voltage is represented as a stiff voltage source. Considering the dc-link capacitance in such models allows the representation of a more realistic, non-stiff dc-link voltage. This particularly refers to the dc-link voltage ripple, which is typically the main origin of the frequency coupling components that occur in the frequency range up to 2 kHz in single-phase PE devices, which occur at distances of multiples of $2f_1$ to the excited frequency as visible in Fig. 2. The impact of neglecting these frequency couplings, i.e., the representation as a linear time independent (LTI) system instead of a linear time periodic systems (LTP) in stability studies has been demonstrated in [30]. Major errors have been shown, if the frequency coupling is neglected for stability assessment. The time-variation of the dc-link voltage can lead to a negative real part of the input impedance of the PE device ([31], [32]). This has to be considered, when studying the entire device by including also the current-control loop and the grid-synchronization, e.g., in terms of a PLL ([33], [34]) as well as for a detailed analysis of the impact of the dc-link voltage on the device stability [35]. However, all studies mentioned earlier are performed from a white-box perspective, i.e., they require *a priori* knowledge about the size of the dc-link capacitance. The measurement-based identification of the dc-link capacitance as presented in this article allows to improve also respective black-box models in the future.

In addition, identifying the real device parameters, such as the capacitance of the dc-link capacitor, contributes to the development of grey-box models using the traditional network elements.

V. Conclusion

This article presents a non-destructive measurement-based identification method of the dc-link capacitance in commercially available single-phase PE devices for low power applications in LV networks. The method requires only a point measurement of the dc-link voltage or the voltage at the inverter bridge on the circuit board and knowledge about the power of the inverter (e.g., by simple measurement at the ac-side terminals). For simulative verification, an error of less than 1% has been achieved. The identified dc-link capacitance is an important component of grey-box models. Compared with the black-box models, such grey-box models can significantly improve the accuracy of power system studies, i.e., in terms of harmonic emission levels or harmonic stability assessment.

Next steps are the application of the proposed method to other commercial inverters and converters. Manufacturers shall be approached with regard to possible monitoring applications. Furthermore, ongoing and future work develops identification methods for the remaining missing components (i.e., the control).

References

[1] X. Wang and F. Blaabjerg, "Harmonic stability in power electronic based power systems: Concept, modeling, and analysis," *IEEE Trans. Smart Grid*, vol. 10, no. 3, pp. 2858–2870, May 2019.

[2] J. H. R. Enslin and P. J. M. Heskes, "Harmonic interaction between a large number of distributed power inverters and the distribution network," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1586–1593, Nov. 2004.

[3] M. Höckel, A. Gut, M. Arnal, R. Schild, P. Steinmann, and S. Schori, "Measurement of voltage instabilities caused by inverters in weak grids," *CIRED - Open Access Proc. J.*, vol. 2017, no. 1, pp. 770–774, Oct. 2017.

[4] E. Möllerstedt and B. Bernhardsson, "Out of control because of harmonics-an analysis of the harmonic response of an inverter locomotive," *IEEE Control Syst.*, vol. 20, no. 4, pp. 70–81, Aug. 2000.

[5] E. Kaufhold, J. Meyer, and P. Schegner, "Impact of grid impedance and their resonance on the stability of single-phase PV-inverters in low voltage grids," in *Proc. IEEE 29th Int. Symp. Ind. Electron.*, Jun. 2020, pp. 880–885.

[6] Int. Electrotechnical Commission 60725, "Consideration of reference impedances and public supply network impedances for use in determining the disturbance characteristics of electrical equipment having a rated curren $\leq$75 a per phase," 2012.

[7] DIN EN 61000-4-7, "Electromagnetic compatibility (EMC) - Testing and measurement techniques," 2009.

[8] E. Kaufhold, J. Meyer, and P. Schegner, "Modular white-box model of single-phase photovoltaic systems for harmonic studies," in *Proc. IEEE Milan Powertech*, Jun. 2019, pp. 1–6.
[9] E. Kaufhold, J. Meyer, P. Schegner, A. S. Abdelsamad, and J. M. A. Myrzik, "Comparison of solvers for time-domain simulations of single-phase photovoltaic systems," in *Proc. Int. Conf. Smart Grids Energy Syst.*, Nov. 2020, pp. 550–555.
[10] R. E. Kalman, "A new approach to linear filtering and prediction problems," *J. Basic Eng.*, vol. 82, no. 1, pp. 35–45, Mar. 1960.
[11] K. Abdennadher, P. Venet, G. Rojat, J. M. Rétif, and C. Rosset, "A real-time predictive-maintenance system of aluminum electrolytic capacitors used in uninterrupted power supplies," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1644–1652, Jul./Aug. 2010.
[12] B. H. Lin, J. T. Tsai, and K. L. Lian, "A non-invasive method for estimating circuit and control parameters of voltage source converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4911–4921, Dec. 2019.
[13] A. G. Abo-Khalil and D. C. Lee, "DC-link capacitance estimation in AC/DC/AC PWM converters using voltage injection," *IEEE Trans. Ind. Appl.*, vol. 44, no. 5, pp. 1631–1637, Sep./Oct. 2008.
[14] J. Kukkola and M. Hinkkanen, "Method for DC-link capacitance identification in voltage-source converters," in *Proc. Int. Symp. Power Electron., Elect. Drives, Automat. Motion*, 2016, pp. 34–40.
[15] E. Kaufhold, J. Meyer, and P. Schegner, "Black-box identification of grid-side filter circuit for improved modelling of single-phase power electronic devices for harmonic studies," *Electr. Power Syst. Res.*, vol. 199, Oct. 2021, Art. no. 107421.
[16] S. R. Hall and N. M. Wereley, "Generalized Nyquist stability criterion for linear time periodic systems," in *Proc. Amer. Control Conf.*, 1990, pp. 1518–1525.
[17] S. Cobben, W. Kling, and J. Myrzik, "The making and purpose of harmonic fingerprints," in *Proc. 19th Int. Conf. Electricity Distrib.*, 2007, pp. 21–24.
[18] D. Gallo, R. Langella, M. Luiso, A. Testa, and N. R. Watson, "A new test procedure to measure power electronic devices' frequency coupling admittance," *IEEE Trans. Instrum. Meas.*, vol. 67, no. 10, pp. 2401–2409, Oct. 2018.
[19] L. P. Frater, A. R. Wood, and N. R. Watson, "Linearisation of non-linear loads by phase dependent frequency coupling admittance matrices," in *Proc. 16th Power Syst. Comput. Conf.*, 2008, pp. 1–7.
[20] E. Kaufhold, J. Meyer, S. Muller, and P. Schegner, "Probabilistic stability analysis for commercial low power inverters based on measured grid impedances," in *Proc. 9th Int. Conf. Power Energy Syst.*, Dec. 2019, pp. 1–6.
[21] N. Patcharaprakiti *et al.*, "Modeling of single phase inverter of photovoltaic system using Hammerstein–Wiener nonlinear system identification," *Current Appl. Phys.*, vol. 10, no. 3, pp. S532–S536, May 2010.
[22] A. S. Abdelsamad, M. A. Johanna Myrzik, E. Kaufhold, J. Meyer, and P. Schegner, "Nonlinear identification approach for black-box modeling of voltage source converter harmonic characteristics," in *Proc. IEEE Electr. Power Energy Conf.*, Nov. 2020, pp. 1–5.
[23] H. Soliman, H. Wang, and F. Blaabjerg, "A review of the condition monitoring of capacitors in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4976–4989, Nov./Dec. 2016.
[24] P. Sundararajan *et al.*, "Condition monitoring of DC-link capacitors using Goertzel algorithm for failure precursor parameter and temperature estimation," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6386–6396, Jun. 2020.
[25] M. W. Ahmad, P. N. Kumar, A. Arya, and S. Anand, "Noninvasive technique for DC-link capacitance estimation in single-phase inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3693–3696, May 2018.
[26] Y. Wu and X. Du, "A VEN condition monitoring method of DC-link capacitors for power converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 1296–1306, Feb. 2019.
[27] K. Yao, W. Tang, X. Bi, and J. Lyu, "An online monitoring scheme of DC-link capacitor's ESR and C for a boost PFC converter," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5944–5951, Aug. 2016.
[28] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters*. Piscataway, NJ, USA: IEEE, 2003.
[29] Y. Liu, H. Wang, M. Huang, X. Zha, and Y. Liu, "Influence of DC link capacitance on power efficiency of single-phase inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 1498–1504.
[30] J. Kwon, X. Wang, F. Blaabjerg, and C. L. Bak, "Comparison of LTI and LTP models for stability analysis of grid converters," in *Proc. IEEE 17th Workshop Control Model. Power Electron.*, Jun. 2016, pp. 1–8.
[31] L. Harnefors, X. Wang, A. G. Yepes, and F. Blaabjerg, "Passivity-based stability assessment of grid-connected VSCs—An overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 116–125, Mar. 2016.
[32] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3323–3334, Dec. 2007.
[33] A. Rygg, M. Molinas, C. Zhang, and X. Cai, "A modified sequence-domain impedance definition and its equivalence to the dq-domain impedance definition for the stability analysis of AC power electronic systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1383–1396, Dec. 2016.
[34] M. K. Bakhshizadeh *et al.*, "Couplings in phase domain impedance modeling of grid-connected converters," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6792–6796, Oct. 2016.
[35] D. Lu, X. Wang, and F. Blaabjerg, "Impedance-based analysis of DC-link voltage dynamics in voltage-source converters," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3973–3985, Apr. 2019.

Elias Kaufhold (Student Member, IEEE) received the Dipl.-Ing. degree in electrical engineering from Technische Universität Dresden, Dresden, Germany, in 2018.

He is currently with the Institute of Electrical Power Systems, Technische Universität Dresden. His research interests include model identification methods, modeling approaches and the assessment and stability analysis of grid-coupled power electronic devices in low voltage networks with respect to power quality in the frequency range up to 2 kHz.

Jan Meyer (Senior Member, IEEE) received the Dipl.-Ing. and Ph.D. degrees in electrical power engineering and the Postdoctoral qualification in power quality from Technische Universität Dresden, Dresden, Germany, in 1994, 2004, and 2018, respectively.

He is currently with Technische Universität Dresden as a Senior Lecturer and a Team Leader of the Power Quality Research Group. His research interests include network disturbances and their assessment, especially for distortion below and above 2 kHz, methods and accuracy of power quality measurements as well as efficient analysis methods for big data amounts from power quality measurement campaigns.

Dr. Meyer is a member of several CIGRE and IEEE working groups related to network disturbances, a member of the CIRED TC, as well as the Vice-Chair of the German Mirror Committee for IEC SC77A.

Peter Schegner (Senior Member, IEEE) received the Dipl.-Ing. degree in electrical power engineering from the Darmstadt University of Technology, Darmstadt, Germany, in 1981, and the Ph.D. degree with a thesis on the earth-fault distance protection from Saarland University, Saarbrücken, Germany, in 1989.

After that, he worked as a System Engineer in the field of power system control and became a member of the Scientific Staff with Saarland University. Then, he worked as the Head of the Development Department of Protection Systems, AEG, Frankfurt A.M., Germany. Later, he became a Full Professor and the Head of the Institute of Electrical Power Systems and High Voltage Engineering of the Technische Universität Dresden, Germany.