Line-Frequency-Isolation Flexible AC-Link Converter Based on Direct AC-AC Choppers

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***Abstract*—Line-frequency-isolation flexible ac-link converter based on direct ac–ac choppers (FACL) is a novel ac–ac power conversion device expected to realize voltage compensation and power flow control. Compared with the traditional voltage source inverter (VSI) based devices, FACL has no dc-link capacitors that lead to high equipment failure rate. First, this article systematically introduces FACL. The power conversion principle of FACL is analyzed, and the output comparison between the unipolar and bipolar FACL is presented. Then, a high-performance bipolar FACL is proposed. It eliminates the shortcomings of the existing FACL topologies, such as bidirectional switches, undesirable phase shift, and restricted output range. Additionally, for facilitating the control of FACLs, a variant of the conventional dq reference frame called DQ-ABC synchronous rotating reference frame (DSRRF) is adopted. DSRRF provides a platform for the flexible operation in the form of dc between two three-phase voltages, which is beneficial to FACL control. On the basis of DSRRF, the closed-loop control strategy of FACLs is designed so that the decoupling control and closed-loop control of the output voltage amplitude and phase can be achieved conveniently. Finally, the open-loop and closed-loop experimental tests are carried out based on a 1-kW experimental prototype to verify the theoretical analysis.**

***Index Terms*—Closed-loop control strategy, controllable amplitude and phase, DQ-ABC synchronous rotating reference frame (DSRRF), eliminating dc-link, line-frequency-isolation ac–ac.**

I. Introduction

TO ENHANCE the flexibility and controllability of the power grid operation, coupling power electronic devices to the power grid has become an effective method. Over the past three decades, voltage source inverter (VSI) based devices have been widely studied, such as dynamic voltage regulator [1], [2], static synchronous compensator [3], [4], static synchronous series compensator [5], [6], and unified power flow controller [7], [8]. However, they all contain large volume dc-link capacitors, which usually result in high equipment failure rate, short life cycle, and high maintenance cost [9]–[10].

Therefore, a shift from VSI-based topologies to direct ac–ac converters is envisioned in ac-to-ac high-power conversion [11], [14]. This shift is supported mainly because the direct ac–ac converters do not require bulky dc-link capacitors [15]. The electrolytic capacitor of VSI-based device exhibits reliability and safety issues that contribute to a short life, which is still one of the major technical bottlenecks [16]. Comparatively, the film-based capacitor in direct ac-ac converter has higher security and reliability [17]. It is also found that a direct ac–ac converter has lower losses compared with a single-phase VSI-based back-to-back converter. This has been justified previously in specific test cases [l8], [19].

FACL is a voltage-source type direct ac–ac device without dc-link and has attracted a growing number of attention in recent years [20]–[29]. The detailed comparison of the articles presented in [20]–[29] is presented in Table II. The two kinds of configurations of FACL are shown in Fig. 1. FACL has two ac input ports U_{I1} and U_{I2}, which are the input sources of two direct ac–ac choppers. The output of FACL is a line-frequency ac voltage U_O with controllable and flexible amplitude and phase. U_O is obtained by the series connection of two direct ac–ac choppers' output ports and the *LC* low-pass filtering. The two single-phase line-frequency-isolation transformers T_1 and T_2 constitute the ac-link of FACL. The ac-link works as the interface of line-frequency ac voltages and also provides galvanic isolation. In Fig. 1(a), T_1 and T_2 are set at the input side. While in Fig. 1(b), they are set at the output side. According to the polarity of the direct ac–ac chopper used to construct FACL, FACL can be divided into two types: unipolar FACL (based on direct ac–ac chopper with unipolar voltage gain) and bipolar FACL (based on direct ac–ac chopper with bipolar voltage gain).

Through the ac-link of FACL, the input voltages or output voltage can be coupled with a three-phase system. Fig. 2 shows two typical applications of FACL. The input voltages of FACLs are obtained from node E. The output voltages of FACLs are connected in series with the node E three-phase voltages respectively. The load is divided into passive load and active load. When the passive load is connected to node G, FACL is

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TABLE I
CONSTRAINT CONDITIONS OF FOUR DUTY CYCLES AND THE COMPOSITION OF OUTPUT VOLTAGE

Modes	Voltage transfer rates		Duty cycles	Output voltage
1	$Q_1\neq0$ $Q_2\neq0$	$Q_1>0$ $Q_2>0$	$d_1>d_2$, $d_3>d_4$	$V_{FA}=Q_1V_{lin}+Q_2V_{rin}$
		$Q_1>0$ $Q_2<0$	$d_1>d_2$, $d_3<d_4$	
		$Q_1<0$ $Q_2>0$	$d_1<d_2$, $d_3>d_4$	
		$Q_1<0$ $Q_2<0$	$d_1<d_2$, $d_3<d_4$	
2	$Q_1=0$ $Q_2\neq0$	$Q_1=0$ $Q_2<0$	$d_1=d_2$, $d_3<d_4$	$V_{FA}=Q_2V_{rin}$
		$Q_1=0$ $Q_2>0$	$d_1=d_2$, $d_3>d_4$	
	$Q_1\neq0$ $Q_2=0$	$Q_1>0$ $Q_2=0$	$d_1>d_2$, $d_3=d_4$	$V_{FA}=Q_1V_{lin}$
		$Q_1<0$ $Q_2=0$	$d_1<d_2$, $d_3=d_4$	
3	$Q_1=0$, $Q_2=0$		$d_1=d_2$, $d_3=d_4$	$V_{FA}=0$

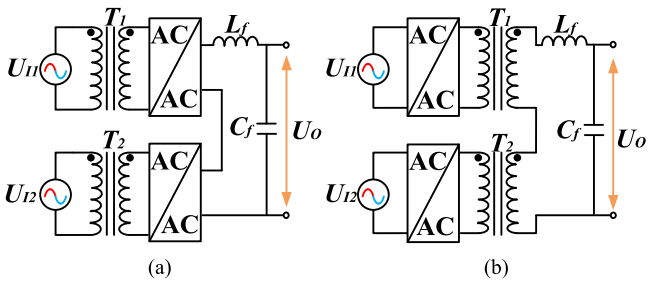

Fig. 1. Two kinds of configurations of FACL. (a) Transformers are set at the input side. (b) Transformers are set at the output side.

employed as voltage compensator [20]–[27]. If voltage sags or swells occur at node E, the compensator will inject appropriate voltage *Uo* in series with node E voltage to maintain the desired load voltage. Specifically, it is more attractive for this kind of voltage compensator where the voltage fluctuation with phase jump needs to be eliminated. When the active load is connected to node G, FACL is employed as power flow controller [27]–[29]. Due to the output voltage *Uo* having controllable amplitude and phase, the node F voltage can be regulated actively. As a result, the power flow control between node F and node G can be realized.

It can be seen in Fig. 2 that the highly controllable ac output voltage *Uo* plays a crucial role in applications. However, the amplitude and phase of FACL's output voltage *Uo* are coupled from the perspective of control. Because both of them are related to duty cycles simultaneously. Furthermore, it is difficult to realize closed-loop control of the output voltage amplitude and phase simultaneously and independently. In the published literature about FACL [20]–[29], no effective solution is provided.

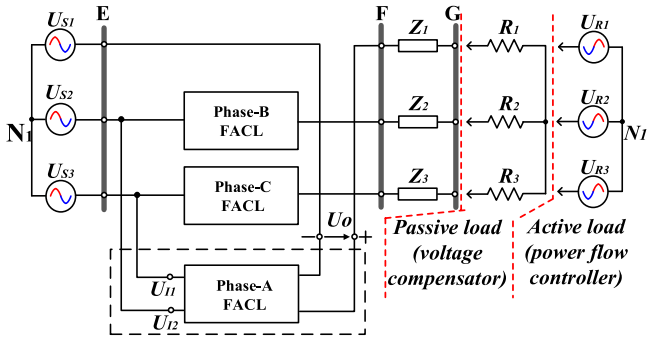

Fig. 2. Two typical applications of FACL.

For facilitating the control of FACLs, a variant of the conventional dq0 reference frame called DQ-ABC synchronous rotating reference frame (DSRRF) is adopted in this article. In DSRRF, two three-phase voltages are able to realize flexible operation. One is in the form of general vector and the other is in the form of "equivalent phasor," which will be introduced in Section IV. Based on DSRRF, the closed-loop control strategy of FACLs is designed so that the decoupling control and closed-loop control can be achieved conveniently.

Moreover, to address the shortcomings of the existing FACL topologies [20]–[29], such as bidirectional switches, undesirable phase shift, and restricted output range, a new bipolar FACL based on BT-ac is proposed [30]–[31]. It has four independently controllable degrees of freedom, which ensures that the output voltage of the converter is flexible and adjustable in all four quadrants. Besides, there are no bidirectional switches switching in a complementary manner, and the commutation problems are avoided [32]. Each chopper leg's output voltage can remain in-phase with its power source so that there is no undesirable phase shift in FACL's output voltage.

The rest of this article is organized as follows. In Section II, the power conversion principle of FACL is analyzed, and the output ranges of unipolar and bipolar FACL are compared. Section III introduces the topology and the operation principles of the proposed new bipolar FACL. The comparison with other FACLs in the published literature is also presented in this section. DSRRF and the closed-loop control strategy are analyzed in Section IV. Section V presents the results of simulation and experimental tests. Finally, Section VI concludes this article.

II. POWER CONVERSION PRINCIPLE AND OUTPUT COMPARSION OF FACL

For the comprehensive analysis of FACL's power conversion principle and output voltage, a three-phase FACL system is built, as shown in Fig. 3. The three-phase voltages of node ST supply power to three FACLs. The B-phase voltage and C-phase voltage are the inputs of FACL I, C-phase voltage and A-phase voltage are the inputs of FACL II, concurrently, A-phase voltage and B-phase voltage are the inputs of FACL III. The output voltages of FACLs I–III constitute the new three-phase voltages of node FO, and they are directly connected to passive load. It should be noted that the specific topology of FACL is not limited.

TABLE II
COMPARISON OF THE PROPOSED FACL AND THE FACLS IN THE PUBLISHED LITERATURE

	Proposed in this paper [31] (Fig. 9)	Proposed in [20]-[21] (Fig. 12(a))	Proposed in [22]-[23] (Fig. 12(a))	Proposed in [24] (Fig. 12(b))	Proposed in [25]-[28] (Fig. 12(c))	Proposed in [29] (Fig. 12(d))
Type	Bipolar FACL	Unipolar FACL	Unipolar FACL	Unipolar FACL	Bipolar FACL	Bipolar FACL
Switch count	16	20	24	16	8	8
Passive component count	Seven capacitors, one inductor	Four capacitors, four inductors	Four capacitors, four inductors	Six capacitors, ten inductors	Six capacitors, six inductors	Six capacitors, six inductors
Undesirable phase shift	No	No	No	No	Yes when D>0.5	No
Feasible range of duty cycle	0 to 1	0 to 1	0 to 1	0 to 1	0 to 0.5	0.5 per mode
Output voltage range	Four quadrants	One quadrant	Two quadrants	One quadrant	One quadrant	Four quadrants
Bidirectional switches problems	No	No	No	No	Yes	Yes
Adopt transformer with center tape	No	No	No	No	No	Yes
Voltage stress	U_{in}	U_{in}	U_{in}	U_{in}	U_{in}	$2U_{in}$

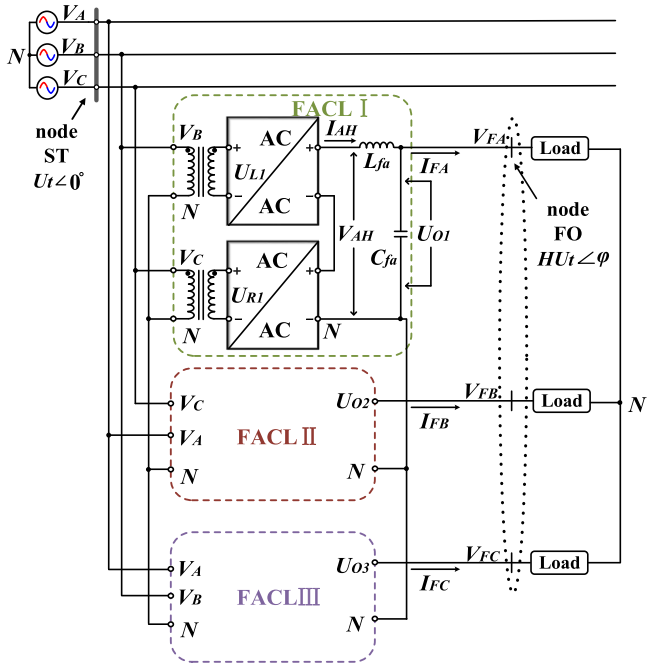

Fig. 3. Three-phase FACL system.

In this section, the power conversion principle and the output comparison between the unipolar and bipolar FACL are analyzed in detail.

A. Power Conversion Principle of FACL

To avoid redundant discussion, the FACL I is taken as an example for analysis. FACL II and III are similar to it. The voltages of node ST can be defined as formulas

$$\left.\begin{aligned} V_A &= \sqrt{2}U_t \sin(\omega t) \\ V_B &= \sqrt{2}U_t \sin(\omega t - \tfrac{2}{3}\pi) \\ V_C &= \sqrt{2}U_t \sin(\omega t + \tfrac{2}{3}\pi) \end{aligned}\right\}. \tag{1}$$

In the above equations, V_A, V_B, and V_C are the phase voltages of A, B, and C phases respectively. U_t is the root-mean-square (rms) value of phase voltage. ω is the angular frequency of sine wave. The voltage transfer ratios of two direct ac–ac choppers in FACL I are defined as Q_1 and Q_2, respectively. They reflect the voltage gain between the output voltage and the input voltage. The isolation transformer's winding ratio between the primary side and the secondary side is defined as 1: n. According to formula (1), the A-phase voltage V_{FA} of node FO, which is the output voltage of FACL I, and its phasor can be expressed as

$$\begin{aligned} V_{FA} = \; & \sqrt{2}nQ_1U_t \sin(wt - \tfrac{2}{3}\pi) \\ & + \sqrt{2}nQ_2U_t \sin(wt + \tfrac{2}{3}\pi) \end{aligned} \tag{2}$$

$$\dot{V}_{FA} = HU_t\angle\varphi. \tag{3}$$

In (3), H is the ratio coefficient between node ST voltage amplitude and node FO voltage amplitude. φ is the phase difference angle of node FO relative to node ST. For intuitively expressing the voltage amplitude and phase angle of node FO with voltage transfer ratios Q_1 and Q_2, the following equations are given as:

$$H = n\sqrt{{Q_1}^2 + {Q_2}^2 - Q_1Q_2} \tag{4}$$

$$\varphi = \arctan\left[-\frac{\sqrt{3}(Q_2 - Q_1)}{Q_1 + Q_2}\right]. \tag{5}$$

The demonstration of formulas (4) and (5) is presented in the Appendix. It can be seen from formula (4) that the voltage amplitude of V_{FA} has three controllable degrees of freedom, namely, voltage transfer ratios Q_1 and Q_2, the winding ratio n of the isolation transformer. It can be pointed out that the voltage amplitude adjustment range of FACL I's output can be extended by increasing the winding ratio n. When n is fixed in practical application, the flexible adjustment of ratio coefficient H can be accomplished by changing the voltage transfer ratios Q_1 and Q_2 continuously. Formula (5) indicates that the phase

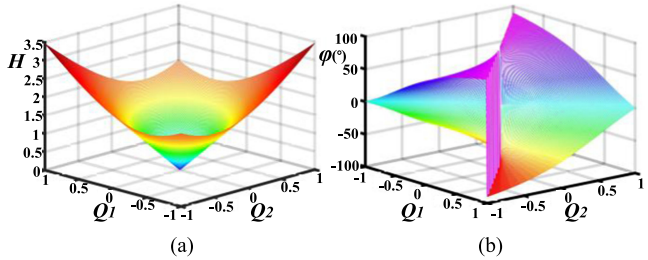

Fig. 4. Adjustment range of bipolar FACL's output voltage when the winding ratio n is 2. (a) Relationship between H and the voltage transfer ratios. (b) Relationship between φ and the voltage transfer ratios.

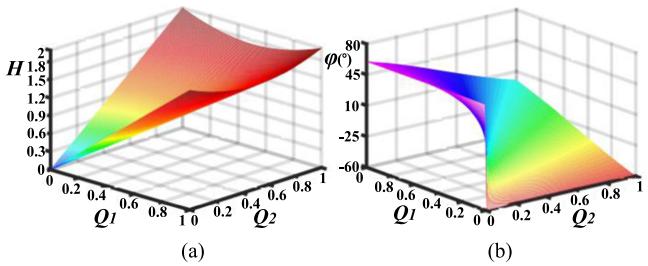

Fig. 5. Adjustment range of unipolar FACL's output voltage when the winding ratio n is 2. (a) Relationship between H and the voltage transfer ratios. (b) Relationship between φ and the voltage transfer ratios.

difference angle φ is only related to the two voltage transfer ratios. It should be noted that formulas (2)–(5) are based on the direct ac–ac chopper with no phase shift between its input voltage and output voltage. For most unipolar FACLs, both ranges of voltage transfer ratios Q_1 and Q_2 are [0, 1], and those of most bipolar FACLs are $[-1, 1]$. When the winding ratio n is 2, Fig. 4 shows the adjustment range of ratio coefficient H and phase difference angle φ of bipolar FACL. Moreover, Fig. 5 shows the adjustment range of H and φ of unipolar FACL.

B. Output Comparsion Between Bipolar and Unipolar FACL

According to the coplanar vector theorem, two noncollinear and nonzero vectors can form any vector in the same plane. The output voltage phasor of FACL can be equivalent to the vector synthesis of two voltage phasors injected by the input power supplies. In the three-phase FACL system shown in Fig. 3, the B-phase voltage phasor and C-phase voltage phasor of node ST can be regarded as two nonzero and noncollinear vectors in the same plane. By changing the values of two voltage transfer ratios Q_1 and Q_2, the amplitude and phase angle of the synthesized phasor $\dot{V}_{FA}$ can be regulated. Figs. 6 and 7 show the voltage phasor synthesis principle of bipolar FACL and unipolar FACL, respectively, with the transformer winding ratio $n = 2$. When FACL works in different quadrants, the relationships among Q_1, Q_2, and 0, the amplitude and phase relationships between the A-phase voltage of node ST and the A-phase voltage of node FO are noted in Figs. 6 and 7.

The radius of the gray circle in figures is equal to the length of node ST's phase voltage phasor, which represents U_t. The

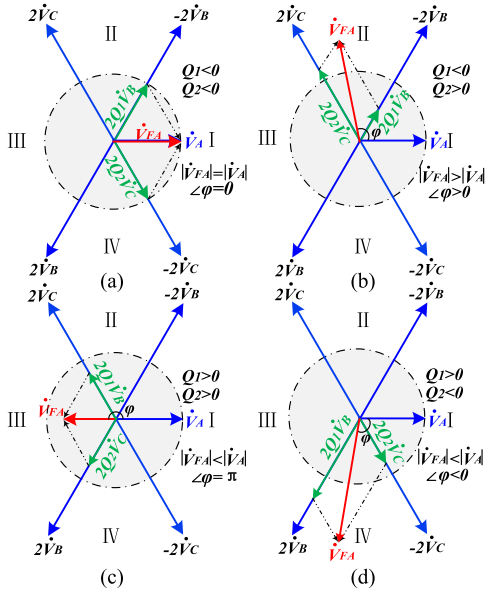

Fig. 6. Voltage phasor synthesis principle of bipolar FACL. (a) Working in quadrant I. (b) Working in quadrant II. (c) Working in quadrant III. (d) Working in quadrant IV.

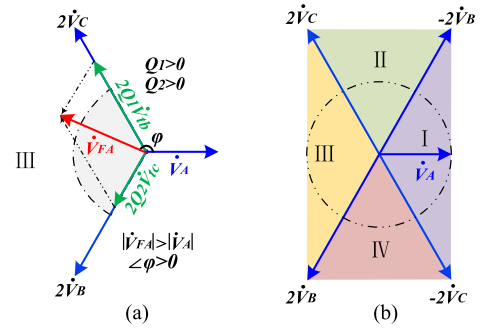

Fig. 7. Voltage phasor synthesis principle of unipolar FACL. (a) Working in quadrant III. (b) Four feasible working quadrants.

length of the blue coordinate axis, which is the rms value of transformer's secondary side voltage, is twice of U_t. For bipolar FACL, since both the ranges of Q_1 and Q_2 are from -1 to 1, the full amplitude and bipolarity utilization of two input voltage phasors can be realized. Consequently, $\dot{V}_{FA}$ can be regulated flexibly in all four quadrants. Due to the limited voltage transfer ratios, the unipolar FACL can only be regulated in a single quadrant of four. But it can work in any single quadrant of four by changing the polarity of FACL's input voltages, as shown in Fig. 7(b).

The output voltage range of bipolar FACLs is shown in Fig. 8(a). It is a diamond with a side length of 4 U_t. The output voltage range of unipolar FACL is composed of a diamond with a side length of $2U_t$, as shown in Fig. 8(b). In both Fig. 8(a) and(b), the starting point of phasor $\dot{V}_{FA}$ is the origin. According to the values of Q_1 and Q_2, the end point can be any point in the diamond including the boundary.

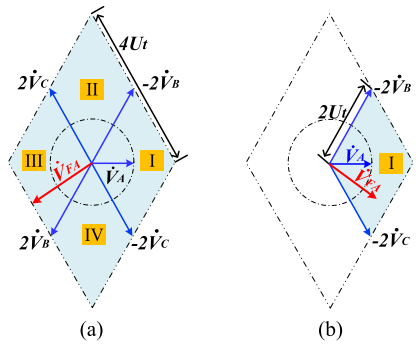

Fig. 8. Output voltage range of FACL. (a) Bipolar FACL. (b) Unipolar FACL.

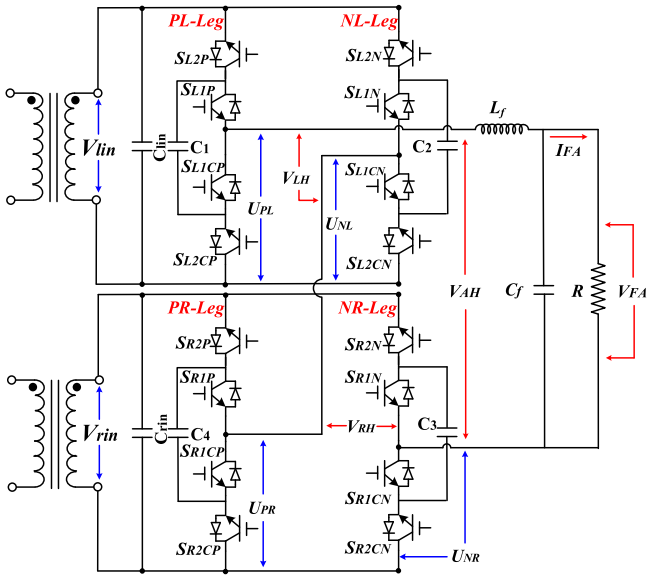

Fig. 9. Topology of the proposed FACL.

III. Proposed New Bipolar FACL

A. Topology of the Proposed FACL

Among the FACLs in the published literature [20]–[29], there are some shortcomings, such as limited output range, bidirectional switches, and undesirable phase shift. To find a high-performance topology that eliminates these problems, a new bipolar FACL based on BT-AC is proposed in this section [30]–[31].

The topology of the proposed FACL is shown in Fig. 9. It can work as any single-phase FACL of the three-phase FACL system previously presented in Fig. 3. The proposed FACL contains four two-level nondifferential ac chopper legs. They are defined as PL-Leg, NL-Leg, NR-Leg, and PR-Leg respectively in Fig. 9. Each chopper leg consists of four IGBTs and a clamping capacitor for absorbing the energy stored in the stray inductance of the line. $V_{\rm lin}$ and $V_{\rm rin}$ are the input ac voltage sources allowing any voltage amplitude and initial phase. V_{lin} supplies power to PL-Leg and NL-Leg. $V_{\rm rin}$ supplies power to NR-Leg and PR-Leg. To improve the quality of the output voltage, two input capacitors named $C_{\rm lin}$ and $C_{\rm rin}$ are placed at the two input ports respectively. L_f and C_f constitute the *LC* low-pass filter.

Each ac chopper leg has an independent duty cycle with a value of 0 to 1. The duty cycle of PL-Leg, NL-Leg, PR-Leg, and NR-Leg are defined as d_1,d_2, d_3, and d_4 respectively. In each switching cycle, the two levels of $U_{\rm PL}$ and $U_{\rm NL}$ are $V_{\rm lin}$'s instantaneous voltage and zero, and those of $U_{\rm PR}$ and $U_{\rm NR}$ are $V_{\rm rin}$'s instantaneous voltage and zero. The relationship among the output voltage V_{FA}, the input voltage $V_{\rm lin}$ and $V_{\rm rin}$ of the converter is as follows:

$$\begin{aligned} V_{FA} = &\quad U_{\rm PL} - U_{\rm NL} + U_{\rm PR} - U_{\rm NR} \\ = &\quad (d_1 - d_2)V_{\rm lin} + (d_3 - d_4)V_{\rm rin}. \end{aligned} \tag{6}$$

Since PL-Leg, NL-Leg, and $V_{\rm lin}$ have a common sharing ground, NR-Leg, PR-Leg, and $V_{\rm rin}$ have a common sharing ground, the ac chopper legs are nondifferential, and the output of each ac chopper leg can keep in-phase with its power source. As a result, there is no undesirable phase shift in V_{FA}. The voltage transfer ratio Q_1 is equal to the difference between duty cycles d_1 and d_2. Similarly, the voltage transfer ratio Q_2 is equal to the difference between duty cycles d_3 and d_4. Then, according to formula (6), the relationship between the output voltage phasor and the two input voltage phasors is shown in formula

$$\dot{V_{FA}} = Q_1 \dot{V_{\rm lin}} + Q_2 \dot{V_{\rm rin}}. \tag{7}$$

Since the duty cycle of each ac chopper leg has a value of 0 to 1, the voltage transfer ratios Q_1 and Q_2 of the converter range from -1 to 1. Two bipolar voltage transfer ratios ensure the wide output range and flexible regulation of the output voltage amplitude and phase angle in all four quadrants.

B. Operation Principles of the Proposed FACL

The modulation principles of PL-Leg and NL-Leg are as follows [31]. When $V_{\rm lin}$ is at positive half-wave, S_{L2P}, S_{L2CP}, S_{L2N},and S_{L2CN} are in normally open state and the gate signals of S_{L1P}, S_{L1CP}, S_{L1N}, and S_{L1CN} are shown in Fig. 10(a). When $V_{\rm lin}$ is at negative half-wave, S_{L1P}, S_{L1CP}, S_{L1N}, and S_{L1CN} are in normally open state and the gate signals of S_{L2P}, S_{L2CP}, S_{L2N}, and S_{L2CN} are shown in Fig. 10(b). As the modulation strategies of NR-Leg and PR-Leg are similar to those mentioned above, the detailed analysis is not given. It can not be ignored that all duty cycles including d_3 and d_4 share one triangular carrier.

Combining with the topology and the modulation principles, there are no bidirectional switches switching in a complementary manner. Moreover, the unique ac chopper leg structure makes the current always have a circulation loop. The safe and effective commutation can be realized without additional snubber circuit or commutation control strategy. Although the ac chopper leg contains four IGBTs, only two of them are in high frequency switching state, and the other two are in normally open state in each half-wave period.

According to the energy supplies of two input power sources, the FACL has three operation modes, as given in Table I. When

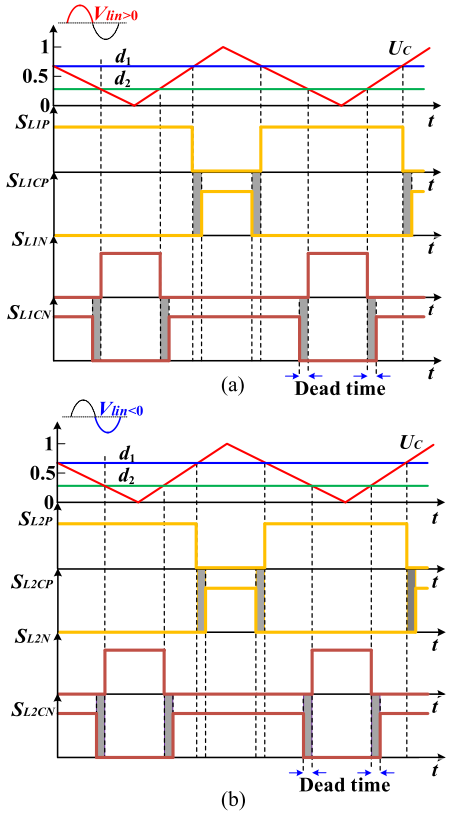

Fig. 10. Comparison principles between duty cycles and the carrier for PL-Leg and NL-*Leg*. (a) $V_{\rm lin}$ is at positive half-wave. (b) $V_{\rm lin}$ is at negative half-wave.

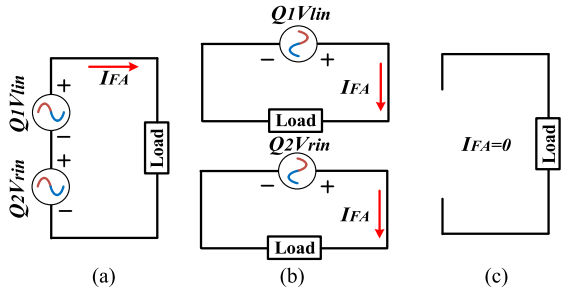

Fig. 11. Equivalent circuits of FACL working in different operation modes.

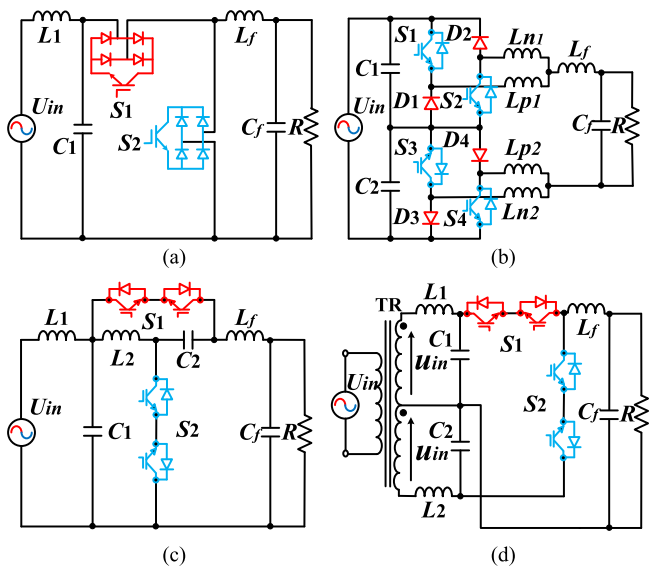

Fig. 12. Topologies of the direct ac–ac choppers in other FACLs. (a) PWM ac chopper in [20]–[23]. (b) Switching cell structured ac–ac converter in [24]. (c) Cuk B2 matrix-reactance chopper in [25]–[28]. (d) Conventional matrix chopper in [29].

the FACL is in operation mode 1, the voltage transfer ratios Q_1 and Q_2 are all taken as any nonzero value among $[-1, 1]$. In this condition, the output voltage V_{FA} is composed of two input voltages. The input voltage sources $V_{\rm lin}$ and $V_{\rm rin}$ both provide energy to the load. When the FACL works in operation mode 2, one of the voltage transfer ratios is 0, and the other ranges from -1 to 1. In this mode, the output voltage V_{FA} is composed of a single input voltage. That means there is only one input power source, $V_{\rm lin}$ or $V_{\rm rin}$, providing energy to the load. In the situation that FACL works in mode 3, both the two voltage transfer ratios are taken as 0, and the FACL is in a blocking state with no output. The two input power supplies do not provide energy in mode 3. Table I gives the constraint conditions of four duty cycles d_1, d_2, d_3, d_4, and the composition of output voltage V_{FA} in each operation mode. Meanwhile, the equivalent circuits of FACL working in different operation modes are shown in Fig. 11.

C. Comparison With Other FACLs

The FACL employed to compensate voltage sags with phase jump in [20]–[21] is unipolar. Fig. 12(a) shows the pulsewidth-modulated (PWM) ac chopper used to structure the FACL. It can be seen that this topology contains a small number of IGBTs. But the diode bridge, which consists of four diodes, is utilized to achieve the feature of bidirectional switches. Moreover, as S_1 and S_2 are switched in a complementary manner, this topology may have commutation problems caused by the delayed response of semiconductor switching devices. Due to the characteristics of unipolar FACL, the output voltage amplitude and phase angle can only be adjusted in one of the four quadrants.

To extend the output range, an improved FACL is proposed in [22] and [23]. It uses the same PWM ac chopper as [20]–[21]. But additional four switches are set at the input side of FACL to switch the power source of the PWM ac chopper. Although a wider output range is achieved, the reliability and dynamic response performance are affected and the risk of power supply interruption of the PWM ac chopper will increase.

A unipolar FACL is proposed in [24] to realize voltage compensation. It is based on the switching cell structured ac–ac converter, as shown in Fig. 12(b). The switching cell structure employs switches with series-coupled fast recovery diodes and adds a small inductance in phase leg. It can solve the shoot-through and commutation problems, but there are many passive components in the topology. Besides, the output range is one of the four quadrants.

The bipolar FACL proposed in [25]–[28] is on the basis of Cuk B2 matrix-reactance chopper, as shown in Fig. 12(c). It is designed to realize voltage compensation and power flow

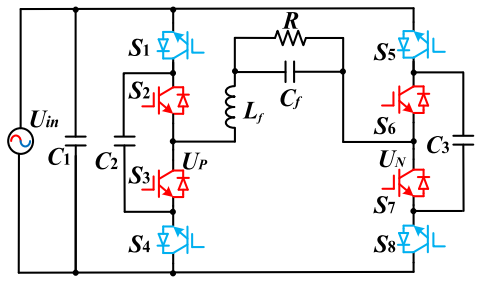

Fig. 13. BT-ac converter in [31].

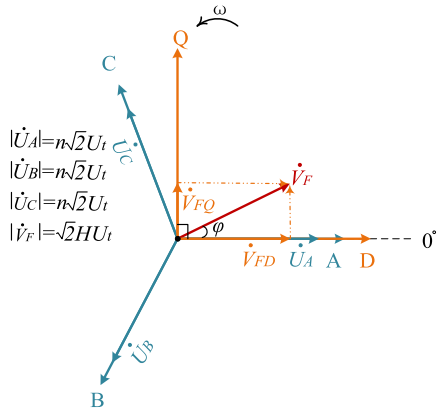

Fig. 14. Equivalent phasors of node ST three-phase voltages and the general vector of node FO three-phase voltages in DSRRF when the time is $t = 0$s.

control. Specifically, the chopper works in in-phase buck mode for $0<D<0.5$, antiphase buck mode for $0.5<D<0.67$, antiphase boost mode for $0.67<D<1$. However, the chopper has strongly nonlinear characteristics, and the practicable adjustment range of duty cycle D is small. When the converter operates in antiphase buck mode and antiphase boost mode, the output voltage phase will shift seriously. Therefore, it is better for the chopper to work in $0<D<0.5$ in-phase buck mode. The output voltage range is reduced.

In an effort to obtain a nonrestrictive adjustment range of duty cycle, [29] proposed a bipolar FACL with the function of power flow control. The FACL is based on conventional matrix chopper [33], as shown in Fig. 12(d). The chopper contains two bidirectional switches and a center-tapped transformer. The duty cycle is feasible in the range of 0 to 1, and there is no undesirable phase shift both in in-phase buck mode and antiphase buck mode. The output voltage is adjustable in four quadrants. However, the bidirectional switches may lead to commutation problems [32], and the requirements of transformer increase.

Fig. 13 shows the BT-ac converter [31] of the proposed bipolar FACL. BT-ac has two duty cycles, and both of them can be adjusted without constraint. Due to the output ports U_P, U_N, and the power source sharing a common ground, the in-phase or antiphase between the input and output voltage is ensured. Moreover, no bidirectional switches are switching in a complementary manner, and the commutation problems are avoided. The output voltage of the proposed FACL is adjustable in four quadrants. Table II gives the comparison of the proposed FACL and the FACLs in the published literature.

IV. DQ-ABC Synchronous Rotating Reference Frame and Closed-Loop Control Strategy

It can be obtained from formulas (4) and (5) that both the amplitude and phase of FACL's output voltage are related to the voltage transfer ratios Q_1 and Q_2 simultaneously. When the values of Q_1 and Q_2 change, both the amplitude and phase will be influenced. As a result, the closed-loop control of the output voltage amplitude and phase simultaneously and independently can not be realized by directly adjusting the values of voltage transfer ratios. It is also a common problem for FACLs. According to the analysis in Section II, through the vector synthesis of node ST's three voltage phasors multiplied by voltage transfer ratios, respectively, the desired three output voltage phasors of FACLs can be obtained. However, it is meaningless to make a parallel projection from the general vector of node FO three-phase voltages to the axes of the conventional DQ-ABC frame for vector synthesis. Because the general vector is rotating, and the a-axis, b-axis, and c-axis are static. The quantities on the axes are not phasors. Furthermore, the closed-loop control and decoupling control are more difficult to achieve. For facilitating the control of FACLs, a variant of the conventional dq reference frame called DSRRF is adopted in this section. In DSRRF, the vector synthesis and voltage transfer ratios calculation are realized conveniently and intuitively. Then, based on the superiorities of DSRRF, a closed-loop control strategy of FACL is designed.

A. DQ-ABC Synchronous Rotating Reference Frame

DSRRF adds three synchronous rotating axes to the conventional dq reference frame, namely, A-axis, B-axis, and C-axis, as shown in Fig. 14. Among them, Q-axis has a phase advance of 90° relative to D-axis, B-axis has a phase lag of 120° relative to A-axis, and C-axis has a phase advance of 120° relative to A-axis. Besides, the dotted line is the 0°-axis.

The concept of equivalent phasor is introduced here. Three equivalent phasors refer to three vectors in DSRRF located in A-axis, B-axis, and C-axis, respectively. They represent three corresponding phase voltages of a node. The equivalent phasor has two parameters, length, and phase angle. The length of each equivalent phasor is equal to the amplitude of the corresponding phase voltage. Meanwhile, the angle between the equivalent phasor and 0°-axis represents the phase angle of the corresponding phase voltage at a certain time. Therefore, the amplitude and phase information of three-phase voltages can be described by equivalent phasors in real-time in DSRRF. Additionally, the concepts and characteristics of D-axis and Q-axis are the same as those of the conventional dq reference frame. The vectors on the D-axis and Q-axis are the projections of general vector. All coordinate axes and vectors in the reference frame will rotate anticlockwise at the speed of power grid angular frequency ω from $t = 0$s. The angle between the A-axis and the 0°-axis represents the phase angle of A-phase. It is also the initial phase angle of a three-phase voltage when the time is 0s.

Furthermore, the three-phase FACL system shown in Fig. 3 can be analyzed conveniently in DSRRF. Since the input voltages of FACLs are provided by node ST, the three equivalent phasors $\dot{U}_A$, $\dot{U}_B$, and $\dot{U}_C$ of node ST's three-phase voltages are placed in *A*-axis, *B*-axis, and *C*-axis, respectively, as shown in Fig. 14. According to formula (1), the lengths of all equivalent phasors are $\mathrm{n}\sqrt{2}U_t$considering the transformer winding ratio n. Since the initial phase of node ST is 0°, the *A*-axis and 0°-axis coincide at the time of $t = 0$s.

The three-phase voltage phasors of node FO can be defined as formula

$$\left.\begin{aligned} \dot{V_{FA}} &= HU_t e^{j\varphi} \\ \dot{V_{FB}} &= HU_t e^{j\varphi - 120^\circ} \\ \dot{V_{FC}} &= HU_t e^{j\varphi + 120^\circ} \end{aligned}\right\}. \tag{8}$$

According to formula (8), we can get that the angle between $\dot{V_F}$, which is the general vector of node FO three-phase voltages, and 0°-axis at $t = 0$ s is φ, as shown in Fig. 14. Moreover, the length of $\dot{V_F}$ is $\sqrt{2}HU_t$. $\dot{V}_{FD}$ and $\dot{V}_{FQ}$ are the general vector's projections on *D*-axis and *Q*-axis, respectively. In the following time, all coordinate axes and vectors will rotate anticlockwise at the speed of ω. Thus, all the input three-phase voltages and the output three-phase voltages of the three-phase FACL system are placed in DSRRF, and the amplitude and phase relationship among them can be established in real-time.

One of the important advantages of DSRRF is that through real-time sampling, the amplitude and phase relationships among the general vector and the equivalent phasors are the same as those among the two corresponding three-phase voltages. Besides, since all the lengths of equivalent phasors and general vectors in DSRRF are the amplitudes of the corresponding phase voltages, the flexible operation between two three-phase voltages can be realized in the form of dc.

B. Closed-Loop Control Strategy of FACL

Based on DSRRF and the designed closed-loop control strategy, the decoupling control and closed-loop control of the output voltage amplitude and phase can be achieved conveniently. The closed-loop control strategy of FACLs is analyzed and derived from the following four steps.

1) In the previous section, the input three-phase voltages and the output three-phase voltages of the three-phase FACL system have been placed in DSRRF, as illustrated in Fig. 14. Then, a phase-locked loop (PLL) based on Park's transformation is designed to keep *D*-axis and *A*-axis coincident. Its control block diagram is shown in Fig. 15. In the control block diagram, the three-phase voltages of node ST are obtained through acquisition circuit. After Park's transformation and a series of operations, the phase angle γ is acquired. γ is used as the feedback value of the Park's transformation matrix. In this way, the equivalent phasor of node ST A-phase voltage and D-axis will be locked in the same phase. So, the *D*-axis and *i*-axis remain coincident in DSRRF at any time. In Fig. 15, it should be noted that the input port with a solid circle of the divider is the numerator.

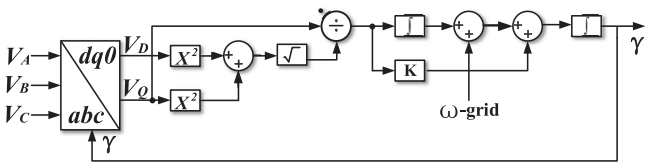

Fig. 15. PLL based on Park's transformation.

2) V_{AS}, V_{BS}, and V_{CS} are defined as the reference values of node FO three-phase voltages. The waveforms of V_{AS}, V_{BS}, and V_{CS} are digital and generated in a controller through programming according to the desired amplitude and initial phase. Then, Park's transformation of the reference values is carried out. The time-varying ac quantities are transformed into *D*-axis vector $\dot{V}_{FD}$ and *Q*-axis vector $\dot{V}_{FQ}$ with constant length in DSRRF. After that, the general vector $\dot{V_F}$ can be synthesized by $\dot{V}_{FD}$ and $\dot{V}_{FQ}$, as illustrated in Fig. 14. The rated three-phase voltages of node FO are represented by the general vector $\dot{V_F}$ in DSRRF. It is particularly important that the angle γ obtained by the control method in Fig. 15 is used in the process of Park's transformation of V_{AS}, V_{BS}, and V_{CS}. In this way, $\dot{V_F}$ will keep ahead of $\dot{U}_A$ angle φ in DSRRF. As analyzed in the previous section, the amplitude and phase relationships among the general vectors and the equivalent phasors in DSRRF are the same as those among the corresponding two three-phase voltages. So, the phase difference between the node FO voltage and the node ST voltage can be stabilized to φ. Through the above operations, the phase relationship among the input voltages and the output voltages of FACLs is established in DSRRF, and the closed-loop control of the phase angle is achieved independently.

3) According to the principle of general vector, the general vector $\dot{V_F}$ and the A-phase phasor $\dot{V}_{FA}$ have the same phase angle, and the length of $\dot{V_F}$ is $\sqrt{2}$ times the length of $\dot{V}_{FA}$. So the $\dot{V}_{FA}$ can be represented by $\dot{V_F}$. As analyzed in Section II, the output voltage $\dot{V}_{FA}$ of FACL I in Fig. 3 is equivalent to the vector synthesis of node ST's B-phase voltage phasor and C-phase voltage phasor multiplied by the voltage transfer ratios Q_1 and Q_2, respectively. Therefore, the general vector $\dot{V_F}$ is projected parallel to the reverse extension line of *B*-axis and *C*-axis, as shown in Fig. 16. The feature that the vector synthesis of the general vectors and the equivalent vectors can be realized in DSRRF is utilized here. That also means the operation between two three-phase voltages is achieved in real-time.

In the light of each side length and angle of the triangles in Fig. 16, the following equation can be listed according to the law of sines:

$$\frac{\left|\dot{V_F}\right|}{\sin(\pi/3)} = \frac{-Q_2\left|\dot{U_C}\right|}{\sin(\pi/3-\varphi)} = \frac{-Q_1\left|\dot{U_B}\right|}{\sin(\pi/3+\varphi)}. \tag{9}$$

Due to the general vector $\dot{V_F}$ is synthesized by the *D*-axis vector $\dot{V}_{FD}$ and *Q*-axis vector $\dot{V}_{FQ}$, formulas (10) and (11) can

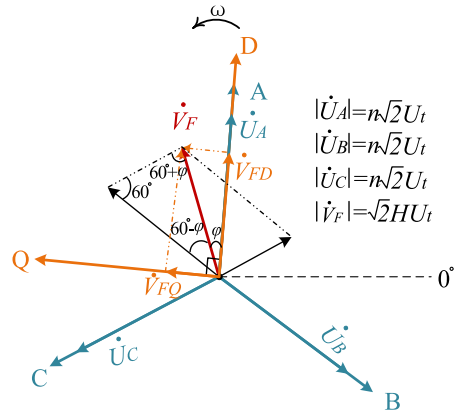

Fig. 16. Vector synthesis between the general vector and the equivalent vectors in DSRRF.

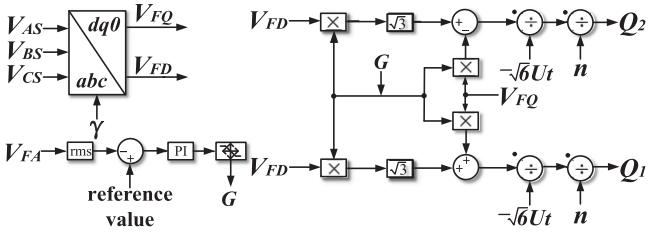

Fig. 17. Control strategy for obtaining voltage transfer ratios.

be derived from Fig. 16

$$\sin\varphi = \frac{\left|\dot{V}_{FQ}\right|}{\left|\dot{V}_F\right|} \tag{10}$$

$$\cos\varphi = \frac{\left|\dot{V}_{FD}\right|}{\left|\dot{V}_F\right|}. \tag{11}$$

By combining formulas (9)–(11), the values of voltage transfer ratios Q_1 and Q_2 can be expressed as

$$Q_1 = \frac{\sqrt{3}\left|\dot{V}_{FD}\right| + \left|\dot{V}_{FQ}\right|}{-\sqrt{6}nU_t} \tag{12}$$

$$Q_2 = \frac{\sqrt{3}\left|\dot{V}_{FD}\right| - \left|\dot{V}_{FQ}\right|}{-\sqrt{6}nU_t}. \tag{13}$$

4) Considering the amplitude of the output voltage may be lower than the reference value caused by converter losses and duty cycle losses, a PI controller is added to the control system to make the output voltage amplitude of FACL stable at the reference value. Based on the above analyses, the control strategy aiming to obtain voltage transfer ratios Q_1 and Q_2 is shown in Fig. 17. It should be noted that G is the output of the PI module after passing through the limiter. In the next step, G is

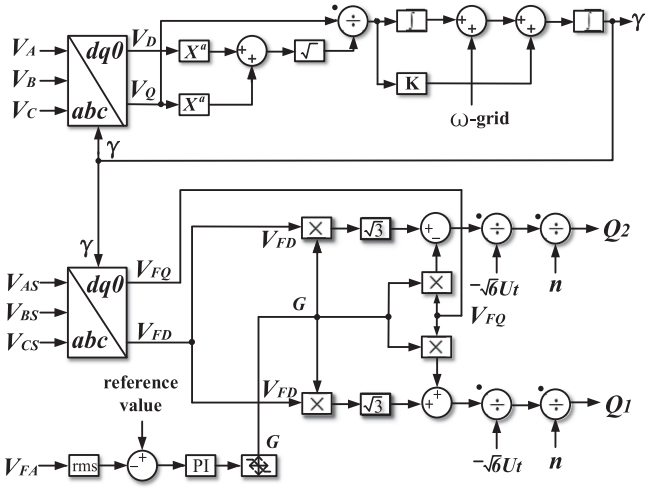

Fig. 18. Complete control block diagram of the designed closed-loop control strategy.

used to compensate for the value of Q_1 and Q_2, which contributes to the voltage amplitude closed-loop control of node FO. The PI parameters *Kp* and *Ti* can be obtained by Ziegler–Nichols method and further tuning [34], [35]. In Fig. 17, n is the isolation transformer's winding ratio and U_t is the rms value of node ST voltage. The detailed derivation process of the equations presented in Fig. 17 is given in the Appendix. When the grid is in normal operation, the three FACLs of Fig. 3 use the same voltage transfer ratios.

In this section, the closed-loop control strategy is designed based on DSRRF, twice Park's transformation, and PI controller. The DSRRF and the designed control strategy are interdependent. They constitute the contribution together to the field of FACL control. The complete control block diagram is shown in Fig. 18. It can be seen that there is no complex operation and high-order function. The correctness and feasibility are verified in the following simulations and experiments.

V. Simulation and Experiment

A. Simulation Results

Based on Fig. 3, the three-phase FACL simulation system is built on the platform of PSIM. The proposed new bipolar FACL and control strategy are applied. The simulation results and analyses are presented in this section. Table III gives the specific simulation parameter settings.

The simulation waveforms under open-loop control are illustrated in Fig. 19. To meet the set parameters of node FO voltage in Table III, Q_1 is -0.13 and Q_2 is -0.72 after calculating according to formulas (4) and (5). The loads are $R = 16\ \Omega$, and $L = 53$ mH. It can be seen from Fig. 19 that the amplitude and initial phase of node FO voltage meet the set values well in the simulation. Moreover, the output of FACL is stable and the power quality is good. V_{AH} and I_{AH} in Fig. 19(b) are unfiltered output voltage and output current of FACL I. It can be seen that there is no large impulse voltage or current in high-frequency

TABLE III
SIMULATION PARAMETER SETTINGS

Parameters	Values
Voltage effective value of node ST U_t	220/V
Voltage initial phase of node ST	0/rad
Voltage effective value of node FO HU_t	85/V
Voltage initial phase of node FO φ	5 π /18/rad
IGBT switching frequency	10k/Hz
Filter inductance L_f	1/mH
Filter capacitor C_f	30/uF
Transformer winding ratio n	380:220
Input capacitor C_{lin}, C_{rin}	40/uF
Clamping capacitor C_1-C_4	10/uF

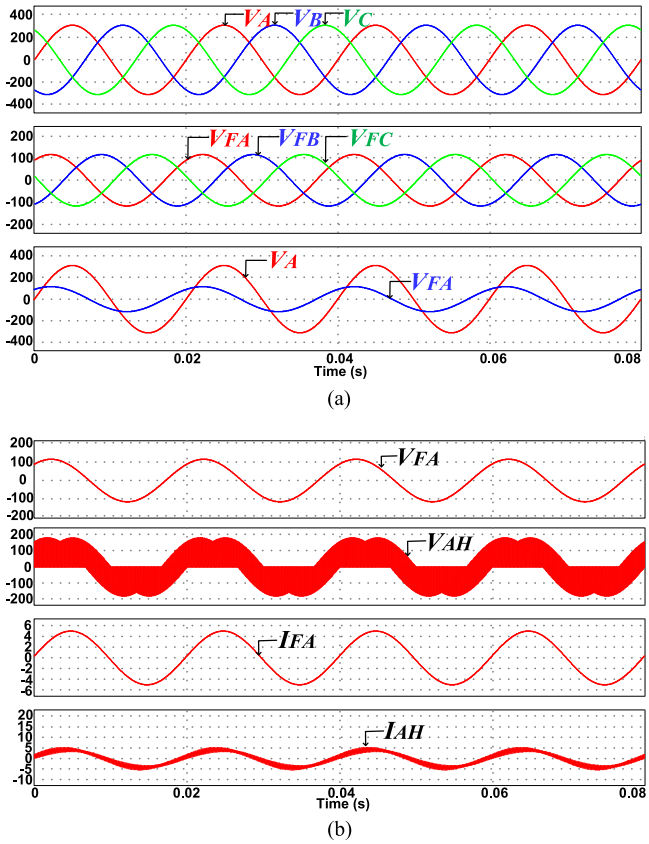

Fig. 19. Simulation results of FACL under open-loop control. (a) Three-phase voltage of node ST and output voltages. (b) High frequency quantities before filter and line frequency quantities of output side.

quantities, which ensures the safety and stability of the proposed FACL during operation.

The simulation results based on the closed-loop control strategy designed in the previous section are shown in Fig. 20. In the simulation, the input source supplying energy to FACL I, II, and III are unstable owing to voltage sag and swell of node ST. In Fig. 20, U_t does not fluctuate in [0–0.03s] period, and the voltage parameters of node FO meet the set values. Then in [0.03–0.06 s] period, U_t drops 50 V (rms). As a result, V_{FA}, V_{FB}, and V_{FC} drop at the time of $t = 0.03$s. However, due to the closed-loop control, the voltage of node FO returns to the set value after a short dynamic regulation process. Furthermore, in the [0.06–1s] period, U_t rises 60 V and the output voltages of

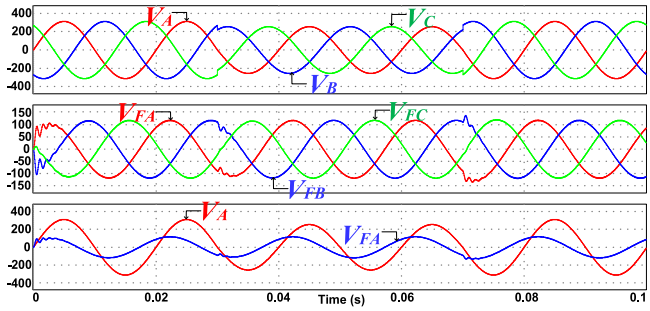

Fig. 20. Simulation results of FACL based on the closed-loop control strategy.

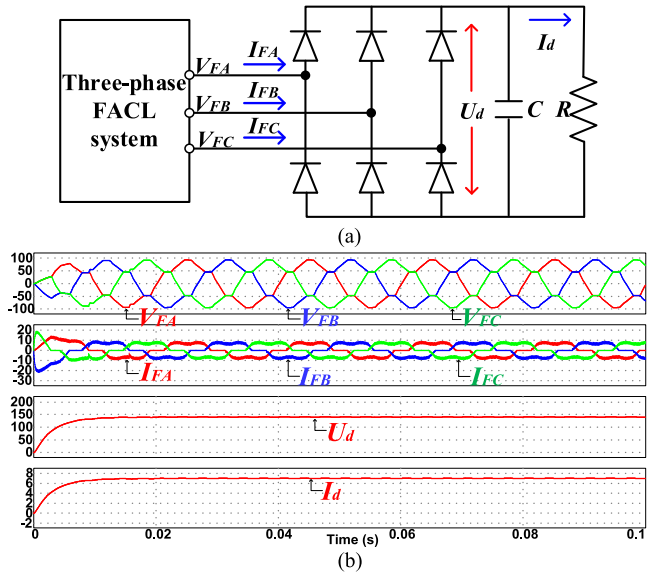

Fig. 21. Simulation results of the proposed FACL operating with nonlinear load. (a) Nonlinear load. (b) Simulation waveforms.

FACLs are capable of returning to the set value and remaining stable. It cannot be ignored that the phase difference of node FO voltage relative to node ST voltage can be kept constant all the time.

In the three-phase FACL simulation system, the results indicate that the output voltages of FACLs with controllable amplitude and initial phase can be obtained based on the proposed FACL and control strategy. The simulation results are in accordance with the theoretical analysis.

Additionally, Fig. 21 shows the simulation results of the three-phase FACL system operating with nonlinear load. The nonlinear load consists of a three-phase uncontrollable rectifier bridge with a capacitor filter and a resistive load, as shown in Fig. 21(a). Both voltage transfer ratios Q_1 and Q_2 are -0.7, and the resistive load is 20 Ω. The output voltages and currents of three FACLs and the dc voltage U_d, dc current I_d are displayed in Fig. 21(b). The results show that the dc quantities U_d and I_d have good quality. There are also voltage distortions on ac side because of the voltage drop caused by the harmonic current.

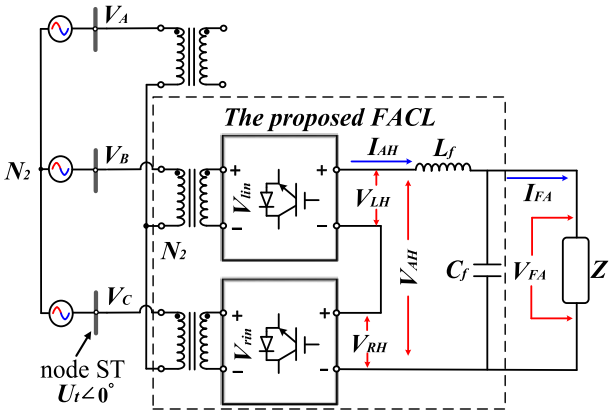

Fig. 22. Working condition of the experimental prototype.

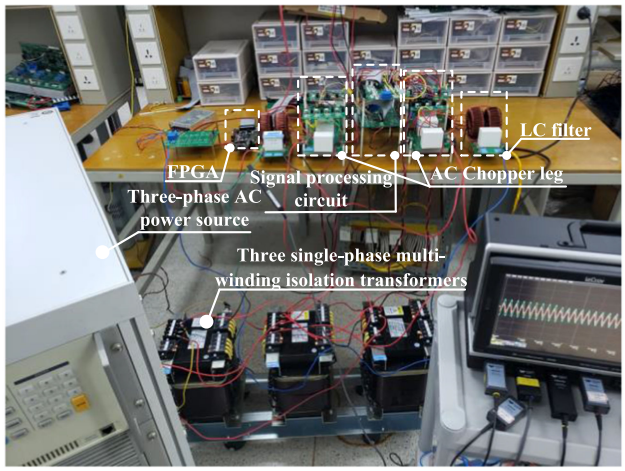

Fig. 23. Photographs of the experimental prototype. (a) Whole prototype. (b) Partial circuit board.

B. Experimental Results of FACL

To better verify the correctness and feasibility of the proposed FACL, DSRRF, and designed closed-loop control strategy, an experimental prototype of single-phase FACL is designed and built. The working condition of the experiment is illustrated in Fig. 22. The model of IGBT is FGY75N60SMD. The set value of FACL's output voltage amplitude and phase may vary in different tests. The other experimental parameters are the same as those of Table III. In addition, FPGA is selected as the controller because of its parallel operation, strong computing capability, and a large number of I/O ports. Fig. 23 shows the photographs of the experimental prototype. Based on the prototype, the open-loop and closed-loop experiments are carried out.

1) Open-Loop Experimental Tests: The open-loop experimental tests are carried out to verify the topology of the proposed FACL. The results of the proposed FACL working in all three operation modes are presented. The experimental results prove the wide output voltage range, no udesirable phase shift, continuous load current, and low component stress. During all the open-loop experiments, the input voltage of the transformer's primary side is $U_t = 220$V (rms).

Fig. 24(a) shows the gate signals of S_{L1P}, S_{R2N}, S_{L1CP}, and S_{R2P}, respectively. At this time, the duty cycles are $d_1 = 0.9$, $d_2 = 0.3$, $d_3 = 0.35$, and $d_4 = 0.95$. It can be seen that the switches operate at high frequency during only half of a line frequency cycle and operate at a normally open state during the other half. Fig. 24(b) shows the enlarged waveforms of the corresponding switch signals. It should be noted that to prevent the ac chopper legs from shoot-through fault, a dead time of 2.5 μs is set in consideration of the turn-ON and turn-OFF process of IGBT, as shown in Fig. 24(c). Fig. 24(d) shows the voltage waveforms of IGBT S_{L1P} and S_{R1N}, clamping capacitors C_1 and C_3. It can be seen that the IGBTs and clamping capacitors in the proposed FACL do not bear impulse voltage. The voltage stress is the peak value of the input voltage.

Fig. 25 shows the experimental waveforms when the load Z is pure resistive $R = 14\ \Omega$. The duty cycles are $d_1 = 0.9$, $d_2 = 0.4$, $d_3 = 0.45$, and $d_4 = 0.95$. That means the voltage transfer ratios are $Q_1 = 0.5$, and $Q_2 = -0.5$. Fig. 25(a) shows the output voltage

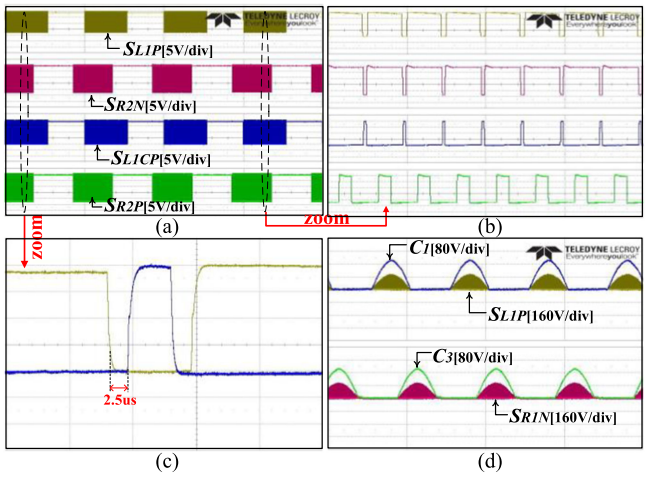

Fig. 24. Partial switching signals and voltage waveforms of IGBTs and clamping capacitors. (a) Gate signals of S_{L1P}, S_{R2N}, S_{L1CP}, and S_{R2P}. (b) Enlarged waveforms of gate signals. (c) Display of dead time. (d) Voltage waveforms of IGBT S_{L1P} and S_{R1N}, clamping capacitor C_1 and C_3.

V_{FA}, output current I_{FA}, and high-frequency voltage V_{LH}, V_{RH} of Fig. 22. Fig. 25(b) shows the waveforms of I_{FA}, V_{FA}, and A-phase voltage of node ST V_A. It can be seen that the output voltage V_{FA} lags behind V_A 90 degrees, and V_{FA}, I_{FA} remain the same phase. The amplitude and phase of the proposed FACL's

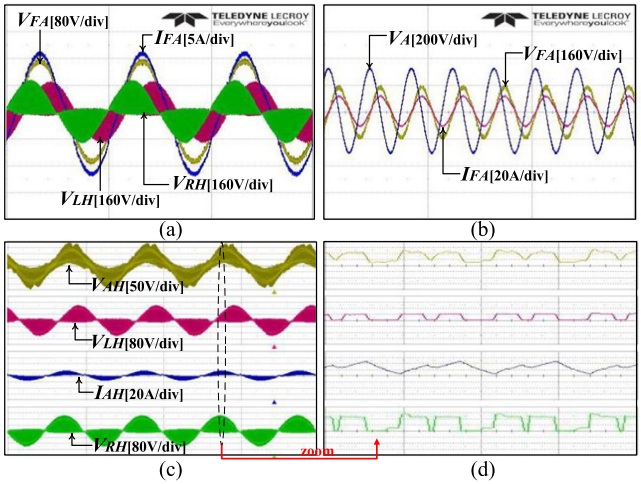

Fig. 25. Experimental results of FACL under open-loop control with resistive load ($U_t = 220$ V, $R = 14\ \Omega$, $Q_1 = 0.5$, and $Q_2 = -0.5$). (a) Waveforms of the output voltage V_{FA}, output current I_{FA}, and high-frequency voltage V_{LH}, V_{RH}. (b) Waveforms of I_{FA}, V_{FA}, and A-phase voltage of node ST V_A. (c) Waveforms of the voltage and current before filtering V_{AH} and I_{AH}, high-frequency voltage V_{LH} and V_{RH}. (d) Enlarged waveforms of each quantity in the dotted ellipse.

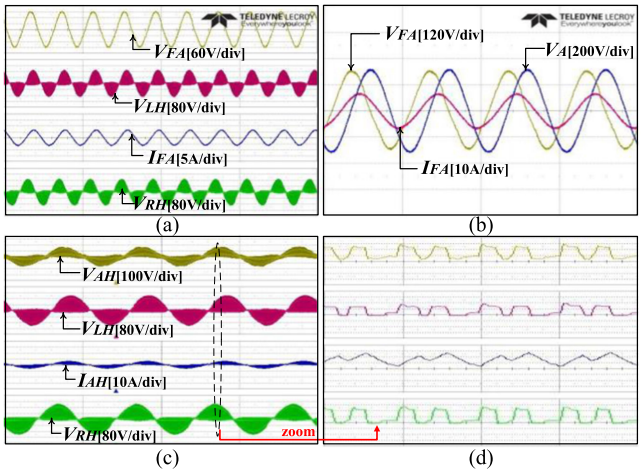

Fig. 26. Experimental results of FACL under open-loop control with resistance-inductance load ($U_t = 220$ V, $R = 20\ \Omega$, $L = 53$ mH, $Q_1 = -0.6$, and $Q_2 = 0.6$). (a) Waveforms of the output voltage V_{FA}, output current I_{FA} and high-frequency voltage V_{LH}, V_{RH}. (b) Waveforms of I_{FA}, V_{FA}, and A-phase voltage of node ST V_A. (c) Waveforms of the voltage and current before filtering V_{AH} and I_{AH}, high-frequency voltage V_{LH} and V_{RH}. (d) Enlarged waveforms of each quantity in the dotted ellipse.

output are consistent with the set voltage transfer ratios, and there is no undesirable phase shift. The voltage and current before filtering V_{AH}, I_{AH}, high-frequency voltage V_{LH} and V_{RH} are shown in Fig. 25(c). Fig. 25(d) presents the enlarged waveforms of each quantity in Fig. 25(c).

Also, the experiment with resistance-inductance load is carried out. The resistance $R = 20\ \Omega$ and the inductance $L = 53$ mH. The duty cycles are set as $d_1 = 0.3$, $d_2 = 0.9$, $d_3 = 0.8$, and $d_4 = 0.2$. At this time, the voltage transfer ratios are $Q_1 = -0.6$, and $Q_2 = 0.6$. The output voltage V_{FA}, output current I_{FA}, high-frequency voltage V_{LH} and V_{RH} are shown in Fig. 26(a). It

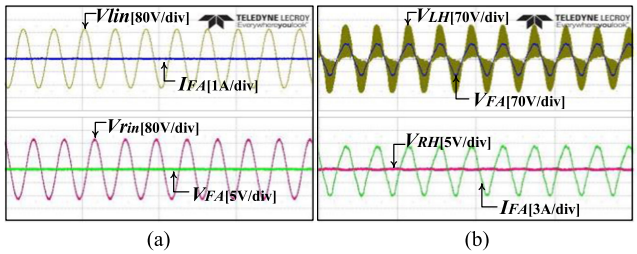

Fig. 27. Experimental results of FACL under operation modes 2 and 3. (a) Under operation mode 3. (b) Under operation mode 2.

can be seen that the output power quality is good. To observe the phase information more clearly, Fig. 26(b) shows V_A, V_{FA}, and I_{FA} in a single grid. It can be seen that the output voltage V_{FA} is 90° ahead of V_A and the amplitude and phase relationships conform to the set voltage transfer ratios. Moreover, due to the inductance of load Z, I_{FA} lags 40° behind V_{FA}. Fig. 26(c) shows the output voltage and current before filtering V_{AH}, I_{AH}, high-frequency voltage V_{LH} and V_{RH}. Fig. 26(d) shows the enlarged waveforms of the dotted ellipse in Fig. 26(c). It can be seen that the output current of the converter has four operation processes, and all of them are above the 0 scale line, which proves that the output current of the proposed FACL will not be discontinuous.

For further verifying the proposed FACL, the experimental results of working in operation modes 3 and 2 with resistive load $R = 16\ \Omega$ are presented in Fig. 27(a) and (b) respectively. Fig. 27(a) presents the waveforms of input voltage $V_{\rm lin}$ and $V_{\rm rin}$, output voltage V_{FA}, and output current I_{FA}. The duty cycles are $d_1 = 0.2$, $d_2 = 0.2$, $d_3 = 0.3$, $d_4 = 0.3$, and the voltage transfer ratios are $Q_1 = 0$, $Q_2 = 0$. It can be seen that in operation mode 3, the output of FACL is 0 and FACL is in blocking mode. When the converter is working in operation mode 2, V_{FA}, I_{FA}, the high-frequency voltage V_{LH} and V_{RH}, are shown in Fig. 27(b). At this time, $d_1 = 0.75$, $d_2 = 0.3$, $d_3 = 0.8$, and $d_4 = 0.8$, which means the voltage transfer ratios are $Q_1 = 0.45$, $Q_2 = 0$. It can be seen that the output voltage of FACL in this mode is composed of only a single input voltage, and V_{RH} is almost zero. The performance of the proposed FACL working in operation modes 3 and 2 is verified, and the experimental results are consistent with the theoretical analysis.

2) Closed-Loop Experimental Tests: To prove DSRRF and the designed closed-loop control strategy, the closed-loop experimental tests are carried out. The experimental results show that the decoupling control and closed-loop control of the FACL's output voltage amplitude and phase are achieved. In the experiments, the output voltage set value of FACL is 90 V (rms), and the phase difference $\varphi = -180°$. The input voltage rated value is $U_t = 220$ V, and the load is $R = 30\ \Omega$. The experimental results are as follows.

Fig. 28(a) shows the waveforms of node ST three-phase voltages V_A, V_B, V_C, and output voltage V_{FA}. During the period in Fig. 28(a), U_t drops from 220 to 180 V and then rises to 220 V after a while. This process keeps cyclic. It can be seen that when there is fluctuation, V_{FA} can restore to the set value within a

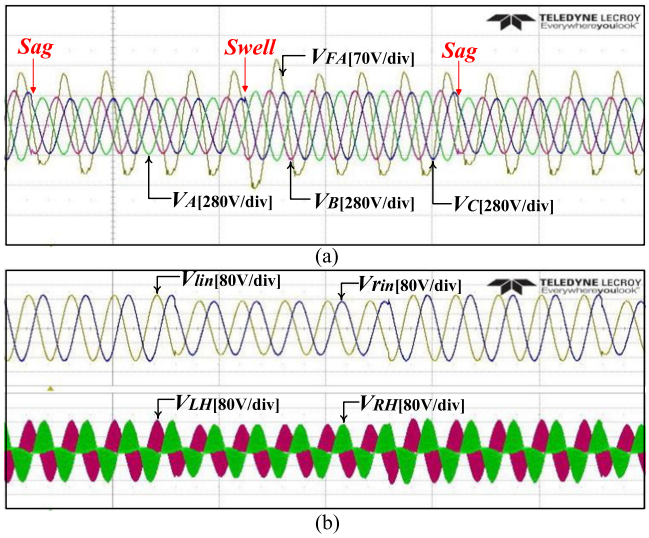

Fig. 28. Experimental results of FACL under closed-loop control with resistive load ($V_{FA} = 90$V, $\varphi = -180°$ $R = 30$ Ω). (a) Waveforms of the node ST three-phase voltages V_A, V_B, V_C and output voltage V_{FA}. (b) Waveforms of the input voltages $V_{\rm lin}$ and $V_{\rm rin}$, the high-frequency voltages V_{LH} and V_{RH} of the output side.

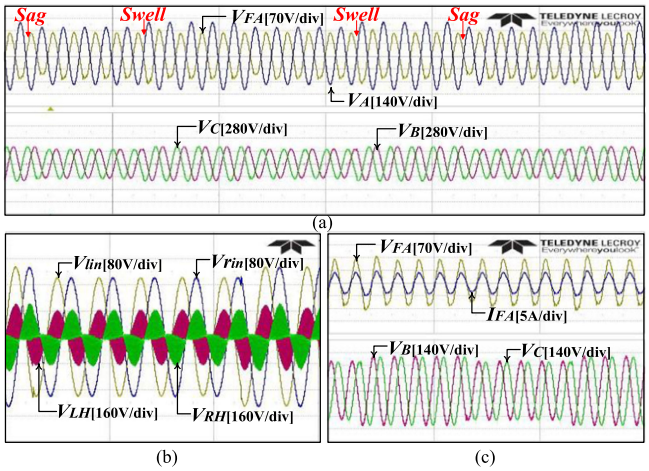

Fig. 29. Experimental results of FACL under closed-loop control with resistive load ($V_{FA} = 90$ V, $\varphi = -180°$, $R = 30$ Ω). (a) Waveforms of the node ST three-phase voltages V_A, V_B, V_C and output voltage V_{FA}. (b) Waveforms of the input voltages $V_{\rm lin}$ and $V_{\rm rin}$, the high frequency voltages V_{LH} and V_{RH} of the output side. (c) Waveforms of V_{FA}, V_B, V_C and output current I_{FA}.

line frequency cycle. Moreover, V_{FA} keeps antiphase with V_A. The results verify that the amplitude and phase of FACL's output voltage can be stabilized at the set value under the closed-loop control. The input voltage $V_{\rm lin}$ and $V_{\rm rin}$ of the proposed FACL, the high-frequency voltage V_{LH} and V_{RH} of the output side are shown in Fig. 28(b).

When the rms value U_t of the three-phase input voltage suddenly rises higher than the rated value 220 V, the waveforms of the experimental results are presented in Fig. 29. Fig. 29(a) shows the node ST three-phase voltages V_A, V_B, V_C, and output

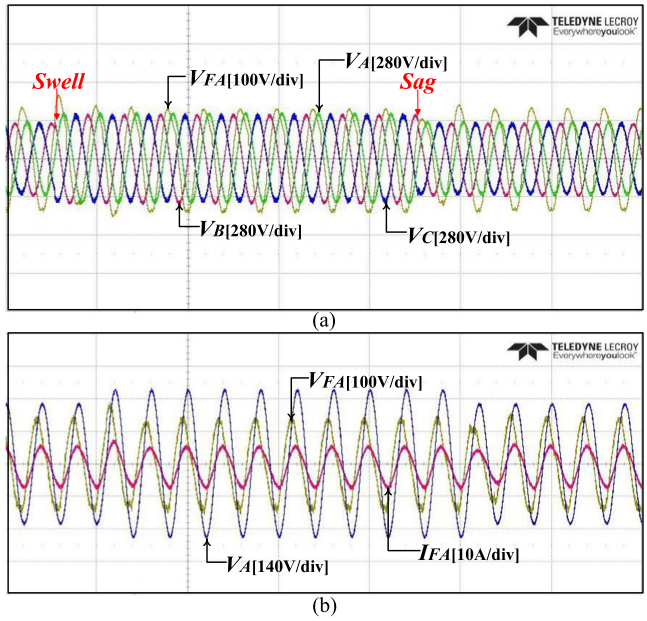

Fig. 30. Experimental results of FACL under closed-loop control with resistance-inductance load ($V_{FA} = 85$ V, $\varphi = 50°$, $R = 16$ Ω, $L = 53$ mH). (a) Waveforms of the node ST three-phase voltages V_A, V_B, V_C and output voltage V_{FA}. (b) Waveforms of V_{FA}, V_A and output current I_{FA}.

voltage V_{FA}. U_t fluctuates periodically between 220 and 260 V. In this situation, V_{FA} can still be stabilized at 90V, and the phase difference φ can be stabilized at $-180°$. The input voltage $V_{\rm lin}$ and $V_{\rm rin}$, the high-frequency voltage V_{LH} and V_{RH} of the output side are shown in Fig. 29(b). Fig. 29(c) shows the waveforms of transformer's primary side voltage V_B and V_C, output current I_{FA}, and output voltage V_{FA}.

For increasing the diversity of experiments and achieving more comprehensive verification, Fig. 30 shows the experimental results under further changes in operating conditions. The rated value of FACL's output voltage is 85 V (rms), the phase difference $\varphi = 50°$, and the load Z is resistance-inductance load $R = 16$ Ω, and $L = 53$ mH. The input voltage effective value U_t drops to 180 V periodically. Fig. 30(a) shows the waveforms of node ST three-phase voltages V_A, V_B, V_C and output voltage V_{FA}. It can be seen that when the input voltage fluctuates, V_{FA} will be influenced instantaneously, but it is capable of returning to 85 V after a short period of dynamic regulation. Fig. 30(b) shows V_A, the output current I_{FA} and the output voltage V_{FA} in a single grid. V_{FA} keeps ahead of V_A 50°, which conforms to the set value. Moreover, due to the existence of inductive load, I_{FA} lags behind V_{FA} about 46°.

VI. Conclusion

In this article, the configurations, characteristics, applications, and research status of FACLs are introduced systematically. Based on the three-phase FACL system, the power conversion principle of FACL is analyzed, and the operation characteristics between unipolar and bipolar FACL are compared. Besides, a high-performance bipolar FACL based on BT-ac is proposed.

It adopts four independent controllable degrees of freedom, which makes the output voltage regulable in all four quadrants. Compared with the existing FACLs, it has the advantages of wide output range, no undesirable phase shift, and no bidirectional switches problems.

A variant of the conventional dq reference frame called DSRRF, and a closed-loop control strategy for FACLs are proposed. DSRRF provides a platform for the flexible operation in the form of dc between two three-phase voltages, which is beneficial to FACL control. Based on DSRRF and the designed closed-loop control strategy, the decoupling control and closed-loop control of the FACL's output voltage amplitude and phase are achieved conveniently. Finally, the correctness and feasibility of the proposed FACL, DSRRF, and the closed-loop control strategy are verified by simulations and experiments.

APPENDIX

The demonstration of (4) and (5) is presented through

$$\begin{aligned}V_{FA} &= \sqrt{2}nQ_1U_t\sin(wt-\frac{2}{3}\pi)+\sqrt{2}nQ_2U_t\sin(wt+\frac{2}{3}\pi)\\ &= \sqrt{2}nU_t\left[Q_1\sin(wt-\frac{2}{3}\pi)+Q_2\sin(wt+\frac{2}{3}\pi)\right]\\ &= \sqrt{2}nU_t\left[Q_1\sin wt\cos\frac{2}{3}\pi-Q_1\cos wt\sin\frac{2}{3}\pi\right.\\ &\quad\left.+\,Q_2\sin wt\cos\frac{2}{3}\pi+Q_2\cos wt\sin\frac{2}{3}\pi\right]\\ &= \sqrt{2}nU_t\left[-\frac{1}{2}Q_1\sin wt-\frac{\sqrt{3}}{2}Q_1\cos wt-\frac{1}{2}Q_2\sin wt\right.\\ &\quad\left.+\,\frac{\sqrt{3}}{2}Q_2\cos wt\right]\\ &= \sqrt{2}nU_t\left[-\frac{1}{2}(Q_1+Q_2)\sin wt+\frac{\sqrt{3}}{2}(Q_2-Q_1)\cos wt\right]\\ &= \sqrt{2}nU_tT\sin(wt+\varphi)\end{aligned}\tag{14}$$

$$\begin{aligned}T &= \sqrt{\left[-\frac{1}{2}(Q_1+Q_2)\right]^2+\left[\frac{\sqrt{3}}{2}(Q_2-Q_1)\right]^2}\\ &= \sqrt{\frac{1}{4}(Q_1+Q_2)^2+\frac{3}{4}(Q_2-Q_1)^2}\\ &= \sqrt{\frac{1}{4}\left({Q_1}^2+{Q_2}^2+2Q_1Q_2\right)+\frac{3}{4}\left({Q_1}^2+{Q_2}^2-2Q_1Q_2\right)}\\ &= \sqrt{{Q_1}^2+{Q_2}^2-Q_1Q_2}\end{aligned}\tag{15}$$

$$\begin{aligned}\varphi &= \arctan\left[\frac{\frac{\sqrt{3}}{2}(Q_2-Q_1)}{-\frac{1}{2}(Q_1+Q_2)}\right]\\ &= \arctan\left[-\frac{\sqrt{3}(Q_2-Q_1)}{Q_1+Q_2}\right]\end{aligned}\tag{16}$$

$$\dot{V_{FA}} = HU_t\angle\varphi\tag{17}$$

$$\begin{aligned}H &= nT\\ &= n\sqrt{{Q_1}^2+{Q_2}^2-Q_1Q_2}.\end{aligned}\tag{18}$$

The detailed derivation process of the equations presented in the block diagram of Fig. 17 is given as

$$\frac{\left|\dot{V_F}\right|}{\sin(\pi/3)}=\frac{-Q_2\left|\dot{U_C}\right|}{\sin(\pi/3-\varphi)}=\frac{-Q_1\left|\dot{U_B}\right|}{\sin(\pi/3+\varphi)}\tag{19}$$

$$\sin\varphi=\frac{\left|\dot{V_{FQ}}\right|}{\left|\dot{V_F}\right|}\tag{20}$$

$$\cos\varphi=\frac{\left|\dot{V_{FD}}\right|}{\left|\dot{V_F}\right|}\tag{21}$$

$$\begin{aligned}\frac{\left|\dot{V_F}\right|}{\sin(\pi/3)} &= \frac{-Q_2\left|\dot{U_C}\right|}{\sin(\pi/3-\varphi)}\\ Q_2 &= \frac{\left|\dot{V_F}\right|\sin(\pi/3-\varphi)}{-\sin(\pi/3)\left|\dot{U_C}\right|}\\ &= \frac{\left|\dot{V_F}\right|\left[\sin(\pi/3)\cos\varphi-\cos(\pi/3)\sin\varphi\right]}{-\sin(\pi/3)\left|\dot{U_C}\right|}\\ &= \frac{\left|\dot{V_F}\right|\left[\frac{\sqrt{3}}{2}\cos\varphi-\frac{1}{2}\sin\varphi\right]}{-\frac{\sqrt{3}}{2}\left|\dot{U_C}\right|}\end{aligned}\tag{22}$$

$$\begin{aligned}Q_2 &= \frac{\left|\dot{V_F}\right|\left[\frac{\sqrt{3}}{2}\frac{\left|\dot{V_{FD}}\right|}{\left|\dot{V_F}\right|}-\frac{1}{2}\frac{\left|\dot{V_{FQ}}\right|}{\left|\dot{V_F}\right|}\right]}{-\frac{\sqrt{3}}{2}\bullet n\sqrt{2}U_t}\\ &= \frac{\sqrt{3}\left|\dot{V_{FD}}\right|-\left|\dot{V_{FQ}}\right|}{-\sqrt{6}nU_t}\end{aligned}\tag{23}$$

$$\frac{\left|\dot{V_F}\right|}{\sin(\pi/3)} = \frac{-Q_1\left|\dot{U_B}\right|}{\sin(\pi/3+\varphi)}$$

$$\begin{aligned} Q_1 &= \frac{\left|\dot{V_F}\right|\sin(\pi/3+\varphi)}{-\sin(\pi/3)\left|\dot{U_B}\right|} \\ &= \frac{\left|\dot{V_F}\right|\left[\sin(\pi/3)\cos\varphi+\cos(\pi/3)\sin\varphi\right]}{-\sin(\pi/3)\left|\dot{U_B}\right|} \\ &= \frac{\left|\dot{V_F}\right|\left[\frac{\sqrt{3}}{2}\cos\varphi+\frac{1}{2}\sin\varphi\right]}{-\frac{\sqrt{3}}{2}\left|\dot{U_B}\right|} \end{aligned} \tag{24}$$

$$\begin{aligned} Q_1 &= \frac{\left|\dot{V_F}\right|\left[\frac{\sqrt{3}}{2}\frac{\left|\dot{V_{FD}}\right|}{\left|\dot{V_F}\right|}+\frac{1}{2}\frac{\left|\dot{V_{FQ}}\right|}{\left|\dot{V_F}\right|}\right]}{-\frac{\sqrt{3}}{2}\bullet n\sqrt{2}U_t} \\ &= \frac{\sqrt{3}\left|\dot{V_{FD}}\right|+\left|\dot{V_{FQ}}\right|}{-\sqrt{6}nU_t}. \end{aligned} \tag{25}$$

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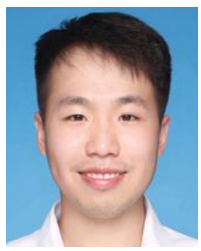

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