Investigation and On-Board Detection of Gate-Open Failure in SiC MOSFETs

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***Abstract*—Gate-open failures in power semiconductors occur when the gate-bond wire cracks or lifts-off leading to loss of gate control. In molded discrete devices, this failure mode may occur intermittently making it very challenging to analyze and detect. In this article, intermittent gate-open failures are comprehensively investigated in the context of discrete silicon carbide (SiC) MOSFETs. First, the MOSFET's behavior under various possible gate-open failure scenarios is analyzed in detail through simulations. Several SiC MOSFETs are aged on a dc power cycling setup and gate-open failure mechanism is verified through systematic multistep failure analysis, which includes on-board characterization, nondestructive C-SAM analysis, decapsulation, and optical inspection followed by scanning electron microscopy analysis of the failed devices. To understand the potential mechanism behind gate-open failure in SiC MOSFETs, thermo-mechanical finite element analysis analysis is performed on a high-fidelity model that shows interfacial shear stress at gate-bond. Furthermore, a robust on-board technique for reliable cycle-by-cycle detection of gate-open faults is proposed. The proposed technique is experimentally verified for all possible fault scenarios and shown to detect faults in as low as 150 ns. It is shown that compared to the traditional DESAT protection scheme, the proposed mechanism can prevent potential shoot-through events that may be caused by gate-open failure.**

***Index Terms*—Bond-wire, condition monitoring, reliability, silicon carbide (SiC) MOSFETs.**

I. Introduction

SILICON carbide (SiC) power MOSFETs are expected to enable a significant improvement in efficiency of power converters across different application areas [1]. However, comprehensively understanding and improving their reliability remains an ongoing challenge [2]–[4]. To this end, standard accelerated aging tests are often used to proactively test long term device reliability within a short duration. Among the standard tests, dc power cycling is widely used to accelerate package related aging mechanisms in power MOSFETs [5], [6]. Bond-wire heel cracking, bond-wire liftoff, and die attach solder layer delamination are the common failure modes observed in this test [7]–[11]. In addition to the above modes, power MOSFETs could also fail due to gate bond-wire liftoff or cracking leading to a gate-open failure [12]. The consequent loss of gate control can lead to unwanted drain to source conduction, large increase in threshold voltage or open circuit failure of device [13]. This mode of failure, however, is relatively uncommon in silicon (Si) MOSFETs and IGBTs and has not been studied widely in literature. Like Si MOSFETs and IGBTs, commercial discrete SiC MOSFETs are typically available in TO-247-3, TO-247-4, and TO-263-7 packages [14], [15]. However, SiC MOSFETs generally have a much smaller die and fundamentally different material properties [16]. Therefore, package related failure modes in Si devices cannot be assumed to apply similarly to SiC devices. In particular, relatively thinner and longer gate bond wires due to smaller die and die placement can potentially increase SiC devices' susceptibility to gate-open failures. Moreover, the properties of the epoxy mold compound (EMC) material used in SiC MOSFETs need to be different to enable operation at higher temperature [17], [18]. Therefore, it is crucial to study gate-open failure mode specifically in the context of SiC MOSFETs.

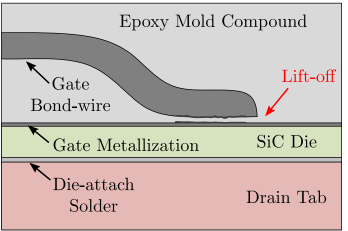

Fig. 1. Illustration of gate-open failure in discrete SiC MOSFET due bond-wire liftoff.

Gate-open failures in discrete devices are often intermittent in nature. In a typical discrete SiC MOSFET, the die and gate bond-wire are encapsulated in EMC as shown in Fig. 1. In case of gate bond-wire liftoff, the EMC may hold the bond-wire to the pad and cause the contact to exist [19]. However, during device operation, the relative displacement of various components in the package due to thermal changes can lead to intermittent gate contact. The device functions normally except

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during brief instances of loss of gate contact. Therefore, the intermittency of gate-open faults makes them very challenging to detect reliably. Given their elusive nature, comprehensive failure analysis of gate-open faults is also challenging [13]. Undetected intermittent gate-open failures during dc power cycling tests can lead to incorrect device lifetime estimation [20]. Moreover, in certain converter topologies, temporary disturbances caused by intermittent gate-open failures can be compensated by the control loop and potentially go undetected for a long time. For example, in synchronous converters, if a gate-open failure of the synchronous switch prevents it from turning ON, the switch's body-diode starts conducting. Therefore, except a decrease in its efficiency, the converter appears to operate nominally.

To address the above challenges, the first goal of this article is to investigate the occurrence of gate-open failures in discrete SiC MOSFETs. To reliably detect gate-open failure during dc power cycling or converter operation, it is important to first understand the electrical behavior of an SiC MOSFET under all possible gate-open failure scenarios. Therefore, the state of device's gate and channel under gate-open faults are comprehensively analyzed through SPICE simulations and analytical modeling. Furthermore, the devices under test (DUTs) are aged using dc power cycling test. An on-board characterization technique is presented to detect gate-open failures during dc power cycling. Gate-open failure is detected in four of the DUTs. In order to verify the occurrence of gate-open failure in the failed devices, first, nondestructive acoustic microscopy analysis is performed to identify damage sites. Thereafter, the failed devices are carefully decapsulated and inspected through optical microscopy and scanning electron microscopy (SEM). To understand the mechanism behind gate-open failures, a thermo-mechanical finite element analysis (FEA) is performed on a high fidelity model of the DUT. It is shown that deformation caused by coefficient of thermal expansion (CTE) mismatch between various elements of the package causes interfacial shear stress in the gate bond. The stress is concentrated at the interface causing the gate bond wire to shear off. The simulations are repeated for two different properties of the EMC in order to analyze the impact of EMC's CTE on the gate bond stress. In addition to investigating gate-open failure, this article also proposes a robust on-board technique for cycle-by-cycle detection of gate-open failures. The failure detection circuit and logic is presented in detail. Through experimental verification, it is shown that the proposed technique can detect gate-open failure in as low as 150 ns. This enables the prevention of potentially catastrophic shoot-through events in a conduction type gate-open failure scenario. Furthermore, the proposed technique can reliably detect gate-open failures in third quadrant operation, which is not covered by conventional protection techniques.

II. Gate-Open Failure Analysis and On-Board Characterization

A. MOSFET's Behavior Under Various Gate-Open Failure Scenarios

Given the challenges in capturing intermittent gate-open failures, it is important to first understand the electrical behavior of a SiC MOSFET under gate-open failure. For the purpose of

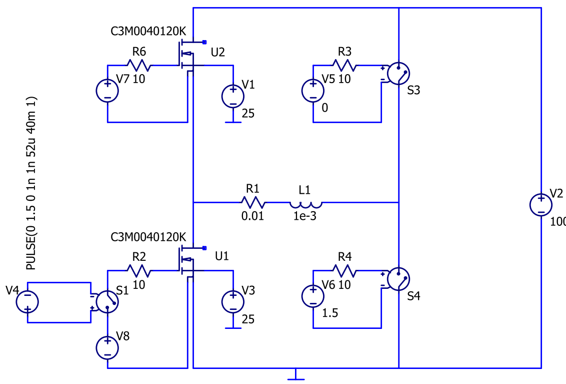
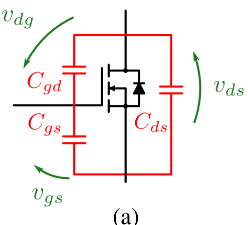
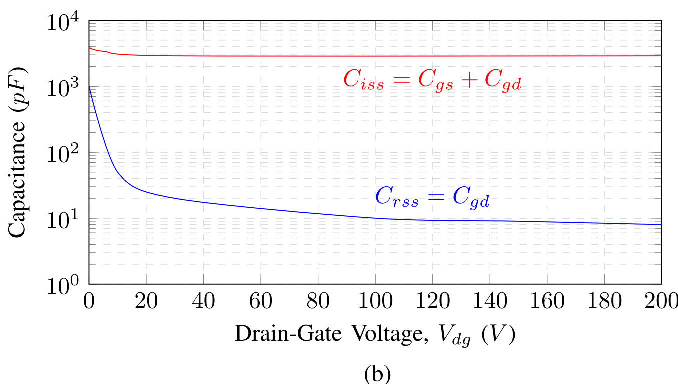


Fig. 2. SPICE simulation circuit for analysis of MOSFET's behavior under gate-open fault.



(a)



(b)

Fig. 3. (a) Parasitic capacitance in a MOSFET. (b) C_{gd} versus V_{dg} from device datasheet [22].

this analysis, the circuit shown in Fig. 2 is simulated in LTspice. Manufacturer provided SPICE model is used for the DUT, $U1$. Gate-open fault is simulated by connecting an ideal switch $S1$ in the gate path of $U1$. The timing of the $S1$'s opening is changed to simulate different gate-open failure scenarios. Furthermore, switches $S3$ and $S4$ are used to change the operational quadrant of the DUT. Specifically, when $S3$ is closed and $S4$ is open, $U1$ operates in the first quadrant ($Q1$) during its on interval. Similarly, when $S4$ is closed and $S3$ is open, $U1$ acts as the synchronous free-wheeling switch during its on interval and thus operates in the third quadrant ($Q3$).

Before discussing the simulation results, analytical expressions for the DUT gate voltage under fault (V_{gs}^{f}) are derived. Fig. 3(a) shows the electrical model of the DUT with parasitic capacitances. In case of a gate-open fault, the gate is electrically isolated and floating. Consequently, the charge on C_{gd} and C_{gs} is conserved. If the DUT's drain–source voltage after fault (V_{ds}^{f}) is different from before fault (V_{ds}^{pf}), the voltage across C_{gs} and

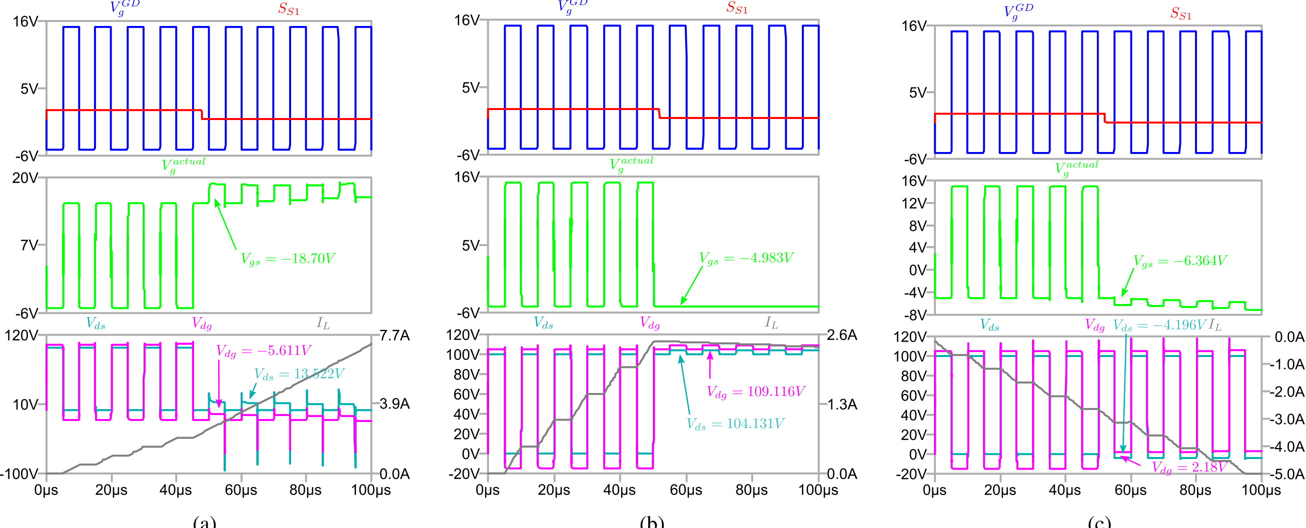


Fig. 4. Simulation waveforms under (a) conduction fault, (b) $Q1$ open fault, and (c) $Q3$ open fault.

C_{gd} changes correspondingly as given by (1)–(4). However, the charge on C_{gd} and C_{gs} changes by the same amount (ΔQ_f), since it is conserved. DUT's V_{gs}^f under fault, in this case, can be obtained using (5), where the relation between ΔQ_f and V_{dg} is given by (6) since C_{gd}, unlike C_{gs}, is nonlinear and a function of V_{gd} as shown in Fig. 3(b). The value of the integral can be obtained by calculating the corresponding area under the C_{gd} versus V_{gd} curve obtained from manufacturer's datasheet. In cases where V_{dg} is large or $V_{dg} \leq 0$, C_{gd} is nearly constant and can be approximated by (7) [21]. (6) then reduces to (8) and using (9), postfault V_{gs}^f is given by (10). Moreover, when V_{dg} is large, usually $C_{gd} << C_{gs}$. Therefore, (10) can be further approximated to (11). These equations are used in conjunction with the SPICE simulation results to understand the MOSFET's behavior under various gate-open fault scenarios as discussed further

$$\Delta V_{ds} = V_{ds}^f - V_{ds}^{pf} \tag{1}$$

$$\Delta V_{dg} = -(V_{gd}^f - V_{gd}^{pf}) \tag{2}$$

$$\Delta V_{gs} = V_{gs}^f - V_{gs}^{pf} = \frac{\Delta Q_f}{C_{gs}} \tag{3}$$

$$\Delta V_{ds} = \Delta V_{dg} + \Delta V_{gs} \tag{4}$$

$$V_{gs}^f = V_{gs}^{pf} + \frac{\Delta Q_f}{C_{gs}} \tag{5}$$

$$\text{where } \Delta Q_f = \int_{V_{dg}^{pf}}^{V_{dg}^f} C_{gd}(v_{dg})dv. \tag{6}$$

If V_{dg} is large or $V_{dg} \leq 0$, C_{gd} is almost constant. Then

$$C_{gd} = C_{gd}(V_{dg}^{pf}) = C_{gd}(V_{dg}^f) \tag{7}$$

$$\Delta Q_f = C_{gd}\Delta V_{dg} \tag{8}$$

$$\Delta V_{ds} = \Delta Q_f \left(\frac{1}{C_{gd}} + \frac{1}{C_{gs}}\right) \tag{9}$$

$$V_{gs}^f = V_{gs}^{pf} + \left(\frac{C_{gd}}{C_{gd} + C_{gs}}\right) \Delta V_{ds}. \tag{10}$$

If V_{dg} is large, $C_{gd} << C_{gs}$. Therefore, V_{gs}^f can be approximated to

$$V_{gs}^f = V_{gs}^{pf} + \left(\frac{C_{gd}}{C_{gs}}\right) \Delta V_{ds}. \tag{11}$$

1) Case 1–Conduction Fault: First, gate-open failure event can occur when the DUT is ON. As shown in Fig. 4(a), this is mimicked by opening $S1$ when DUT is ON. In the subsequent off period when gate driver voltage, V_g^{GD} is low, the DUT's actual gate-voltage, V_g^{actual} remains high. During this period, the shoot-through current in $U1$ starts rising as soon as $U2$ turns ON. As shown, this causes V_{ds} and thus V_{dg} to increase. From (5) and (6), it is evident that V_{gs} increases further. Due to SiC MOSFET's high transconductance, an increase in V_{gs} results in significant decrease in $U1$'s ON-state resistance, thus preventing a further increase in V_{ds}. From Fig. 4(a), it is seen that $V_{ds}^f = 13.54$ V and $\Delta V_{ds} = 13.455$ V. Since, $V_{dg}^{pf} < V_{dg}^f < 0$, C_{gd} can be assumed constant such that $C_{gd} = 1000$ pF and $C_{gs} = 2900$ pF. By using (10) and known $V_{gs}^{pf} = 15$ V, V_{gs}^f is calculated as $V_{gs}^f = 18.45$ V ($\Delta V_{gs} = 3.45$ V). This is very close to experimentally observed value of 18.70 V. Therefore, a conduction fault causes the gate voltage of the failed device to increase further and prevents it from turning OFF. Furthermore, this also causes unequal short-circuit energy dissipation between the high-side and low-side devices. Since majority of the power is dissipated in the complementary high-side switch, it may be damaged if the fault is not isolated.

2) Case 2a - Open Fault in Q1 Operation: Alternatively, gate-open failure can occur when the $U1$ is OFF. The DUT gate voltage remains low in this case even in $U1$'s ON interval. Since $U2$ is OFF in this interval, the body-diode of $U2$ turns ON to provide a free wheeling path to inductor current (I_{L1}). As shown in Fig. 4(b) $\Delta V_{ds} = 4.13$ V, which is equal to the forward

voltage drop of $U2$'s body-diode. Since $V_{ds}^{f} \approx V_{ds}^{pf} = 100$ V, C_{gd} can be assumed to be constant at $C_{gd} = 10$ pF. From (11), $\Delta V_{gs} = 0.015$ V and $V_{gs}^{f} = -4.985$ V, which is very close to experimentally obtained value of -4.983 V. Therefore, in case of an open type gate-open fault in Q1 operation, the DUT's gate voltage remains nearly constant and the device remains OFF. It is also seen from Fig. 4(b) that the inductor current is decaying due to $U2$'s body-diode loss. Moreover, as the application voltage increases ΔV_{gs} becomes increasingly insignificant.

3) Case 2b—Open Fault in Q3 Operation: Finally, an open type gate-open fault may occur when the device is operating in Q3. In such a case, the device experiences a gate-open fault when it is OFF as shown in Fig. 4(c). When the device is subsequently turned ON, the device's channel fails to turn ON. However, since the device is operating in Q3, its body-diode starts conducting. ΔV_{ds} and ΔV_{dg} are negative. Consequently, from (5) and (6), the DUT's gate voltage decreases further. Since V_{gs}^{pf} is negative, V_{gs}^{f} becomes more negative as clearly seen in Fig. 4(c). Obtaining V_{gs}^{f}, requires the solution of (6). In Fig. 3(b), $V_{dg}^{pf} = 100$ V and $V_{dg}^{f} = 2.1808$ V. By assuming C_{gd} to be piecewise exponential function in these intervals, the approximate value of ΔQ_f is obtained as $\Delta Q_f = 4149.36$ nC. V_{gs}^{f} thus calculated from (5) is $V_{gs}^{f} = -6.43$ V. This is in close agreement with value obtained from simulation i.e., $V_{gs}^{f} = -6.35$ V. Therefore, it can be safely concluded that under gate-open failure in Q3 operation, the DUT remains OFF with its gate voltage becoming more negative.

The above analysis proves that under all three fault scenarios, the device's state gets latched when a gate-open fault occurs. Specifically for conduction type and Q3-open type fault scenarios, gate-open failure has a positive feedback effect on device's gate voltage. This implies that the device's operational state under fault is stable and does not slowly change over time. Similar behavior is also observed for Q1-open failure scenario. However, in this case although the fault has a negative feedback effect on gate-voltage, the magnitude is negligible. This understanding is essential in developing on-board gate-open failure detection technique. It is important to note, however, that due to its intermittent nature, a device with a particular gate-open fault type may temporarily recover and later show another fault type. For example, unless isolated, a device with open type fault may have temporary re-establishment of gate-contact due to bond-wire movement and then show a conduction fault. The intermittent nature, in particular, makes accurate characterization and detection of gate-open faults extremely challenging.

B. DC Power Cycling Test Methodology

Fig. 5(a) shows the high level schematic of the dc power cycling setup used in this study. Each leg of the setup has one DUT and a main switch (MSW) in series. The MSW is used for safe fault detection and isolation. Multiple legs are connected in parallel across the main power supply. One leg is on at any given time, heating up corresponding DUT. As shown in Fig. 5(b), when the DUT reaches its maximum junction temperature ($T_{j-\max}$), it is turned OFF for cooling and the next DUT is turned ON. The cycles are repeated till device failure. This setup allows independent control of ΔT_j of each DUT.

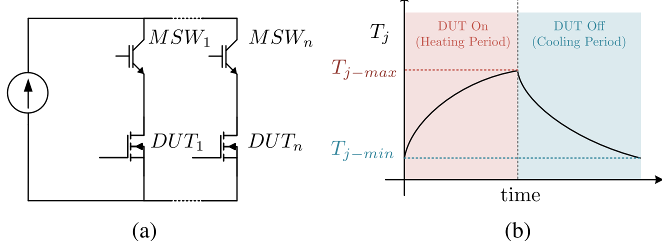


Fig. 5. (a) DC power cycling schematic. (b) Typical testing cycle.

TABLE I
DC POWER CYCLING TEST RESULTS

DUT No.	T_j Swing	T_j Mean	ΔT_j	Cycles to Failure(N_f)
DUT1-A	$55°C - 150°C$	$102.5°C$	$95°C$	6000
DUT1-B	$55°C - 150°C$	$102.5°C$	$95°C$	7200
DUT2-A	$35°C - 150°C$	$92.5°C$	$115°C$	8000
DUT2-B	$35°C - 150°C$	$92.5°C$	$115°C$	7800

In this article, a total of eight devices, in two groups of four are tested under two different ΔT_j conditions. Of these, two devices in each batch are detected with gate-open failure as shown in Table I. The devices used are 1000 V, 22 A SiC MOSFET in TO-247-4 package is selected for this article. The table also shows the recorded cycles to failure (N_f) corresponding to each of the devices. Here, failure is defined as the first detection of gate-open fault. Comprehensive failure analysis of these devices is discussed further.

C. On-Board Failure Characterization

1) On-Board Failure Characterization Technique: Based on the understanding of electrical behavior of devices with intermittent gate-open failure, an on-board failure characterization technique is proposed. Fig. 6 shows the operation of the dc power cycling setup [23]. During heating period, as shown in Fig. 6(a), both MSW and the DUT are ON. Therefore, the DUT drain current is $I_{d-\mathrm{DUT}} > 0$. However, during DUT cooling period, the DUT and MSW are turned ON alternatively during intervals labeled as T_n' [see Fig. 6(b)] and T_n [see Fig. 6(c)]. In this study, $T_n' \approx 20$ ms and $T_n \approx 2$ ms are selected. This process is repeated throughout the DUT cooling period. For a healthy DUT, $I_{d-\mathrm{DUT}} = 0$ during T_n' and T_n.

In case of a conduction type gate-open fault, since the DUT fails to turn-OFF, $I_{d-DUT} > 0$ during the interval T_n as shown in Fig. 6(d). The on-board controller of the dc power cycling test bench detects this current and identifies the fault. T_n' interval is necessary to charge the DUT gate to check for intermittent failure. Specifically, the proposed technique verifies the gate function of the DUT by repeatedly charging and discharging the DUT gate. In case the gate contact is temporarily lost, the DUT gate fails to discharge and shows a conduction fault. The MSW isolates the DUT during the testing process. However, in this setup, the DUT can be checked for open fault only at the beginning of heating period as shown in Fig. 6(e). If $I_{d-\mathrm{DUT}} = 0$ when both DUT and MSW are turned ON, it implies the DUT has

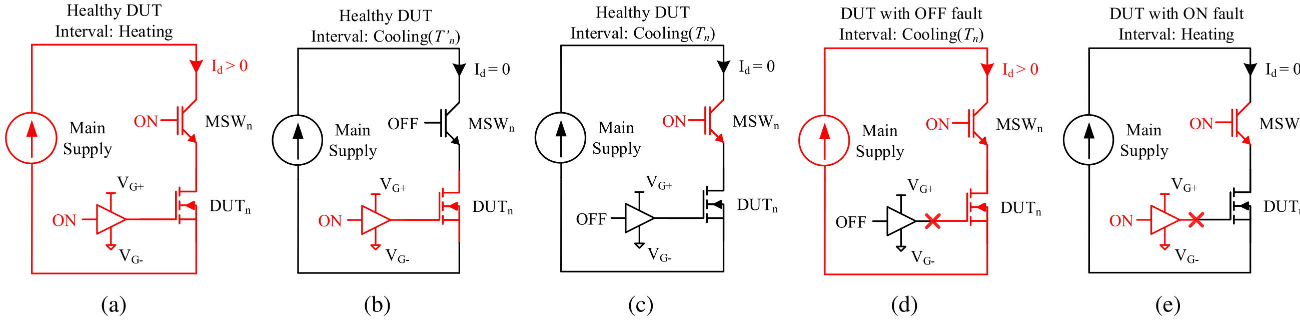


Fig. 6. Operation of a single leg of the dc power cycling test setup during (a) heating interval for a healthy DUT, (b) cooling T'_n interval for a healthy DUT, (c) cooling T_n interval for a healthy DUT, (d) cooling T_n interval for a DUT showing OFF fault, and (e) heating interval for a DUT with ON fault.

TABLE II
FAILURE CONDITIONS FOR ON-BOARD GATE-OPEN FAULT CHARACTERIZATION

Interval	MSW Status	DUT GD Status	Expected Condition	Observed Condition	Fault Type
Cooling (T_n)	On	Off	$I_d = 0$	$I_d > 0$	Q1 Conduction Fault
Heating	On	On	$I_d > 0$	$I_d = 0$	Q1 Open Fault

TABLE III
MATERIAL PROPERTIES USED FOR FEA SIMULATION

Element	Material	Density (kg/m^3)	CTE (ppm/$^\circ C$)	Young's Modulus (GPa)
Drain tab, Gate lead	Copper	8300	18	110
Gate bond-wire	Aluminium	2770	23	71
EMC	-	1780	10	30
Die	SiC	3100	2.75	400

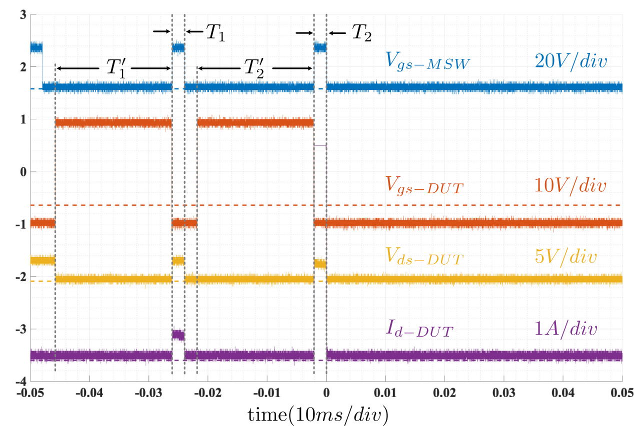


Fig. 7. On-board characterization result for DUT showing intermittent OFF fault (Case 1).

an open fault. Moreover, since the DUT does not operate in Q3 in dc power cycling, it is not checked for. Failure conditions for on-board fault characterization of gate-open faults are summarized in Table III.

2) Results of On-Board Characterization: The result from on-board characterization study of DUT 1-A experiencing intermittent gate-open failure during dc power cycling is shown in Fig. 7. As observed, during intervals T_1 and T_2 when DUT is OFF and MSW is ON, a current is flowing through the DUT indicating a conduction fault. It must be noted, however, that the magnitude of current in interval T_1 is ~ 0.5A, whereas in T_2 it is ~ 4A. In fact, current probe setting for detecting the small current in T_1 leads to probe saturation at high current during T_2, making the current peak unclear. It implies that drain to source impedance during T_1 is high, whereas the channel is fully open during T_2. Also, no current is observed before the interval T_1. This clearly shows that the gate-open failure in this case is intermittent in nature. Moreover, the significant decrease in drain–source resistance during T_2 compared with T_1 could be because of a temporary gate contact during T'_2 when the DUT is ON. Fig. 8 shows scope result of another on-board characterization study of a failed DUT. In this case, conduction fault is observed in interval T_1 prior to which the device appears to be healthy, again highlighting the intermittency of the fault. During T_1, the current through the DUT is ~ 3.5 A. It must be noted that the DUT is tested for failure during its cooling interval when another DUT is heating up. Therefore, in case of conduction fault, approximately half of the main power supply current flows through the failed DUT. Since the main power supply current setting for this test is 7 A, it implies that the failed DUT's channel is fully ON. Therefore, it can concluded that the gate-open failure occurred when the DUT is ON during T'_1. In this case, since the gate is fully charged, a gate-open failure during T'_1 interval leads to DUT staying on during T_1.

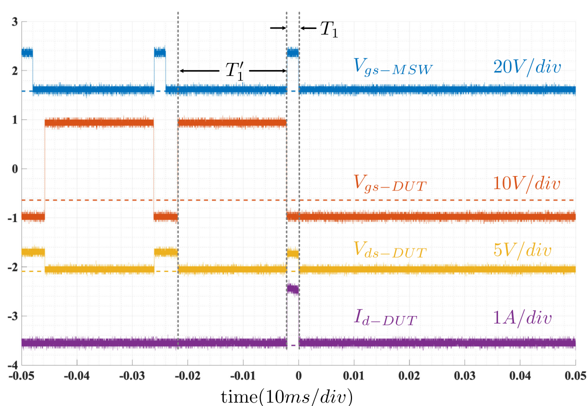


Fig. 8. On-board characterization result for DUT showing intermittent OFF fault (Case 2).

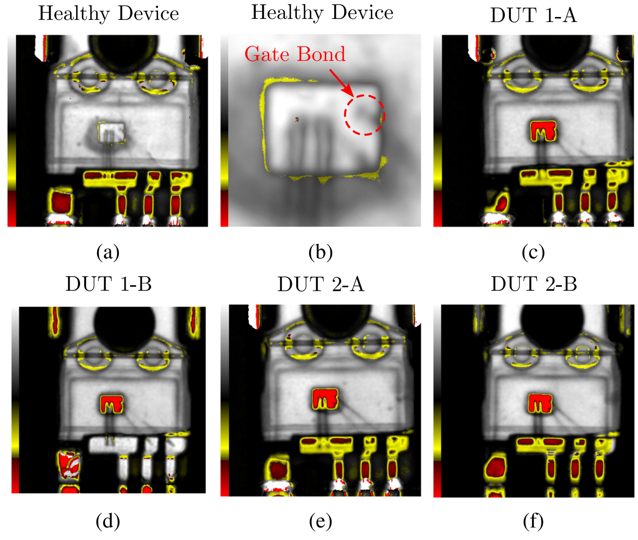


Fig. 9. C-SAM images of (a) healthy device, (b) close-up of healthy device die, (c) DUT 1-A, (d) DUT 1-B, (e) DUT 2-A, and (f) DUT 2-B.

III. Detailed Failure Analysis

A. Nondestructive C-SAM Analysis

After on-board characterization, nondestructive failure analysis is performed on the failed DUTs using confocal scanning acoustic microscopy (C-SAM) to verify the occurrence of gate-open failure mechanism in the failed devices. Fig. 9 shows C-SAM images of a healthy device. The red and yellow areas inside the package represent delamination sites. It is seen that there is almost no delamination in a healthy device package. Gate bond pad area is indicated in Fig. 9(b), which does not show any delamination either. However, the C-SAM images of all the failed DUTs show delamination over the entire die area as seen in Fig. 9(c)–(f). The delamination sites indicate that the mold compound above the die has moved relative to the die. The relative motion between the die and mold compound can exert shear forces on the gate bond-wire causing it to lift-off. This also provides possible explanation for intermittency of the failure. During dc power cycling, as the device heats up and cools down, the mold compound expands and contracts relative to the die, thereby moving the gate bond-wire. Therefore, during these intervals, the gate bond-wire can temporarily have instances of sufficient contact with the gate bond-pad on the die, causing the device to function normally.

B. Optical Microscopy

The failed DUTs were carefully decapsulated to verify the gate-open failure hypothesis. Fig. 10(a) and (b) shows the images of the DUTs 1-B and 2-B obtained using an optical microscope. The devices were inspected under $1000x$ magnification. As indicated on the top-right corner of each image, the gate-bond wires clearly show clean liftoff from the gate bond-pad. The power source and kelvin source connections, on the other hand, appear normal. This conclusively proves gate-open failure in these devices.

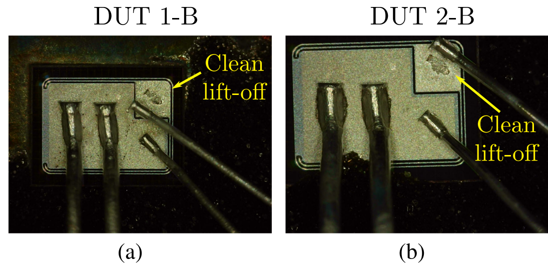


Fig. 10. Optical microscopy images of (a) DUT 1-B and (b) DUT 2-B.

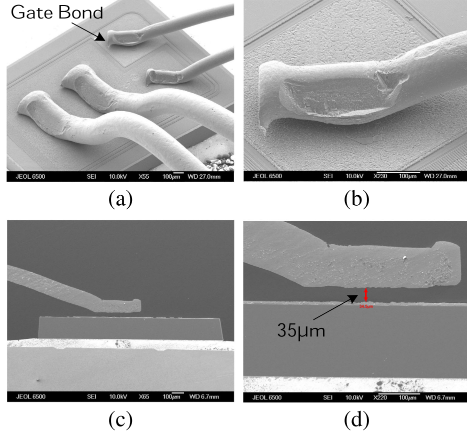


Fig. 11. (a) SEM image of decapsulated DUT die showing gate bond pad. (b) Close up image of gate bond pad showing gate bond liftoff. (c) Cross-sectional SEM of gate bond clearly showing a clean lift-off. (d) Close up of gate bond showing a 35 μm liftoff height.

C. Cross-Sectioning and SEM Analysis

To further investigate gate-open failure, DUT 1-A was carefully decapsulated and inspected using scanning electron microscopy (SEM). Fig. 11(a) shows the SEM image of the exposed DUT die. The close-up image of the gate bond site is shown in Fig. 11(b). It is clearly seen that the gate bond-wire is slightly lifted off the gate bond pad. Furthermore, the device is carefully encapsulated using a low viscosity epoxy resin. This prevents the movement of gate bond wire due to the flow of the resin during encapsulation. Thereafter, the encapsulated device is smoothly ground parallel to the gate bond wire plane. Further SEM inspection of the device clearly indicates a clean lift-off of the gate bond-wire as shown in Fig. 11(c). The close-up of the gate bond in Fig. 11(d) shows that the bond-wire is lifted-off by ~ 35 μm. It must be noted that before investigation, the DUT showed drain–source open failure without any recovery to normal operation. Fig. 12 shows a highly magnified SEM image of the gate site. The gate bond weld area is indicated in the figure. From the roughness observed on the gate-bond pad under the weld area, it can be deduced that the separation occurs in the bulk of the gate bond-wire. This type of lift-off is typically caused by interfacial shear stress in the gate-bond [24].

D. FEA Analysis of Gate-Bond Failure Mechanism

In order to explain the potential mechanism for gate bond-wire liftoff in SiC MOSFETs observed during dc power cycling, a

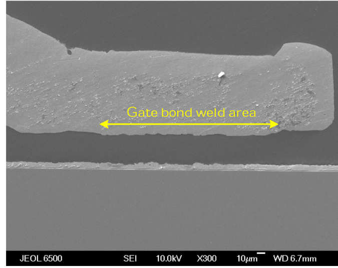


Fig. 12. Highly magnified cross-sectional SEM image of gate bond.

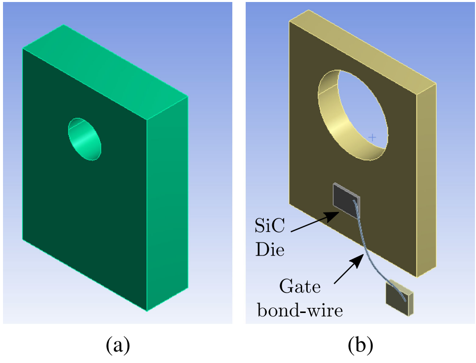


Fig. 13. Device model for FEA analysis (a) entire model (b) with EMC hidden

thermo-mechanical FEA analysis is performed in ANSYS, the results of which are discussed here. First, a high fidelity model of the DUT is developed as shown in Fig. 13(a) and (b). The external dimensions are obtained from manufacturer datasheet. Gate bond-wire diameter and aspect ratio is obtained by combining information from C-SAM images, optical microscopy of decapsulated, cross sectioned devices, and SEM images. To simplify the analysis, only internal gate lead and gate-bond wire are modeled. The source, drain leads and source bond-wires are ignored as they do not have significant thermal or mechanical implications on gate-bond itself. Furthermore, generally known properties for materials, such as copper, aluminium, and SiC, are chosen. This gives fairly accurate results since properties of these materials do not vary widely for the given application. The material properties of EMC, however, are proprietary knowledge and may vary between manufacturers. Therefore, for each property a representative value from known range of values for EMC used in power semiconductor applications is chosen [17], [18]. The chosen material properties are listed in Table III.

In the first step, a transient thermal simulation is performed to obtain device's temperature data at the end of the heating interval. For this, the SiC die is configured as an internal heat source, the value of which is set as the calculated DUT power loss during dc power cycling test. Since the DUT is only cooled by natural air convection cooling, a convection coefficient is set for the entire external surface of the device. The simulation is run for 50 s and results obtained are shown in Fig. 14(a) and (b). It is seen that the maximum temperature of 152.16 °C is in close agreement with experimental setting of 150 °C.

The temperature data obtained from transient thermal simulation are used to perform static structural analysis. For structural analysis, two adjacent corners at the bottom of the device are translationally constrained in all three directions. However, the rotational axes are free to allow warping and deformation. This is similar to the condition when device leads are soldered to the PCB. The physical deformation in the device due to heating is shown in Fig. 15(a) and (b). The deformation factor is exaggerated to clearly show warping of the package. The resulting shear stress on the gate wire-bond is seen in Fig. 16(a). It is seen that the bond-wire experiences shear stress at the gate bond interface. This is consistent with bond-wire liftoff mechanism as observed in the analysis of failed devices [25]. In Fig. 16(b), the resulting interfacial shear strain is shown. The strain is relatively high in the bond wire since aluminium, which is the bond-wire material, has a much lower elastic modulus than SiC, which is relatively hard. This can result in fatigue occurring in the bulk of the bond wire which is consistent with the observation in Fig. 12. The effect of EMC's properties on the shear stress in the gate bond is studied by varying the EMC's CTE as shown in Fig. 16(c) and (d). The probed maximum shear stress for EMC $CTE_{EMC} = 10$ ppm/°C is 134.12 MPa, whereas it is 139.46 MPa for the case when $CTE_{EMC} = 5$ ppm/°C. Since the deformation mainly occurs due to CTE mismatch between EMC and the copper drain tab whose $CTE_{Cu} = 18$ ppm/°C, the larger CTE mismatch in the case when $CTE_{EMC} = 5$ ppm/°C causes greater deformation and thus causes greater shear stress in the gate-bond interface. This also shows that the shear stress in the gate bond interface is a function of the EMC property. This is crucial because of two complementary reasons. First,

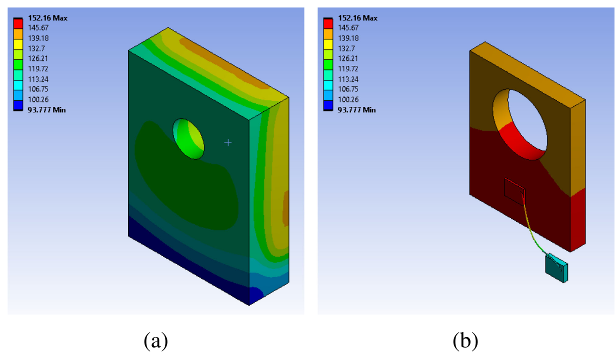


Fig. 14. Temperature distribution across device from transient thermal simulation for (a) entire device (b) with EMC hidden.

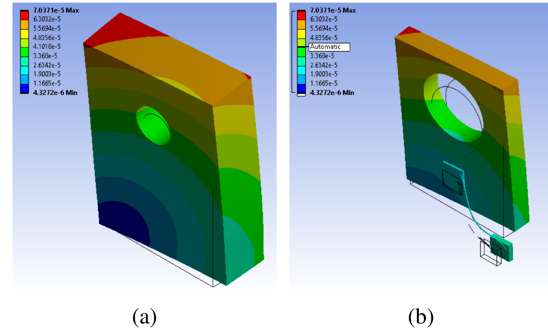


Fig. 15. Device deformation under heating for (a) entire device (b) with EMC hidden. Wireframe represents undeformed device.

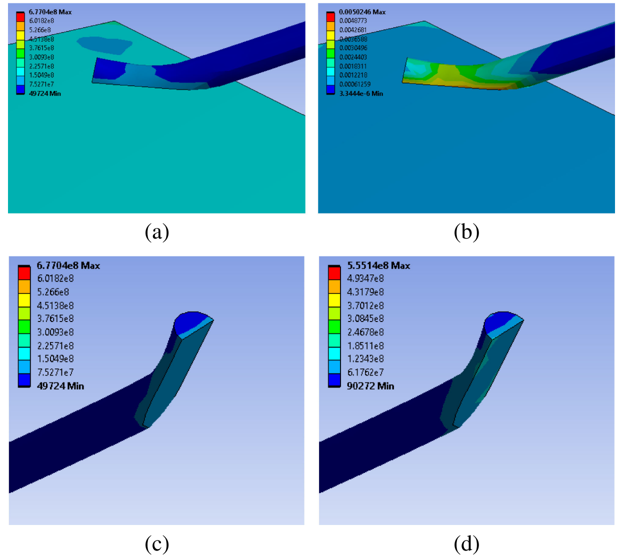


Fig. 16. (a) Maximum shear stress and (b) maximum elastic shear strain at the gate bond site with EMC and drain-tab hidden for $\mathrm{CTE_{EMC}} = 10$ ppm/°C. (c) Maximum shear stress at gate-bond wire for $\mathrm{CTE_{EMC}} = 10$ ppm/°C. (d) Maximum shear stress at gate-bond wire for $\mathrm{CTE_{EMC}} = 5$ ppm/°C.

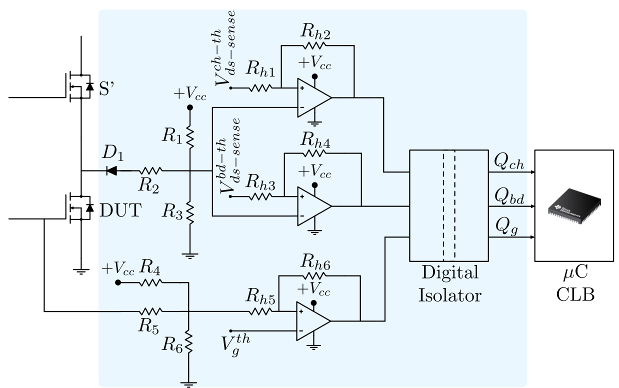


Fig. 17. Schematic diagram of the proposed gate failure detection circuit.

due to the relatively smaller size of SiC die, the gate-bond wire itself is thinnner compared to traditional Si devices. This reduces the overall gate bond strength and critical shear stress becomes lower. Second, due to the relatively higher operating temperatures of SiC devices, the thermo-mechanical properties of EMC used for SiC devices are different [15], [18]. Therefore, it is crucial to consider the effect of EMC's properties on device warping and thus the possibility of gate wire-bond liftoff.

IV. On-Board Detection of Gate-Open Failure

A. Proposed On-Board Detection Circuit

1) Detection Circuit: Fig. 17 shows the schematic of the proposed gate-open failure detection circuit. The DUT is represented by the low-side MOSFET and S' is the complementary high-side switch. The detection circuit comprises of two resistor sensing networks. The first network consisting of resistors R_1, R_2, R_3, and D_1 is used to measure the drain–source voltage across the DUT ($V_{ds-\mathrm{DUT}}$). $D1$ blocks the high OFF-state voltage across the device. By choosing appropriate values of R_1, R_2, R_3, it can be ensured that the output of the $V_{ds-\mathrm{DUT}}$ sensing network ($V_{ds-\mathrm{sense}}$) is always positive for both positive and negative values of $V_{ds-\mathrm{DUT}}$. This allows the comparators to be operated with single-ended supply derived from the gate-driver's supply voltage thus making the design simpler. R_4, R_5 and R_6 form the second network that is used to sense the DUT's gate voltage ($V_{g-\mathrm{DUT}}$). In this case as well, the appropriate choice of resistor values ensures that the sensed gate voltage ($V_{gs-\mathrm{sense}}$) is positive even for bipolar gate operation as is common in high-power SiC applications. The relation between $V_{ds-\mathrm{DUT}}$, $V_{gs-\mathrm{DUT}}$ and $V_{ds-\mathrm{sense}}$, $V_{gs-\mathrm{sense}}$ is given by (12),(13), and (14), respectively. The output of the $V_{ds-\mathrm{DUT}}$ sensing network is connected to the inverting inputs of comparators U_{ch} and U_{bd}. The noninverting inputs of the comparators are fixed threshold values $V_{ds-\mathrm{sense}}^{ch-th}$ and $V_{ds-\mathrm{sense}}^{bd-th}$, respectively. A third comparator, U_g is used to detect the state of applied gate voltage. The inverting and noninverting inputs of this comparator are connected to V_{gs}^{th} and $V_{gs-\mathrm{sense}}$, respectively. The outputs of all the comparators are passed to the MCU through a digital isolator. The digital isolator ensures galvanic isolation between power and logic side grounds. Also since the proposed circuit relies on gate drive power supply, it can be used with both high-side and low-side switch configurations

$$V_{ds-\mathrm{sense}} = \tag{12}$$

$$\begin{cases} \frac{V_{cc}R_3}{R_1+R_3} \\ \text{if } V_{ds-\mathrm{DUT}} \leq \frac{V_{cc}R_3}{R_1+R_3} + V_{D1} \\ \\ \frac{R_2R_3V_{cc}+R_1R_3(V_{D1}+V_{ds-\mathrm{DUT}})}{R_1R_2+R_2R_3+R_3R_1} \\ \text{if } V_{ds-\mathrm{DUT}} > \frac{V_{cc}R_3}{R_1+R_3} + V_{D1} \end{cases} \tag{13}$$

$$V_{gs-\mathrm{sense}} = \frac{V_{cc} + V_{gs-\mathrm{DUT}}}{(R_1+R_2)(R_1||R_2||R_3)}. \tag{14}$$

2) Principle of Operation: The objective of using the detection circuit is to accurately identify the DUT's state of operation. More specifically, the detection circuit identifies the conduction state of the DUT's channel and the state of the applied gate voltage by sensing $V_{ds-\mathrm{DUT}}$ and $V_{gs-\mathrm{DUT}}$, respectively. To illustrate the operation of the proposed detection circuit, a commercial SiC MOSFET is considered as the DUT [22]. The output $V-I$ curve of the device for $V_{gs} = 15$ V and $V_{gs} = -4$ V at junction temperature, $T_j = 55$ °C is plotted in Fig. 18. The plots are obtained by using the manufacturer provided SPICE model. As shown, for an application with a maximum instantaneous current $I_{\max}^{+} = 15$ A, the device's $V_{ds} = 1.81$ V. Due to MOSFET's symmetrical structure, the DUT's channel conducts for Q3 operation as well. Consequently, for $I_{\max}^{-} = -15$ A and $V_{ds} = -1.81$ V. Therefore, for the given application when $-1.81\ \mathrm{V} \leq V_{ds} \leq 1.81$ V, it can be safely concluded that the device's channel is conducting. Choosing $V_{ds}^{ch-th} = 2.5$ V ensures that when the device channel is conducting, the output of comparator U_{ch} is high and thus $Q_{ch} = 1$. However, in this case, $Q_{ch} = 1$ even when $V_{ds} < -1.81$ V. This is possible when the device channel is OFF and the body-diode conducts during Q3 operation. Therefore, additional information is required to determine the state of the device channel during Q3 operation. For this reason, a second

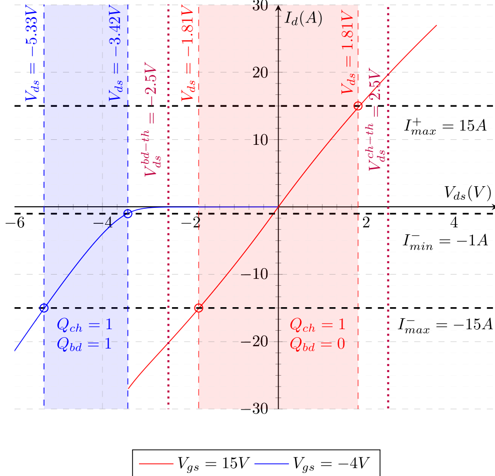


Fig. 18. Device operating points on the output curve to analyze choice of detection circuit threshold parameters.

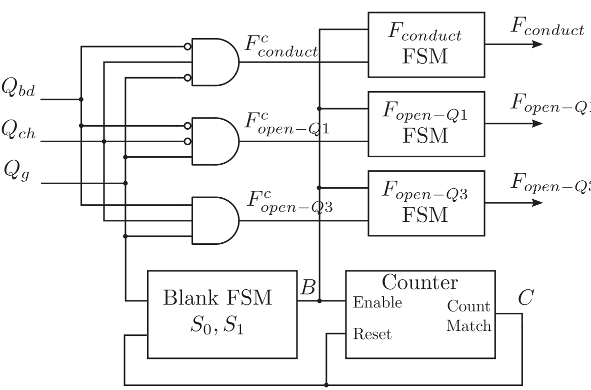


Fig. 19. Overall schematic diagram of CLB based fault detection logic.

TABLE IV
FAULT IDENTIFICATION TABLE

Q_{ch}	Q_{bd}	Q_g	Device state-of-health	Combinational fault logic
0	0	0	No conduction	
0	0	1	Open fault ($F^c_{open-Q1}$)	$\overline{Q_{ch}Q_{bd}}Q_g$
0	1	0	Invalid	
0	1	1	Invalid	
1	0	0	Q1 conduction fault ($F^c_{conduct}$)	$Q_{ch}\overline{Q_{bd}Q_g}$
1	0	1	Q1/Q3 channel conduction	
1	1	0	Q3 Body-diode conduction	
1	1	1	Q3 Open fault ($F^c_{open-Q3}$)	$Q_{ch}Q_{bd}Q_g$

comparator U_{bd} is used. As seen from Fig. 18, for the given application, the body-diode forward voltage drop varies between -3.42 V to -5.33 V depending on the instantaneous current value. Therefore, if $V_{ds}^{bd-th} = -2.5$ V, the output of U_{bd} and thus Q_{bd} gives the state of body-diode conduction. In summary, the digital outputs Q_{ch} and Q_{bd} provide complete information about the state of the device channel and body-diode. Furthermore, the output of comparator U_g corresponds to the applied gate voltage. $Q_g = 1$ when V_g is high and vice-versa. To ensure accurate fault detection, the thresholds must be carefully chosen depending on device's operating points in Q1 and Q3 for the particular application.

B. Failure Detection Logic

The outputs of the previously discussed detection circuit are connected to a microcontroller (MCU) for processing. The MCU used in this study is a Texas Instruments TMS320F280041 C with a configurable logic block (CLB). A CLB is an MCU peripheral that is functionally similar to an FPGA or CPLD [26]. Therefore, using CLB allows hardware level logic signal processing instead of software like in a typical MCU. This makes failure detection independent of the main control algorithm and eliminates any related overhead while allowing the failure detection logic to internally and quickly trip PWM outputs. The failure detection logic is implemented using combinational look up table (LUT) elements and finite state machines (FSMs). The details of the implementation are discussed further.

Fig. 19 shows the high-level schematic of the proposed fault detection logic. The fundamental idea of the failure detection logic is to check for inconsistency between the DUT's gate and channel operation. As previously discussed, gate-open failure leads to a loss of control over device's conduction state. Therefore, tracking the device state during a gate transition event can allow detection of a gate-open failure. For the proposed detection circuit, the state-of-health of the DUT corresponding to different combinations of the comparator outputs Q_{ch}, Q_{bd} and Q_g is shown in Table IV. Combinational fault signals (F^c_{conduct}, $F^c_{\text{open}-Q1}$ and $F^c_{\text{open}-Q3}$) corresponding to each type of fault can be obtained using logic gates. However, merely using combinational signals for detecting gate-open failure may lead to false positives. Delays associated with device switching and signal propagation during transition events may appear as momentary inconsistency in device operation. Therefore, it is important to differentiate between true failures and false positives while minimizing the fault detection time. For this reason, a blanking logic is implemented using a four-state FSM and a counter. The state transition diagram for the blanking FSM is shown in Fig. 20(a). When the gate input, Q_g, changes, the blanking FSM transitions to a blank state and sets the corresponding output B high. This event also starts a counter that counts to a preset blanking value. Upon reaching the preset value, a match ouput (C) is set high by the counter. C then transitions the blankingFSM out of blank state i.e., B becomes low and also resets the counter. By adjusting the count value, blanking window can be modified as per application requirement. The blanking FSM automatically provides input hysteresis within the blanking time window thus making the logic immune to noise related transition events. In addition to the blanking FSM, four-state FSMs are also used

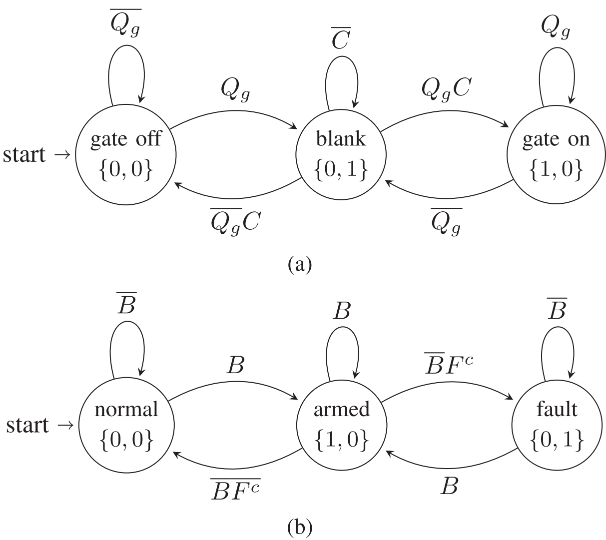


Fig. 20. State-transition diagrams for (a) blanking FSM and (b) fault FSM.

for each of the fault outputs. Every fault FSM has two inputs- the corresponding combinational fault signal (F_x^c) and the blank signal B. A transition on B "arms" the fault FSM. At the end of the blanking window, when B goes low, the the fault FSM either transitions to a normal state or a fault state depending on the value of the corresponding F_x^c. The fault output remains latched until the next gate transition event. This logic enables cycle-by-cycle fault detection and provides reset capability. The state equations for blanking FSM and fault FSM are given in (23)–(25) and (26)–(28), respectively.

$$S_{0-\text{next}} = \overline{S_0}S_1Q_gQ_c + S_0\overline{S_1}Q_g \tag{15}$$

$$S_{1-\text{next}} = \overline{S_0}\,\overline{S_1}Q_g + \overline{S_0}S_1\overline{Q_c} + S_0\overline{S_1Q_g} \tag{16}$$

$$B = S_1 \tag{17}$$

$$S_{0-\text{next}} = (\overline{S_0} + \overline{S_1})B \tag{18}$$

$$S_{1-\text{next}} = (\overline{S_0}S_1 + S_0\overline{S_1F^c})\overline{B} \tag{19}$$

$$F_{\text{out}} = S_1. \tag{20}$$

V. Experimental Verification

In this section, the functioning of proposed gate-open failure detection technique is experimentally verified for all the possible failure scenarios. The highly intermittent and unpredictable nature of gate-open failures makes it nearly impossible to recreate these faults on-demand. This is especially important since, as previously discussed in Section II, the exact instance of fault occurrence determines the state of the failed MOSFET's gate and consequently its behavior under fault. Therefore, in order to comprehensively validate the functioning of the proposed detection technique under different failure scenarios, a gate-open fault emulation technique is used. The schematic of the experimental gate-open failure detection circuit is shown in Fig. 21(a). The DUT is plugged into this detection circuit and the board itself has external connections compatible with a TO-247 PCB footprint. The external drain and source connections are routed directly

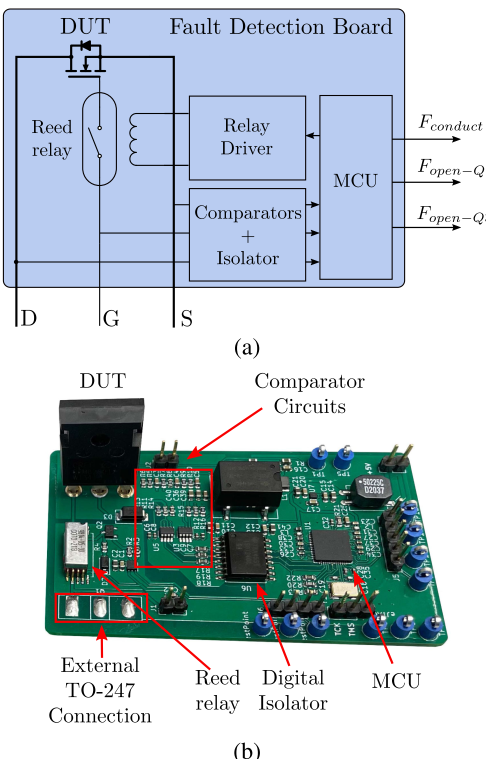


Fig. 21. (a) Schematic and (b) actual prototype of the proposed gate-open failure detection circuit board.

to the respective DUT leads. The gate connection, however, passes through an ultrafast reed relay. Under normal operation, the relay is closed and the DUT behaves normally. To emulate a gate-open fault, the relay is opened, which mimics the physical disconnection of the gate bond-wire under actual failure. The picture of the developed prototype board is shown in Fig. 21(b). The gate voltage applied by the gate driver is sensed for failure detection purpose. The previously discussed failure detection logic is implemented on the on-board MCU, which generates the fault signals. In actual applications, the logic can be implemented directly on the main control MCU. The proposed detection technique is experimentally verified under all failure scenarios using a synchronous boost topology. In the following sections, the gate-open failure emulation strategy is first verified followed by verification of the proposed detection technique.

A. Characterization and Verification of Gate-Open Failure Emulation Technique

In order to reliably emulate gate-open failure during converter operation, it necessary to precisely time the opening of the reed relay with respect to the applied gate signals. To this end, the relay release time is experimentally characterized, the results of which are shown in Table V. Based on the values in the table, the worst case relay opening time can be approximated to <10 μs. Consequently, for 10 kHz converter operating frequency and D = 0.5, the relay should operate within half of the switching period (=50 μs). This is verified in actual converter operation as shown in Fig. 22. The relay is commanded to open soon

TABLE V
CHARACTERIZATION OF RELAY RELEASE TIME

Gate Voltage	Release Time
5V	$4.68\mu s$
8V	$5.24\mu s$
12V	$5.76\mu s$

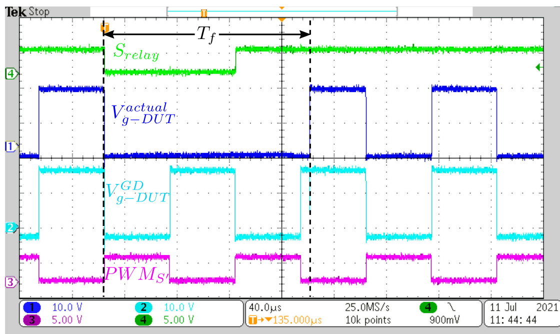


Fig. 22. Verification of fault emulation technique.

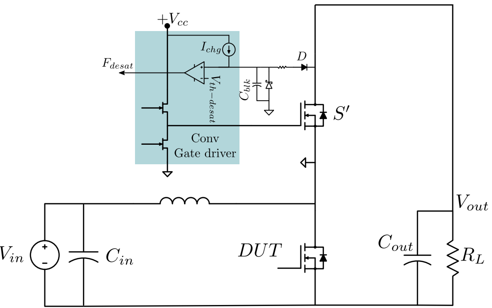


Fig. 23. Synchronous boost converter used for experimental validation of the proposed gate-open failure detection technique.

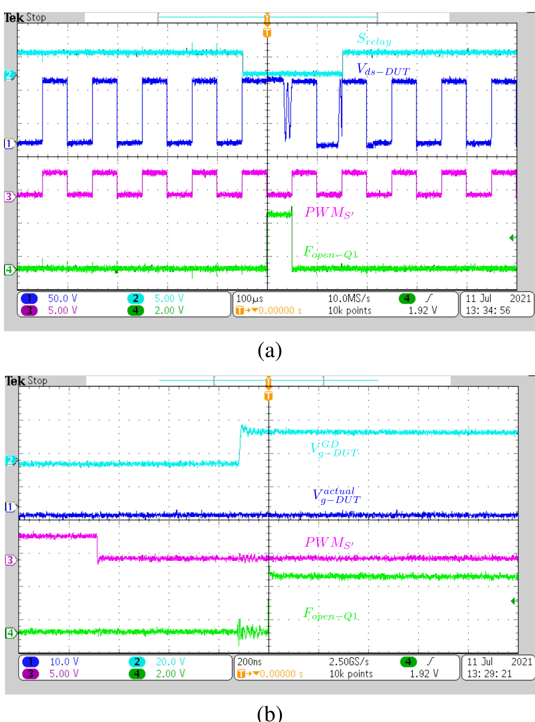


Fig. 24. Experimental verification of (a) $Q1$ open fault detection and (b) fault detection timing.

after the DUT turns OFF, as indicated by the falling edge of the relay drive signal (S_{relay}). In the subsequent on interval, although the gate driver voltage ($V_{g-\text{DUT}}^{GD}$) is high, the actual DUT gate voltage ($V_{g-\text{DUT}}^{\text{actual}}$) remains low. This floating gate behavior is consistent with a gate-open fault. Similarly, if the relay is open when $V_{g-\text{DUT}}^{\text{actual}}$ is high, it will remain high even when $V_{g-\text{DUT}}^{\text{GD}}$ is low. It must be noted that for these experiments, the relay is reconnected after 1–2 switching intervals to allow normal converter operation. The theoretical fault interval is given by T_f, at the end of which the relay closes (including contact bounce) and $V_{g-\text{DUT}}^{\text{actual}}$ starts following $V_{g-\text{DUT}}^{\text{GD}}$.

B. Verification of Failure Detection Under Q1 Operation

The synchronous boost configuration used to verify failure detection under Q1 operation of the DUT is shown in Fig. 23. The specifications of the boost converter are as follows- $V_{\text{in}} = 50$ V, $V_{\text{out}} = 100$ V, $f_{\text{sw}} = 10$ kHz, $D = 0.5$, $C_{\text{in}} = 50\ \mu$F, $C_{\text{out}} = 1800\ \mu$F, and $R_L = 180\ \Omega$. For Q1 operation, the DUT is configured as the low side switch and S' is the complementary high-side switch. Under Q1 operation of the DUT, an open or conduction type gate-open failure may occur as discussed in Section II. Each of these scenarios is verified as follows.

1) Q1 Open Fault: Fig. 24(a) shows the waveform for verification of Q1 open fault detection. The gate relay is opened when S_{relay} goes low. In the subsequent on period, the DUT fails to turn ON. Consequently, even though the complementary synchronous switch is OFF (PWM$_{S'}$), its body-diode is forward biased and the drain–source voltage across the DUT ($V_{ds-\text{DUT}}$) remains at 100 V as shown in the figure. Therefore, Q1 open fault ($F_{\text{open}-Q1}$) is raised during the DUT's ON interval. The timing of the fault signal is verified in Fig. 24(b). As seen, the delay between rising edges of $V_{g-\text{DUT}}^{\text{GD}}$ and $F_{\text{open}-Q1}$ is 120 ns. This delay includes the delay caused by comparators, digital isolator, and blanking interval.

2) Q1 Conduction Fault: Fig. 25(a) shows the experimental waveforms in case of a conduction fault. In this case, the gate relay is opened when $V_{g-\text{GD}}$ is high to emulate an on period gate-open fault. As seen, the DUT fails to turn off when $V_{g-\text{GD}}$ goes low. In the figure, this condition is represented by V_{ds} remaining low when DUT should turn ON. The fault output ($F_{\text{cond}-Q1}$) is used as a trip signal for the PWM generator. Therefore, it seen that the gate signals of both the DUT and S' are low after the fault is raised. The timing of the fault signal is shown in Fig. 25(b). $F_{\text{cond}-Q1}$ goes high 150 ns after $V_{g-\text{GD}}$ goes low. This is lower than the deadtime between the high side and low side switching signals which, for this experiment, is set at a fixed value of 400 ns. Therefore, the gate signal for S' remains low because of PWM trip action. Consequently, fast fault detection prevents a shoot-through event in case of conduction type gate-open failure scenario.

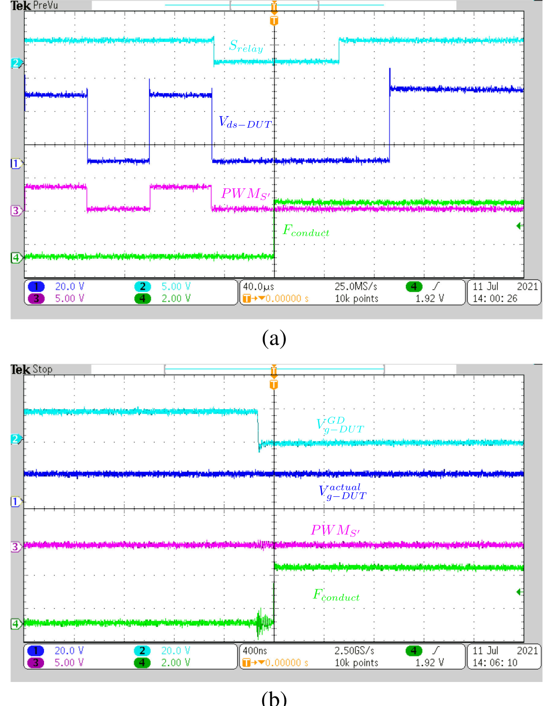


Fig. 25. Experimental verification of (a) conduction fault detection and (b) conduction fault detection timing.

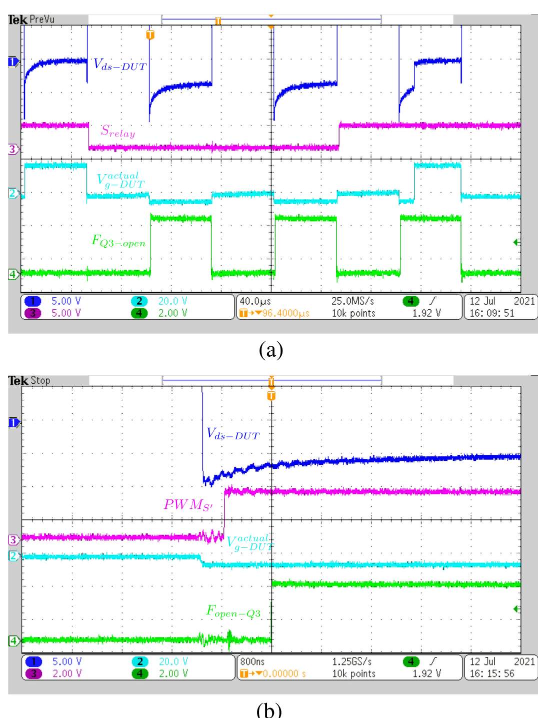


Fig. 26. Experimental verification of (a) $Q3$ open fault detection and (b) fault detection timing.

C. Verification of Failure Detection Under Q3 (Synchronous) Operation

For experimental verification of failure detection in Q3 mode of operation, the position of S' and DUT in Fig. 23 is interchanged. Specifically, the DUT operated as the synchronous switch. The experimental waveforms for verification of proposed gate-open failure detection technique in Q3 open type fault scenario in shown in Fig. 26(a). As seen when the relay is opened, $V_{g-\text{DUT}}^{\text{actual}}$ remains low even during the on intervals. Moreover, as discussed in Section II, $V_{g-\text{DUT}}^{\text{actual}}$ becomes more negative when the diode turns ON, which is indicated by large negative $V^{ds-\text{DUT}}$. For these intervals, it is seen that $F_{\text{open}-Q3}$ is high. The timing of the fault signal is verified in Fig. 26(b). Unlike the previous cases, it seen that $F_{\text{open}-Q3}$ is asserted 800 ns after $\text{PWM}_{S'}$ rising edge. It is because, for Q3 open faults, the blanking time necessarily has to be greater than switching dead-time. Since the body-diode is on during the dead-time, using a blanking value less than that would trigger a false positive. Moreover, since this a safe failure mode, the delay in failure detection is not a significant factor as long as the fault is detected within the off period.

D. Comparison of Proposed Technique to Traditional DESAT Protection Scheme

DESAT protection schemes are traditionally used to protect the switching device against high-current events that may occur during faults. Many modern commercial gate drivers have built-in DESAT protection feature. A typical DESAT protection circuit is shown across S' in Fig. 23. In case of a fault, when $V_{ds}^{S'}$ exceeds $V_{cc} + V_D$, the current source starts charging the

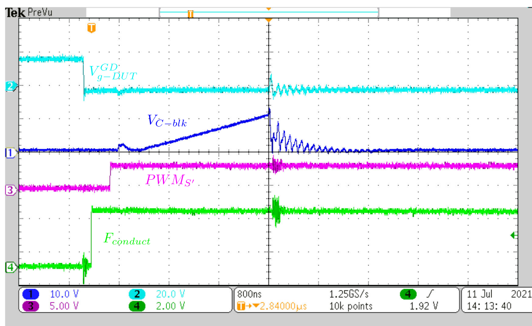


Fig. 27. Comparison of proposed fault detection circuit with conventional DESAT protection scheme.

blanking capacitor C_{blk}. When voltage across the blanking capacitor exceeds the desat threshold ($V_{th-\text{desat}}$), the switch is turned OFF and a fault signal is raised. Conventional DESAT protection scheme is compared to the proposed gate-open failure detection technique for different gate-open failure scenarios as described below.

1) Q1 Open Fault: In this case, if present, DESAT protection of the faulty switch is triggered since the switch is in blocking state and I_{chg} charges C_{blk}. However, the conventional DESAT scheme will not able to differentiate between an open fault caused by gate-open failure and an over-current saturation fault. On the other hand, the proposed fault detection circuit is triggered only in case of a Q1 open fault caused by gate-open failure. As described above, the proposed gate-open failure detection circuit is not active throughout the ON/OFF interval and only makes a single shot detection at the end of blanking period which

in this case is 60 ns. Since most switches are unlikely to saturate within this time, saturation fault in most cases will not trigger $F_{\text{open}-Q1}$.

2) Q1 Conduction Fault: In case of a conduction type gate-open fault, the resulting shoot-through event may trigger the DESAT protection feature of the complementary switch's gate driver, which could theoretically protect against a conduction gate-open fault. Fig. 27 shows the comparison between proposed fault detection technique and DESAT scheme. The setup is similar to Fig. 23. However, F_{conduct} does not trip the PWM outputs in this case. For the conventional gate driver used, $C_{\text{blk}} = 60$ pF, $I_{\text{chg}} = 0.5$ mA and $V_{th-\text{desat}} = 9$ V. It is seen that it takes 2.5 μs from $\text{PWM}_{S'}$ rising edge to DESAT fault getting triggered. As shown above, with the proposed technique, F_{conduct} is asserted in 150 ns and since this is less than the dead-time, PWM is tripped and shoot-through is prevented. In the case of DESAT based protection, however, a shoot-through current is necessary to saturate the switches and trigger the fault. This is especially important since SiC MOSFETs unlike Si IGBTs have lower short-circuit withstand capability due to their relatively smaller die size [27]. Moreover, SiC MOSFETs do not have a well-defined knee point on the output curve and have high power dissipation in saturation [28]. In addition, the shoot-through event may cause thermal runway in not only the power switches, but also to other system components as well. Furthermore, DESAT scheme cannot different between saturation event caused by gate-open fault or a different fault mechanism. Because of these reasons, the proposed gate-open failure detection has advantages over traditional protection schemes in detecting conduction type fault.

3) Q3 Open Fault: Conventional DESAT scheme cannot detect this fault type since it is deactivated during the switch off time. Moreover, since this is a soft-failure where the converter may seem to be healthy apart from deteriorated efficiency, it is very challenging for most conventional protection mechanism to detect open failure in Q3 operation. Therefore, the proposed failure detection circuit can reliably detect Q3 open type failures. This is especially useful since the intermittent nature of gate-open failure may cause the device to recover from Q3 open failure and later show conduction type failure.

VI. Conclusion

In this article, intermittent gate-open failure is investigated in the context of discrete SiC devices. The electrical behavior of MOSFET under gate-open failure is first analyzed. Failed devices from dc power cycling test are inspected analyzed using a systematic multistep process. Given the intermittent and elusive nature of gate-open failure, the methods used in this article maybe be used as a guide for gate-open failure analysis. FEA analysis is used to identify potential mechanism for gate-open failure. While the gate-bond itself does not carry a large current, it is shown that it experiences interfacial shear stress due to deformation caused by CTE mismatch between various device elements. A larger CTE mismatch between EMC and copper drain tab is shown to increase the maximum shear stress. Thereafter, an on-board failure detection technique is proposed for all types of gate-open failure modes. The specific nature of gate-open failure is exploited to create a fast failure detection technique that is inherently selective and robust. Through comparison and experimental verification, it shown that the proposed technique is not only capable of detecting all gate-open failure modes but also differentiate between gate-open failure and other failure modes. Specifically, potentially dangerous conduction type failure mode is detected within the switching dead-time, thus preventing a shoot-through event in switching leg.

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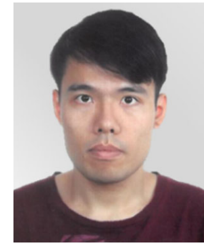

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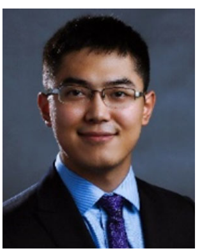

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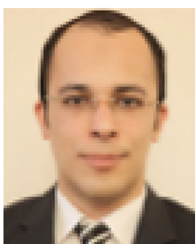

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