Differential Input Current Regulation in Parallel Output Connected Battery Power Modules

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***Abstract*—Parallel output connected converters have been widely investigated with a focus on equal current and power sharing. However, parallel output connected battery power modules (BPMs) require unequal currents to enable state-of-charge (SOC) control in active battery management systems (BMS.) This article presents simple differential input current regulation for SOC control. Compared with equal current sharing, differential current regulation is more critical on the system stability due to the cross-coupling between the paralleled BPMs. The article proposes design guidelines that enable differential current control while considering the cross-coupling between the paralleled BPMs. The small-signal model of a battery brick consisting of *N* parallel output connected BPMs that operate in boost mode is presented. This article shows the effect of paralleling and differential currents on the individual input current regulation loops. Simulations and experiments verify the analysis. Experimental validation using a 300-W prototype consisting of three parallel output connected battery modules in an active BMS is presented.**

***Index Terms*—Active balancing, battery management systems (BMSs), battery power modules (BPMs), current regulation, current sharing, differential current control, small-signal analysis, state-of-charge (SOC) control.**

I. Introduction

A TYPICAL high-voltage (HV) lithium-ion (Li-ion) battery pack consists of a number of parallel and series connected Li-ion cells. The battery management system (BMS) and cell balancing algorithms ensure that all cells are utilized within their safety limits by employing passive or active balancing circuits [1]–[6]. Individual cell current control is the backbone in cell balancing algorithms. For instance, the state-of-charge (SOC) of the jth cell, SOC_j is a function in the cell current

$$\text{SOC}_j(t) = \text{SOC}_{j,0} - \frac{1}{Q_j}\int_0^t i_{gj}(t)dt \tag{1}$$

where $\text{SOC}_{j,0}$ is the initial SOC of the cell at $t = 0$, i_{gj} is the cell current, and Q_j is the cell capacity. For different initial SOCs, the individual cell currents must be different such that $i_{g1} \neq i_{g2} \cdots \neq i_{gN}$ to achieve SOC balancing [7]–[11]. Moreover, state-of-health (SOH) control enables reconditioning the battery cells for second-life applications, where the balancing currents are substantially different to reduce the cell capacity imbalance in minimal time [12].

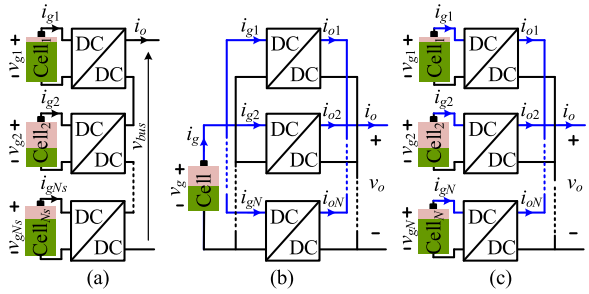

Fig. 1. Modular power architectures. (a) Modular battery with N_s series output connected BPMs. (b) Modular input-parallel output-parallel architecture. (c) Parallel output connected BPMs.

A battery power module (BPM) is a power converter connected across a battery cell and integrates the BMS functions into the converter module's operation [13]. BPMs simplify and improve SOC and SOH control because they enable individual cell-level control. As a result, series output connected BPMs have emerged to replace the central dc/dc converters in large battery packs, as shown in Fig. 1(a) [14]–[21]. The N_s series output connected BPMs have been studied with a focus on output voltage regulation in [17]–[21]. Output current regulation in N_s series output connected BPMs has been proposed in [16], which requires output current measurement in addition to the cell current sensing for the BMS algorithms.

Increasing a system's output current by paralleling modular converters, as demonstrated in Fig. 1(b), has been widely investigated [22]–[28]. However, to ensure reliability and modularity, the main focus has been on equal current sharing, i.e., $i_1 = i_2 \cdots = i_N = i_g/N$ [29]–[36]. On the other hand, Fig. 1(c) shows the parallel output connected BPMs, where the objective

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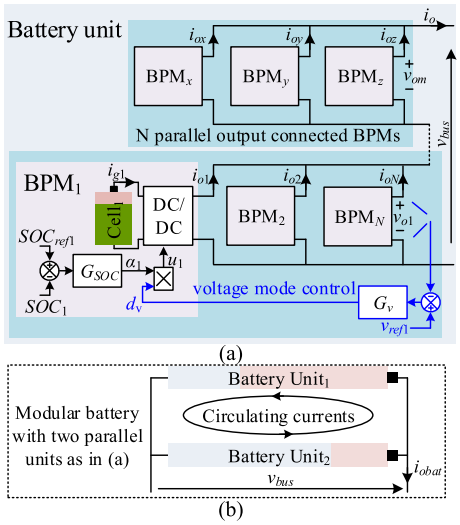

Fig. 2. Limitations of the conventional voltage regulation approach. (a) Battery unit consisting of parallel and series output connected BPMs in voltage mode. (b) Modular battery with two units in parallel.

is differential input current regulation, i.e., $i_{g1} \neq i_{g2} \cdots \neq i_{gN}$, enabling individual cell SOC and SOH control. If the N paralleled BPMs operate with equal input currents, tuning the input current compensator may seem a straightforward exercise at first glance. However, the control-to-input current transfer function of a single BPM varies significantly as all BPMs track different currents. However, the complexity in designing the current controller has rarely been addressed. Therefore, new control models and controller design guidelines that enable differential input current regulation in parallel output connected BPMs are needed, which are presented in this article.

In [13], parallel operation of BPMs has been presented by utilizing buck–boost converters focusing on steady-state operation to emphasize the SOC balancing capabilities. In [19], hierarchical SOC balancing between the battery cells in a multi-input single-output converter has been demonstrated. Fig. 2(a) depicts a simplified diagram for the conventional output voltage regulation approach, which is leveraged in [19]. The N parallel output connected modules share a single output voltage loop G_v that generates a common control command d_v. However, N SOC balancing compensators are utilized, where the jth SOC compensator output is α_j and the final control command for the jth BPM is $u_j = \alpha_j d_v$. The product $\alpha_j d_v$ is nonlinear, where setting the saturation limits for protection is cumbersome.

Employing the conventional output voltage regulation approach in BPMs results in a battery unit that appears as a voltage source [37], limiting the paralleling capability between the battery units due to the circulating currents, as shown in Fig. 2(b). Input current regulation in BPMs eliminates the system-level drawbacks of the typical voltage regulation approach [37]. However, [37] lacks controller design procedures that enable differential input current regulation for individual SOC and SOH control. The main contributions of this article include the following.

1) The article presents differential input current regulation in parallel output connected BPMs for SOC and SOH control, which is different from equal current sharing in multiple parallel output connected converter modules [22]–[36].
2) The article proposes controller design guidelines for differential input current regulation.

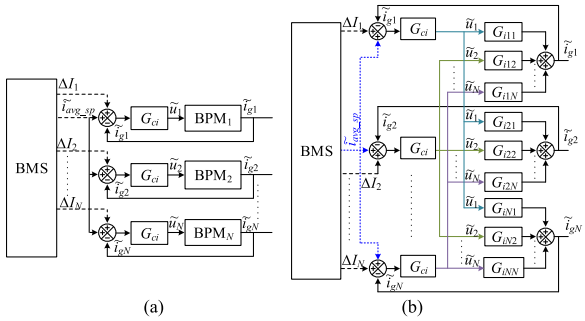

Fig. 3. Battery balancing approach. (a) Modular input current regulation approach. (b) Closed-loop model of the modular approach.

The remaining sections of this article are organized as follows. Section II explains the input current regulation strategy with N paralleled BPMs. Section III develops the generalized small-signal model for N parallel BPMs operating in boost mode by considering the cross-coupling. Section IV presents the controller design procedure for the critical scenarios in battery balancing applications. Section V verifies the analysis and controller design procedure in a switching model simulation. Section VI validates the approach on a 300-W battery brick consisting of three parallel output connected BPMs with four-switch buck–boost converters. Finally Section VII concludes this article.

II. Differential Input Current Control

Fig. 3(a) depicts the proposed differential input current regulation approach in paralleled BPMs. Each BPM utilizes a single current compensator G_{ci} to track the input current reference by adjusting the BPM's control command $\tilde{u}_j$. In Fig. 3(a), the BMS adjusts the individual input current references of all BPMs according to the balancing objectives. The jth BPM current reference consists of two components: 1) a common current reference in all BPMs $\tilde{i}_{\text{avg\_SP}}$ that is critical for system-level operation, and 2) the balancing current reference ΔI_j. The proposed approach is simple and preserves linearity as the balancing current ΔI_j is added to the common current reference $\tilde{i}_{\text{avg\_SP}}$ as the total input current reference for the jth BPM.

By paralleling N BPMs that are driven by individual control commands, the battery brick becomes a multi-input, multi-output (MIMO) system. Fig. 3(b) shows the closed-loop model of the N paralleled BPM considering only the control variables. For the jth BPM, there is a single direct control-to-input current $\frac{\tilde{i}_{gj}}{\tilde{u}_j}$ transfer function, and $N-1$ cross-coupling (indirect) transfer functions with respect to each BPM $\frac{\tilde{i}_{gj}}{\tilde{u}_i}$, which can be written in a matrix form

$$G_{\text{mat}} = \begin{bmatrix} G_{11} & G_{12} & \cdot\cdot & G_{1N} \\ G_{21} & G_{22} & \cdot\cdot & G_{2N} \\ \cdot\cdot & \cdot\cdot & \cdot\cdot & \cdot\cdot \\ G_{N1} & G_{N2} & \cdot\cdot & G_{NN} \end{bmatrix} \tag{2}$$

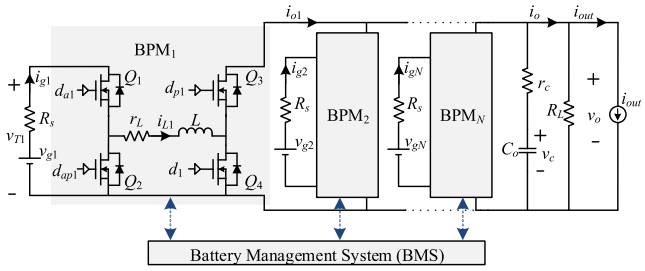

Fig. 4. N parallel output connected BPMs with four-switch buck–boost converters.

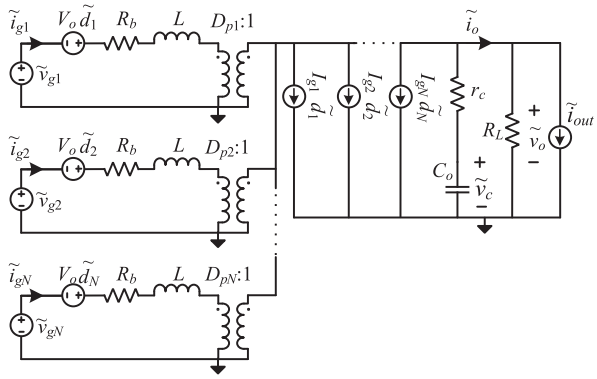

Fig. 5. Small-signal equivalent circuit model of the N parallel BPMs operating in boost mode.

where G_{mat} is of order N that varies with the number of BPMs in operation. The small-signal input current equation of the jth BPM is the superposition of the ith BPM control-to-input current G_{ji} transfer functions that depend on the operation modes of all BPMs

$$\tilde{i}_{gj} = \sum_{k=1}^{N} G_{jk}\tilde{u}_k \tag{3}$$

$$G_{\text{sharing}} = \left.\frac{\tilde{i}_{gj}}{\tilde{d}_j}\right|_{N=1} = \left. G_{jj}\right|_{N=1}. \tag{4}$$

Small-signal analysis by averaging the entire brick for equal current sharing between the N BPMs [28] will reduce the control-to-input current transfer function to a single BPM operation (4). However, the transient response of the input current loops will substantially change with differential currents and different control commands for balancing. It is critical to accommodate for the varying nature and balancing requirements with paralleled BPMs in the compensator G_{ci} design procedure. From the small-signal closed-loop model, shown in Fig. 3(b) and G_{mat} (2)

$$\underline{\tilde{i}_g} = G_{ci}G_{\text{mat}}\left[I + G_{ci}G_{\text{mat}}\right]^{-1}\underline{\tilde{i}}_{g,\text{ref}} \tag{5}$$

where $\underline{\tilde{i}}_{g,\text{ref}}$ is the current reference vector for the N BPMs, and I is the identity matrix. The system's transient behavior is governed by the denominator of the general solution in (5) that varies with the balancing strategy, where G_{mat} is critical for the compensator G_{ci} design procedure. In order to formulate the transfer matrix G_{mat}, a small-signal model for the paralleled BPMs is required, which is discussed in Section III.

III. Small-Signal Analysis of Paralleled Battery Power Modules

In this article, each BPM employs a four-switch buck–boost converter that operates in either buck or boost modes [38], [39]. Fig. 4 shows a battery brick consisting of N parallel output connected BPMs with four-switch buck–boost converters, where C_o is the lumped output capacitance of all modules with an effective series resistance r_c. The load across the brick is a parallel combination of a resistance R_L and a current source/load i_{out}, where v_o is the output voltage across the brick. By matching the sensing circuitry and board layout, tolerances within the modules can be minimized. The current sense resistance R_s and the effective series resistance r_L of the inductance L may be assumed identical for all converters. Moreover, the jth BPM is connected across a single battery whose terminal voltage is v_{gj}. Furthermore, the BPM is driven by two independent duty cycles for buck and boost modes that are denoted by d_{aj} and d_j, respectively. The complementary duty cycles for buck and boost modes are d_{apj} and d_{pj}, respectively.

The N paralleled BPMs operate in buck mode to provide soft-starting capabilities; however, in normal operation, the BPMs are in boost mode. In a well-designed system, the N BPMs operate simultaneously in the same mode. Furthermore, balancing is enabled when the converters operate in boost mode. Therefore, the control-to-input current transfer functions will be derived as the N BPMs operate in boost mode for clarity.

Fig. 5 shows the small-signal equivalent circuit model of the N paralleled BPMs in boost mode, where R_b is the series resistance in the input current path $R_b = R_s + r_L$. Fig. 5 is linearized around an equilibrium operating point of all modules at a steady-state output voltage V_o. The equilibrium operating point of the jth BPM is given by the complementary duty ratio D_{pj}, steady-state input current I_{gj}, and cell voltage V_{gj}. The jth BPM transfer functions are obtained by setting the independent sources for the ith BPMs in Fig. 5 to zero, such that $\tilde{v}_{gi} = 0$, and $\tilde{d}_i = 0$. Therefore, by solving the reduced circuit, the effective load as seen by the jth BPM is formulated in (8), which depends on the operating point of the N parallel connected BPMs. The direct control-to-input current transfer function $\frac{\tilde{i}_{gj}}{\tilde{d}_j}$ of the jth BPM is derived

$$Z_{\text{load}} = R_L \left\| \left(r_c + \frac{1}{sC_o}\right)\right. \tag{6}$$

$$\beta_1 = -D_{pj}^2 + \sum_{k=1}^{N} D_{pk}^2 \tag{7}$$

$$Z_{\text{oBooost},j} = \frac{R_b + sL}{D_{pj}^2} + \left[\left(\frac{R_b + sL}{\beta_1}\right) \left\| Z_{\text{load}}\right.\right] \tag{8}$$

$$G_{jj} = \frac{\tilde{i}_{gj}}{\tilde{d}_j} = \frac{1}{\left(1 + \frac{s}{\frac{R_b}{L}}\right)} \frac{a_0 + a_1 s + a_s s^2}{b_0 + b_1 s + b_2 s^2} \tag{9}$$

TABLE I
SWITCHING MODEL PARAMETERS

Parameter	Value
Current sense resistance R_s	1 mΩ
Inductor ESR r_L	1 mΩ
Inductance L	320 nH
Output capacitor per BPM C_o/N	120 μF
Capacitor ESR per BPM $r_c \cdot N$	1 mΩ
Cell terminal voltage range V_g	3.6 - 4 V
Battery cell capacity Q_g	25 Ah
BPM rated input current I_g	25 A (1C-rate)
Switching frequency f_s	200 kHz

where

$$b_2 = LC_o\left(r_c + R_L\right) \tag{10}$$

$$b_1 = C_o r_c\left(R_b + R_L\sum_{k=1}^{N} D_{pk}^2\right) + C_o R_L R_b + L \tag{11}$$

$$b_0 = R_b + R_L\sum_{k=1}^{N} D_{pk}^2 \tag{12}$$

$$a_2 = LC_o\left[V_o R_L + r_c\left(V_o + I_{gj}R_L D_{pj}\right)\right] \tag{13}$$

$$a_1 = \left(V_o + I_{gj}R_L D_{pj}\right)\cdot\left(L + C_o r_c R_b\right) + C_o R_L V_o\left(R_b + r_c\beta_1\right) \tag{14}$$

$$a_0 = R_b\left(V_o + I_{gj}R_L D_{pj}\right) + V_o R_L \beta_1. \tag{15}$$

Considering that the individual BPMs operate with different duty ratios for balancing, β in (7) dictates the system transient behavior, which is unique with differential current control. Similarly, the cross-coupling transfer function from the jth duty cycle to ith module input current G_{ij} is derived

$$G_{ij} = \frac{\tilde{i}_{gi}}{\tilde{d}_j} = \frac{1}{\left(1 + \frac{s}{\frac{R_b}{L}}\right)}\frac{\text{Num}_{\text{boos},ij}}{b_0 + b_1 s + b_2 s^2} \tag{16}$$

$$\text{Num}_{\text{boos},ij} = D_{pi}R_L\left(1 + C_o r_c s\right)\left(I_{gj}\left(R_b + Ls\right) - V_o D_{pj}\right) \tag{17}$$

where D_{pi} is the steady-state complementary duty ratio of the ith module.

A switching model simulation in MATLAB/PLECS verifies the small-signal analysis by measuring the control-to-input current transfer functions at different numbers of paralleled modules N. Table I summarizes the simulation parameters. The terminal voltages of the cells are evenly distributed between 3.6 and 4.0 V, as the brick supplies the rated resistive load. Fig. 6 shows that the simulated transfer functions match the analytically derived expressions in (9) and (16) at $N = 1$, 2, 3, and 15 parallel BPMs. At low frequencies, the magnitude of G_{jj} increases with N, as shown in Fig. 6(a).

With current sharing as the objective (4) or, equivalently, if the battery brick is formed by a single BPM, i.e., $N = 1$, $\beta_1 = 0$, the zeros of (9) are real, and a pole-zero cancelation occurs at $-R_b/L$. Consequently, (9) simplifies to the control-to-input current transfer function of a single BPM employing a boost converter supplying its rated resistive load $R_{L,\text{single}} = NR_L$. Moreover, in the general $N \neq 1$ case, the zeros of (9) are complex at a resonant frequency below the resonant frequency of the complex poles. Additionally, when $N \neq 1$ modules are connected in parallel, the pole at $-R_b/L$ in (9) introduces a phase delay in the system, as shown in Fig. 6(b). Therefore, designing the current loop compensator G_{ci} for a single BPM operation or equal current sharing, i.e., $N = 1$, could lead to instability with differential current control, i.e., $N \neq 1$ that is further discussed in the following sections. Fig. 6(c) shows that the cross-coupling gain decreases with the number of converters (17) because of the dependence on R_L. Moreover, the frequency coefficients in (17) do not depend on the number of converters. The phase is dominated by the denominator with an insignificant effect from the number of converters, as shown in Fig. 6(d).

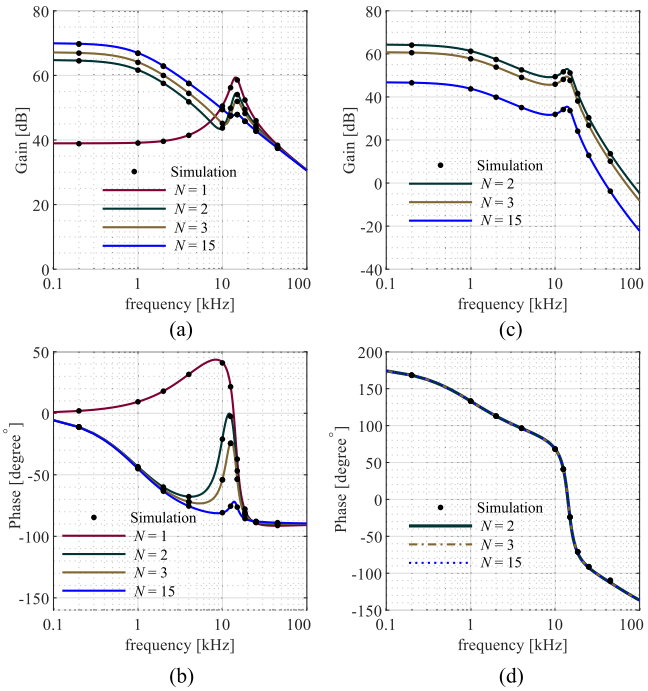

Fig. 6. Verification of the transfer functions. Direct control-to-input current transfer function G_{jj} magnitude in (a) magnitude and phase in (b). Cross-coupling control-to-input current transfer function G_{ij} magnitude in (c) magnitude and phase in (d).

IV. CONTROLLER DESIGN GUIDELINES

The small-signal analysis highlights the phase delay in the input current transfer functions as the number of BPMs in operation varies or with differential input currents, which is typical with battery balancing. In this section, three extreme balancing cases are considered for the controller design procedure. Section IV-A evaluates the compensated loop gain when a single BPM operates in a stand-alone mode or at equal current sharing with N BPMs. Section IV-B evaluates the compensated loop gain when $N - 1$ BPMs operate at equal input currents while applying a differential current offset Δi in a single BPM.

Section IV-C evaluates the compensated loop gain when current offsets are introduced to all BPMs. Section IV-D discusses the controller design.

A. Current Sharing at Balanced SOCs

Assume that N BPMs track the same current reference, such that $i_{g1} = i_{g2} = i_{gN}$, which is similar to a single BPM in operating a stand-alone mode, i.e., $N = 1$ (4). The compensated loop gain is obtained from the denominator of the system solution (5) that takes the form

$$T_{\text{sharing}}(s) = G_{ci}G_{\text{sharing}} = G_{ci}G_{jj}\Big|_{N=1} \tag{18}$$

$$T_{iCLsin}(s) = \frac{T_{\text{sharing}}(s)}{1 + T_{\text{s}}(s)} \tag{19}$$

where $T_{iCLsin}(s)$ is the current closed-loop gain with equal current sharing. At $N = 1$, the direct transfer function gain is the smallest compared to $N > 1$ cases, as shown in Fig. 6(a); however, the phase is the largest, as shown in Fig. 6(b). Thus, this scenario is the least critical operation mode for the controller design.

B. Differential Current in a Single BPM

Assume that $N - 1$ BPMs track the same current reference while introducing a differential current to a single BPM, such that $i_{g1} = i_{g2} = i_{g3} \cdots = i_{gN-1} \neq i_{gN}$. Therefore, the transient behavior is dominated by direct and all cross-coupling transfer functions in G_{mat}. The compensated loop gain T_{CiEx} is obtained from the denominator of the system solution, which is dominated by the determinant of (5)

$$T_{iCLEx}(s) = \frac{T_{CiEx}(s)}{1 + T_{CiEx}(s)}, \tag{20}$$

$$T_{CiEx}(s) = \left[G_{jj}^2 - (N-1)\,G_{ij}^2 + (N-2)\,G_{jj}G_{ij}\right] G_{ci}^2 + G_{jj}G_{ci} \tag{21}$$

where $T_{iCLEx}(s)$ is the current closed-loop gain with differential current sharing in a single BPM. The transient response in this scenario is faster than in equal current sharing case.

C. Differential Currents With N BPMs for SOC Balancing

Assume that N BPMs track different currents, such that $i_{g1} \neq i_{g2} \neq i_{gN}$ while maintaining the same output voltage. This is a typical mode in battery balancing applications, where current offsets Δi_j are introduced to the N BPMs around the common current i_{avg}, such that $\sum_{j=1}^{N} \Delta i_j = 0$. Under the assumption that the output voltage remains the same, the cross-coupling transfer functions can be ignored, where the compensated loop gain T_{ci} is governed by the diagonal elements in the solution of (5)

$$T_{ci}(s) = G_{ci}G_{jj}, \tag{22}$$

$$T_{iCL}(s) = \frac{T_{ci}(s)}{1 + T_{ci}(s)} \tag{23}$$

where $T_{TiCL}(s)$ is the current closed-loop gain with differential currents in all BPMs.

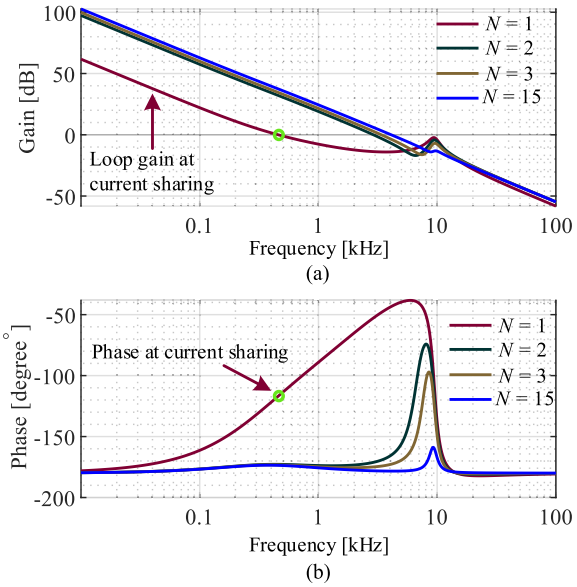

Fig. 7. Bode plot of the compensated loop gain with $G_{ci} = G_{\text{csharing}}$ at different N cases. (a) Magnitude. (b) Phase.

D. Controller Design

Designing the current compensator G_{ci} by considering only current sharing as in case (A) and ignoring the phase reduction with differential currents as in case (C) can lead to instability. For instance, assume that each BPM employs a current compensator that takes the form

$$G_{ci} = G_{\text{cdiff}} = \frac{K_1}{s} + \frac{K_2}{s^2} \tag{24}$$

where G_{csharing} is designed for equal current sharing, i.e., $N = 1$. The expressions (6)–(22) are evaluated for $N = 1$, $N = 2$, $N = 3$, and $N = 15$ using the BPM parameters in Table I. Fig. 7 illustrates the compensated loop gain, where the compensator gains $K_1 = 27.6$ and $K_2 = 57\ 974$ are tuned to achieve a crossover frequency of 460 Hz and a phase margin of 63° at current sharing, i.e., $N = 1$ and rated BPM current $I_g = 25$ A. Table II lists the crossover frequency and phase margins at the different N cases. Although the phase margin is 60° at $N = 1$, the phase margin diminishes for $N > 1$, as shown in Fig. 7. The gain of the direct transfer functions in the general N case G_{jj} increases with the number of BPMs N, as shown in Fig. 6(a); however, the phase reduces with the number of BPMs N, as shown in Fig. 6(b). Consequently, the input current loops tend to become faster and unstable for $N > 1$, as listed in Table II. Thus, the typical compensator design method can lead to instability, and a new design method that enables differential current control is required.

In this article, the battery brick consists of $N = 3$ parallel output connected BPMs. Each BPM employs a current compensator that takes the form

$$G_{ci} = G_{\text{cdiff}} = K_p + \frac{K_i}{s}. \tag{25}$$

By utilizing the compensated loop gain that is evaluated in (22), i.e., in case (C), the compensator parameters are chosen to achieve a crossover frequency of 1.1 kHz and a phase margin of

TABLE II
COMPARISON BETWEEN THE CURRENT SHARING COMPENSATOR AND DIFFERENTIAL CURRENT CONTROL COMPENSATOR

		$G_{csharing} = 27.6/s + 57974/s^2$		$G_{cdiff} = 0.001/\pi + 2/s$	
Operating point	Number of BPMs	Phase margin [°]	Crossover frequency [Hz]	Phase margin [°]	Crossover frequency [Hz]
$I_g = 25$ A,	$N = 1$ (current sharing)	63	460	93.1	39.6
$V_g = 4$ V,	$N = 2$	8.84	2900	68.7	901
$M(D) = 2.5$,	$N = 3$	5.78	3380	69.8	1110
(1C−rate)	$N = 15$	1.67	4100	71.6	1440
$I_g = 12.5$ A,	$N = 1$ (current sharing)	55	290	92.2	19.8
$V_g = 4$ V,	$N = 2$	5.82	2880	68	899
$M(D) = 2.5$,	$N = 3$	3.95	3370	69.3	1110
(0.5C−rate)	$N = 15$	1.49	4100	71.6	1450

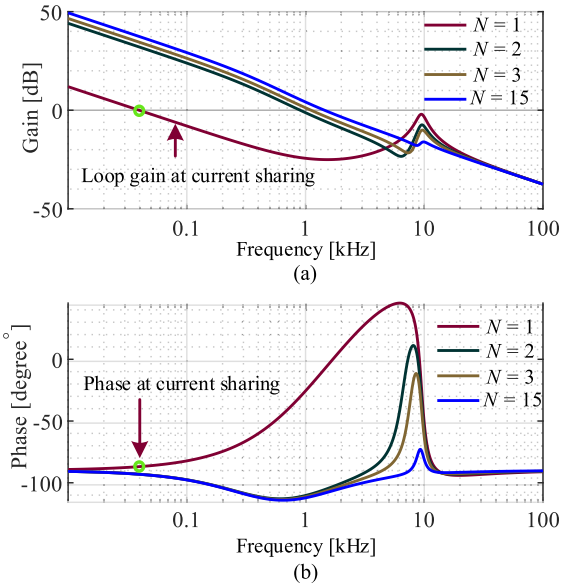

Fig. 8. Bode plot of the compensated loop gain with $G_{ci} = G_{\text{cdiff}}$ at different N cases. (a) Magnitude. (b) Phase.

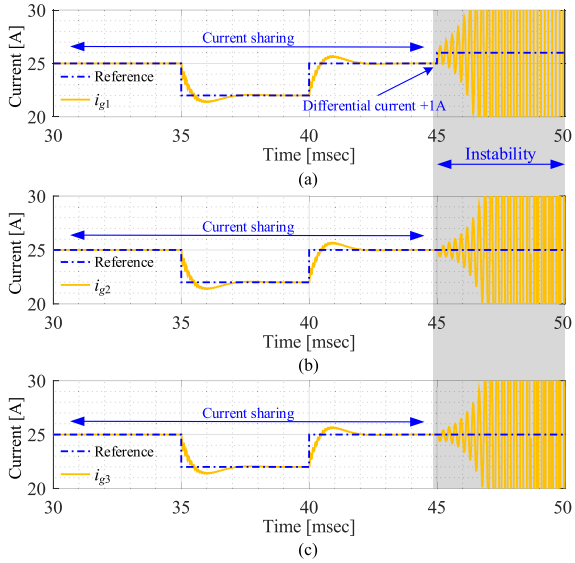

Fig. 9. Switching model simulation results with a current sharing compensator $G_{ci} = G_{\text{cdiff}}$.

70° at $N = 3$. The PI current compensator gains are

$$K_i = 2, K_p = \frac{0.001}{\pi}. \tag{26}$$

Table II lists the crossover frequency and phase margins at the different N cases. In terms of phase margin and crossover frequency, the compensator performance is acceptable for both current sharing and differential currents. The bode plot for the compensated loop gain is shown in Fig. 8, confirming that the bandwidth of the system is the slowest at equal current sharing.

V. SIMULATION RESULTS

The switching model simulation for the $N = 3$ case is leveraged to verify the analysis presented in the previous sections and the controller design. Table I lists the simulation model parameters. Section V-A verifies that designing the controller for current sharing may lead to instability with differential currents. Section V-B verifies that the switching model response at current current sharing matches the closed-loop model (19), which is discussed in Section IV-A, i.e., case (A). Section V-D verifies that the closed-loop model (23) matches the switching model response when differential currents are applied in two BPMs, which is discussed in Section IV-C, i.e., case (C). Section V-C verifies that the closed-loop model (20) predicts the switching model response when differential current is introduced in a single.

A. Current Sharing Controller Instability

In this section, each of the three BPMs utilizes the compensator $G_{ci} = G_{\text{csharing}}$, which is designed for current sharing scenarios. Fig. 9 shows the switching model simulation results after averaging the input currents in the three BPMs over the switching cycle of 5 μs. Prior to 35 ms, the three BPMs regulate their input currents at 25 A. Between 35 and 40 ms, the common current reference in the three BPMs changes between 20 and 25 A. The three current compensators track the common current reference, as shown in Fig. 9. Since the three BPMs utilize a current compensator that is designed for current sharing scenarios, the current loops are stable prior to 45 ms. At 45 ms, a differential current offset is introduced to the first BPM Δi_1 =+1 A, as shown in Fig. 9(a). On the other hand, the input current references in the second and third BPMs remain at +25 A. However, the input current loops in the three BPMs become unstable, as shown in Fig. 9. The instability in the current

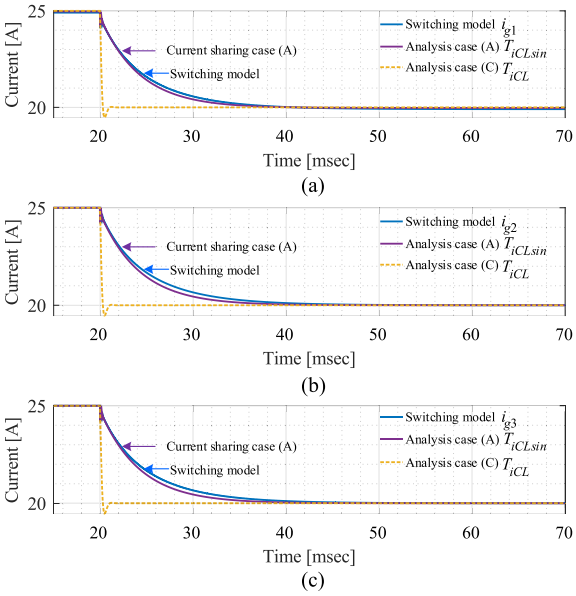

Fig. 10. Switching model simulation results—step change in the common input current.

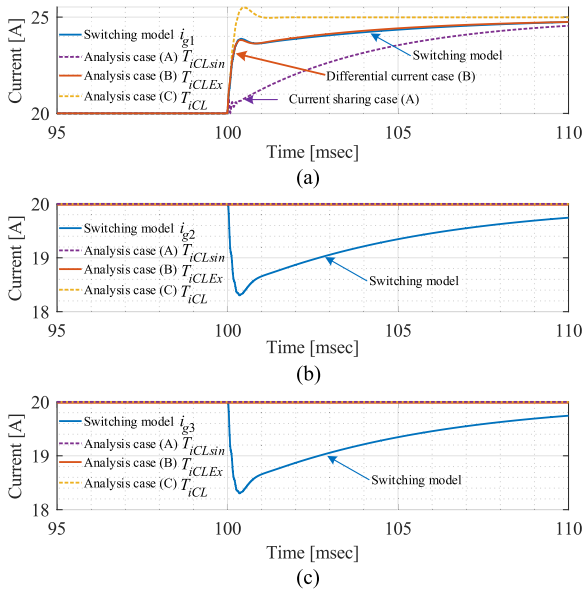

Fig. 11. Switching model simulation results—introduction of a single input current offset.

loops is anticipated at the $N = 3$ case, as listed in Table II with the current sharing compensator $G_{ci} = G_{c\text{sharing}}$. Therefore, this section clearly shows that designing the current loop using the conventional current sharing approach can lead to instability with differential currents.

B. Current Sharing Closed-Loop Model

In this section, each of the three BPMs utilizes the compensator $G_{ci} = G_{c\text{diff}}$ that considers the differential currents with three BPMs. Fig. 10 shows the switching model simulation results after averaging the input currents. Moreover, Fig. 10 shows the analytical closed-loop responses for current sharing $T_{iCLsin}(s)$ and the analytical closed-loop model with differential currents $T_{iCL}(s)$. Prior to 20 ms, the three BPMs regulate their input currents at 25 A. At 20 ms, the current reference in the three BPMs changes to 25 A, which is tracked by the three current loops, as shown in Fig. 10, emulating case (A) in Section IV-A. The analytical closed-loop model for current sharing $T_{iCLsin}(s)$ replicates the system dynamics because the individual BPMs can be treated as a single converter at this operating point, i.e., $N = 1$. On the other hand, $T_{iCL}(s)$ is valid when differential input currents are introduced to the BPMs, such that $\sum_{j=1}^{3} \Delta i_j = 0$. Thus, the response due to the change in the current reference in all BPMs is replicated exclusively by $T_{iCLsin}(s)$. Fig. 11 clearly shows that the slowest transient response occurs with current sharing; thus, current sharing is the least critical operating mode in parallel output connected BPMs.

C. Closed-Loop Model for a Differential Current in a Single BPM

The switching model simulation is extended to verify the analysis when a differential input current is introduced to a single BPM, emulating case (B) in Section IV-B. Prior to 100 ms, the three BPMs track a 20-A current reference, as shown in Fig. 11. At 100 ms, the current reference in the first BPM changes to 25 A, where the designed compensator $G_{c\text{diff}}$ regulates the input current in BPM_1, as shown in Fig. 11. However, the same scenario results in instability with the current sharing controller $G_{c\text{sharing}}$, as shown in Fig. 9. Furthermore, Fig. 11 shows that the analytical closed-loop responses with a differential current in a single BPM $T_{iCLEx}(s)$ replicates the dynamics in the input current i_{g1}. On the other hand, $T_{iCL}(s)$ (23) assumes that differential input currents are introduced to the BPMs, such that $\sum_{j=1}^{3} \Delta i_j = 0$. Therefore, $T_{iCL}(s)$ does not match the switching model response of i_{g1} in this scenario; however, $T_{iCL}(s)$ provides an approximation for the rise-time of i_{g1}. Moreover, the change in the input current of BPM_1 results in disturbances in the input currents i_{g2} and i_{g3}, as shown by the dotted lines in Fig. 11(b) and (c) due to the cross-coupling transfer functions. The analytical expressions $T_{iCL}(s)$, $T_{iCLEx}(s)$, and $T_{iCLsin}(s)$ rely on their individual control commands and do not include the control commands of the other BPMs, i.e., single-input single-output systems. However, the three paralleled BPMs form a MIMO system, where a change in the control command of BPM_1 perturbs i_{g2} and i_{g3}. Consequently, the disturbances in i_{g2} and i_{g3} are not replicated by $T_{iCL}(s)$, $T_{iCLEx}(s)$, and $T_{iCLsin}(s)$ in BPM_2 and BPM_3.

D. Differential Currents in Two BPMs

The switching model simulation is extended to verify the analysis when differential input currents are introduced to the BPMs, such that $\sum_{j=1}^{3} \Delta i_j = 0$, emulating case (C) in Section IV-C. Prior to 200 ms, the three BPMs regulate their input currents at 20 A, as shown in Fig. 12. At 200 ms, an input current offset of +5 A is introduced to BPM_3, and an input current offset of –5 A is introduced to BPM_1. The compensator $G_{c\text{diff}}$ is designed at this operating point; therefore, the first and third BPMs track

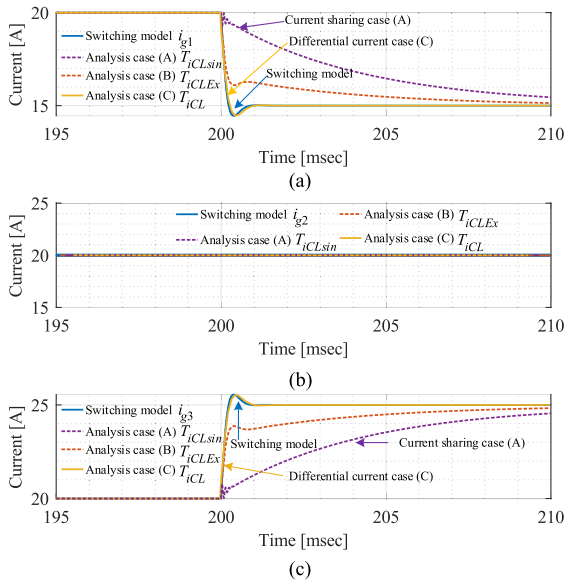

Fig. 12. Switching model simulation results—introduction of two input current offsets.

the new current references at +15 and +25 A, respectively, as shown in Fig. 12(a) and (c). Moreover, the approximated closed-loop response $T_{iCL}(s)$ matches the switching model input current responses for i_{g1} and i_{g3}, as shown in Fig. 12(a) and (c), respectively, verifying the analysis in the previous sections. Moreover, with differential current control, the input currents rise at approximately 20 kA/s, which is well-predicted by the analytical expression for $T_{iCL}(s)$. The closed-loop response $T_{iCL}(s)$ matches the switching model simulation because the two input currents offsets cancel the change in the dc output voltage. Although the analytical expression $T_{iCLEx}(s)$ provides an approximation for the rise-time of the input current, it does not match the input current response because the current changes in two BPMs. Furthermore, the closed-loop response due to $T_{iCLsin}(s)$ is significantly different and slower than the switching model response or $T_{iCL}(s)$, as shown in Fig. 12(a) and (c), proving that the differential current control is fundamentally different from the equal current sharing. Moreover, the simulation results show stable and acceptable performance with the designed compensator $G_{ci} = G_{\text{cdiff}}$. which enables differential current regulation, verifying the analysis and controller design procedure.

VI. Experimental Results

Fig. 13 shows a validation prototype consisting of three BPMs utilizing four-switch buck–boost converters. Table III summarizes the prototype parameters. Each BPM is connected across a single 25 Ah Panasonic NMC battery cell. The input port of the converter is rated for 25 A, i.e., 1C-rate. Converter modulation and control are implemented in a single microcontroller. Three digital current regulation loops are implemented in the microcontroller by discretizing the PI compensator in (25) using Tustin approximation with the same parameters, as summarized in (26).

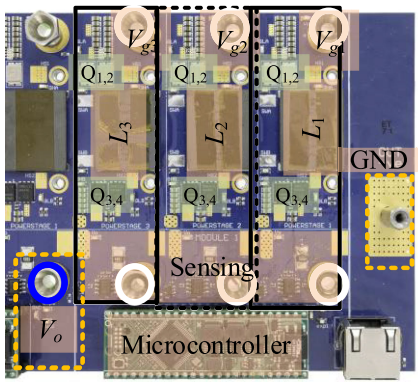

Fig. 13. Experimental prototype consisting of three parallel output connected four-switch buck–boost converters.

TABLE III
Prototype Parameters

Parameter	Part Number
Buck stage switches Q_{1-2}	BSB008NE2LX (Infineon)
Boost stage switches Q_{3-4}	BSC009NE2LS5I (Infineon)
Half-bridge gate driver	UCC27211A (TI)
Current sense resistor (1 mΩ, 1%)	CRE2512-FZ-R001E-2 (Bourns)
Differential amplifier (feedback loop)	THS4531 (TI)
Inductance L_{1-3}	320 nH
Output capacitance C_o	360 μF
Input capacitance per BPM	120 μF
Microcontroller	TMS320F280049 (TI)
Switching frequency f_s	200 kHz

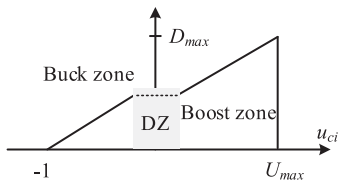

Fig. 14. Duty cycle and operation mode for a given compensator output.

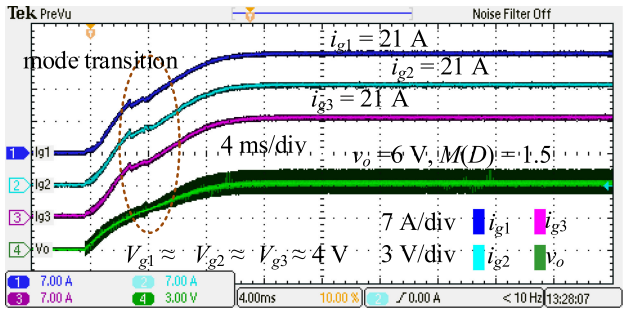

Fig. 15. Experimental results with equal current sharing in discharging mode—startup in boost mode in a 250-W load.

Fig. 14 shows the current loop compensator saturated output between $[-1, D_{\max}]$ and the corresponding operation mode. It is worth to mention that there are different schemes for avoiding the dead-zone in four-switch buck–boost converters, which is beyond the scope of this article [38], [39].

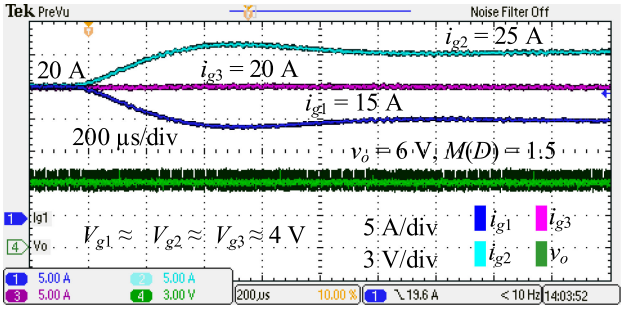

Fig. 16. Experimental results with differential currents in discharging mode—step change of ±5 A in the balancing current of two modules.

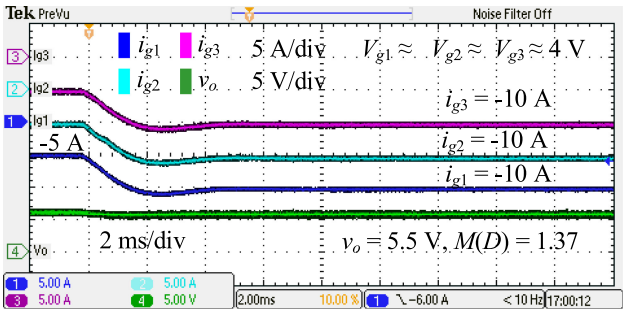

Fig. 17. Equal current sharing in charging mode—step change of −5 A in the charging current all BPMs in current sharing.

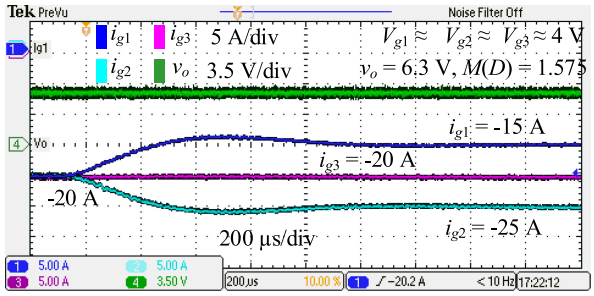

Fig. 18. Differential current in charging operation—step change of ±5 A in the balancing current of two modules.

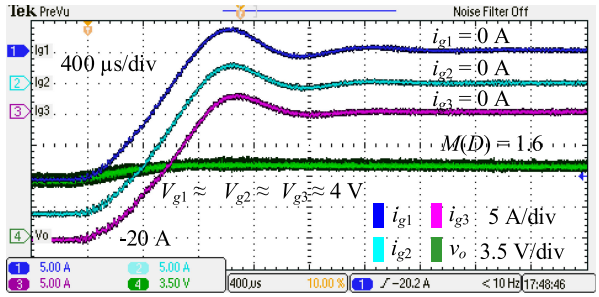

Fig. 19. End of charge/shutdown operation—step change in the charging current from –20 to 0 A.

Fig. 15 shows a startup experiment with current sharing at a 250-W load in boost mode, where all input currents track a 21-A reference. At startup, the BPMs operate in buck mode that provides a soft starting mechanism by regulating the input currents, as shown in Fig. 15. Although the brick exhibits a nonlinearity because of employing four-switch buck–boost converters, the transition between buck and boost modes is smooth, as shown in Fig. 15.

Fig. 16 shows a typical active BMS operation, where all BPMs initially regulate their input currents at an equal current reference of 20 A, i.e., 0.8C-rate of the battery cell. To validate the differential current capability, the BMS introduces an input current offset of ±5 A only to the second and first modules, respectively. Fig. 16 shows that the individual current regulation loops track the new current references, whereas the current loop of the third module maintains the initial 20-A input current reference, emulating case (C) in Section V-D. From Fig. 16, with differential current control, the BPMs input currents rise at approximately 20 kA/s that is nearly matching the switching model simulation results.

From the timescale in Figs. 15 and 16, it is deduced that the system response is faster with differential current control, which ensures that differential current scenarios are more critical to the stability of the paralleled BPMs. Figs. 15 and 16 validate the controller design procedure and analysis presented in the previous sections in discharging modes.

The three parallel output connected BPMs charge in boost mode. In Fig. 17, the three modules regulate their input currents at −5 A, where the bus voltage is approximately 6 V at $M(D) = 1.5$. The BMS adjusts the charging currents to −10 A that is tracked by the three BPMs as a current sharing scenario, emulating case (A) in the controller design section. With equal current sharing control, the BPM input currents rise at approximately 5 kA/s, as shown in Fig. 17. Fig. 17 shows that the designed controller successfully regulates the three input currents even for current sharing in charging modes.

Fig. 18 illustrates a balancing scenario in the charging mode. Initially, the three modules regulate their input currents at –20 A to absorb 240 W. Then, the BMS introduces an input current offset of ±5 A to the first and second modules, respectively, emulating case (C) in the controller design section. From Fig. 18, with differential current control, the BPM input currents rise at approximately 20 kA/s that is nearly four times the differential current case. The system's transient response is significantly faster with differential current control for balancing, which is why designing a compensator exclusively for current sharing is critical on the overall system stability.

To demonstrate the end of charging operation, Fig. 19 shows a shutdown scenario, where the three modules regulate their input currents from a −20 A reference to 0 A. The individual controllers maintain the input currents at 0 A, validating the designed controller and its ability for integration in an active BMS.

The experimental results validate the designed controller in regulating the input currents of the paralleled BPMs for both differential and equal current sharing in discharging and charging modes. Moreover, the experimental results show that the system's transient response is substantially faster with differential current control in comparison with current sharing. The experimental results validate the analysis and controller design for the practical BMS balancing scenarios. It is important to

mention that the analysis presented in this article assumes that the paralleled BPMs operate in the same mode. Therefore, when some BPMs operate in buck mode, while other BPMs operate in boost mode, further analysis will be required to enable this emerging battery balancing concept.

VII. Conclusion

This article focuses on differential input current regulation with N parallel output connected BPMs for individual SOC control in an active BMS. Small-signal analysis based on individual current loops shows the differences in the direct control-to-input current transfer functions with the number of paralleled BPMs N. Analysis and simulations have proven that designing the current loop compensator for current sharing or for a single BPM operation may lead to instability with differential current control. A current loop compensator is designed by leveraging the small-signal analysis in boost mode of operation. The designed controller is verified in simulations and validated experimentally by utilizing a 300-W battery brick consisting of three parallel output connected BPMs employing four-switch buck–boost dc/dc converters. Experimental results validate successful input current regulation in most practical cases of a BMS that require differential currents or equal current sharing.

References

[1] X. Tang *et al.*, "Run-to-run control for active balancing of lithium iron phosphate battery packs," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1499–1512, Feb. 2020.

[2] Y. Yang, K. Hu, and C. Tsai, "Digital battery management design for point-of-load applications with cell balancing," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6365–6375, Aug. 2020.

[3] M. Kim and S. Han, "Novel data-efficient mechanism-agnostic capacity fade model for Li-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 6267–6275, Jul. 2020.

[4] M. Koseoglou, E. Tsioumas, N. Jabbour, and C. Mademlis, "Highly effective cell equalization in a lithium-ion battery management system," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 2088–2099, Feb. 2020.

[5] Z. B. Omariba, L. Zhang, and D. Sun, "Review of battery cell balancing methodologies for optimizing battery pack performance in electric vehicles," *IEEE Access*, vol. 7, pp. 129335–129352, 2019.

[6] D. F. Frost and D. A. Howey, "Completely decentralized active balancing battery management system," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 729–738, Jan. 2018.

[7] M. Evzelman, M. M. Ur Rehman, K. Hathaway, R. Zane, D. Costinett, and D. Maksimovic, "Active balancing system for electric vehicles with incorporated low-voltage bus," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7887–7895, Nov. 2016.

[8] Y. Chen, X. Liu, Y. Cui, J. Zou, and S. Yang, "A multiwinding transformer cell-to-cell active equalization method for lithium-ion batteries with reduced number of driving circuits," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4916–4929, Jul. 2016.

[9] H. Rahimi-Eichi, U. Ojha, F. Baronti, and M. Chow, "Battery management system: An overview of its application in the smart grid and electric vehicles," *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 4–16, Jun. 2013.

[10] H. Park, C. Kim, C. Kim, G. Moon, and J. Lee, "A modularized charge equalizer for an HEV lithium-ion battery string," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1464–1476, May 2009.

[11] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-charge (SOC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, Jun. 2009.

[12] M. Rasheed, M. Kamel, H. Wang, R. Zane, and K. Smith, "Investigation of active life balancing to recondition Li-ion battery packs for 2nd life," in *Proc. IEEE 21st Workshop Control Model. Power Electron.*, 2020, pp. 1–7.

[13] C. Moo, K. S. Ng, and Y. Hsieh, "Parallel operation of battery power modules," *IEEE Trans. Energy Convers.*, vol. 23, no. 2, pp. 701–707, Jun. 2008.

[14] C. Liu, X. Cai, and Q. Chen, "Self-adaptation control of second-life battery energy storage system based on cascaded H-bridge converter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1428–1441, Jun. 2020.

[15] C. Liu, N. Gao, X. Cai, and R. Li, "Differentiation power control of modules in second-life battery energy storage system based on cascaded H-bridge converter," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6609–6624, Jun. 2020.

[16] S. M. Chowdhury, M. O. Badawy, Y. Sozer, and J. A. D. A. Garcia, "A novel battery management system using the duality of the adaptive droop control theory," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5078–5088, Sep. 2019.

[17] W. Huang and J. A. Abu Qahouq, "Energy sharing control scheme for state-of-charge balancing of distributed battery energy storage system," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2764–2776, May 2015.

[18] Y. Li and Y. Han, "A module-integrated distributed battery energy storage and management system," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8260–8270, Dec. 2016.

[19] Y. Cao and J. AbuQahouq, "Hierarchical SOC balancing controller for battery energy storage system," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9386–9397, Oct. 2021.

[20] N. Mukherjee and D. Strickland, "Control of cascaded DC-DC converter-based hybrid battery energy storage systems-Part I: Stability issue," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2340–2349, Apr. 2016.

[21] N. Mukherjee and D. Strickland, "Control of cascaded DC-DC converter-based hybrid battery energy storage systems-Part II: Lyapunov approach," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 3050–3059, May 2016.

[22] K. I. Hwu and Y. H. Chen, "Current sharing control strategy based on phase link," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 701–713, Feb. 2012.

[23] D. Sha, Z. Guo, and X. Liao, "Cross-feedback output-current-sharing control for input-series-output-parallel modular DC-DC converters," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2762–2771, Nov. 2010.

[24] A. Kelly, "Current share in multiphase DC-DC converters using digital filtering techniques," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 212–220, Jan. 2009.

[25] W. Chen, X. Ruan, H. Yan, and C. K. Tse, "DC/DC conversion systems consisting of multiple converter modules: Stability, control, and experimental verifications," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1463–1474, Jun. 2009.

[26] H. Mao, L. Yao, C. Wang, and I. Batarseh, "Analysis of inductor current sharing in nonisolated and isolated multiphase DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3379–3388, Dec. 2007.

[27] Y. Panov and M. M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 776–783, Nov. 2001.

[28] G. Garcera, M. Pascual, and E. Figueres, "Robust average current-mode control of multimodule parallel DC-DC PWM converter systems with improved dynamic response," *IEEE Trans. Ind. Appl.*, vol. 48, no. 5, pp. 995–1005, Oct. 2001.

[29] C. J. Chen, Z. Y. Zeng, C. H. Cheng, and F. T. Lin, "Comprehensive analysis and design of current-balance loop in constant on-time controlled multi-phase buck converter," *IEEE Access*, vol. 8, pp. 184752–184764, 2020.

[30] W. Jiang, X. Zhang, F. Guo, J. Chen, P. Wang, and L. H. Koh, "Large-signal stability of interleave boost converter system with constant power load using sliding-mode control," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9450–9459, Nov. 2020.

[31] Y. Xia, M. Yu, Y. Peng, and W. Wei, "Modeling and analysis of circulating currents among input-parallel output-parallel nonisolated converters," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8412–8426, Oct. 2018.

[32] H. Li *et al.*, "An extended stability analysis method for paralleled DC-DC converters system with considering the periodic disturbance based on floquet theory," *IEEE Access*, vol. 8, pp. 9023–9036, 2020.

[33] J. Gordillo and C. Aguilar, "A simple sensorless current sharing technique for multiphase DC-DC buck converters," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3480–3489, May 2017.

[34] D. Sha, J. Zhang, X. Wang, and W. Yuan, "Dynamic response improvements of parallel-connected bidirectional DC-DC converters for electrical drive powered by low-voltage battery employing optimized feedforward control," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7783–7794, Oct. 2017.

[35] W. Huang and J. A. Abu Qahouq, "Input voltage ripple-based sensorless current sharing autotuning controller for multiphase DC-DC converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4117–4125, Sep./Oct. 2016.
[36] R. F. Foley, R. C. Kavanagh, and M. G. Egan, "Sensorless current estimation and sharing in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2936–2946, Jun. 2012.
[37] M. Kamel, R. Zane, and D. Maksimovic, "Voltage sharing with series output connected battery modules in a plug-and-play DC microgrid," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13118–13127, Nov. 2021.
[38] D. C. Jones and R. W. Erickson, "A nonlinear state machine for dead zone avoidance and mitigation in a synchronous noninverting buck-boost converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 467–480, Jan. 2013.
[39] L. Jia, X. Sun, Z. Zheng, X. Ma, and L. Dai, "Multimode smooth switching strategy for eliminating the operational dead zone in noninverting buck-boost converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3106–3113, Mar. 2020.

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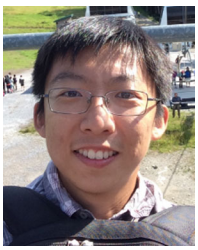

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