Control and Modulation of a Single-Phase AC/DC Converter With Smooth Bidirectional Mode Switching and Symmetrical Decoupling Voltage Compensation

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***Abstract*—In this article, a bidirectional single-phase ac/dc converter with active power decoupling (APD) and smooth mode switching is proposed. Power decoupling techniques have been proved efficient in the reduction of bulky dc bus electrolytic capacitors (E-caps) for single-phase low-power level conversion systems. However, it is found that when dealing with transient conditions such as sudden bidirectional switching or steep load changes, the whole system may be vulnerable and unstable under greatly reduced E-caps situation. None of the existing researches carefully examine such dc bus transient characteristics with bidirectionality under decoupling situation. By multiusing the APD cell, the proposed dc bus voltage suppression strategy is capable of both dc bus voltage ripple elimination and load disturbance rejection under transient conditions. Moreover, the proposed controller involves a dead-time compensation to achieve symmetrical power decoupling voltage without additional sensors for decoupling circuit, which ensures the maximum ripple power suppression ability as well as achieves minimum capacitance requirements. Finally, a 1-kW, 110-Vrms, and 50-Hz single-phase ac/dc prototype has been built and evaluated. Theoretical predictions are compared favorably with experimental results.**

***Index Terms*—Active power decoupling (APD), bidirectional switching, double-line frequency, single-phase ac/dc converters.**

NOMENCLATURE

C	DC offset value of decoupling voltage.
C_1	Filter capacitor of grid side.
C_{bus}	DC bus capacitor.
C_{dp}	Decoupling capacitor of *LC* branch.
$d_{(k+n)1}$	Duty cycle of PFC.
$d_{(k+n)2}$	Duty cycle of APD.
d_{output}	Turn-ON duty cycle of S_3.
$\hat{d}_{k1}$	Disturbance of PFC duty cycle.
$\hat{d}_{k2}$	Disturbance of APD duty cycle.
D_{e1}	Equilibrium values of PFC duty cycle.
D_{e2}	Equilibrium values of APD duty cycle.
D_{deadtime}	Dead-time of two switches in phase-B.
f_s	Switching frequency.
f_o	Line frequency.
f_{dp}	Resonant frequency of the *LC* decoupling branch.
H_{if}	Feedback coefficient of inner inductor current.
H_{vg}	Feedback coefficient of grid voltage.
H_{vf}	Feedback coefficient of dc bus voltage.
i_b	Current flowing into phase-B.
i_{load}	Load current of R_{dc}.
is	DC current source of dc bus.
i_{dc}	Total load current at dc bus side.
i_g	Grid current.
$i_g{}^*$	Grid current reference of inner current controller.
i_{err}	Error of the inner inductor current.
i_{ripple}	Current rejected from decoupling circuit.
i_{L1}	Inductor current of L_1.
i_{dp}	Inductor current of L_{dp}.
I_{load}	Amplitude of load current.
I_s	Amplitude of dc current source.
I_g	Amplitude of i_g.
k_{i_v}	Integral coefficient of outer voltage loop.
k_{p_v}	Proportional coefficient of outer voltage loop.
L_g	Grid side inductance.
L_{dp}	Decoupling inductor of *LC* branch.
L_1	Boost inductor of H-bridge.
p_s	Grid side power.
p_{ripple}	Decoupling ripple power.
p_{load}	DC bus side power.
R_g	Grid side resistance.
R_{dc}	Resistive load of dc bus.
u_{PFC}	Control output for regulating i_g and v_{dc}.
u_{APD}	Control output for regulating v_{dp} and v_{dc}.

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v_{ab}	Neutral point voltage between phase-A and phase-B.
v_b	Neutral point voltage of phase-B.
v_g	Grid voltage.
v_{dp}	Decoupling voltage of C_{dp}.
v_{dc}	DC bus voltage of C_{bus}.
v_{err}	Error of the dc bus voltage.
v_{rip}	Error of decoupling ripple voltage.
$v_{\mathrm{dc}}{}^{*}$	DC bus voltage reference of outer voltage controller.
V_g	Amplitude of v_g.
V_{dc}	DC component of dc bus voltage.
V_m	Modulation voltage.
$V_{\mathrm{ref\_}c}$	Coefficient of decoupling fluctuation reference.
$V_{\mathrm{ref^{\cdot}ripple}}$	Decoupling ripple voltage value according to v_{err}.
T_s	Switching cycle.
T_{ON}	Time when u_{PFC} equals to 1.
T_{OFF}	Time when u_{PFC} equals to 0.
X_e	Equilibrium values of state vector.
$x(t)$	State vector.
$u(t)$	Input vector.
$z(t)$	Controllable output vector.
γ_s	Minimum level of disturbance attenuation of *is*.
γ_r	Minimum level of disturbance attenuation of i_{ripple}.
φ	Decoupling phase.
ω	Angular frequency of grid voltage.
$\|\|y\|\|_2$	Euclidian norm of decoupling ripple energy.
$\|\|z\|\|_2$	Euclidian norm of controllable output.
$\|\|H(s)\|\|_\infty$	Infinite norm of transfer functions.

I. INTRODUCTION

BIDIRECTIONAL single-phase ac/dc converters have been broadly used in a wide range of residential and low-power level industrial applications, including electric vehicle (EV) on-board chargers for vehicle-to-grid (V2G) or grid-to-vehicle modes, energy storage power conversion systems, and other power supplies [1]–[4]. Fig. 1 gives the configuration of a hybrid ac/dc microgrid system for residential applications. As shown in Fig. 1, the bidirectional ac/dc converter acts as the power stage interface between the power grid and electric appliance. By effectively obtaining unity power factor and low-input harmonic currents at ac side while maintaining stable bus voltage at dc side, it is introduced to achieve a more harmonized ac/dc distribution system, which is so called enabling technology for the development of the new, clean, and sustainable energy [4], [5].

However, an inherent double-line frequency ripple power (DFRP) oscillation consistently exists during the power conversion process in single-phase ac/dc applications, which will cause a second-order harmonic power oscillation at the dc port [6]. Especially for the specific dc source like batteries and fuel cells, the DFRP will lead to certain thermal issues and lifetime reduction [7]. To solve this, numerous topologies and control methods with active power decoupling (APD) function have been specifically compared and summarized in [8]–[10]. The basic way to realize APD is to transfer the second-order ripple power away from dc side to power decoupling cells such as a small film capacitor or other energy storage elements. Then the whole system will realize electrolytic capacitor-less (E-Capless) by embedding decoupling capacitor to substitute E-cap and achieve high power density and high reliability [6]–[10]. According to the comprehensive surveys in [10], power decoupling topologies are mainly divided into three categories, which are rectifiers (ac/dc converter), inverters (dc/ac converter), and bidirectional converters. It could be further classified as single-stage and two-stage, isolated and nonisolated, dependent and independent based on different topologies and their applications.

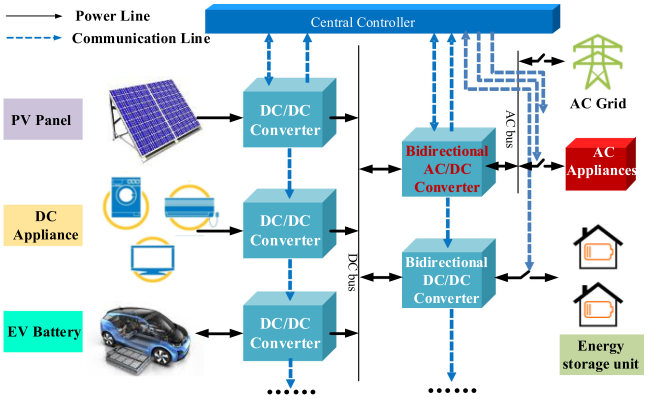


Fig. 1. Configuration of a hybrid ac/dc microgrid system for residential applications.

Among those topologies, usually we demonstrate the effectiveness of the power decoupling method by how much dc bus capacitor reduction it would bring, or the suppression effect of the DFRP, but none of the existing APD researches pay attention to the relationship between the dc bus port-capacitance characteristics and the dynamic response of bidirectional mode switching. In [11], APD is achieved by controlling the current on the decoupling capacitor with an extra phase leg. It evaluates the voltage source converter and current source converter, which are valid for both rectifier and inverter operation, but not mention the dynamic bidirectional switching matters. The topology used in [12] also consists of a third leg, along with an energy storage capacitor and a smoothing inductor for energy buffering. It only gives the transient waveforms of bidirectional converter switching between rectifier and inverter modes and simply demonstrates its effectiveness in the two modes of operation, without further theoretical analysis of its stability or robustness under transient conditions. One thing remains unsolved in [12] is that the total harmonic distortion (THD) of gird current is large during bidirectional switching and may affect the quality of power supply. The same H-bridge topology and the addition phase leg is also analyzed in [13] with a space-vector pulsewidth modulation (PWM) control method. It calculates two possible solutions for decoupling angle for three specific cases: rectifier (PF $= 1$), inverter (PF $= -1$), and STATCOM (PF $= 0$), with the minimum voltage and current stress. However, analysis of transient mode switching process is not included in [13], only giving the steady-state waveforms in different cases.

Chen *et al.* [14] proposed a bidirectional digital control structure with two independent controllers in a two-stage bidirectional topology. Here, a small-signal perturbation from the grid voltage is added into current loop. However, this perturbation cannot be completely eliminated by voltage feedforward control and only one mode transition is given in [14]. Besides, for all the aforementioned topologies, another phase leg with more switches and sensors are added to the original H-bridge structure, which would end up with more losses and costs, making decoupling topology inefficient.

Instead of adding more switches and sensors like the structures discussed in [11]–[14], a more effective voltage-sensorless controller with adaptive power decoupling function is proposed in [15]. The concept is based on sharing one leg with power decoupling circuit, where the decoupling branch LC is connected to the dc side through shared leg. With such arrangement, the energy storage components are greatly reduced, making it possible to replace the large E-caps with small-value film capacitors. The key advantage of proposed controller in [15] is that there is no need to add any additional active switches or extra measurement circuits. Thus, its implementation only requires three measurement circuits which are originally included in the H-bridge topology, as well as film capacitors with longer life expectancy.

The discussions in [15] are confined to the APD controller design in steady state, where the load power is unidirectional with a simple resistor at dc side. Therefore, in this article, performances of a bidirectional single-phase APD converter in which dc bus is connected with a current source and a resistive load, are studied and illustrated. In fact, the bidirectional switching response characteristics are critical for different types of single-phase converters, which would greatly impact the DFRP reduction effect and the feasibility of the control scheme. Taken EV battery charger with V2G capability as an example, a successful bidirectional ac/dc charger should effectively control the power flow between the grid and the EV battery, as well as performing other ancillary functions such as unity power factor and ripple power suppression on battery side [2]. Since the transient switching action of V2G energy storage equipment will cause certain impact to the power grid, the corresponding dynamic response of two-stage converters should meet the dynamic response requirements of the power grid during bidirectional switching. When the smart grid gives the EV a power feedback signal, the on-board EV battery needs to immediately feed the energy back to the grid. During this period, the dynamic response characteristics are closely related to the two-stage single-phase ac/dc converter [3]. Fig. 2 shows a bidirectional two-stage ac/dc converter used in V2G application with direct EV battery connection, which can actually be used for grid balancing and offsetting area-wide intermittency in renewable energy generation. Zhang and Ruan [7] have analyzed how dc bus port-impedance characteristics impact the second harmonic current reduction control scheme for two-stage converters. If targeting at the substitute of intermediate E-caps with film capacitors, the dynamic response of the former decoupling stage is vital to the latter stage of dc/dc converter, dc source, or dc load.

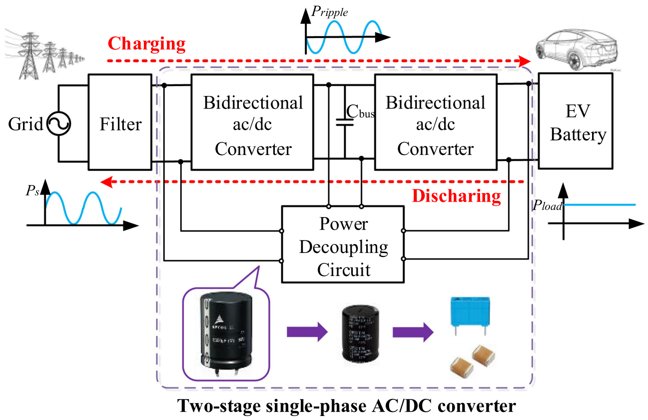


Fig. 2. Typical architecture of a bidirectional two-stage single-phase ac/dc converter used in V2G application.

In the most decoupling circuits, the DFRP is transferred to the decoupling branch, then the dc bus capacitance will be greatly reduced, or even be completely removed. Under such E-Capless condition, there is no large capacitor used for load disturbance rejection. Therefore, the whole system may be vulnerable and unstable during transient conditions such as steep load changes or bidirectional mode switching, leading to the deterioration of the dynamic performance. As a result, the performance of the high-voltage film capacitors still cannot compete with E-Caps [6]. In order to lessen the dependency of the dc bus capacitance, most power decoupling branches are composed of passive energy storage elements along with controllable switches, which means, other than the ability of DFRP suppression, the added decoupling cell could be multiused for reducing the voltage or current surge under transient conditions. If appropriate control strategy is adopted, it can do both power decoupling function and fast dynamic response under transient disturbance. However, this fact was not demonstrated in the previous publications. Therefore, it is of great significance to investigate the dynamic characteristics under bidirectional switching for single-phase APD converters.

This article extends the scope of study by applying the APD controller proposed in [15] with smooth bidirectional mode switching and better decoupling performance. The control target is to guarantee the dynamic response during power fluctuation and bidirectional mode switching from rectifier to inverter, and vice versa, with no added detection for any voltage or current information from decoupling branch. In addition, another objective of this article is to analyze and solve the asymmetry problem of decoupling voltage caused by different commutation direction of multiplexing bridge arm. The decoupling voltage waveforms in [16]–[19] all show different levels of asymmetry. Due to the inconsistency of inductor current direction during dead-time commutation, the asymmetry of decoupling voltage under positive and negative half cycle will occur. Then a dead-time compensation strategy (DTCS) is proposed to effectively improve the maximum ripple suppression ability as well as achieve minimum capacitance requirements in the power decoupling H-bridge topology. The main contribution

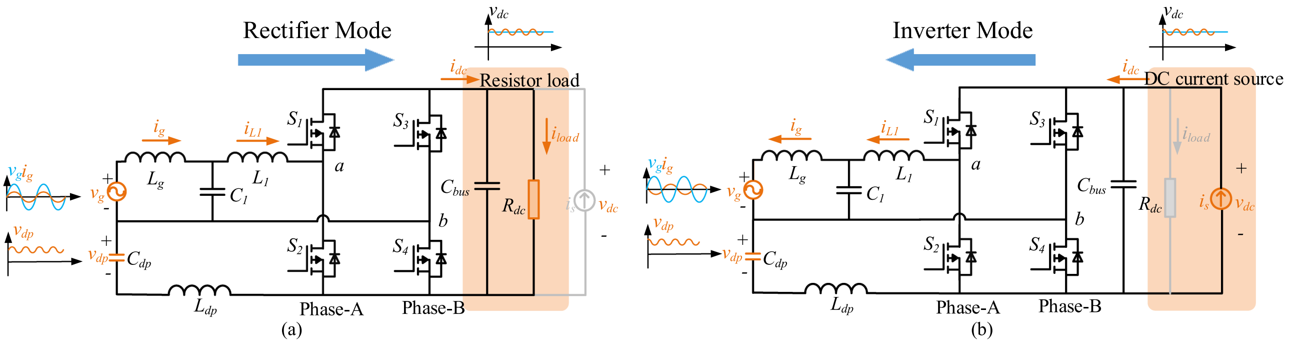


Fig. 3. Circuit configuration of the bidirectional single-phase APD converter with different power flow. (a) Unity power factor rectifier mode. (b) Grid-connected inverter mode.

of this article focuses on solving the dynamic response issues for decoupling topology under greatly reduced E-cap situation while maintaining great decoupling function. The designed APD controller proves to be simple and straightforward with strong adaptation and robustness under both steady and transient states.

The rest of this article is organized as follows. Section II presents the proposed configuration along with its bidirectional power flow analysis. The proposed dc bus voltage suppression strategy is also described in Section II. System modeling and robustness analysis of the proposed dc bus voltage suppression controller are performed in Section III. Section IV explains the asymmetry causes of decoupling voltage and puts up with a DTCS. In Section V, both the steady-state and dynamic performance of the converter is verified through simulation and experimental results. Finally, Section VI concludes this article.

II. PROPOSED DC BUS VOLTAGE SUPPRESSION CONTROLLER FOR BIDIRECTIONAL CONVERTER

A. Power Flow Analysis of Bidirectional Multifunctional Power Decoupling Converter

Fig. 3 shows the circuit configuration of the bidirectional single-phase ac/dc converter with an APD cell. It works simply as a typical totem-pole mode without L_{dp} and C_{dp}, which can be briefly described as below: S_1&S_2 pair are switched in a complementary fashion with high switching frequency to charge and discharge the boost inductor L_1, while low-frequency switches S_3 and S_4 are used for rectification.

In order to achieve dc bus capacitor reduction under the same ripple power, an auxiliary decoupling energy storage circuit consisting of a series LC branch is added between the cathode and the ground. Thus, the bus side voltage can be viewed as a bias dc voltage with the double-line frequency ripple, while S_3 and S_4 and the added LC branch form a conventional buck circuit. Since S_3 and S_4 are working at low frequency (50 Hz), they can be reused to transfer the ripple power from C_{bus} to C_{dp}. With accurate modeling and optimal control strategy, both PFC and APD functions can be achieved at the same time. Assuming a continuous conduction mode, the original four switches (S_1, S_2 on phase-A and S_3, S_4 on phase-B) would operate in either ON or OFF states in a different way.

This circuit also allows bidirectional switching and can support both the rectifier mode and the inverter mode, which is shown in Fig. 3. For a rectifier, a pure resistive load R_{dc} is connected to the dc bus capacitor with a load current i_{load}. For inversion, the converter is tied to the ac grid, while a current source *is* paralleled to C_{bus} is used to emulate a dc source converter with an output source current of i_s. Fig. 3 also gives the simple diagram for voltage or current reference (grid voltage v_g, grid current i_g, decoupling voltage v_{dp} and bus voltage v_{dc}). It is noticeable that for inverter mode, the grid current reference i_g^* should have a phase-shift angle for π rad to the grid voltage, as opposed to rectifier mode with no phase-shift angle for unity power factor, which causes a difference of $\pi/2$ rad for the decoupling voltage reference v_{dp}.

B. DC Bus Voltage Overshoot Calculation During Load Disturbance

For a traditional single-phase ac/dc converter, normally the large capacitor C_{bus} at dc side is used for both voltage ripple suppression and load disturbance rejection. However, in most power decoupling circuits, the bus capacitor is largely reduced or even removed [20], [21]. Even though it can realize the same voltage ripple suppression function with a much smaller bus capacitance in the steady state, there still exists a big problem of a certain overshoot/undershoot of v_{dc} during transient period. The following analysis examines the relationship between dc bus capacitance characteristics and corresponding dynamic response of a bidirectional power decoupling converter. Different step responses of v_{dc} during bidirectional switching under certain power level demonstrate the necessity of load disturbance rejection.

For most ac/dc converters, usually a double-loop control strategy is adopted to achieve the PFC function, which can be modeled shown in Fig. 4. The outer voltage controller is used to generate an inner current reference for the current controller. Since the bandwidth of inner current loop is much higher than that of outer voltage loop, it can be approximately considered as a proportional part in small-signal modeling [22].

By regarding the circuit in Fig. 4 as a two-port model, according to instantaneous-power-conservation theory, the relationship

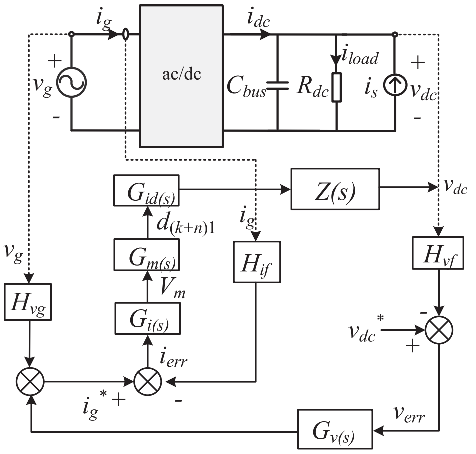


Fig. 4. Typical double-loop control model for single-phase ac/dc converter.

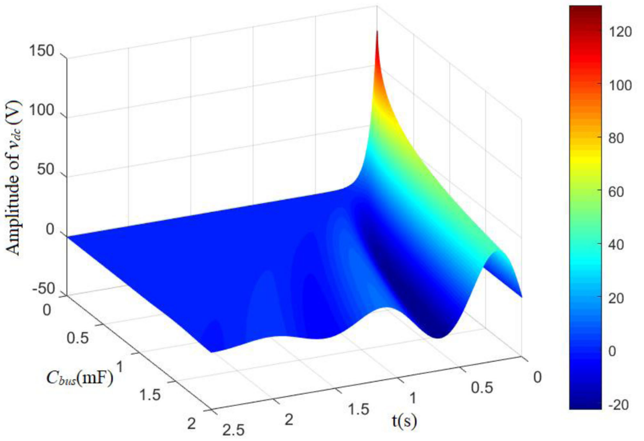


Fig. 5. Step responses of v_{dc} under dc source disturbance with different C_{bus}.

between ac port and dc port can be expressed as

$$v_g i_g = v_{\mathrm{dc}} i_{\mathrm{dc}} = v_{\mathrm{dc}}(i_{\mathrm{load}} + i_s) \tag{1}$$

Where i_{load} stands for resistive load current and *is* stands for dc source current. The value of i_{load} and *is* determines whether the circuit is working in rectifier or inverter mode. After applying the disturbance on i_g, i_{load}, v_{dc}, and *is*, (1) can be presented as

$$\begin{aligned} v_g(I_g + \hat{i}_g)V_g H_{vg} &= (V_{\mathrm{dc}} + \hat{v}_{\mathrm{dc}})(I_{\mathrm{load}} + \hat{i}_{\mathrm{load}}) \\ &\quad + (V_{\mathrm{dc}} + \hat{v}_{dc})(I_s + \hat{i}_s). \end{aligned} \tag{2}$$

From Fig. 4, (3) could be obtained as

$$\begin{cases} \hat{i}_g = -H_{if}\hat{v}_{\mathrm{dc}}\frac{k_{p\_v}s + k_{i\_v}}{s} \\ \hat{v}_{\mathrm{dc}} = \hat{i}_{\mathrm{load}}(R_{\mathrm{dc}} // \frac{1}{sC_{\mathrm{bus}}}). \end{cases} \tag{3}$$

Substituting (3) into (2), the small-signal transfer function of $G_{vs}(s)$ can be derived as

$$\begin{aligned} G_{vs}(s) &= \frac{\hat{v}_{\mathrm{dc}}}{\hat{i}_s}\Big|_{v_g=V_g} \\ &= -\frac{V_{\mathrm{dc}}}{V_{\mathrm{dc}}C_{\mathrm{bus}}s + \frac{H_{if}H_{vg}{V_g}^2 k_{i\_v}}{s} + H_{if}H_{vg}{V_g}^2 k_{p\_v} + I_{\mathrm{load}} + I_s + \frac{V_{\mathrm{dc}}}{R_{\mathrm{dc}}}}. \end{aligned} \tag{4}$$

$G_{vs}(s)$ represents the voltage variation of v_{dc} under the disturbance of *is*. It can be seen from (4) that the expression of $G_{vs}(s)$ is related to the size of dc bus capacitance, the proportional and integral (PI) factor and the current value of dc load and dc source. Take other parameters as constant, we only focus on the fact that a larger C_{bus} will decrease the overshoot voltage. Suppose the grid voltage is 220 V_{rms}, the dc bus voltage is 800 V and the injection power from *is* is 3 kW. Thus, step responses of dc bus voltage under dc source disturbance with different C_{bus} is shown in Fig. 5. The red zone represents an overshoot greater than 100 V, which is not acceptable and should be suppressed during bidirectional switching.

However, in the APD situation, we hope to replace the electrolytic capacitor (E-cap) by the long lifetime film capacitor serving as the dc bus capacitor [6]. Usually the value of film capacitor is far less than that of E-cap under the same voltage level. To realize film capacitor replacement more effectively and practically, reducing dc bus capacitance to under 100 μF is recommended, which means the overshoot of v_{dc} would end up to 120 V according to Fig. 5. The large overshoot of bus voltage will cause system instability impacts and bring damage to dc bus components. Therefore, it is of great significance to reduce or even eliminate the overshoot of the dc bus voltage.

C. Load Disturbance Rejection Strategy by Adopting Decoupling Cell

As mentioned above, during bidirectional switching, there is a certain overshoot/undershoot on v_{dc}. The voltage overshoot appears when switching from the rectifier to the inverter mode, and an undershoot occurs when the inverter mode switches back to the rectifier. According to (4), three ways to suppress the surge of v_{dc} are concluded as follows:

Strategy A: Increase the value of C_{bus}.
Strategy B: Increase PI value of outer voltage loop, or inner current feedback coefficient.
Strategy C: Absorb by other decoupling circuits.

Strategy A is simple and straightforward, but less effective than *Strategy* B and C. Additional capacitors clearly go against the original intention of power decoupling and will increase the cost of the whole system [7]. *Strategy* B pays attention to the controller parameter optimization and is also easy to achieve [23]–[25]. However, the piecewise constant function of PI will cause hysteresis, making it easier to vibrate at PI segment points. Also, the inner current feedback coefficient can be altered to increase the ac current so that the power grid can absorb the instantaneous power impact caused by part of switching. However, this method will affect the quality of grid current and may lead to the degradation of the power factor. *Strategy* C uses other circuits to absorb high-power impact, which would increase the circuit volume and cost. However, in this section, the decoupling cell of the LC branch is reused to perform the load disturbance rejection. It is controlled to reduce the voltage ripple in steady states and suppress the voltage overshoot under transient conditions. Also, no additional active switch or extra measurement circuit is added to realize the smooth mode switching, and there is no need to detect the power flow direction of the system.

For the proposed circuit in Fig. 3, there are four switching combinations (S_1&S_3, S_1&S_4,S_2&S_3, S_2&S_4). While S_2&S_4 or S_1&S_3 are ON, v_{ab} equals to 0. These two combinations can be mutually replaced when L_1 is charged. Then the turn-ON time of S_3 and S_4 determines the charge and discharge of the LC decoupling cell. Therefore, by controlling two switching combinations S_2&S_4 and S_1&S_3, no other switch is needed in this circuit, therefore realizing multiplex modulation.

Detailed steady-state modulation strategy has already been discussed in [15]. Since switches S_3 and S_4 are reused for decoupling, it means the sum of $d_{(k+n)1}$ and $d_{(k+n)2}$ will always be less than 1, and dc voltage utilization will be less than 0.5 to realize multiplex modulation. Here $d_{(k+n)1}$ and $d_{(k+n)2}$ are defined as two separate duty cycles of PFC and APD, which are settled as follows:

$$\begin{cases} d_{(k+n)1} = \frac{v_g}{v_{\mathrm{dc}}} \\ d_{(k+n)2} = \frac{v_{dp}}{v_{\mathrm{dc}}} \end{cases} \tag{5}$$

where *k* stands for the *k*th switching cycle, and *n* represents that the circuit have been through *n* switching cycles from the *k*th cycle to the $(k+n)$th cycle. However, different from [15], since there is no additional detection for decoupling voltage v_{dp}, the calculation of v_{dp} will be difficult to obtain in actual transient process of bidirectional switching. Besides, different power flow will end up with a difference of $\pi/2$ rad for the decoupling voltage reference. How to realize nondetection switching of APD and load disturbance rejection simultaneously causes challenges for the bus voltage controller, and will be solved in the following discussion.

To realize nondetection switching, steady-state modulation in [15] is no longer effective under transient situation, so it is necessary to impose another switching modulation strategy for the APD circuit. When starting bidirectional mode switching (assuming that the rectifier mode is switched to the inverter mode), the dc bus voltage will rise, which will be detected by the outer voltage controller. If v_{dc} is higher than a certain value, instead of implementing the duty cycle during steady state in (5), $d_{(k+n)2}$ of the decoupling circuit will be reassigned depending on the polarity of the grid voltage, which is shown in Fig. 6.

The duty cycle of the PFC during bidirectional switching is the same as the steady state, while the decoupling duty cycle is set to the maximum value in this switching cycle. In this case, S_3 in phase-B could constantly turn ON to its maximum extent during bidirectional switching, transferring the power surge energy from the bus voltage to the decoupling branch. The objective of this strategy is to achieve the maximum ripple suppression during bidirectional mode switching. To be more specific, operation of the bidirectional mode switching strategy for the APD converter can be divided into four modes depending on the polarity of the grid voltage and the grid current, as shown in Table I. When the grid voltage is in the positive half period ($v_g > 0$), duty ratios of the PFC and the APD are settled as

$$\begin{cases} d_{(k+n)1} = \frac{v_g}{v_{\mathrm{dc}}} \\ d_{(k+n)2} = 1 - \frac{v_g}{v_{\mathrm{dc}}}. \end{cases} \tag{6}$$

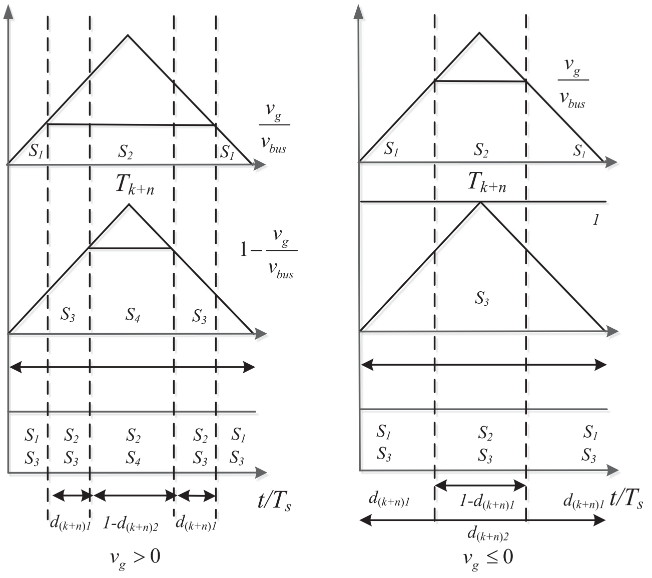


Fig. 6. Bidirectional mode switching modulation strategy during one switching period.

TABLE I
DIFFERENT WORKING MODES DURING BIDIRECTIONAL SWITCHING

	Mode 1	Mode 2	Mode 3	Mode 4
v_g	Positive	Negative	Positive	Negative
i_g	Positive	Negative	Negative	Positive
Bidirectional mode	Rectifier	Rectifier	Inverter	Inverter
PFC output u_{PFC}	$d_{(k+n)1}$	1- $d_{(k+n)1}$	$d_{(k+n)1}$	1- $d_{(k+n)1}$
APD output u_{APD}	1- $d_{(k+n)1}$	Fixed duty ratio 1	1- $d_{(k+n)1}$	Fixed duty ratio 1

When the grid voltage is in the negative half period ($v_g \leq 0$), duty ratios of the PFC and the APD are settled as

$$\begin{cases} d_{(k+n)1} = \frac{v_g}{v_{\mathrm{dc}}} \\ d_{(k+n)2} = 1. \end{cases} \tag{7}$$

Table I illustrates four different modes of operation during bidirectional switching. In mode 1 and mode 2, power is transferred from the grid side to the dc side (e.g., dc/dc converter, dc load, or dc source) and the converter is in the rectifier mode. In mode 3 and mode 4, power is transferred from the dc side to the grid side and the converter is working as an inverter. By following the duty ratios in (6) and (7), the decoupled branch plays an important role of energy buffer in bidirectional switching. The purpose of the LC branch buck circuit is to multiplex the two switches of phase-B, transfer the dc bus voltage impulse to the decoupling capacitor during bidirectional mode switching, and improve the dynamic step response. It is noteworthy that the sum of $d_{(k+n)1}$ and $d_{(k+n)2}$ should always be less than 1 to prevent over modulation, which explains the difference in the positive and negative half period. When $v_g \leq 0$, $v_g + v_{dp} < v_{\mathrm{dc}}$ is always true, therefore the $d_{(k+n)2}$ could be 1.

Fig. 7 illustrates the control diagrams for sensorless decoupling ripple voltage. It can be seen that the decoupling ripple voltage loop is a semi close-loop with negative v_{dc} feedback,

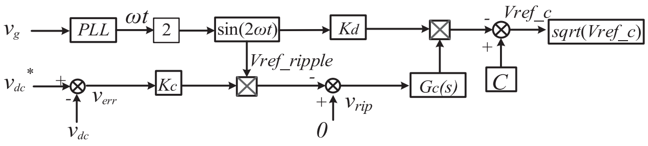


Fig. 7. Control diagram for sensorless decoupling ripple voltage control.

thus it is unnecessary to detect the circuit direction when the decoupling power is switched in two directions. Whether the circuit state is switched from charging direction to discharging or vice versa, the control can realize unified modulation, increase the dynamic response speed of the two-stage converter, and realize power decoupling and suppress load disturbance rejection. Meanwhile, the power factor of grid side can be controlled to regulate both active and reactive power flow.

III. STABILITY AND ROBUSTNESS ANALYSIS OF PROPOSED SENSORLESS DECOUPLING CONTROLLER

In the previous section, the dc bus voltage suppression strategy for smooth bidirectional switching has been given. In this section, the transient performance and the robustness of such strategy will be discussed in detail. Since the PFC and APD control are independent of each other, the decoupling topology can be equivalent to another separate bidirectional circuit to study its robust performance under external disturbances. The control target is to keep the dc bus voltage stable under external perturbations.

A. Sensorless Controller in System Modeling

As mentioned in [15], the key to achieve good performance of bidirectional ac/dc converter is accurate decoupling reference tracking. Due to the existence of different forms of disturbances, closed-loop reference-generation methods are suggested for more effective and accurate ripple-port reference generation [13]. Considering the circuit configuration illustrated in Fig. 3, the state-space equation of this APD circuit can be reviewed as a three-port system, which can be expressed as

$$\begin{bmatrix} L_1 & 0 & 0 \\ 0 & C_{\mathrm{bus}} & 0 \\ 0 & 0 & C_{dp} \end{bmatrix} \begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{\mathrm{dc}} \\ \dot{v}_{dp} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{\mathrm{dc}} \\ v_{dp} \end{bmatrix} + \begin{bmatrix} B_{11} & B_{13} \\ B_{21} & B_{23} \\ B_{31} & B_{33} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{\mathrm{dc}} \end{bmatrix}. \quad (8)$$

Here, the inductor current i_{L1}, instead of the grid side current i_g, is selected as the ac-port state variable for only i_{L1} is measured to acquire the input of inner current loop. Therefore, it is chosen as the ac port state variable for modeling convenience. Besides, the dynamics of the internal passive components are neglected.

In (8), the coefficient matrices of **A** and **B** represent the effect of the two separate control inputs of the PFC and the decoupling circuit and are not necessarily diagonal matrixes, which lead to a highly coupled and nonlinear system [13]. Such cross-coupling of the disturbance at the three-port and the two control inputs will introduce cross-interference for each control loop, and then deteriorate the reference tracking performance and system stability of the APD circuit.

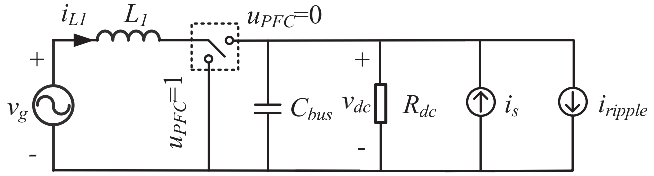


Fig. 8. Equivalent boost topology of an H-bridge converter.

Therefore, in this article where both the PFC control and the APD control are totally separated, the decoupling voltage reference varies directly from the load change instead of indirect methods by detecting two main circuit currents to get the third one. Only two voltage sensors (for measuring v_g and v_{dc}) and one current sensor (for measuring i_{L1}) are needed to complete the APD control. The three sensors are originally needed in the PFC controller, while the decoupling voltage v_{dp} is not a direct control variable and is determined by the dynamics of v_g and v_{dc}. According to Li *et al.* [13], v_{dp} is redundant and can be disregarded during the system modeling process, and (8) can be simplified as

$$\begin{bmatrix} L_1 & 0 \\ 0 & C_{\mathrm{bus}} \end{bmatrix} \begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{\mathrm{dc}} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{\mathrm{dc}} \\ v_{dp} \end{bmatrix} + \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{\mathrm{dc}} \end{bmatrix}. \quad (9)$$

In (9), only the dynamics at the ac port i_{L1} and that at the dc port v_{dc} are described. This model is more accurate for the three-port system [13], but only suitable for steady states. For such sensorless controller, it should be able to deal with certain parasitic parameters change and possess strong adaptation and robustness under normal or abnormal conditions. In order to analyze the stability and robustness during transient situations, a state-space model for bidirectional mode switching is built with additional variables of disturbance signals [26]–[28].

B. State-Space Model of Totem-Pole Bridgeless Boost PFC Converter With Additional Variables

Fig. 8 illustrates the simplified diagram of an H-bridge converter and the dynamic behavior during T_{ON} ($u_{\mathrm{PFC}} = 1$) and T_{OFF} ($u_{\mathrm{PFC}} = 0$), which is equivalent to a boost converter with a resister load R_{dc}, dc current source i_s, and ripple current i_{ripple}. Here, the u_{PFC} decides the PWM controller for S_1 and S_2 of phase-A. First consider it as a simple boost converter with no output disturbance and decoupling, we can obtain

$$\dot{x}(t) = [\mathbf{A_{on}} x(t) + \mathbf{B_{on}}]u(t) + [\mathbf{A_{off}} x(t) + \mathbf{B_{off}}][1 - u(t)] \quad (10)$$

where

$$\mathbf{A_{on}} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_{\mathrm{dc}} C_{\mathrm{bus}}} \end{bmatrix}, \mathbf{A_{off}} = \begin{bmatrix} 0 & -\frac{1}{L_1} \\ \frac{1}{C_{\mathrm{bus}}} & -\frac{1}{R_{\mathrm{dc}} C_{\mathrm{bus}}} \end{bmatrix}$$

$$\mathbf{B_{on}} = \mathbf{B_{off}} = \begin{bmatrix} \frac{V_g}{L_1} \\ 0 \end{bmatrix}, \dot{x}(t) = \begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{\mathrm{dc}} \end{bmatrix}. \quad (11)$$

The state vector components include i_{L1} and v_{dc}. These two variables are measurable and available for feedback purposes. The grid voltage v_g is considered as a constant value V_g representing the feed voltage. After applying the disturbance on *x*(*t*) and *d*(*t*), the system variables consist of two components:

$$\begin{cases} \langle x(t)\rangle|_{T_s} = X_e + \hat{x}_s \\ \langle d_{(k+n)1}(t)\rangle|_{T_s} = D_{e1} + \hat{d}_{k1} \end{cases} \tag{12}$$

where $X_e = [I_{L1}V_{\mathrm{dc}}]^T$ and D_{e1} are the equilibrium values, $\hat{x}_s = [\hat{i}_{L1}\hat{v}_{\mathrm{dc}}]^T$ and $\hat{d}_{k1}$ are the disturbance of $x(t)$ and $d_{(k+n)1}(t)$, respectively. Then, (10) can be decomposed into the steady-state and the disturbance components, that is

$$\begin{cases} \dot{\hat{x}}_s = \mathbf{A}\hat{x}_s + \mathbf{B}\hat{d}_{k1} + \mathbf{B}''\hat{x}_s\hat{d}_{k1} \\ \mathbf{A} = \mathbf{A_{off}} + (\mathbf{A_{on}} - \mathbf{A_{off}})D_{e1} \\ \mathbf{B} = (\mathbf{A_{on}} - \mathbf{A_{off}})X_e \\ \mathbf{B}'' = \mathbf{A_{on}} - \mathbf{A_{off}}. \end{cases} \tag{13}$$

By ignoring the second-order parts $\hat{x}_s\hat{d}_{s1}$, the small signal state-space model around the equilibrium is corresponding to

$$\dot{\hat{x}}_s = \mathbf{A}\hat{x}_s + \mathbf{B}\hat{d}_{k1} \tag{14}$$

where

$$\mathbf{A} = \begin{bmatrix} 0 & -\frac{1-D_{e1}}{L_1} \\ \frac{1-D_{e1}}{C_{\mathrm{bus}}} & -\frac{1}{R_{\mathrm{dc}}C_{\mathrm{bus}}} \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{V_g}{(1-D_{e1})L_1} \\ -\frac{V_g}{(1-D_{e1})^2 R_{\mathrm{dc}}C_{\mathrm{bus}}} \end{bmatrix}. \tag{15}$$

The steady-state operating point could be obtained as

$$I_{L1} = \frac{V_g}{(1-D_{e1})^2 R_{\mathrm{dc}}}, V_{\mathrm{dc}} = \frac{V_g}{1-D_{e1}}. \tag{16}$$

To achieve great transient performance in load step and smooth bidirectional switching between the rectifier and the inverter mode, the arbitrary exogenous disturbances are taken into consideration under different operation modes. As mentioned earlier, since PFC control and APD control are totally independent from each other. In this case, we only have to focus on the decoupling circuit and how much influence it would exert on the original H-bridge during transient process.

Since no additional decoupling detection is added, it is important to analyze its dynamic robustness to deal with disturbance uncertainty. In this section, we review the H-bridge converter dynamics and complement the model with two additional state variables in Fig. 7: 1) the input integral error of the output voltage v_{err}, and 2) the integral error of decoupling ripple voltage v_{rip} obtained from two nonlinear cross-product terms ($v_{\mathrm{dc}}{}^*-v_{\mathrm{dc}}$)sin(*2ωt*). To design the system compensators, plant transfer functions must be derived. The state-space representation in (14) is rewritten as

$$\begin{cases} \dot{\hat{x}}_s = \mathbf{A'_s}\hat{x}_s + \mathbf{B'_k}\hat{d}_{k1} + \mathbf{B'_s}\hat{i}_s + \mathbf{B'_r}\hat{i}_{\mathrm{ripple}} \\ \hat{z} = \mathbf{C_z}\hat{x}_s + \mathbf{D_z}\hat{d}_{k1} + \mathbf{D_s}\hat{i}_s + \mathbf{D_r}\hat{i}_{\mathrm{ripple}} \end{cases} \tag{17}$$

where

$$x_s = [i_{L1}(t)v_{\mathrm{dc}}(t)v_{\mathrm{err}}(t)v_{\mathrm{rip}}(t)]^T, z = [v_{\mathrm{dc}}(t)]. \tag{18}$$

The output *z* stands for the dc bus voltage v_{dc}, which represents the controlled output and should meet the control requirements. At the equilibrium state, v_{err} equals to zero. Therefore, V_{err} is constant. As is shown in Fig. 8, the disturbance vector has two sources. One is defined as an output current source i_s to characterize the output impedance of the converter and decide whether in the rectifier or inverter mode. Such output impedance influences the output voltage v_{dc} behavior by changing the output current i_s, which shows a great uncertainty, but can be restrained by another internal disturbance i_{ripple} achieved by the voltage suppression strategy discussed in Section II. i_{ripple} represents the dc bus ripple fluctuation and is modeled as the decoupling circuit ripple rejection opposite to the output disturbances i_s. In order to prove that the added decoupling cell is able to deal with ripple suppression and meet dynamic requirements, v_{err} and v_{rip} are substituted into state variable matrix x_s, yielding

$$\begin{cases} \hat{v}_{\mathrm{err}}(t) = V_{\mathrm{ref}} - \hat{v}_{\mathrm{dc}} = -\hat{v}_{\mathrm{dc}} \\ \hat{v}_{\mathrm{rip}}(t) = L_{dp}\hat{i}_{\mathrm{ripple}}(t) + D_{e2}\hat{v}_{\mathrm{dc}} + \frac{V_g}{(1-D_{e1})}\hat{d}_{k2}. \end{cases} \tag{19}$$

According to Fig. 6 in Section II, when adopting the energy buffer strategy in bidirectional switching, the duty cycles of the PFC and the APD has the following relationships:

$$\begin{cases} \langle d_{(k+n)2}(t)\rangle|_{T_s} = D_{e2} + \hat{d}_{k2} \\ D_{e2} = 1 - D_{e1} \\ \hat{d}_{k2} = 1 - \hat{d}_{k1} = -\hat{d}_{k1}. \end{cases} \tag{20}$$

Substituting (15) and (20) into (19), the coefficient matrices of the state-space representation in (17) could be obtained in (21). According to (21), the inner LC decoupling branch and the external dc source are regarded as two different disturbance signals, and the direction of decoupling disturbance i_{ripple} is proved to be opposite to dc source disturbance i_s. The state-space equations of dc bus voltage fluctuation v_{err} and decoupling voltage fluctuation v_{rip} are obtained, respectively. Next, to ensure good reference tracking and effective disturbance rejection, linear matrix inequality (LMI) technique for stability insurance is employed in the existing control solutions. The robustness of the system at the switching moment is analyzed by calculating the infinite norm H_∞ of transfer functions to describe transient characteristics [29]–[31]:

$$\mathbf{A'_s} = \begin{bmatrix} 0 & -\frac{1-D_{e1}}{L_1} & 0 & 0 \\ \frac{1-D_{e1}}{C_{\mathrm{bus}}} & -\frac{1}{R_{\mathrm{dc}}C_{\mathrm{bus}}} & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & D_{e2} & 0 & 0 \end{bmatrix}$$

$$\mathbf{B'_k} = \begin{bmatrix} \frac{V_g}{(1-D_{e1})L_1} \\ -\frac{V_g}{(1-D_{e1})^2 R_{\mathrm{dc}}C_{\mathrm{bus}}} \\ 0 \\ -\frac{V_g}{(1-D_{e1})} \end{bmatrix}, \mathbf{B'_s} = \begin{bmatrix} 0 \\ \frac{1}{C_{\mathrm{bus}}} \\ 0 \\ 0 \end{bmatrix}$$

$$\mathbf{B'_r} = \begin{bmatrix} 0 \\ \frac{-(1-D_{e1})^2}{C_{dp}} \\ 0 \\ L_{dp} \end{bmatrix}$$

$$\mathbf{C_z} = [0\,1\,0\,0]\,, \mathbf{D_z} = [0], \mathbf{D_s} = [0], \mathbf{D_r} = [0]. \tag{21}$$

C. H$_\infty$ *Control LMIs for Stability Insurance*

As previously mentioned, the decoupling controller could be regarded as a semi close-loop system, the robustness of which is better than that of closed-loop system in [17], [18]. In this section, the maximum impact value of dc bus voltage fluctuation affected by external disturbance will be calculated by establishing the LMI conditions and analyzing the H_∞ performance. Here, H_∞ defines the maximum gain from input finite energy to output energy, which can be equivalent to the maximum impact of external disturbance on dc bus voltage fluctuation. If the system does not diverge during exerted maximum power of switching, then the proposed dc bus voltage suppression strategy is proved to be effective and robust under other circumstances.

First, consider that the feedback controlled system in (17) with a linear feedback $d_{k1}(t) = \mathbf{K}x_s(t)$ is affected by the disturbance signal i_{ripple} and i_s, then (17) can be rewritten as

$$\begin{cases} \dot{\hat{x}}_s = (\mathbf{A'_s} + \mathbf{B'_k K})\hat{x}_s + \mathbf{B'_s}\hat{i}_s + \mathbf{B'_r}\hat{i}_{\text{ripple}} \\ \hat{z} = \mathbf{C_z}\hat{x}_s. \end{cases} \tag{22}$$

Compared with the general closed-loop system equation, there are three additional terms in (22), which are the disturbance terms including i_s and i_{ripple}, and the controllable output term *z*. For the disturbance terms, usually they are not measurable for the whole system, while the controllable output *z* is the dc bus voltage whose performance can be measured by two indexes–double-line frequency ripple voltage in steady state and voltage overshoot/undershoot in transient switching period. The decoupling topology could prove to be effective and robust in suppressing bus voltage fluctuation by calculating the maximum surge value of *z* affected by external disturbance. If whole system will not diverge within this maximum value range, then the proposed APD controller is proved to be possessed of load disturbance suppression ability. In other words, the problem of stabilizing the semi-closed-loop system and minimizing the influence of disturbance on the controllable output *z* can be equivalent to the problem of solving the H_∞ norm of the transfer function using the LMI approach.

In the description of generalized control plants, the performance index of v_{dc} can be expressed by the H_∞ norm of the closed-loop transfer function matrix. The H_∞ norm of a stable transfer function *f*(*s*) is the peak value of $|f\,(j\omega)|$, which could be used to evaluate the minimum attenuation level of an external disturbance. Considering the general transfer function *H*(*s*) from disturbances ω to outputs *z*, the H_∞ norm of this system is equal to

$$||H(s)||_\infty = \sup_{\omega(t)\neq 0} \frac{||z||_2}{||\omega||_2} \tag{23}$$

where $||\cdot||_\infty$ and$||\cdot||_2$ stand for the infinity and the Euclidian norms, respectively.

TABLE II
KEY PARAMETERS FOR ANALYSIS AND DESIGN

Symbol	Parameter	Value
P_o	Power	1 kW
V_{dc}	DC bus voltage	400 V
V_g	Grid voltage	110 V$_{\text{rms}}$
f_o	Line frequency	50 Hz
f_s	Switching frequency	50 kHz
L_g	Grid side inductor	165 μH
L_1	Converter side inductor	954 μH
C_1	Grid side filter capacitor	3.3 μF
C_{bus}	DC bus capacitor	120 μF
C_{dp}	Decoupling capacitor	90 μF
L_{dp}	Decoupling inductor	400 μH

In the previous section, we have established the transfer function relationship between the state-space parameter matrix and the transfer function matrix. Next, the fluctuation range of v_{dc} during system switching will be calculated and the system will be proved to be stable under certain limited disturbance. In order to impose restrictions on the controller gain vector $\mathbf{K}$ so that the exerted maximum energy gain of *z* is not larger a certain value γ_s, which is

$$||z||_2 < \gamma_s||\hat{i}_s||_2, \forall \hat{i}_s \in L_2. \tag{24}$$

Also, another gain value of the disturbance signal i_{ripple} exerted for voltage suppression is determined as

$$||y||_2 < \gamma_r||\hat{i}_{\text{ripple}}||_2, \forall \hat{i}_{\text{ripple}} \in L_2. \tag{25}$$

Then the preceding constraints (24) and (25) can be expressed by creating the following inequality equations in (26) and (27), respectively, based on the theorem adapted from [32]:

$$\begin{bmatrix} \mathbf{A'_s W} + \mathbf{W A'_s}^T + \mathbf{B'_k Y} + \mathbf{B'_k}^T \mathbf{Y}^T & \mathbf{B'_s} & \mathbf{W}^T \mathbf{C_z}^T \\ \mathbf{B'_s}^T & -\gamma_s I & 0 \\ \mathbf{C_z W} & 0 & -\gamma_s I \end{bmatrix} < 0 \tag{26}$$

$$\begin{bmatrix} \mathbf{A'_s W} + \mathbf{W A'_s}^T + \mathbf{B'_k Y} + \mathbf{B'_k}^T \mathbf{Y}^T & \mathbf{B'_r} & \mathbf{W}^T \mathbf{C_z}^T \\ \mathbf{B'_r}^T & -\gamma_r I & 0 \\ \mathbf{C_z W} & 0 & -\gamma_r I \end{bmatrix} < 0. \tag{27}$$

According to the Bounded Real Lemma, if and only if there is a symmetric definite positive matrix system **W** and a matrix ***Y*** holding the following inequality, system in (15) is stabilizable by linear feedback. We hope to impose restrictions on the controller gain vector **K** to make sure the gain of *z* is not larger than a certain value γ_s. Then instantiate the parameters corresponding to the experimental prototype, and use Matlab LMI Toolbox solving (26) and (27). The calculation procedure consists of finding the feedback gain **K** so that the current disturbance rejection is maximized, as well as minimizing the parameter γ_s being limited by the decoupling ripple gain γ_r. Given the parameters in Table II, the optimal state-feedback controller **K** can be obtained as

$$\mathbf{K} = [-0.0034 - 0.00145.73834385]. \tag{28}$$

Then a guaranteed H_∞ bound from disturbances to outputs of $\gamma_s = 2.74$, which corresponds to 11.28 dB, and $\gamma_r = 2.56$, which corresponds to 10.56 dB. These two disturbance gain values are

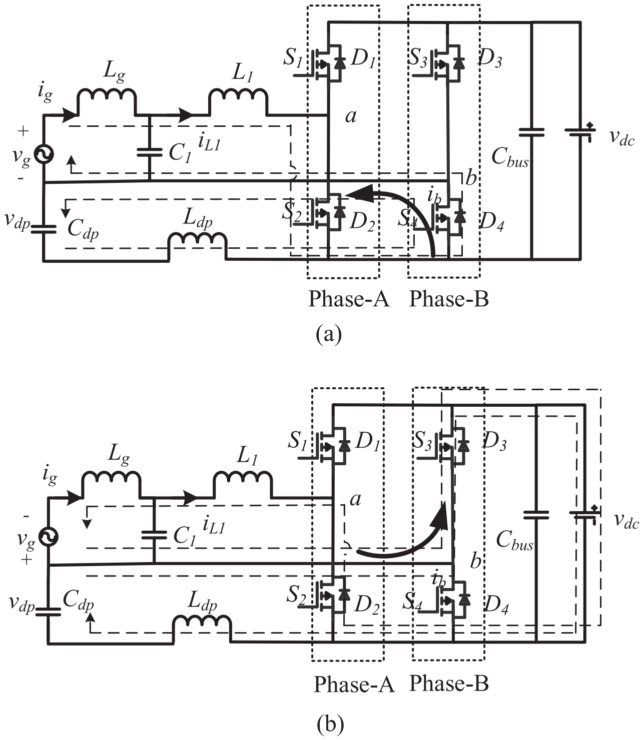


Fig. 9. Schematic diagram of grid current flow direction during positive and negative half cycle commutation for decoupling topology. (a) $i_b > 0$, $v_b = 0$ during D_{deadtime} and (b) $i_b \leqslant 0$, $v_b = V_{dc}$ during D_{deadtime}.

close to each other, which means these two opposite disturbance signals i_{ripple} and i_s can be offset. Therefore, the decoupling energy storage circuit has the enough suppression ability for maximum current rejection under bidirectional switching, which could prove the robustness and stability of the whole system. It also possesses good reference tracking capability dealing with parameter changes.

IV. PROPOSED DEAD-TIME COMPENSATION STRATEGY FOR SOLVING DECOUPLING VOLTAGE ASYMMETRY

A. Causes of Decoupling Voltage Asymmetry

Generally speaking, during the commutation process of H-bridge topology, it is necessary to reserve a period of dead time to prevent the upper and lower switches in one bridge arms turning ON at the same time [33]. Usually the proportion of dead-time is very small in the whole switching cycle, which will not affect the overall performance. However, for the single-phase power decoupling H-bridge topology shown in Fig. 9, the grid current of positive and negative half cycle of grid voltage will flow to different switches of the same bridge arm in dead time, which leads to the asymmetry of decoupling voltage in positive and negative half cycle, which occurs in [16]–[19]. Especially for no-detection situation, the decoupling voltage asymmetry will become more obvious with an increased power level. In this section, detailed analysis and solutions will be given to solve this asymmetry issues in order to improve the maximum ripple suppression ability as well as achieve minimum capacitance requirements in the power decoupling H-bridge topology.

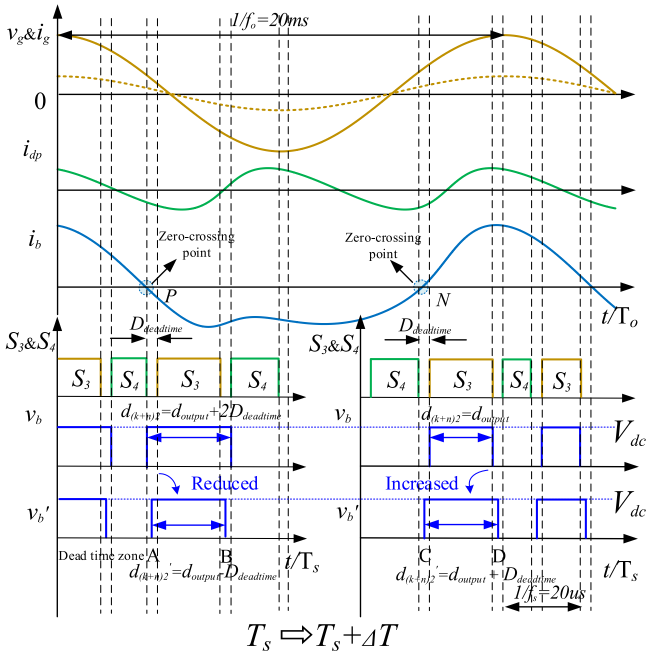


Fig. 10. Dead-time compensation strategy (DTCS) for decoupling voltage under rectifier mode.

Fig. 9 illustrates the grid current flow direction under positive and negative half cycle commutation of the decoupling topology. During positive half cycle of v_g, when switching from S_4 to S_3, there is a D_{deadtime} between those two switches. At this time, the inductor current i_b flows from phase-B to grid. Since i_b cannot change suddenly, neutral point voltage of phase-B v_b equals to 0 during diode freewheeling of S_4. During negative half cycle of v_g, still switching from S_4 to S_3, the inductor current i_b flows into phase-B, making v_b equal to v_{dc} during D_{deadtime}. Ideally, to achieve a good decoupling voltage, the modulation of v_{dp} should be consistent whether under the positive and negative half cycle. Under such circumstances, ever though the given duty ratio of decoupling voltage stays the same from controller, it would cause difference in actual circuit operation.

B. Dead-Time Compensation Strategy for Decoupling Voltage

To solve this problem, a DTCS for decoupling voltage is applied to the positive and negative half cycle decoupling voltage duty cycles of the grid voltage to ensure half cycle symmetry of the decoupling voltage and improve the decoupling performance, as is shown in Fig. 10. Assuming that the turn-ON duty cycle of S_3 is set to d_{output}. During D_{deadtime} when $i_b > 0$, $v_b = 0$, and the actual duty cycle of decoupling phase-B is the given duty cycle where $d_{(k\,+\,n)2} = d_{\text{output}}$; when $i_b \leq 0$, $v_b = V_{\text{dc}}$, and the actual decoupling duty cycle $d_{(k\,+\,n)2}$ is the sum of the given duty cycle and the double of dead-time D_{deadtime}. It can be seen from Fig. 10 that the different flow direction of i_b will cause difference in the actual decoupling duty cycle $d_{(k\,+\,n)2}$, which would lead to the decoupling voltage asymmetry phenomenon. Therefore, a simple and straightforward digital compensation is made for the actual decoupling duty cycle $d_{(k\,+\,n)2}$. That is, when i_b is changed from positive value to negative value (at *P* point), force d_{output} minus D_{deadtime}. Then during the whole period of $i_b > 0$, dead time zones of A and B are cut to half of D_{deadtime}. Correspondingly, when i_b is going through *N* point, force the force d_{output} plus D_{deadtime}, which makes dead-time zones of C and D under $i_b \leq 0$ increase to half of D_{deadtime}. With such compensation method, the decoupling voltage will stay symmetrical during one duty cycle.

After determining the compensation value for the decoupling voltage, next we need to determine when to compensate, which is corresponding to the zero crossing point of i_b. From Fig. 10, the current i_b flowing into and from phase-B is composed of grid current i_g and decoupling current i_{dp}, which can be deduced as follows. Assume that the grid voltage and current are sinusoidal as

$$\begin{cases} v_g(t) = \sqrt{2}V_g\cos(\omega t) \\ i_g(t) = \sqrt{2}I_g\cos(\omega t). \end{cases} \tag{29}$$

Then the ac side input power could be obtained by

$$p_g(t) = v_g(t)i_g(t) = V_gI_g + V_gI_g\cos(2\omega t). \tag{30}$$

Since the phase of decoupling voltage possesses a difference of $\pi/2$ rad between inverter mode and rectifier mode. Define the sign function *sgn*(p_g) in (31) to recognize the power flow as

$$sgn(p_g(t)) = \begin{cases} 1, & p_g(t) > 0 \\ 0, & p_g(t) = 0 \\ -1, & p_g(t) < 0. \end{cases} \tag{31}$$

Assume that the ripple power is totally absorbed by C_{dp}, the decoupling voltage $v_{dp}(t)$ is calculated in (32) shown at the bottom of this page, where the V_{offset} refers to the dc offset of decoupling voltage. Then i_b is the difference of i_g and the derivative of v_{dp}, which is obtained as

$$i_b(t) = i_g(t) - i_{dp}(t) = i_g(t) - C_{dp}\frac{dv_{dp}(t)}{dt}. \tag{33}$$

Substituting (32) into (33), i_b is expressed as (34) shown at the bottom of this page. By ignoring the LCL impedance and grid internal resistance, i_b can be simplified as (35) shown at the bottom of this page.

$$\begin{aligned} i_b(t) &\approx \sqrt{2}I_g\cos(\omega t) \\ &+ \frac{V_gI_g\sin(2\omega t) + \varphi}{\sqrt{\left|sgn(p_g(t))\frac{V_gI_g}{\omega C_{dp}}\cdot\cos(2\omega t+\varphi) + C\right|}}. \end{aligned} \tag{35}$$

Fig. 10 illustrates diagrams of v_g, i_g, i_{dp}, and i_b under the rectifier mode. However, in the actual circuit operation, it is too complex and impractical to calculate the zero crossing point of i_b for compensation. As i_{dp} is generally small, it can be assumed that i_g and i_b are in phase, so that the zero crossing point of i_g is just the zero crossing point of i_b and easier to capture. When the grid current is in the positive half period, assuming that the current and voltage are in the same direction, the duty cycle of decoupling voltage is assigned as

$$d_{(k+n)2}{}' = d_{\text{output}} + D_{\text{deadtime}}. \tag{36}$$

When the grid current is negative, the current and voltage are reversed, and the decoupling voltage duty cycle is set to

$$d_{(k+n)2}{}' = d_{\text{output}} - D_{\text{deadtime}}. \tag{37}$$

In conclusion, the duty cycle assignment of decoupling voltage is only used in the dead-time process when the upper and lower switches are commutating. At this time, the switches in the decoupling bridge arm should be in the turn-OFF state. The sum and difference of decoupling voltage compensation D_{deadtime} is selected to ensure that the PWM signals of upper and lower switches of PFC decoupling multiplexing bridge arm are exactly one PI calculation cycle different, and the reference value of decoupling voltage stays continuous.

C. Procedure to Design the LC Branch

As aforementioned, C_{dp} in the LC branch is used as the main energy storage component, while L_{dp} works as the energy transfer component between C_{dp} and the dc bus. In this APD circuit, the energy density of buffer inductor L_{dp} is far less than C_{dp}, so that the energy stored in L_{dp} could be neglected in the calculation. Once the ripple energy storage requirement is defined, the minimum required capacitance for C_{dp} is fixed by (38) shown at the bottom of the next page. Since the proposed method may introduce common mode noise into the circuit. In this case, there are two criteria for selecting L_{dp}: the first one is to eliminate common mode interference, and the second is the peak current limit which may affect the efficiency. To realize a satisfactory effect of the common mode noise attenuation, the

$$\begin{cases} v_{dp}(t) = \sqrt{\left|sgn(p_g(t))\frac{\sqrt{\left[\omega L_g{I_g}^2 + \omega C_1(V_g - R_gI_g)^2 - \omega^3C_1{L_g}^2I_g^2\right]^2 + \left[V_gI_g - 2\omega^2C_1L_gI_g(V_g - R_gI_g)\right]^2}}{\omega C_{dp}}\cdot\cos(2\omega t+\varphi) + {V_{\text{offset}}}^2\right|} \\ \varphi = \arctan\left(\frac{V_gI_g - 2\omega^2C_1L_gI_g(V_g - R_gI_g)}{\omega L_g{I_g}^2 + \omega C_1(V_g - R_gI_g)^2 - \omega^3C_1{L_g}^2I_g^2}\right) \end{cases} \tag{32}$$

$$\begin{aligned} i_b(t) &= \sqrt{2}I_g\cos(\omega t) \\ &+ \frac{\sqrt{\left[\omega L_g{I_g}^2 + \omega C_1(V_g - R_gI_g)^2 - \omega^3C_1{L_g}^2I_g^2\right]^2 + \left[V_gI_g - 2\omega^2C_1L_gI_g(V_g - R_gI_g)\right]^2}\cdot\sin(2\omega t+\varphi)}{\sqrt{\left|sgn(p_g(t))\frac{\sqrt{\left[\omega L_g{I_g}^2 + \omega C_1(V_g - R_gI_g)^2 - \omega^3C_1{L_g}^2I_g^2\right]^2 + \left[V_gI_g - 2\omega^2C_1L_gI_g(V_g - R_gI_g)\right]^2}}{\omega C_{dp}}\cdot\cos(2\omega t+\varphi) + {V_{\text{offset}}}^2\right|}} \end{aligned} \tag{34}$$

resonant frequency of the added LC decoupling branch, i.e., f_{dp}, is usually designed as 1/10–1/5 of switching frequency f_{sw}, then we can get L_{dp} by

$$f_{dp} = \frac{1}{2\pi\sqrt{L_{dp}C_{dp}}} = \lambda f_{\mathrm{sw}}, \ \left(\frac{1}{10} < \lambda < \frac{1}{5}\right). \tag{39}$$

The larger the inductance of L_{dp} is, the smaller the current ripple of LC branch is and the magnetic loss will certainly be reduced accordingly. Therefore, L_{dp} needs to be bigger than a certain value to make sure the peak current is lower than the requirement. However, the increase of volume and cost of such additional inductor should be considered and weighed. In this circuit, L_{dp} is selected as 400 μH in the system with the 50-kHz switching frequency and 10-A peak current rating considerations.

V. SIMULATIONS AND EXPERIMENTS

A. Simulation Verification

A simulation model of a single-phase bidirectional ac/dc converter consisting of the proposed DTCS is built with PLECS to verify the proposed methods, with the circuit configuration given in Fig. 3. The key parameters are listed in Table II. As can be seen in Table II, the proposed APD method uses a 120 μF main capacitor (C_{bus}) and a 90 μF decoupling capacitor (C_{dp}). Throughout the simulations and experiments, the basic PFC control, bidirectional switching strategy proposed in Section II and APD control without DTCS and with DTCS in Section IV have been adopted to a 1-kW ac/dc converter. Furthermore, different transient conditions are demonstrated and analyzed to prove the effectiveness of bidirectional switching method.

Fig. 11 shows the simulation results of steady state with the APD control under the rectifier mode (1 kW from ac to dc) and the inverter mode (-1 kW from dc to ac). It can be observed that the input ac current is sinusoidally shaped, in phase with line voltage under the rectifier mode in Fig. 11(a) and with a phase-shift angle of π rad under the rectifier mode in Fig. 11(b). The steady-state peak-to-peak dc voltage ripple stays below 4 V with a 120 μF C_{bus} at dc side and a 90 μF C_{dp} at decoupling side, which proves the proposed method could be used in both rectifier and inverter mode. For a traditional PFC converter, C_{bus} needs to be 1.2 mF under 400 V to achieve the same ripple suppression effect, which is about six times the total capacitance (210 μF) of the APD method. This means that the superiority of film capacitors under high voltage is fully embodied and can realize total E-Capless.

The comparison between Fig. 12(a) and (b) illustrates the transition from rectifier (1 kW) to inverter (-1 kW) mode with or without the APD voltage suppression proposed in Section II. Before $t = 1$ s, the system is working as a rectifier under 1 kW. At $t = 1$ s, the system is transferred from a rectifier to an inverter with a current source delivering 2 kW power at the dc side. Fig. 12(a) shows the traditional PFC converter without APD. It can be seen that peak-to-peak dc voltage ripple is up to 18 V with an overshoot voltage of 56 V with a total 210 μF C_{bus} at dc bus Also, there is a grid current surge at the switching transient. Then, by using proposed APD voltage suppression, better transient performance with no current surge has been achieved in Fig. 12(b), as well as a much smaller overshoot voltage of 12 V with a slight dc voltage ripple.

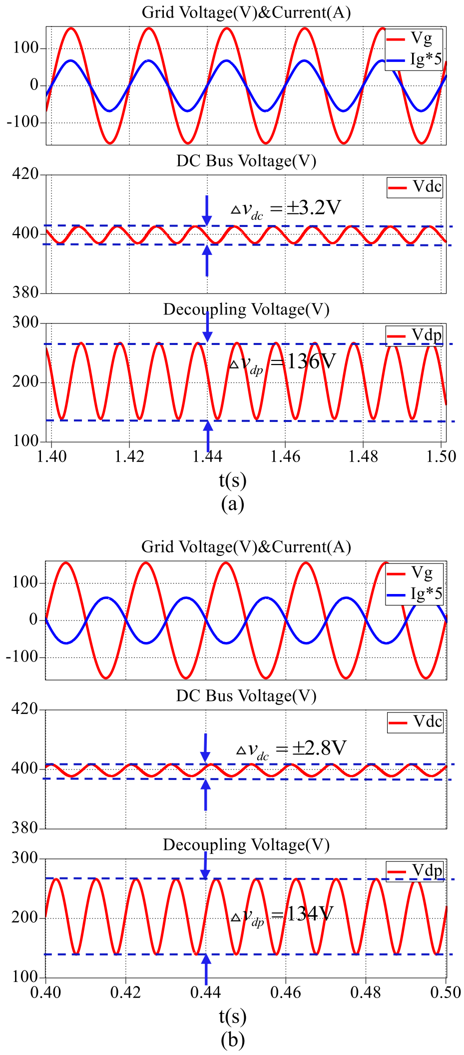


Fig. 11. Simulation of the steady-state waveforms with APD under rated power level. (a) In rectifier mode. (b) In inverter mode.

Fig. 13 illustrates the dynamic response of reverse flow change from inverter (-1 kW) to rectifier (1 kW) mode. Same as Fig. 12, the power flow signal given to the current source is shut down at $t = 1$ s, thus making it transfer from the inverter mode back to the rectifier mode. Such full-load operation mode switching

$$C_{dp} = \frac{\sqrt{\left[\omega L_g {I_g}^2 + \omega C_1 (V_g - R_g I_g)^2 - \omega^3 C_1 {L_g}^2 I_g^2\right]^2 + \left[V_g I_g - 2\omega^2 C_1 L_g I_g (V_g - R_g I_g)\right]^2}}{\omega({v_{dp}}^2 - {V_{\mathrm{offset}}}^2)} \cdot \cos(2\omega t + \phi) \tag{38}$$

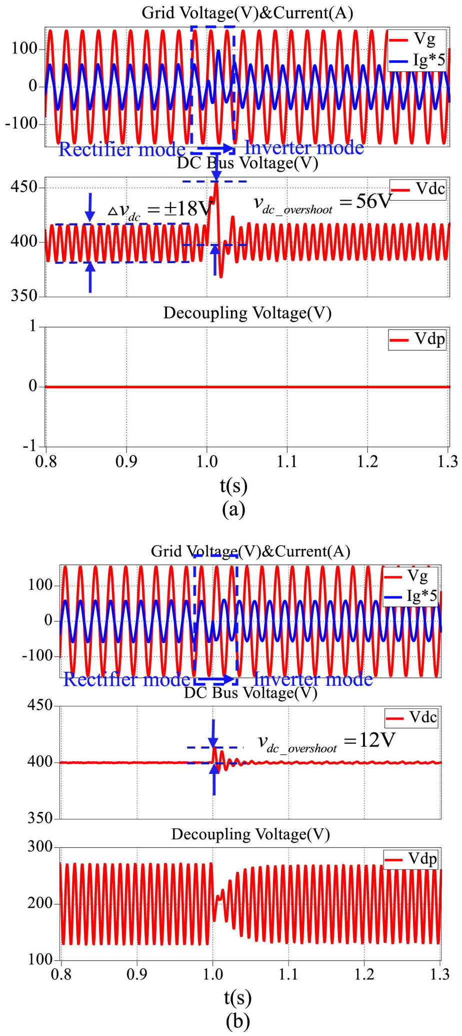


Fig. 12. Simulation of the bidirectional switching form rectifier (1 kW) to inverter (−1 kW) mode. (a) Without APD voltage suppression. (b) With APD voltage suppression.

will inevitably lead to a drop of the dc bus voltage with a maximum deviation of 50 V under traditional PFC converter without APD, shown in Fig. 13(a). Fig. 13(b) shows the result of current flow changing back to rectifier mode with the APD voltage suppression exerted. Obviously, the undershoot of dc voltage decreases from 50 to 12 V by adopting APD suppression control. Also, we can clearly see that the peak-to-peak dc voltage ripple is largely reduced. During bidirectional switching period, the whole system maintains a great THD, and the decoupling voltage follows the dc voltage closely with an undershoot to ensure the suppression effect. Both Figs. 12(b) and 13(b) prove that the proposed power decoupling method could deal with sudden flow change and works for both rectifier and inverter mode.

To further investigate the robustness of the proposed APD controller, in Fig. 14, a sudden grid voltage sag of 50% happened at $t = 1$ s, then the grid voltage returned to the rated value at $t = 1.33$ s. There will be a dc voltage drop and surge at $t = 1$ s and $t = 1.33$ s, respectively. From the comparison of

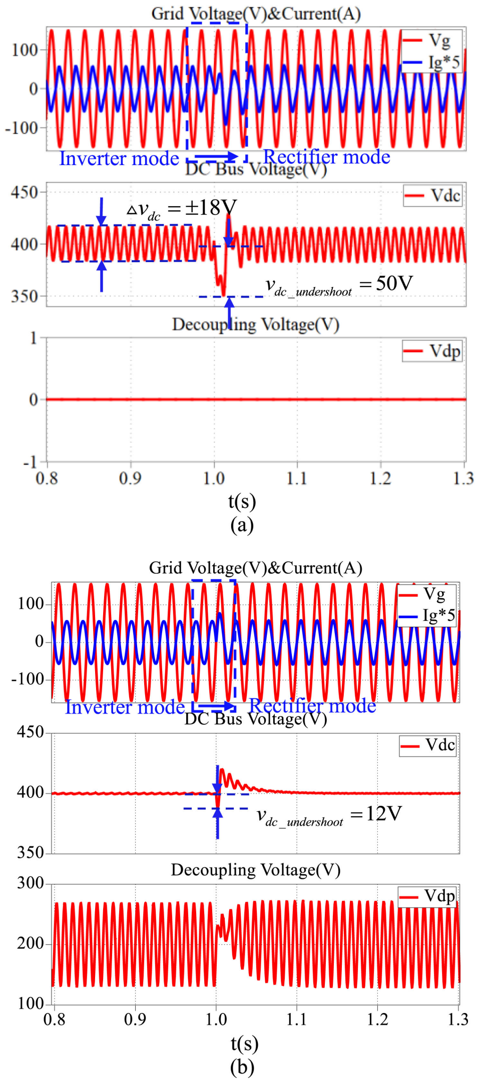


Fig. 13. Simulation of the bidirectional switching form inverter (−1 kW) to rectifier (1 kW) mode. (a) Without APD voltage suppression. (b) With APD voltage suppression.

Fig. 14(a) and (b), both the overshoot and undershoot of $v_{\rm dc}$ are reduced to one-forth by adding the APD suppression control. The steady state is reached within 0.1 s. This further illustrates the effectiveness of the proposed method for the dc voltage surge attenuation during transient situations.

B. Experimental Verification

Experimental tests of the single-phase bidirectional ac/dc converter with the APD control have been carried out using a 1-kVA prototype under different transient conditions. The dc bus capacitance and the decoupling capacitance have been set to 120 and 90 μF (with in total seven 30 μF EPCOS film capacitors in parallel), which means the whole prototype has achieved E-Capless in this bidirectional ac/dc circuit.

The ac/dc system test setup is shown in Fig. 15, which includes a single-phase autotransformer, an ac/dc converter, and the parallel connection of a dc source and resistor $R_{\rm load}$

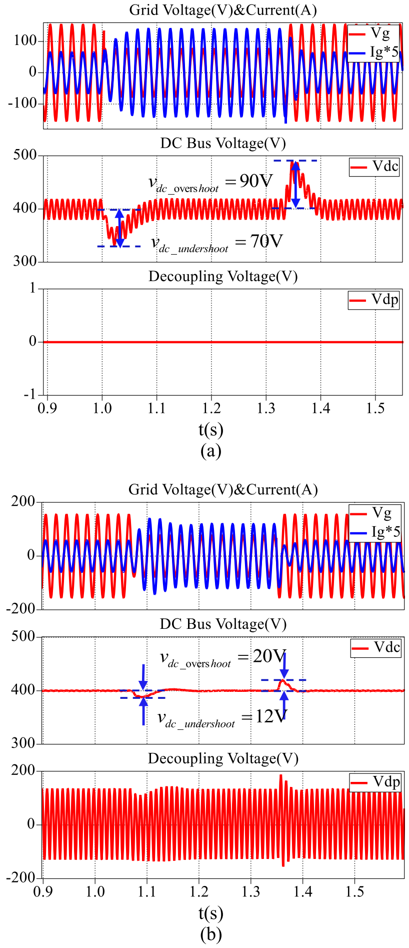


Fig. 14. Dynamic responses of a grid voltage sag of 50%. (a) Without APD voltage suppression control. (b) With APD voltage suppression control.

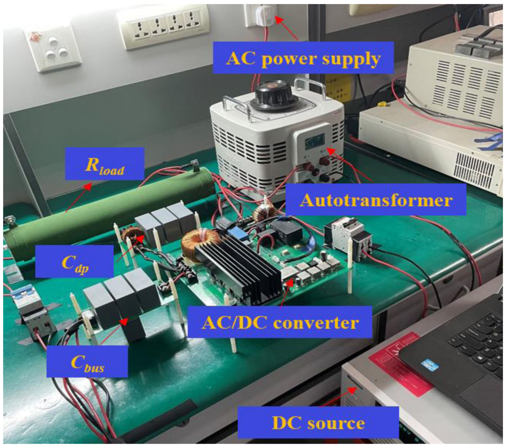


Fig. 15. Laboratory setup for experimental verification.

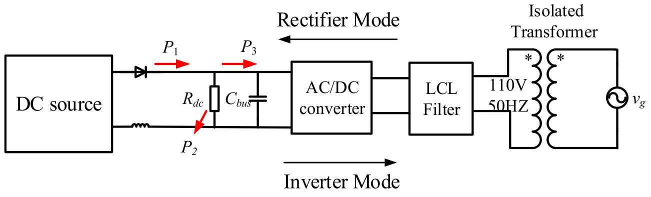


Fig. 16. Experimental structure of the bidirectional ac/dc circuit.

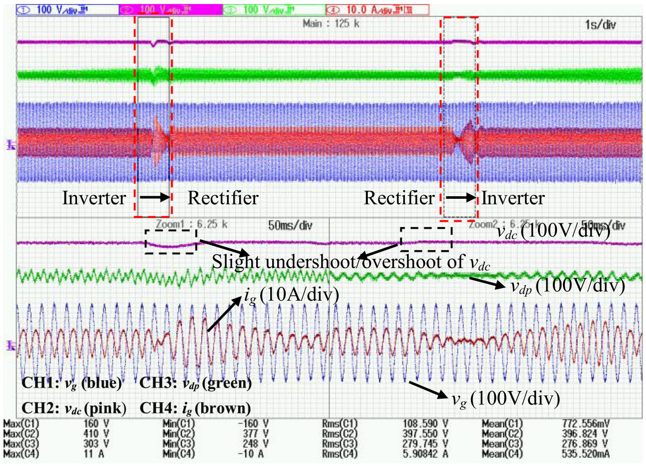


Fig. 17. Mode transition between inverter mode and rectifier mode.

used to simulate a bidirectional dc/dc circuit since dc source is unidirectional. The dc source employs a Chroma 62150H-600S programmable dc power supply for power flow backward, while the input voltage is connected to the power grid through the autotransformer. Control of the bidirectional converter has been implemented with a DSP28335. All the waveforms are recorded by a YOKOGAWA four-channel isolated oscilloscope.

The experimental structure of the bidirectional ac/dc circuit is illustrated in Fig. 16. Suppose that the injected power of dc source is P_1, the absorbed power of R_{dc} is P_2, and the grid-connected power through bidirectional ac/dc circuit is P_3. When the line loss is ignored, the power relationship in Fig. R1 is expressed as $P_1 = P_2 + P_3$. When the dc source is not working, thus $P_2 = -P_3$, the power grid transfers energy to R_{dc} through the bidirectional ac/dc circuit, then the converter works in the rectifier mode. When the dc source outputs a certain power to the dc bus side, set $P_1 = 2P_2$, then there will be $P_2 = P_3$, where the dc source transfers energy to the power grid through bidirectional ac/dc circuit.

Figs. 17–19 show the transient performances of the system during mode transition, step load change, and grid voltage sag cases. Beginning with Fig. 17, we set $R_{\mathrm{load}} = 300\ \Omega$, thus a 500-W loads are placed at the dc side. Then set dc source to input a 1-kW power, and the other 500-W power is dispatched to the grid. Therefore, by turning ON and OFF the dc source, the energy could achieve free flowing in either direction between the ac side and the dc side. As shown in Fig. 17, both the overshoot and undershoot of v_{dc} are slight during bidirectional switching with no current surge, even there is only a merely 120 μF capacitor on the dc side. The required capacitance is reduced more than five times but can still achieve good transient performance. The decoupling voltage is automatically adapted for dc bus voltage suppression. Besides, a seamless transition from the rectifier mode to the inverter mode is accomplished without additional decoupling sensors, which proves the theoretical robustness

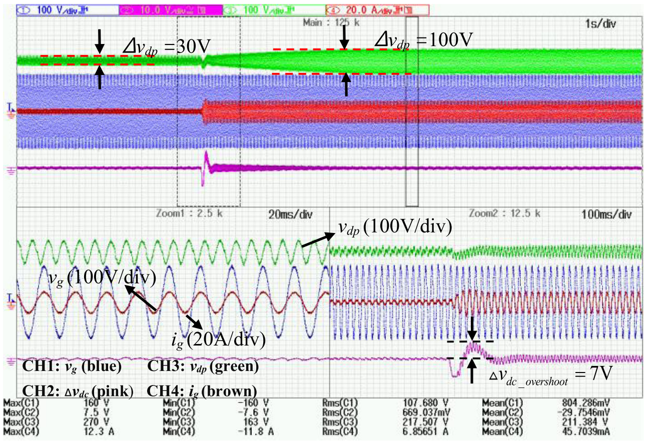


Fig. 18. Waveform of the load step with adaptive APD function.

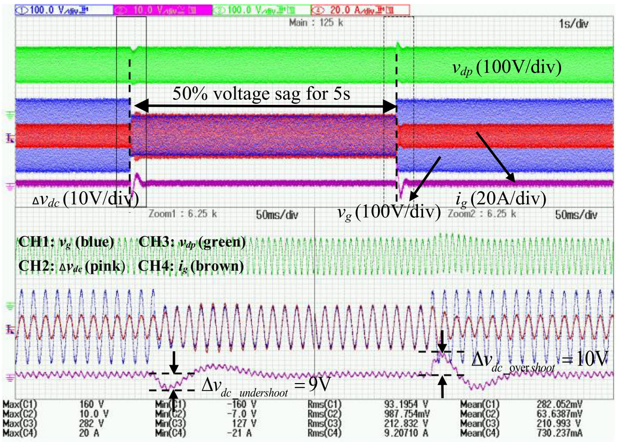
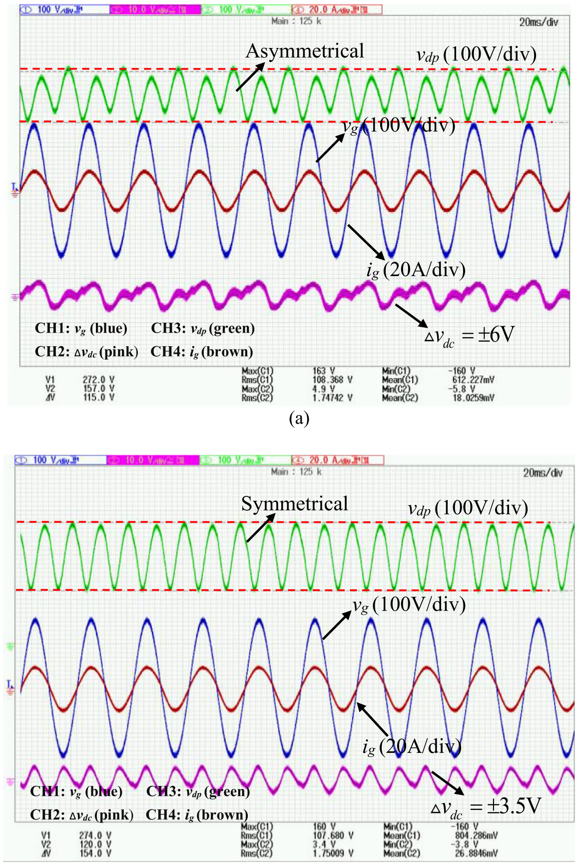


Fig. 19. Dynamic responses of a grid voltage sag of 40% for 5 s. (a) Zoom-in waveforms of v_g dropping from 110 to 55 V_{rms}. (b) Zoom-in waveforms of v_g rising back to 110 V_{rms}.



(a)

(b)

Fig. 20. Comparison of the steady-state waveforms under rectifier mode. (a) Without DTCS control. (b) With DTCS control.

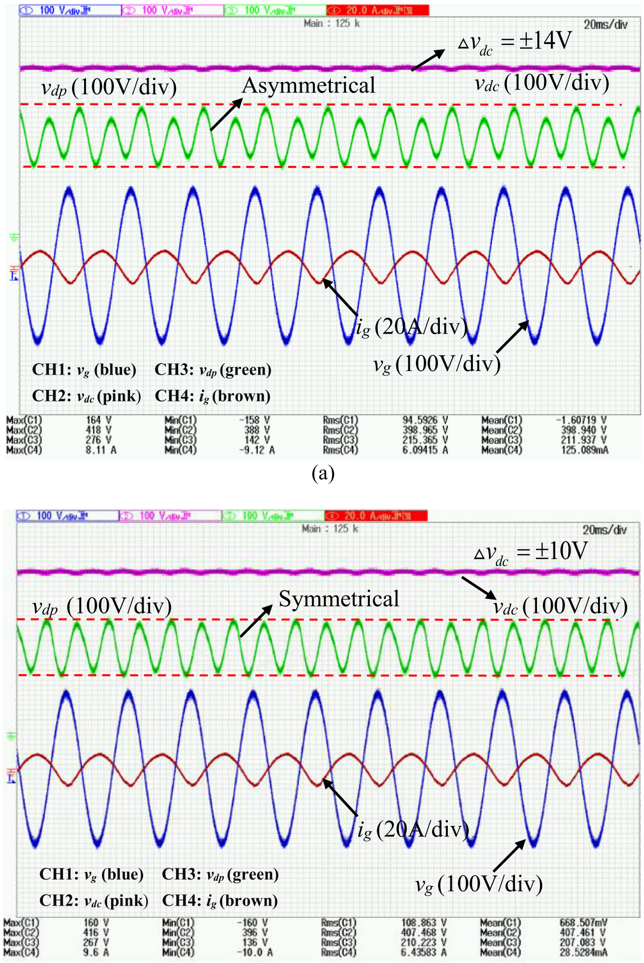
analysis in Section III are compared favorably with experimental results.

The transient performances of step load change with adaptive APD function is shown in Fig. 18, where the pink waveform Δv_{dc} stands for dc voltage ripple with v_{dc} filtering dc component. It can be seen vividly that when the amplitude of Δv_{dp} increases during transient response of load changing, Δv_{dc} decreases following the growth trend of Δv_{dp}, which demonstrates the proposed voltage sensorless controller can adaptively changed according to load variations. In addition, the operation of the rectifier with a voltage sag of 50% from 110 to 55 V_{rms} is shown in Fig. 19. Such voltage sag lasts for 5 s, then the grid voltage is recovered. The overshoot and undershoot of Δv_{dc} are both below 10 V and i_g quickly adjusts itself to track the grid voltage variation. The power factor and THD still remain satisfied condition during load step and voltage sag.

Figs. 20 and 21 illustrate the steady-state waveforms with or without the proposed DTCS control under the rectifier mode and the inverter mode, respectively. By comparing Fig. 20(a) and (b), it can be observed that when adding DTCS into the controller, the amplitude of Δv_{dp} has been fixed to be totally symmetrical, therefore ensuring a maximum decoupling ability. With the same capacitance, the dc voltage ripple Δv_{dc} has been further mitigated from 3% (12 V) of v_{dc} to less than 1.8% (7 V) in the proposed one. The measured THD of the input current under the rectifier mode is 3.56%, and the measured PF is 0.9987. The compensation effect is also reflected under inverter mode with symmetrical waveform of Δv_{dp} shown in Fig. 21(b). When under inverter mode, the load on the dc bus is no longer a pure resistive load as in the rectifier mode. The current i_g will be affected to a certain extent with an increasing amplitude of the double-line frequency ripple voltage on the dc bus, where in case of the inverter mode it will superimpose the inductive reactance on the dc source plus one additional diode. Therefore, the current THD of the inverter mode is worse than that in case of a rectifier. To solve this issue, we could add another grid-current feedforward control to eliminate the distortion by detecting the ripple on the bus voltage. Nevertheless, the effectiveness of the proposed method can be clearly validated by both the simulation and experimental results.

C. Analysis of Applications

This article aims to solve the problems of the dc bus voltage surge during bidirectional mode switching in single-phase



(a)

(b)

Fig. 21. Comparison of the steady-state waveforms under inverter mode. (a) Without DTCS control. (b) With DTCS control.

low-power (1–10 kW) converters used in energy storage dispatching, on-board charger of EVs, and bidirectional V2G applications. The proposed APD voltage suppression method targets to reduce the size of the dc bus capacitance, while maintaining great control performance during transient occasions, which is desired for the applications with requirements of high power density and high reliability. Moreover, since no additional sensor or active switch is added, the proposed control strategy in this article is more suitable for power-decoupling topologies with two or three phase legs, in which at least one phase leg is shared by both the main circuit and power-decoupling circuit, as well as high dc voltage applications where film capacitors of high-voltage rating are available instead of multiple series-connected E-caps.

VI. CONCLUSION

This article extends the study of the concept proposed in [15], in which a voltage-sensorless controller with self-adaptive power decoupling function is used to reduce the dc bus capacitance. By multiusing the decoupling cell, such APD controller has been improved for smooth bidirectional mode switching and symmetrical decoupling voltage compensation. The whole system modeling and stability analysis have been presented. Compared to [15], this article has the following distinctive discussions:

1) Wang *et al.* [15] gives the single-direction steady-state analysis of the proposed decoupling controller only, while this article explores bidirectionality, gives both back and forth power flow analysis and proposes a novel transient modulation strategy during bidirectional switching.
2) The vulnerability of the single-phase ac/dc system under greatly reduced E-caps situation has been analyzed in this article to demonstrate the necessity for voltage suppression during transient performance. The relationship between dc bus port-capacitance characteristics and dynamic response has been discussed.
3) In [15], only phase-B is reused for decoupling energy transfer, while in this article the whole decoupling cell is multiused for dc bus voltage suppression without additional sensors for the decoupling circuit.
4) A dead-time compensation is proposed in this article to achieve a more accurate power decoupling voltage compared to [15], which could ensure the maximum ripple suppression ability as well as achieve minimum capacitance requirements.

A 1-kW, 110-V, and 50-Hz prototype ac/dc converter has been built to demonstrate the results. All E-caps in the prototype are replaced by film capacitors in the experiment, therefore realizing the extension of estimated lifetime. Both simulation and experiment results show that the whole system has strong robustness under transient conditions such as steep load changes or bidirectional mode switching. Moreover, steady-state waveforms under two-direction modes prove the effectiveness of the proposed DTCS. The proposed voltage-sensorless APD controller is possessed of stronger applicability and generality, which can deal with sudden power-flow change and works for both rectifier and inverter mode.

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REFERENCES

[1] K. Mozaffari, M. Amirabadi, and Y. Deshpande, "A single-phase inverter/rectifier topology with suppressed double-frequency ripple," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9282–9295, Nov. 2018.
[2] M. Pahlevani and P. Jain, "A fast DC-bus voltage controller for bidirectional single-phase AC/DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4536–4547, Aug. 2015.
[3] D. Das, N. Weise, K. Basu, R. Baranwal, and N. Mohan, "A bidirectional soft-switched DAB-based single-stage three-phase AC–DC converter for V2G application," *IEEE Trans. Transp. Electrific.*, vol. 5, no. 1, pp. 186–199, Mar. 2019.

[4] M. Pahlevani, S. Eren, J. M. Guerrero, and P. Jain, "A hybrid estimator for active/reactive power control of single-phase distributed generation systems with energy storage," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2919–2936, Apr. 2016.

[5] T. Wu, C. Kuo, L. Lin, and Y. Chen, "DC-bus voltage regulation for a DC distribution system with a single-phase bidirectional inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 210–220, Mar. 2016.

[6] H. Wang, H. S. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the DC-link capacitance in a capacitor-supported system," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1163–1175, Mar. 2014.

[7] L. Zhang and X. Ruan, "Control schemes for reducing second harmonic current in two-stage single-phase converter: An overview from DC-bus port-impedance characteristics," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10341–10358, Oct. 2019.

[8] H. Zhang, X. Li, B. Ge, and R. S. Balog, "Capacitance, dc voltage utilizaton, and current stress: Comparison of double-line frequency ripple power decoupling for single-phase systems," *IEEE Ind. Electron. Mag.*, vol. 11, no. 3, pp. 37–49, Sep. 2017.

[9] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

[10] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. de Rossiter Corrêa, "Low-frequency power decoupling in single-phase applications: A comprehensive overview," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2892–2912, Apr. 2017.

[11] M. A. Vitorino and M. B. de Rossiter Corrêa, "Compensation of DC link pulsation in single-phase static converters," in *Proc. XI Braz. Power Electron. Conf.*, 2011, pp. 753–760.

[12] H. Wu, S. Wong, C. K. Tse, and Q. Chen, "Control and modulation of bidirectional single-phase AC–DC three-phase-leg SPWM converters with active power decoupling and minimal storage capacitance," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4226–4240, Jun. 2016.

[13] S. Li, W. Qi, S. Tan, and S. Y. Hui, "Enhanced automatic-power-decoupling control method for single-phase AC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1816–1828, Feb. 2018.

[14] R. Chen, Y. Liu, and F. Z. Peng, "DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5499–5507, Oct. 2015.

[15] X. Wang, M. Chen, B. Li, and N. Chen, "Multifunction control strategy for single-phase AC/DC power conversion systems with voltage-sensorless power-decoupling function," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13602–13620, Dec. 2020.

[16] X. Wang, L. Jing, B. Li, N. Chen, M. Qiu, and M. Chen, "A multiplexing modulation strategy based on single-phase AC/DC converter with optimized E-Capless function," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 1–6.

[17] H. Sun, H. Wang, and W. Qi, "Automatic power decoupling controller of dependent power decoupling circuit for enhanced transient performance," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1820–1831, Mar. 2019.

[18] W. Ming, Q. Zhong, and X. Zhang, "A single-phase four-switch rectifier with significantly reduced capacitance," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1618–1632, Feb. 2016.

[19] X. Wang, L. Jing, B. Li, N. Chen, M. Qiu, and M. Chen, "An improved power-decoupling scheme with grid inductor phase-shift modification for single-phase converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 2067–2071.

[20] Y. Tang and F. Blaabjerg, "Power decoupling techniques for single-phase power electronics systems—An overview," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 2541–2548.

[21] X. Cao, Q. Zhong, and W. Ming, "Ripple eliminator to smooth DC-bus voltage and reduce the total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2224–2235, Apr. 2015.

[22] R. Zhang, S. Liu, B. Li, N. Zhao, G. Wang, and D. Xu, "Totem-pole bridgeless boost PFC converter based on GaN HEMT for air conditioning applications," in *Proc. 2nd IEEE Conf. Energy Internet Energy Syst. Integr.*, 2018, pp. 1–9.

[23] C. Shin and J. Lee, "An electrolytic capacitor-less bi-directional EV on-board charger using harmonic modulation technique," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5195–5203, Oct. 2014.

[24] S.-G. Kim, W.-H. Oh, and S.-M. Park, "Bidirectional power control strategy in single-phase CHFL converter with active power decoupling circuit," in *Proc. IEEE Veh. Power Propulsion Conf.*, 2019, pp. 1–6.

[25] F. Chen, R. Burgos, and D. Boroyevich, "A bidirectional high-efficiency transformerless converter with common-mode decoupling for the interconnection of AC and DC grids," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1317–1333, Feb. 2019.

[26] R. H. G. Tan and L. Y. H. Hoo, "DC-DC converter modeling and simulation using state space approach," in *Proc. IEEE Conf. Energy Convers.*, 2015, pp. 42–47.

[27] S. Li, W. Qi, S. Tan, and S. Y. Hui, "Integration of an active filter and a single-phase AC/DC converter with reduced capacitance requirement and component count," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4121–4137, Jun. 2016.

[28] W. Zhu, K. Zhou, and M. Cheng, "A bidirectional high-frequency-link single-phase inverter: Modulation, modeling, and control," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4049–4057, Aug. 2014.

[29] D. Mishra and S. Mandal, "Voltage regulation of DC-DC boost converter using H-infinity controller," in *Proc. Int. Symp. Devices, Circuits Syst.*, 2020, pp. 1–5.

[30] J. V. Inglés, P. Garcés, and R. Leyva, "Robust LMI control of a buck-boost converter with low ripple propagation," in *Proc. 20th Mediterranean Conf. Control Automat.*, 2012, pp. 1272–1277.

[31] P. Gahinet and P. Apkarian, "A linear matrix inequality approach to $H\infty$ control," *Int. J. Robust Nonlinear Control*, vol. 4, no. 4, pp. 421–448, 1994.

[32] C. Olalla, R. Leyva, A. El Aroudi, and I. Queinnec, "Robust LQR control for PWM converters: An LMI approach," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2548–2558, Jul. 2009.

[33] J. Yuan, J. Pan, W. Fei, B. Chen, and J. Jia, "An immune-algorithm-based dead-time elimination PWM control strategy in a single-phase inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3964–3975, Jul. 2015.

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