Control Design of a 99% Efficiency Transformerless EV Charger Providing Standardized Grid Services

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***Abstract*—A nonisolated DC charger is proposed for electric vehicle (EV) battery system. The leakage current can be reduced by the novel charging system without bulky transformer. A zero sequence voltage control method is developed to stabilize the common-mode voltage, thus, reduce the leakage current. The proposed fast charger includes two energy conversion stages: DC–DC converter for battery side control; DC–AC converter for grid interface and common-mode voltage control. The parameters of the system with the *LCL* filter are analyzed and optimized for a better performance of grid interface. Grid service functions are designed for the EV charger to provide grid-voltage/frequency compensations. High power (22 kW) and high efficiency (>99%) are achieved with low-leakage current (<20 mA). The experiments are implemented to verify the proposed EV charger system.**

***Index Terms*—Common mode control, electric vehicle supply equipment, grid service, *LCL* filter, nonisolated EV charger.**

I. Introduction

ELECTRIC vehicle (EV) is playing an essential role in the vehicle market. The increasing demand of EV requires a proportionable capability of charging infrastructure. However, the cost and charging time are two main issues that continuously limit a broader application of EV. The two existing issues are all directly related to the charging system. Compared with the fuel station, the EV charging infrastructure is typically involved with charging circuits including the bulky transformer which means more cost. On the other hand, the charging time is longer with battery than refilling a fuel vehicle. Thus, the improvement of charging system, especially for off the board fast charger, is necessary for the development of EV application [1], [2].

The line-frequency transformer is typically installed in a fast charging system, which is bulky and expensive. The schematic of a charging system with line-frequency transformer is shown in Fig. 1, where the transformer is inserted between the grid and the filters of DC–AC converter. The line-frequency transformer accounts for a large portion of the volume and cost. A typical 30 kVA line-frequency transformer can cost more than $2000 and weigh more than 100 kg [3], [4]. Also, the power losses induced by the line-frequency transformer is another issue which will influence the efficiency of the charging system. The typical efficiency of EV three-phase line-frequency transformer is ranged from 97% to 98%. The isolation, however, is a critical component that relates to the regulation of grid-connected current quality, the attenuation of leakage current [5], [6]. Because there exists parasitic path between the chassis of the vehicle and the ground which is excited by the high-frequency common-mode voltage. If not insulated properly, the leakage current will flow through the parasitic path to threaten the human safety.

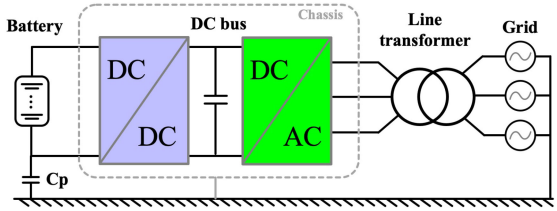

Fig. 1. Typical fast charger system with line-frequency transformer.

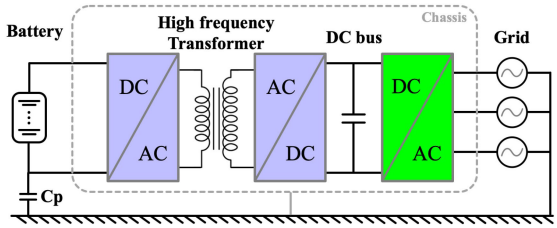

Fig. 2. Typical fast charger system with high-frequency transformer.

A typical solution to reduce the cost and volume of transformer while still maintaining the capability of isolation is to employ a high-frequency transformer instead of line frequency one [4], [7]. The high-frequency transformer charging system is shown in Fig. 2, where the transformer is inserted between the DC–AC converter and battery. This method is capable of blocking the leakage current parasitic paths by adding an extra isolated DC–DC converter [8]. The cost and volume will be significantly reduced compared with the line-frequency transformer system [9]. However, the power losses of the high-frequency transformer is greater than the line frequency one. The typical efficiency of an isolated DC–DC converter is in the range of 94% to 96% [10], [11]. Thus, the cost/volume and power losses are tradeoff for the high- or line-frequency transformer.

Manuscript received June 19, 2021; revised September 17, 2021; accepted October 26, 2021. Date of publication November 4, 2021; date of current version December 31, 2021. Recommended for publication by Associate Editor T. Mishima. *(Corresponding author: Matthias Preindl.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3124987.

Digital Object Identifier 10.1109/TPEL.2021.3124987

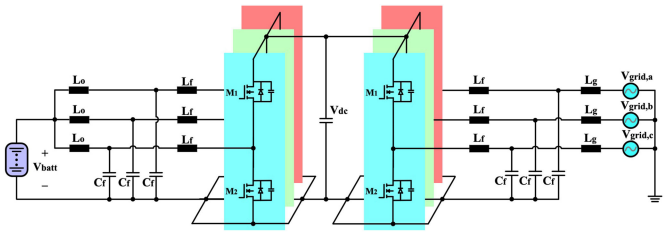


Fig. 3. Circuitry topology of the proposed nonisolated fast charger.

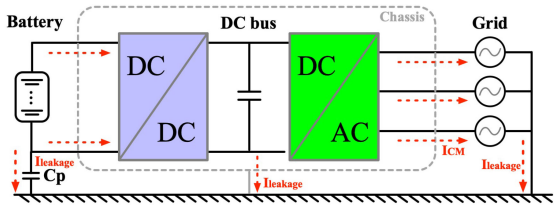


Fig. 4. Leakage current paths in a nonisolated charging system with parasitic capacitance.

The transformer-less energy conversion topologies have also been studied, especially in the photovoltaic systems [12], [13]. Several single-phase or three-phase transformer-less topologies have been developed [14], [15]. However, most of the topologies are implemented by adding extra switches or passive devices to modify the pulsewidth modulation (PWM) modulation method, which induce extra circuitry and control complexity. Zhang *et al.* [16]–[20] proposed several transformerless topologies of single-phase or three-phase inverters to attenuate the leakage current by introducing extra DC or AC bypass circuits. Guo *et al.* [13] and Chee *et al.* [21] developed the solutions by adding an extra switch phase leg to attenuate the common-mode voltage fluctuation. The extra devices will result in more cost, power losses, and modulation complexity. Ayano *et al.* [22] proposed a method to inject the zero-sequence voltage to attenuate the leakage current in motor drive application. This method effectively reduced the leakage current based on a modulation injection perspective rather than from control. Instead of redesigning the topology of the charger circuit by adding more devices, this article proposes a modification on the three phase DC–AC converter topology combined with a novel zero-sequence voltage control method to attenuate the leakage current. Compared with the traditional two-level three-phase inverter, the negative DC bus of the proposed converter is connected to the common point of AC three phase capacitors to create the zero sequence bypassing path. The topology of the proposed DC charger is shown in Fig. 3.

The rest of this article is organized as follows. In Section II, the circuitry model of the proposed EV DC charger is analyzed in detail. The common mode circuit with parasitic path is illustrated. Also the equivalent circuit model in $dq0$ reference frame is analyzed. In Section III, the proposed control method is introduced with zero-sequence voltage controller to stabilize the common-mode voltage. An active damping method of the *LCL* filter interfaced with the grid is designed for the control parameters. In Section IV, the smart functions of grid services and start up procedures are designed to compensate for the grid-voltage/frequency fluctuations. In Section V, the experimental results are shown to validate the proposed DC charger with high efficiency (>99%) high power (22 kW) and low-leakage current. Finally, Section VI concludes this article.

II. Circuitry Modeling

The proposed EV charger topology is shown in Fig. 3, which consists of DC–DC converter connected between the battery and DC bus, DC–AC converter connected between the grid and DC bus. On both side of the phase leg outputs, the filters are designed as *LCL* configurations. Different from the traditional two-level three-phase DC–AC converter, the common point of three-phase capacitors on the DC–AC side is connected to the DC bus negative terminal to create a bypassing path for zero-sequence voltage control. The proposed DC charger topology is nonisolated structure without transformer installed. The common-mode voltage is stabilized by the zero voltage controller to eliminate the leakage current. On DC–DC side, three phases of buck converters are connected in parallel to step up the battery voltage to DC bus and increase the charging power level.

A. Common-Mode Analysis

In a typical nonisolated three-phase grid-connected system, there exists a common-mode parasitic path between the grid neutral and DC ground due to the high-frequency common-mode voltage v_{cm} fluctuation and the equivalent parasitic capacitance C_p [23], [24]. The leakage current i_{leakage} will flow through the common mode path and can be derived as

$$i_{\text{leakage}} = C_p \frac{dv_{\text{cm}}}{dt}. \tag{1}$$

The leakage current is determined mainly by the high-frequency common-mode voltage and parasitic capacitance [25], [26]. The fluctuation of common-mode voltage is induced by the high switching frequency of the circuit and can be expressed as the mean value of three-phase switching legs output voltages v_a, v_b, v_c

$$v_{\text{cm}} = \frac{v_a + v_b + v_c}{3}. \tag{2}$$

The common-mode path of a nonisolated grid-connected converter is shown in Fig. 4, where the red dotted lines with arrows represent the leakage current. This leakage current is excited by the high-frequency fluctuation of common-mode voltage in the parasitic path. So, the leakage current is mainly determined by the following two factors: 1) rate of u_{cm}; 2) parasitic capacitance. First, according to (2), the mean value of three-phase switching legs output voltages is square waveforms with an amplitude of DC bus voltage at switching frequency level. Thus, the rate of change, du_{cm}/dt is high to amplify the leakage current. Second, the parasitic capacitance C_p is another factor to influence the leakage current. The value of C_p varies in the solar and EV charging systems. For a typical photovoltaic system, C_p is ranged between 10 and 100 nF. However, in an EV system, C_p is between 1 and 10 nF. For the safety consideration of the standard requirements, the leakage current is limited to be

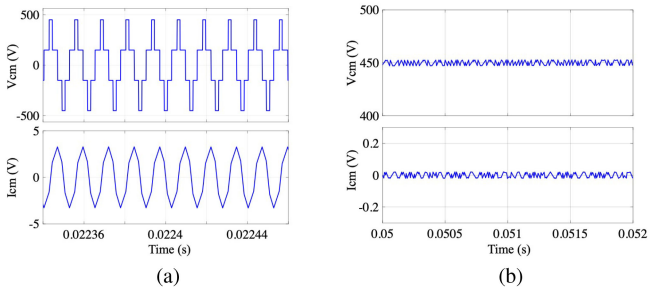


Fig. 5. Comparison of common-mode voltage and leakage current between traditional grid-connected converter and the proposed method. (a) Traditional converter. (b) Proposed method.

no more than 30 mA in an EV system by IEC 62955:2018 and IET Wiring Regulation 18th Edition (BS 7671:2018) Section 722.531.2.101.

To stabilize the common-mode voltage and attenuate the leakage current, the common point of DC–AC three-phase capacitors is connected to the DC bus negative terminal for bypassing the zero-sequence current as is shown in Fig. 3. The proposed zero-sequence voltage controller is aimed at controlling the common-mode voltage to be a constant value of half DC bus voltage, $u_{\rm DC}/2$, instead of a high-frequency fluctuating square waveform. To compare the common mode behavior of the traditional grid-connected converter and the proposed method, the $u_{\rm cm}$ and $i_{\rm leakage}$ are shown in Fig. 5(a) and (b) with 900 V DC bus and 10 nF parasitic capacitance. The common-mode voltage is fluctuating $\pm u_{\rm DC}/2$ with high frequency for the traditional converter and stabilized at $u_{\rm DC}/2$ for the proposed method. And the leakage current is reduced by a factor of 10–20.

B. DC–AC Converter Modeling

The DC–AC converter is directly interfaced with the grid. To maintain a constant common-mode voltage, the proposed control method is based on the $dq0$ coordinate system to leverage the zero-sequence voltage component in the proposed topology. Compared with the abc system, the active/reactive power and common-mode voltage can be controlled independently with d, q, and 0 sequence components in a $dq0$ system. The coordinate system model of the proposed DC–AC converter can be derived from abc reference frame.

1) abc System: The state-space equations in abc system are expressed as

$$\dot{i}_{L,abc} = \frac{1}{L_f}\mathrm{I}u_{x,abc} - \frac{1}{L_f}\mathrm{I}u_{c,abc} \tag{3a}$$

$$\dot{u}_{c,abc} = \frac{1}{C_f}\mathrm{I}i_{L,abc} - \frac{1}{C_f}\mathrm{I}i_{g,abc} \tag{3b}$$

$$\dot{i}_{g,abc} = \frac{1}{L_g}\mathrm{I}u_{c,abc} - \frac{1}{L_g}\mathrm{I}u_{g,abc} \tag{3c}$$

where L_f, C_f, and L_g are the switch side inductor, capacitor, and grid-side inductor, respectively, for the LCL filter. $i_{L,abc}$, $u_{c,abc}$, $i_{g,abc}$, and $u_{x,abc}$ are the switch side inductor current, capacitor voltage, grid-side current, and grid voltage, respectively. $\mathbf{I} \in \mathbb{R}^{3\times 3}$ is the identity matrix.

2) $dq0$ system: Since it is difficult to control the time-varying sinusoidal references in the abc system while convenient to calculate the active/reactive power and stabilize zero-sequence voltage in the $dq0$ system, the state-space model is transformed to $dq0$ reference frame for control purpose of the proposed method. Coordinate system transformation has been widely applied in the three-phase AC systems because the dq system can transfer the time-varying sinusoidal waveforms to equivalent constant DC values. For the implementation of control, the DC values are much easier to be controlled than AC values. However, the traditional methods mainly utilize the dq system without considering the zero-sequence. The proposed topology connects the common point of AC three-phase capacitors to the DC bus negative terminal, which permits to extract the zero-sequence from abc system to $dq0$ system and control the zero-sequence voltage to be half of DC bus voltage. Thus, the $u_{\rm cm}$ can be stabilized accordingly.

For the reference frame transformation with zero-sequence components, the abc system needs to be first transformed to $\alpha\beta0$ and then to $dq0$ system. From abc to $\alpha\beta0$, the Clarke transform is applied as

$$x_{\alpha\beta0} = \mathrm{T}x_{abc} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} x_{abc}. \tag{4}$$

In the $\alpha\beta0$ system, the signals are composed of two orthogonal sinusoidal AC waveforms in α and β frames and a zero-sequence component. A Park transform is implemented second to convert the stationary reference frame of $\alpha\beta0$ to the rotating $dq0$ system which is calculated as

$$x_{dq0} = \mathrm{P}(\theta)x_{\alpha\beta0} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} x_{\alpha\beta0}. \tag{5}$$

θ is the phase angle of the grid which is tracked with a phase-locked-loop (PLL) controller by measuring the grid voltage at the point of common coupling (PCC). Thus, the AC sinusoidal signals in abc are converted to DC values in a rotating $dq0$ frame with a time-varying angle of θ. Considering the control requirements to finally implement the duty cycles in abc format for the PWM modulation, the inverse Clarke and Park transformations are needed to convert the output of control signals from $dq0$ to abc

$$x_{abc} = \mathrm{T}^{-1}x_{\alpha\beta0} = \mathrm{T}^{-1}\mathrm{P}(\theta)^{-1}x_{dq0}. \tag{6}$$

Based on (4) and (5) of the coordinate system transformations, the state-space equations of (3) can be transformed from abc to $dq0$

$$\dot{i}_{L,dq0} = \frac{1}{L_f}\mathrm{I}u_{x,dq0} - \frac{1}{L_f}\mathrm{I}u_{c,dq0} - \omega\mathrm{G}i_{L,dq0} \tag{7a}$$

$$\dot{u}_{c,dq0} = \frac{1}{C_f}\mathrm{I}i_{L,dq0} - \frac{1}{C_f}\mathrm{I}i_{g,dq0} - \omega\mathrm{G}u_{c,dq0} \tag{7b}$$

$$\dot{i}_{g,dq0} = \frac{1}{L_g}\mathrm{I}u_{c,dq0} - \frac{1}{L_g}\mathrm{I}u_{g,dq0} - \omega\mathrm{G}i_{g,dq0} \tag{7c}$$

where ω is the angular velocity of the grid in rad/s. G is the matrix for the coupling terms resulted from the transformation

$$\mathrm{G} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}. \tag{8}$$

By leveraging the $dq0$ state-space equations and the connection of three-phase capacitors common point with DC bus negative terminal, the zero-sequence voltage can be controlled explicitly to stabilize the u_{cm}.

The typical state-space model can be expressed as

$$\dot{x_g}(t) = \mathrm{A_g} x_g(t) + \mathrm{B_g} u_g(t) + \mathrm{E_g} v_g(t) \tag{9a}$$

$$y_g(t) = \mathrm{C_g} x_g(t) \tag{9b}$$

where $x_g(t)$, $u_g(t)$, $y_g(t)$, and $v_g(t)$ are the state, input, output, and exogenous input vectors of the grid-side system. $\mathrm{A_g}$, $\mathrm{B_g}$, $\mathrm{C_g}$, and $\mathrm{E_g}$ are the state, input, output, and exogenous input matrices of the grid side, respectively. The vectors and matrices are expressed in detail as

$$\mathrm{A} = \begin{bmatrix} -\omega\mathrm{G} & -\mathrm{I}/L_f & 0 \\ \mathrm{I}/C_f & -\omega\mathrm{G} & \mathrm{I}/C_f \\ 0 & -\mathrm{I}/L_g & -\omega\mathrm{G} \end{bmatrix}, \mathrm{B} = \begin{bmatrix} \mathrm{I}/\mathbf{L_f} \\ 0 \\ 0 \end{bmatrix} \tag{10a}$$

$$\mathrm{C} = \begin{bmatrix} \mathrm{I}\ 0\ 0 \\ 0\ \mathrm{I}\ 0 \\ 0\ 0\ \mathrm{I} \end{bmatrix}, \mathrm{E} = \begin{bmatrix} 0 \\ 0 \\ -\mathrm{I}/L_f \end{bmatrix} \tag{10b}$$

$$x = \left[i_{L,dq0}^T\ u_{c,dq0}^T\ i_{g,dq0}^T \right]^T, u = \left[u_x \right], v = \left[u_{g,dq0} \right]. \tag{10c}$$

The equivalent circuits of the $dq0$ system for proposed topology of DC–AC side converter has been shown in Fig. 6.

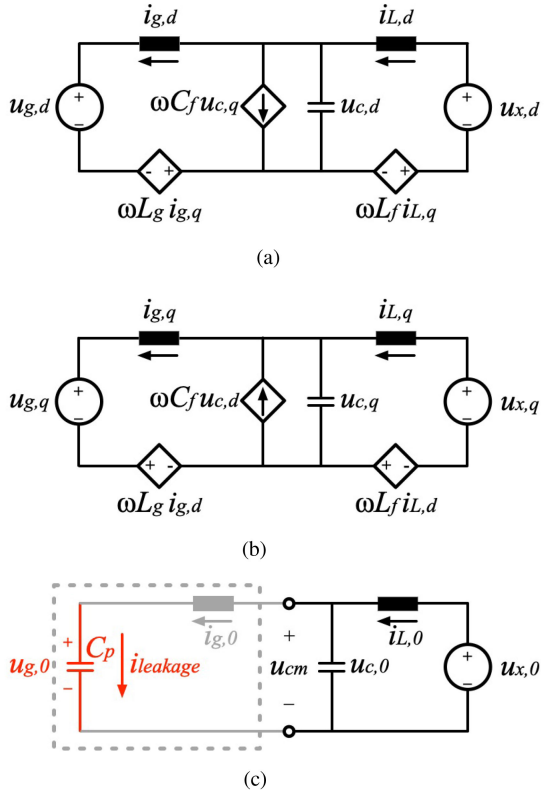


Fig. 6. $dq0$ equivalent circuits of the proposed topology on DC–AC side. (a) d-axis equivalent circuit. (b) q-axis equivalent circuit. (c) 0-axis equivalent circuit.

C. DC–DC Converter Modeling

The DC–DC side converter is designed for stepping up the battery voltage to the DC bus and controlling the battery voltage/current at different working modes. Specifically, during charging/discharging periods, the DC–DC side converter can work at constant current (CC) and constant voltage (CV) modes. Since the signals are all DC values and only the battery side voltage/inductor current are needed to be controlled, the control parameters are simpler than DC–AC side and only switch side inductor/capacitor are necessary to be considered for modeling. The state-space equations of battery side inductor current and capacitor voltage can be derived as

$$\dot{i}_{L,\mathrm{batt}} = N\frac{1}{L_f}u_{x,\mathrm{batt}} - N\frac{1}{L_f}u_{c,\mathrm{batt}} \tag{11a}$$

$$\dot{u}_{c,\mathrm{batt}} = \frac{1}{N}\frac{1}{C_f}i_{L,\mathrm{batt}} - \frac{1}{N}\frac{1}{C_f}i_{o,\mathrm{batt}} \tag{11b}$$

where N, $i_{L,\mathrm{batt}}$, $u_{x,\mathrm{batt}}$, $u_{c,\mathrm{batt}}$, and $i_{o,\mathrm{batt}}$ are the number of phases in parallel, switch leg output voltage, capacitor voltage, and battery current, respectively.

The typical state-space equations of battery side DC–DC converter per phase can be derived as

$$\dot{x_b}(t) = \mathrm{A_b} x_b(t) + \mathrm{B_b} u_b(t) + \mathrm{E_b} v_b(t) \tag{12a}$$

$$y_b(t) = \mathrm{C_b} x_b(t) \tag{12b}$$

where $x_b(t) = [i_{L,\mathrm{batt}}, u_{c,\mathrm{batt}}]$, $u_b(t) = [u_{x,\mathrm{batt}}]$, $y_b(t) = [i_{L,\mathrm{batt}}, u_{c,\mathrm{batt}}]$, and $v_b(t) = [i_{o,\mathrm{batt}}]$ are the state, input, output, and exogenous input vectors of the battery side system, respectively. $\mathrm{A_b} = [0, -N/L_f; 1/NC_f, 0]$, $\mathrm{B_b} = [N/L_f; 0]$, $\mathrm{C_b} = [1, 0; 0, 1]$, and $\mathrm{E_b} = [0; 1/NC_f]$ are the state, input, output, and exogenous input matrices of the battery side, respectively.

D. Filter

The *LCL* filters design for both DC–AC and DC–DC sides are analyzed in this section. For the DC–AC side filter, the main standard that needs to follow is the grid current waveform quality. The specification can be found from IEEE STD 519 to choose the value of grid-side inductor L_g for the attenuation grid current harmonics.

For the switch side inductor, the minimum inductance $L_{f,\mathrm{min}}$ can be determined by the maximum required current ripple $\Delta i_{L,\mathrm{max}}$ with the duty cycle of 0.5, d, switching frequency f_{sw}, and DC bus voltage V_{DC}

$$L_{f,\mathrm{min}} = \frac{d(1-d)V_{\mathrm{DC}}}{f_{\mathrm{sw}}\Delta i_L}. \tag{13}$$

With the desired grid/switch side inductance determined, the capacitance can be designed by the minimum output voltage ripple u_{ripple} and the resonant frequency of the *LCL* filter, ω_{res}.

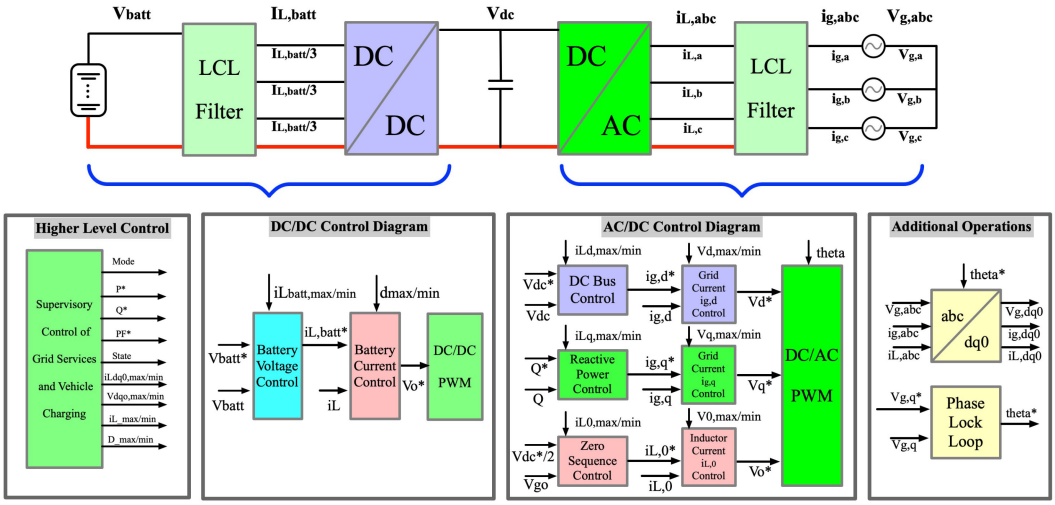


Fig. 7. Proposed control diagram of the nonisolated fast charger.

Specifically, the minimum capacitance is determined by the output voltage ripple which is expressed as

$$C_{f,\min} = \frac{1 - d_{\min}}{8 L_f u_{\text{ripple}}[\%] f_{\text{sw}}^2}. \tag{14}$$

Then, from the minimum available $C_{\min}$, the value of capacitance can be adjusted to determine the resonant frequency of the *LCL* filter system as is shown in

$$\omega_{\text{res}} = \sqrt{\frac{L_f + L_g}{L_f L_g C_f}}. \tag{15}$$

Based on (15), the capacitor values can be finally determined to choose a specific resonant frequency of the *LCL* filter. Then, with the help of ω_{res} and *LCL* parameters, the control bandwidth, ω_c, can be further designed to avoid the excitation. The control stability analysis considering the *LCL* filter and PI parameters interfaced with the grid are illustrated in the following section.

III. Control

The proposed control method of the DC fast charger includes DC–AC and DC–DC controlling sections and the PLL for coordinate transformations. The integrated control diagram is shown in Fig. 7. The zero-sequence voltage is derived from the transformed $dq0$ system and stabilized to attenuate the leakage current. The active and reactive power are controlled separately through d and q components, which can be flowing bidirectionally between the battery and the grid. And the higher level of commands can be sent to provide the grid services for grid-voltage/frequency compensation.

A. DC–AC Control

For the DC–AC side control to be interfaced with the grid, the abc three-phase sinusoidal waveforms are transformed to $dq0$ components [27], [28]. The active and reactive power are controlled in d, q reference frames, respectively [29], [30]. For the common-mode voltage, based on the proposed topology of connecting the three-phase common point with the DC bus negative terminal, the zero-sequence voltage can be controlled to half of DC bus to attenuate the leakage current. The controllers are illustrated as follows.

1) Phase-Locked Loop: The transformations between abc and $dq0$ needs the real-time phase angle information, θ, of the grid voltage [31]. An effective way can be implemented with a PI controller by controlling the q component of the grid voltage $v_{g,d}$ to be zero to derive the angular velocity, ω, of the phase angle. Then, the θ can be calculated with a period of 2π. And based on the active/reactive power calculation in

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{3}{2} \begin{bmatrix} u_{g,d} & u_{g,q} \\ u_{g,q} & -u_{g,d} \end{bmatrix} \begin{bmatrix} i_{g,d} \\ i_{g,q} \end{bmatrix} \tag{16}$$

the d-axis and q-axis represent the active and reactive power, respectively.

2) Active Power Control: The active power control includes the cascaded DC bus voltage controller and grid d current controller to deliver the active power between the DC–DC converter and the grid.

First, for the DC bus controller, the DC-link voltage between the DC–DC and DC–AC converters needs to be maintained to a high reference level to support the AC grid voltage and avoid the saturation of the AC duty cycles. During the charging/discharging modes of the battery to absorb and provide energy, the DC voltage can fluctuate and a PI controller is applied to stabilize the bus voltage and generate a $i_{g,d}^*$ current reference for the following grid d current controller.

Second, the grid d current PI controller will receive the current reference of $i_{g,d}^*$ from the DC bus controller to control the d component of the grid current for maintaining a desired active power to the PWM modulation.

3) Reactive Power Control: The reactive power control is designed to provide grid services for the compensation of grid-voltage fluctuation which consists of a cascaded Q controller and grid q current controller.

First, a Q PI controller is configured to control the desired reactive power as the reference of Q^*. The measurement of

reactive power to be compared with the Q^* reference can be derived from (16).

Second, the grid q current PI controller will receive the current reference of $i^*_{g,q}$ from the Q controller to control the q component of the grid current for maintaining a desired reactive power to the PWM modulation.

4) Zero Voltage Control: For the proposed nonisolated DC fast charger, zero-sequence voltage controller provides the capabilities to stabilize the common-mode voltage and attenuate the leakage current. With the topology modification in Fig. 3 to connect the common point of DC–AC three-phase capacitors and DC bus negative terminal, the zero-sequence voltage can be controlled to be half of DC bus voltage $u_{\rm DC}/2$. Based on (2) and Fig. 6(c), the parasitic capacitor C_p is in parallel with the zero-sequence grid voltage whose change of rate is proportional to the leakage current. Thus, to attenuate the leakage current, the zero-sequence grid voltage needs to be maintained constant. For the proposed control method, as is shown in Fig. 7, the zero-sequence control is composed of two cascaded controllers: zero-sequence voltage controller and zero-sequence inductor current controller.

First, the zero-sequence voltage controller is implemented by tracking the 0 component of grid voltage $u_{g,0}$ as half of DC bus $u_{\rm DC}/2$ to stabilize the common-mode voltage while fully utilize the DC-link voltage.

Second, the zero-sequence inductor current controller will receive the current reference of $i^*_{L,0}$ from the zero-sequence voltage controller to control the zero component of the inductor current and apply the output to the PWM modulation.

It is worthy to note that for the DC–AC converter control, the dq components of current and voltage are all measured at PCC, which are the grid current and grid voltage $i_{g,dq}$ and $v_{g,dq}$, respectively. The motivation is for providing an accurate calculation of active/reactive power to be interfaced with the grid and delivering precise grid services. For the zero-sequence control, the zero-sequence current is measured at the switch inductor side because according to the proposed topology of Fig. 3 and Fig. 6(c), the fluctuation of zero-sequence current on switch inductor side is mostly relevant to the fluctuation of common-mode voltage.

B. DC–DC Control

The DC–DC converter is directly connected between the battery and DC bus to step up the battery voltage to DC link and manage the active power during charging/discharging modes. Based on the proposed DC fast charger power level of 22 kW, three phases of switch legs are connected in parallel. To manage the power flow of the battery during charging/discharging periods, CC mode and CV mode control are achieved with two cascaded PI controllers: battery voltage and battery inductor current controller.

1) CC Mode Control: CC mode control is implemented to push high current from/to the battery by saturating the battery voltage controller. High/low-level voltage references are set during charging/discharging periods to saturate the voltage

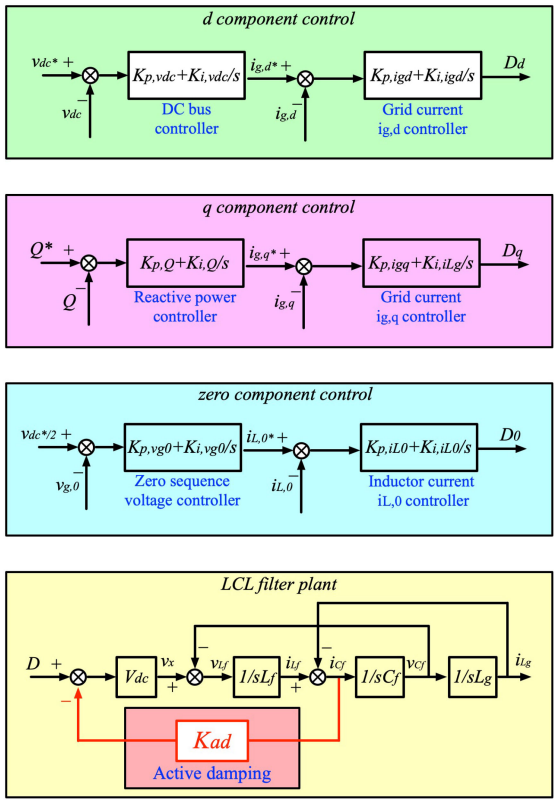


Fig. 8. Plant models of $dq0$ control and *LCL* filter with active damping method.

controller and generate a maximum/minimum output current references to the following battery current controller.

Specifically, during charging mode, the battery voltage reference $v_{\rm batt}$ is set to the high level and the battery voltage PI controller will be kept at saturation in CC mode to generate the maximum saturated output current reference, $i_{L,\rm batt,max}$ to the following CC controller to deliver CC charging to the battery.

During the discharging mode, the battery voltage reference $v_{\rm batt}$ is set to the low level and the CV PI controller will be kept at saturation in CC mode to generate the maximum saturated output current reference, $i_{L,\rm batt,max}$ to the following CC controller to deliver CC discharging back to the grid.

2) CV Mode Control: After the high-power charging/discharging periods of CC mode, the battery voltage will be increased/decreased to a high/low level, which are close to the battery voltage references, respectively, and the battery voltage controller will be away from the saturation mode. Thus, a CV mode control is taking over to finally achieve the targeted battery voltage.

C. Active Damping Control of LCL Filter

The grid side DC–AC control is more critical than DC–DC side because of the interface with grid AC signals and the harmonics resulted from the grid and high-frequency devices. The plant models of the DC–AC side control in $dq0$ frames and the *LCL* filter are derived in Fig. 8. For the *LCL* filter system, an active damping method is developed to feed the three-phase capacitor currents back to the duty cycle with an active damping

gain of K_{ad}. The active damping block is labeled in red in Fig. 8. The motivation of adding the active damping method is that the *LCL* system has the issue of unstability or marginal stability if there is no equivalent resistance in the loop [32], [33]. The transfer function from the input of duty cycle to the output of grid current without active/passive damping can be derived as

$$G_{LCL}(s) = \frac{I_g(s)}{D(s)} = \frac{V_{\text{DC}}}{L_f L_g C_f s^3 + (L_f + L_g)s}. \tag{17}$$

Since the denominator of the transfer function lack of the s^2 term, the system will be unstable or marginally stable due to the resonance which could influence the robustness of the control system. One option to improve the stability is by introducing the passive damping of resistors. However, the extra resistance will result in unnecessary power losses. Thus, another desired method is the active damping by feeding the capacitor current back to the input duty cycle as is shown in the red block of Fig. 8 with a gain of K_{ad}. The transfer function of the *LCL* filter with the active damping can be derived as

$$\begin{aligned} G_{\text{LCL,ad}}(s) &= \frac{I_g(s)}{D(s)} \\ &= \frac{V_{\text{DC}}}{L_f L_g C_f s^3 + V_{\text{DC}} K_{\text{ad}} L_g C_f s^2 + (L_f + L_g)s}. \end{aligned} \tag{18}$$

With the term of s^2 added to the denominator of the transfer function, the *LCL* system stability can be improved by manually adjusting the active capacitor current damping gain, K_{ad}. Doing so, the resonance can be attenuated based on the control gains/bandwidth, active damping gain, and the filter parameters. Equation (18) can be rewritten as the format of damped model of

$$G_{\text{LCL,ad}}(s) = \frac{V_{\text{DC}}}{L_g L_f C_f s(s^2 + 2\zeta\omega_{\text{res}} s + \omega_{\text{res}}^2)} \tag{19}$$

where ζ and ω_{res} represent the damping factor and resonant frequency, respectively. ω_{res} is determined by the *LCL* passive filter values and has been derived in (15). Thus, to compare (18) and (19) of the denominators, the active damping gain, K_{ad}, can be expressed by the *LCL* filter values and damping factor, ζ

$$K_{\text{ad}} = \frac{4\zeta}{V_{\text{DC}}} \sqrt{\frac{L_f(L_f + L_g)}{L_g C_f}}. \tag{20}$$

Since, for a typical second-order system, the damping factor of *LCL* is usually designed as 0.707, the active damping gain can be finally derived. Fig. 9 shows the bode diagrams of the *LCL* filter transfer function under different active damping factors and no active damping cases. The active damping method attenuates the resonance of the *LCL* system.

For the PI controllers, the control gains can be tuned based on the system stability performance of resonant issue. Among the controllers, the inner loop of grid current control is the most critical part because it determines the cut-off frequency, ω_c, which needs to be within the frequency range of $0.3\omega_{\text{res}}$ to avoid the control bandwidth being higher or even close to the resonance frequency. The grid current controller transfer function can be

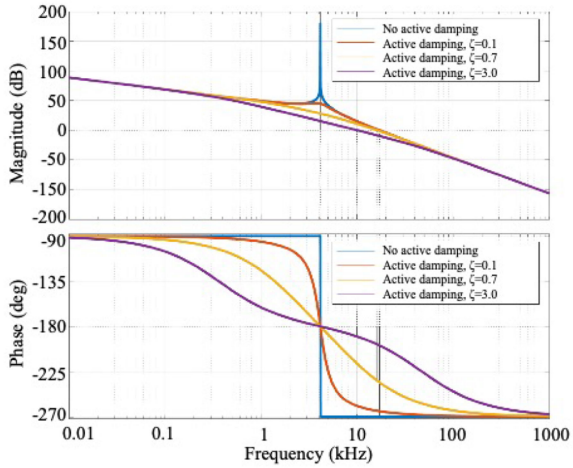


Fig. 9. Bode diagram of *LCL* filter transfer functions with different active damping factors and without active damping factor.

expressed as

$$G_{\text{ig}} = K_{p,\text{ig}} + \frac{K_{p,\text{ig}}}{\tau_c s} \tag{21}$$

where $K_{p,\text{ig}}$ and τ_c are the proportional gain and integral time constant, respectively. $K_{p,\text{ig}}$ is the key parameter that determines the control bandwidth. Since the cut-off frequency is designed to be $0.3\omega_{\text{res}}$, to keep away from the resonant frequency, $K_{p,\text{ig}}$ can be calculated as

$$K_{p,\text{ig}} = \frac{\omega_c(L_f + L_g)}{V_{\text{DC}}}. \tag{22}$$

And the integral time constant, τ, can be derived as $30/\omega_c$ to reduce the steady-state tracking error.

IV. Grid Service

The proposed DC fast charger is designed to have the capability of providing the grid service functions for the compensation of grid-voltage/frequency fluctuations. With the help of active/reactive power controllers shown in Fig. 7 on the d and q reference frames, the charger can respond to the voltage/frequency fluctuations at PCC to provide specific active/reactive power support. The grid services are following the standard of IEEE 1547. Specifically, the grid services mainly include six working modes:

1) constant reactive power (Const-Var) mode;
2) voltage-reactive power (Volt-Var) mode;
3) constant power factor (Const-PF) mode;
4) active–reactive power (P–Q) mode;
5) frequency-active power (Freq-Watt) mode;
6) voltage-active power (Volt-Watt) mode.

A. Constant Reactive Power Mode

In this Const-Var mode, the charger is commanded to provide the specific amount of reactive power injection/absorption capabilities with the grid. According to the grid service item, the charger needs to provide reactive power accounting for up to 44% of the rated apparent power. Fig. 10 shows the provided

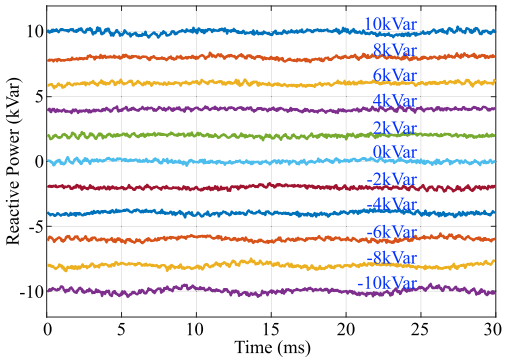


Fig. 10. Experimental reactive power ADC readings in Const-Var mode.

constant reactive power with the commands of references from 0 to 10 kVar injection/absorption with a step of 2 kVar.

B. Const-PF Mode

In the Const-PF mode, the charger is controlled to be operating at a specific power factor. The grid service standard requires the charger to have the capability of providing the power factor in which the reactive power accounts for up to 44% of rated apparent power. Based on the active/reactive power controller in Fig. 7, the desired active power and reactive power can be calculated in (16). The demand of power factor can be maintained by deriving the targeted reactive power from the given active power and power factor as is shown in

$$Q = P\sqrt{\frac{1-\mathrm{PF}^2}{\mathrm{PF}^2}}. \tag{23}$$

Then, the calculated reactive power can be sent to the reactive power controller as the reference to maintain the desired PF. Fig. 11 shows the experimentally captured analog-to-digital converter (ADC) power factor readings from 0.2 to 0.8.

C. Volt-Var Power Mode

In the Volt-Var mode, the charger is configured to provide the required reactive power according to a piecewise linear relation of grid voltage and reactive power. Specifically, when the grid voltage is lower than the rated value, the charger is required to inject reactive power to the grid. On the other hand, if the grid voltage is high than the rated voltage, the charger should absorb reactive power from the grid to compensate for the grid-voltage fluctuation. The Volt-Var relation is derived from the linear curve in Fig. 12(a) and the equations of

$$Q = 25\%S_N, \qquad V_g \le 90\%V_N \tag{24a}$$

$$Q = -\frac{2.5S_N}{V_N}v_g + 2.5S_N, \ 90\%V_N \le v_g \le 110\%V_N \tag{24b}$$

$$Q = -25\%S_N, \qquad V_g \ge 110\%V_N \tag{24c}$$

where V_N and S_N are the rated grid voltage and apparent power, respectively.

Fig. 12(b) shows six experimental testing points from 90% to 110% of the rated grid voltage and captures the corresponding

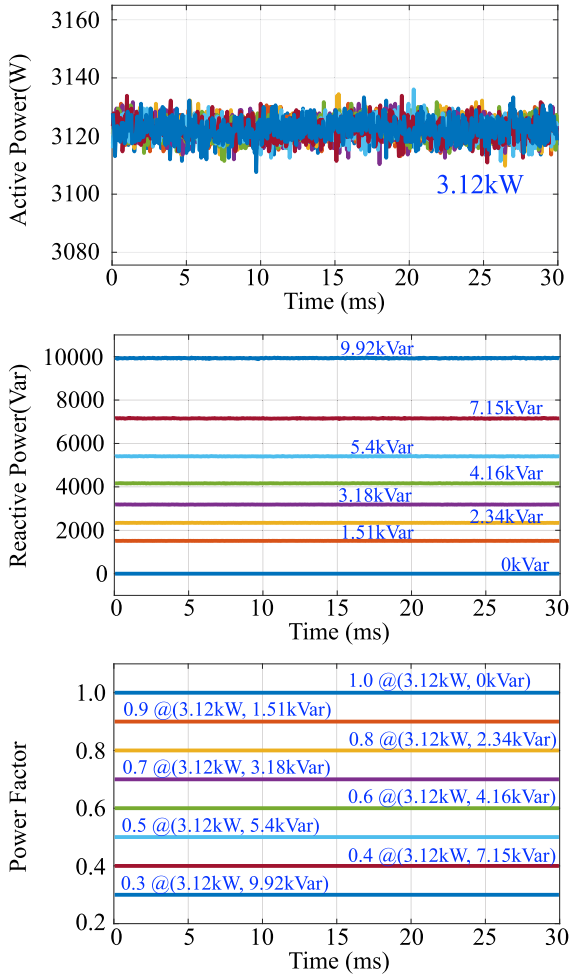


Fig. 11. Experimental power factor ADC readings in Const-PF mode.

reactive power in the Volt-Var mode. It can be seen that the testing points can accurately follow the piecewise linear volt-var curve.

D. P–Q Mode

In the P–Q mode, the reactive power is adjusted based on the output of active power according to a specific piecewise affine curve in Fig. 13(a). Specifically, if the discharging active power is larger than 100% of the rated value, a constant 25% amount of rated apparent power is required to be absorbed from the grid. On the other hand, if the active power output is less than 50% of the rated value, no reactive power is needed. And between 50% and 100% of rated active power, the reactive power should follow the linear curve of

$$Q = 0, \qquad P \le 50\%P_N \tag{25a}$$

$$Q = -\frac{Q_N}{2P_N}P + 25\%Q_N, \ 50\%P_N \le P \le 100\%P_N \tag{25b}$$

$$Q = -25\%S_N, \qquad V_g \ge 110\%V_N. \tag{25c}$$

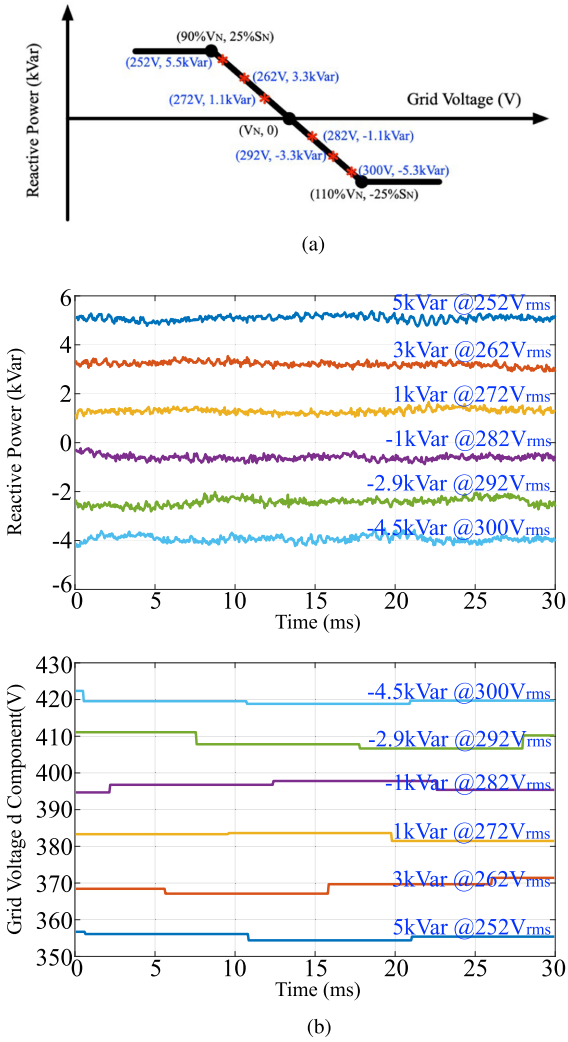


Fig. 12. Volt-Var mode results. (a) Corresponding grid voltage and reactive power curve. (b) Experimental reactive power and grid d voltage ADC readings.

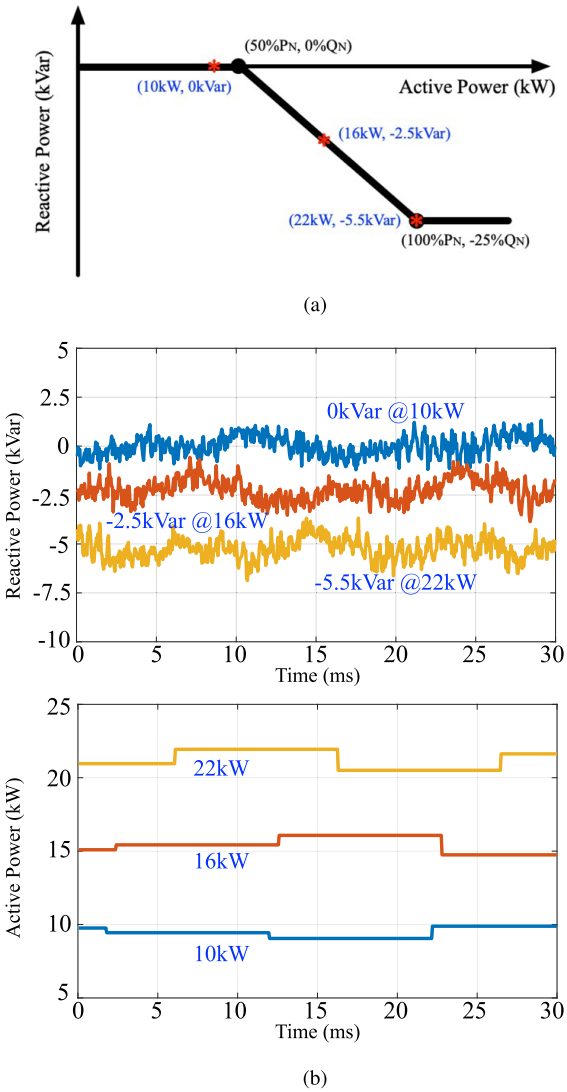


Fig. 13. P–Q mode results. (a) Corresponding active power and reactive power curve. (b) Experimental active power and reactive power ADC readings.

The corresponding active/reactive power data points are measured through ADC and plotted in Fig. 13(b), which conform to the linear curve of the requirement.

E. Freq-Watt Mode

The Freq-Watt mode is designed to compensate for the grid frequency oscillation with adjustable active power. Specifically, when the grid frequency is lower than the rated 60 Hz, the charger is expected to inject more active power to the grid in the discharging mode or absorb less in the charging mode. On the other hand, if the grid frequency is higher than 60 Hz, the charger should inject less active power to the grid in discharging mode or absorb more in the charging mode.

Similar with the Volt-Var mode, the Freq-Watt mode also needs to follow a piecewise linear relation of grid frequency and active power. The grid frequency can be measured from the PLL controller with the grid voltage angular velocity, ω, and divided by 2π. Then, the desired active power can be derived from the linear curve in Fig. 14(a) and the equations as follows:

$$\Delta P\% = \frac{(60 - db_{\mathrm{UF}}) - f}{60k_{\mathrm{UF}}},\ f \le 60 - db_{\mathrm{UF}} \tag{26a}$$

$$\Delta P\% = 0,\quad 60 - db_{\mathrm{UF}} \le f \le 60 + db_{\mathrm{OF}} \tag{26b}$$

$$\Delta P\% = \frac{(60 + db_{\mathrm{UF}}) - f}{60k_{\mathrm{UF}}},\ f \ge 60 + db_{\mathrm{OF}} \tag{26c}$$

where $\Delta P\%$, $db_{\mathrm{UF}}/db_{\mathrm{OF}}$, $k_{\mathrm{UF}}/k_{\mathrm{OF}}$ are the

And based on the DC–DC side control in Fig. 7, the upper and lower saturation limits of CV controller output, $i_{Lbatt,max/min}$, can be adjusted by the following:

$$i_{Lbatt,max/min} = \frac{P}{Nu_{batt}}. \tag{27}$$

Thus, the expected active power will be pushed to compensate the grid frequency fluctuation. A total of 21 testing points are captured in ADC and plotted in Fig. 14, which accurately follow the Freq-Watt curve.

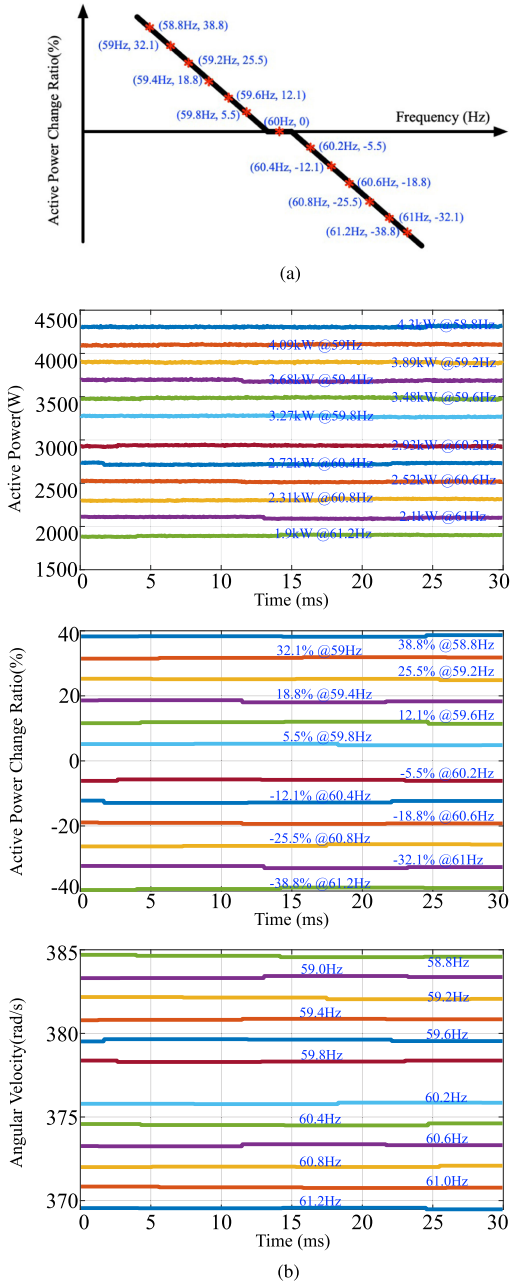


Fig. 14. Freq-Watt mode results. (a) Corresponding grid frequency and active power curve. (b) Experimental active power, changing ratio, and grid frequency ADC readings.

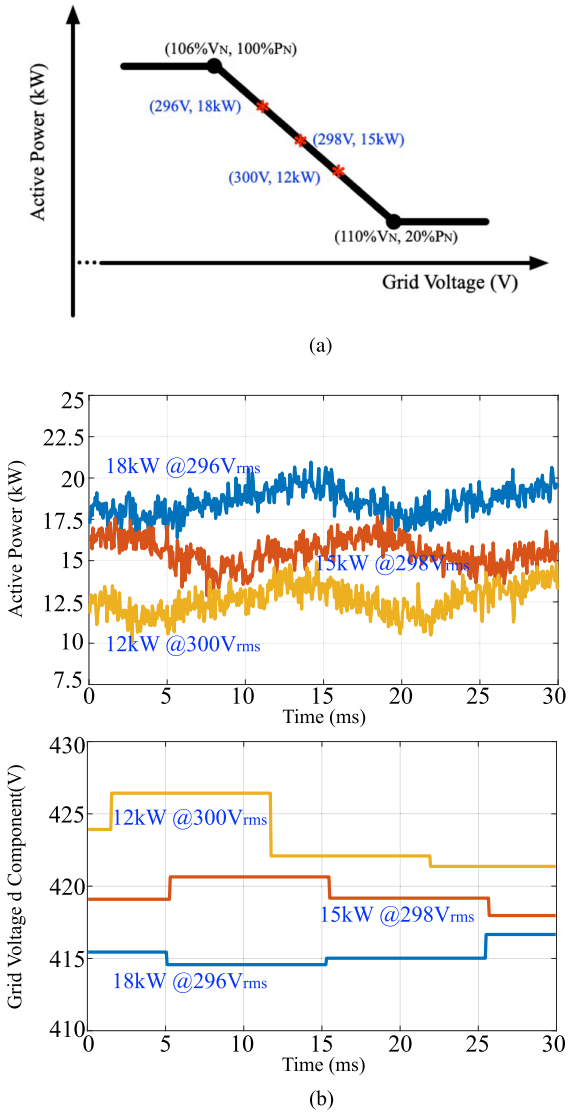


Fig. 15. Volt-Watt mode results.

F. Volt-Watt Mode

In the Volt-Watt mode, the active power is adjusted based on the variation of grid voltage according to a specific piecewise affine curve in Fig. 15(a). Specifically, when the grid voltage is lower than 106% of the rated value, the charger is allowed us to deliver 100% rated power. If the grid voltage is larger than 110% of the rated value, the active power should be reduced to 20% of the rated value. And between 106% and 110% of rated grid voltage range, the output active power should follow the linear curve as follows:

$$P = 100\%P_N, \qquad V_g \le 1.06V_N \tag{28a}$$

$$P = -\frac{20P_N}{V_N}v_g + 22.2P_N, \ 1.06V_N \le v_g \le 1.1\%V_N \tag{28b}$$

$$P = 20\%P_N, \qquad V_g \ge 1.1V_N. \tag{28c}$$

The corresponding active/voltage data points are measured through ADC and plotted in Fig. 15(b) which conform to the linear curve of the requirement.

To summarize the working mechanism of grid service to be configured with the proposed control method, a diagram is shown in Fig. 16. The commands of grid service working mode are received from the higher level platform of Raspberry Pi, which is interfaced with the users or power system operators. In Const-Var, Const-PF, and Volt-Var modes, the reactive power reference, power factor reference, and active power and grid voltage d component are passed to the corresponding grid service

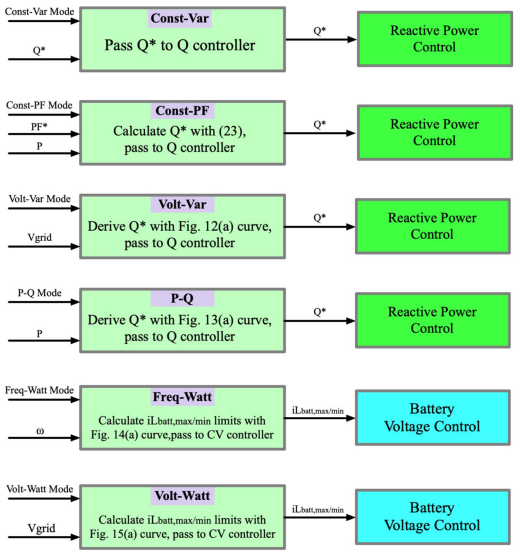


Fig. 16. Working mechanism of grid services to be configured with the controller.

TABLE I
PROTOTYPE PARAMETERS OF THE DC FAST CHARGER (V1: VERSION 1, V2: VERSION 2)

Parameter	Values
Rated power	22kW
DC bus voltage	900V
AC grid voltage	$480V_{AC,L-L}$
Battery voltage	200-650V_{DC}
Switching frequency	V1:20kHz; V2:80kHz
Switch side inductor	V1:450 μH; V2:45 μH
Output side inductor	45 μH
LCL capacitor	V1:36 μF; V2:12 μF
DC bus capacitor	216 μF
Efficiency	V1:99%; V2:98.5%
Leakage current	$\leq$ 30mA

control blocks, respectively, and the desired reactive power reference is calculated and passed to the reactive power controller. In Freq-Watt mode, the grid phase angular velocity is measured through PLL and the battery current limits are derived through Freq-Watt controller then passed to the CV controller.

V. RESULTS

The experimental results of the proposed DC fast charger with high efficiency and low-leakage current are shown in this section. The prototype configuration of hardware parameters and the start-up procedures are introduced. The high-power charging/discharging, steady-state/transient behaviors, common mode leakage current behavior, and efficiency measurement are shown to validate the proposed nonisolated fast charger.

A. Prototype Configuration

The hardware setup of the proposed DC fast charger is introduced in this section. The charger parameters are shown in Table I. Two versions of prototypes are developed including version 1 of 20 kHz switching frequency with 450 μH inductor

TABLE II
FINE-TUNED PI CONTROL PARAMETERS OF THE DC FAST CHARGER

Parameter	Values
dq grid current, $K_{p,ig,dq}$	1.5
dq grid current, $K_{i,ig,dq}$	15.0
Zero-sequence inductor current, $K_{p,iL,0}$	0.2
Zero-sequence inductor current, $K_{i,iL,0}$	2.0
DC bus voltage, $K_{p,vdc}$	-0.2
DC bus voltage, $K_{i,vdc}$	-1.0
Zero-sequence grid voltage, $K_{p,vg,0}$	0.5
Zero-sequence grid voltage, $K_{i,vg,0}$	2.0
Reactive power, $K_{p,Q}$	-0.002
Reactive power, $K_{i,Q}$	-0.02
Battery voltage, $K_{p,vbatt}$	0.001
Battery voltage, $K_{i,vbatt}$	0.01
Battery current, $K_{p,ibatt}$	0.1
Battery current, $K_{i,ibatt}$	1.0
PLL, $K_{p,PLL}$	0.05
PLL, $K_{i,PLL}$	5.0

TABLE III
COMPARISON OF PROPOSED DC CHARGER WITH COMMERCIAL PRODUCTS (V1: VERSION 1, V2: VERSION 2)

	Proposed V1&V2	ChargePoint Express 100	Blink DCFC	Delta EVHU503
Power level	22-24kW	24kW	50kW	50kW
Power flow	Two-way	One-way	One-way	One-way
Output voltage	250-800Vdc	300-500Vdc	n/a	50-1000Vdc
Output current	100A max	62A max	n/a	125A max
Input voltage	380-480Vac	380-480Vac	480Vac	480Vac
Input current	32A	32A	64A	70A
Efficiency	V1:99%; V2:98.5%	94%	92%	94%
Power factor	Auto-select	0.93	0.99	0.99
Total cost	V1:$5k; V2:$2.5k	$12.5k	$34k	$27k
Cost/Watt ($/W)	V1:0.23; V2:0.11	$0.52/W	$0.68/W	$0.52/W
Grid services	Yes	No	No	No
EMC	UL	FCC	UL	IEEE519
Volume	V1:73L; V2:44L	120L	495L	708L
Weight (kg)	V1:55; V2:24;	68	165	290
P_{den} (kW/L)	V1:0.3; V2:0.5;	0.2	0.1	0.07

and version 2 of 80 kHz switching frequency with 45 μH inductor. The charger is capable of interfacing with 480 VAC grid to charge/discharge the battery at a voltage range of 200–650 V. The rated power is 22 kW. The fine-tuned control parameters are shown in Table II , including the PI gains of dq grid current controllers, zero-sequence inductor current controller, DC bus voltage controller, zero-sequence grid voltage controller, reactive power controller, battery voltage/current controllers, and PLL controller. The prototype of the DC fast charger is shown in Fig. 17, which includes the power circuit board, controller board, switch side *LCL* inductors, output side *LCL* inductors, DC bus and *LCL* capacitors, power supplies, AC breaker, DC breaker, residual current device (RCD), and Raspberry Pi. On the power circuit board, three-phase converters on DC–AC and DC–DC side are separately distributed on two sides of the board by the middle DC bus and *LCL* capacitors. The voltage and current sensors are located on two edges of the board for isolation between high power and low power. The DSP controller board, TMS320F28379D is plugged on top side of the board. The Cree SiC MOSFET, C3M0032120 K, is chosen for the per phase switch. For the switch side *LCL* inductors, equivalent AWG8 litz wire 450 μH inductor is designed for the switch side inductors of version 1 as is shown in the middle bottom side of Fig. 17(a)

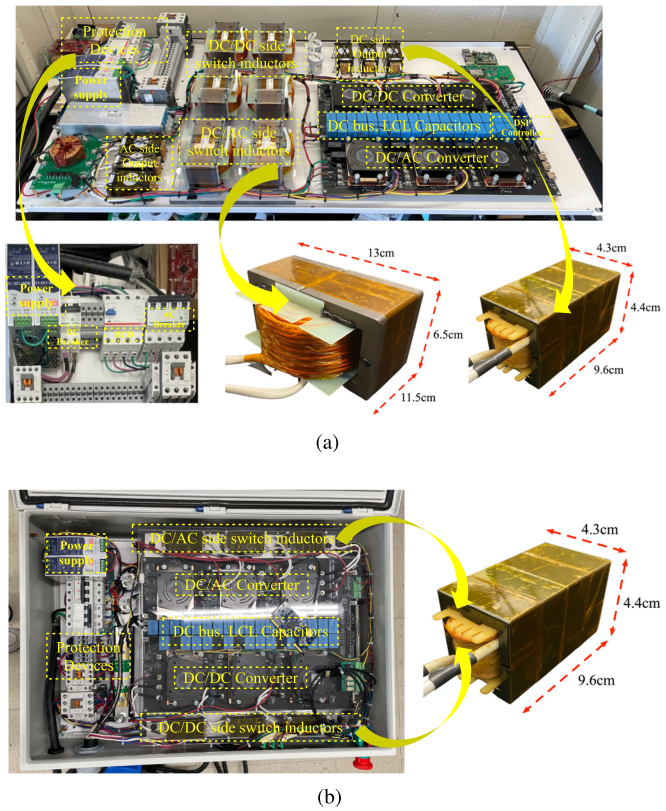


Fig. 17. (a) Version 1 and (b) Version 2 of the proposed DC charger prototype. (a) Version 1 prototpye. (b) Version 2 prototpye.

and AWG12 litz wire 45 μH inductor is designed for version 2 prototypes as is shown in the right side of Fig. 17(b) to filter the high current ripple and reduce the copper losses. For the output side *LCL* inductors, since the current ripple is low, equivalent AWG12 litz wire inductor is designed at 45 μH as is shown in the right bottom side of Fig. 17. To improve the system reliability, protection circuits are placed on both DC and AC output sides including DC breaker, AC breaker, and RCD as is shown in the left bottom side of Fig. 17. The DC, AC breakers will be triggered to disconnect and protect the main circuit from power sources if input/output currents are beyond certain limits. The RCD device is targeted to monitor the common mode leakage current on AC side. If the leakage current exceeds the threshold, the main circuit will be blocked from the grid. Thus, even without the transformer in the power loop, the common mode and differential mode currents are both monitored to guarantee the operational reliability.

B. Start-Up Procedure

For the purpose of avoiding high inrush current and voltage when interfacing with the 480 V grid at the starting point, a start-up procedure is designed with precharging circuit to smoothly enter the high-voltage/high-current mode. The precharging circuit is inserted between the grid-side inductor and PCC, which consists of precharging resistor R_{pre} precharging relay S_{pre}, and main relay S_{main}. The precharging resistor is connected in series with the precharging relay. The main relay is in parallel with

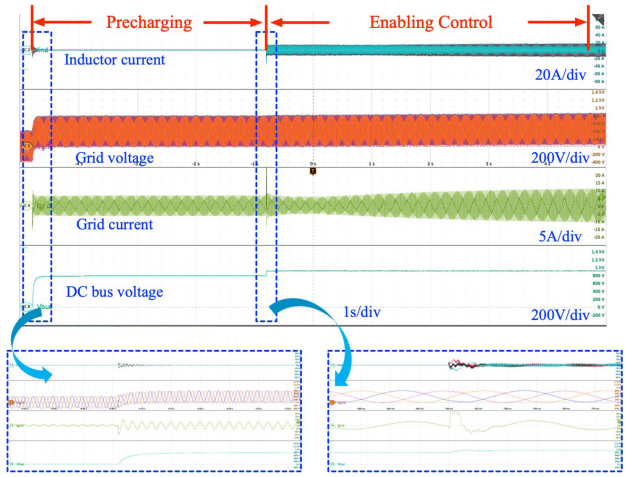


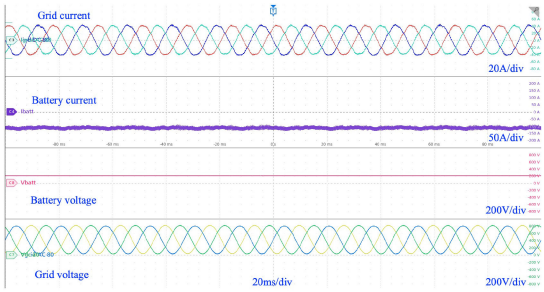
Fig. 18. Experimental transient waveforms of start-up.

the precharging relay and precharging resistor. The function of start-up precharging circuit is to smoothly precharge the DC bus and *LCL* capacitors voltage to a high level with the precharging resistors before enabling control to avoid the inrush current and voltage which could damage the devices or trigger protection.

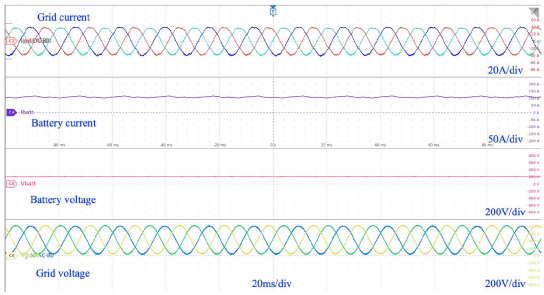
When the start-up function is enabled, the precharging relay S_{pre} is closed and the precharging resistor R_{pre} will be connected in series to the grid to smoothly precharge the DC bus to a high level. If the DC bus voltage is within the range of ($V_{\text{DC,pre,min}}$, $V_{\text{DC,pre,max}}$) after a time period of $T_{\text{pre,check}}$, the main relay S_{main} will be closed and S_{pre} will be opened to disconnect R_{pre} from the grid. Then, the grid voltage is able to be sensed through the grid voltage sensor. If the grid voltage is within the range of ($V_{\text{grid},abc,\text{min}}$, $V_{\text{grid},abc,\text{max}}$), and the grid angular velocity ω_{grid} is within the range of (350, 400) after a time period of $T_{\text{grid,check}}$, the PLL controller is affirmed to be tracked properly with a large proportional gain, $K_{p,\text{PLL}}=-2$. Then, for a better tracking resolution of ω_{grid} with lower oscillation, the $K_{p,\text{PLL}}$ will be reduced to a small value of -0.05 after a time period of $T_{\text{PLL,check1}}$. Then, the ω_{grid} will be further checked with a narrower range of (370, 385) after a time period of $T_{\text{PLL,check2}}$. If the second PLL check is passed, the charger is finally ready to enable the controller on AC side to charge the DC bus voltage to 900 V. Then, if the DC bus voltage is within the range of ($V_{\text{DC,control,min}}$, $V_{\text{DC,control,max}}$) after a time period of $T_{\text{Vdc,check}}$, the controller on DC side is ready to be enabled to deliver power. If any of the checking conditions are violated due to the abnormal conditions of the grid, both the precharging and main relays will be disconnected and the control will be disabled to stand by and wait for the recovery of grid side. Fig. 18 shows the transient waveforms of AC inductor current, grid voltage, grid current, and DC bus voltage during the star-up period which takes less than 5 s.

C. Power Testing

The high-power experimental testing of charging/discharging modes are shown in this section. The rated power 22 kW charging and discharging waveforms of grid current, battery current, battery voltage, and grid voltage are shown in Fig. 19

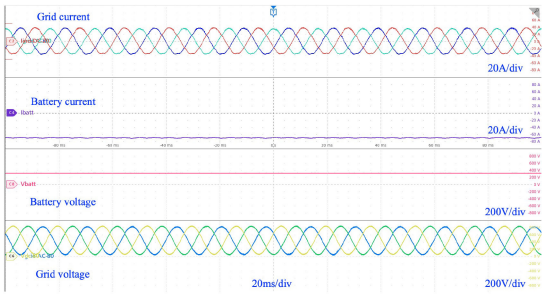


(a)

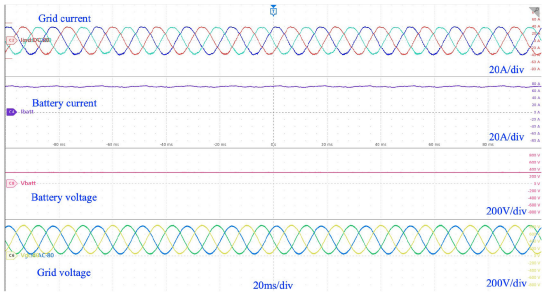


(b)

Fig. 19. Rated power charging/discharging with battery voltage of 200 V. (a) Rated power charging with battery voltage of 200 V. (b) Rated power discharging with battery voltage of 200 V.



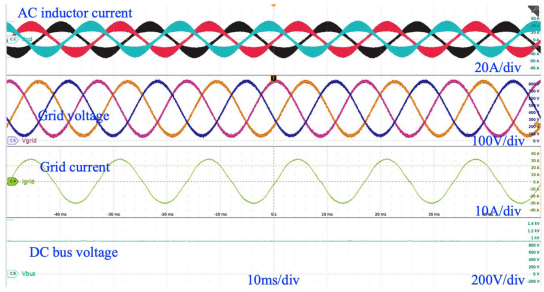
(a)



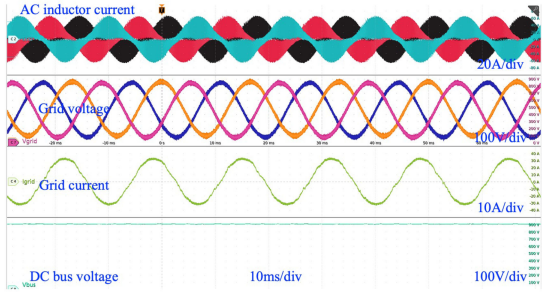
(b)

Fig. 20. Rated power charging/discharging waveforms with battery voltage of 300 V. (a) Rated power charging with battery voltage of 300 V. (b) Rated power discharging with battery voltage of 300 V.

with 200 V battery voltage and Fig. 20 with 300 V battery voltage, respectively. The steady-state waveforms of grid-side inductor current, grid voltage, grid current, and DC bus voltage for version 1 and 2 prototypes are shown in Fig. 21. Also, the transient period waveforms of AC side inductor current, grid

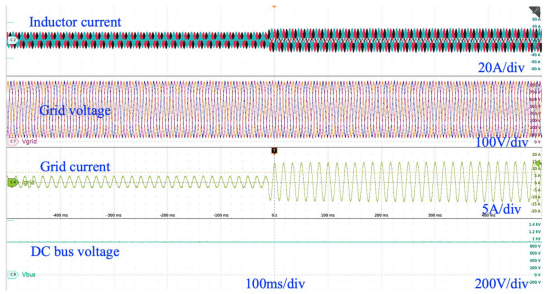


(a)

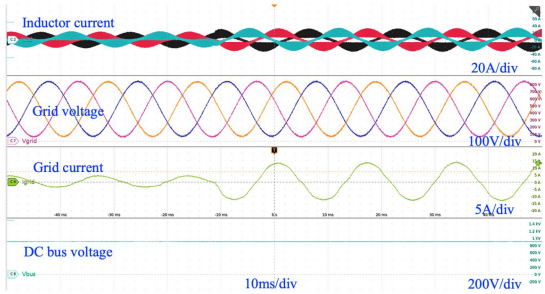


(b)

Fig. 21. Inductor current, grid voltage, grid current, and DC bus voltage waveforms of (a) version 1 and (b) version 2 prototypes. (a) Version 1 waveforms. (b) Version 2 waveforms.



(a)



(b)

Fig. 22. Transient waveforms from 3 kVA to 9 kVA. (a) Transient waveforms. (b) Zoomed transient waveforms.

voltage, grid current, and DC bus voltage with a power step from 3 to 9 kVA are shown in Fig. 22.

Also a full charging and discharging cycle has been implemented on a real battery pack, composed of 72 series-connected battery modules from Energus Power Solution Li8P25RT. Starting from roughly 10% state of charge, a constant 20 A discharging and charging current is applied at the battery pack

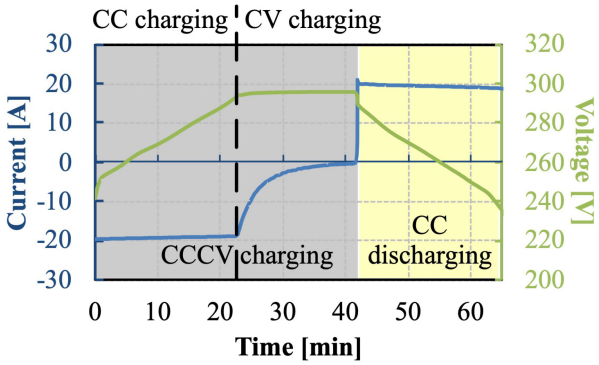


Fig. 23. CCCV charging and CC discharging cycles.

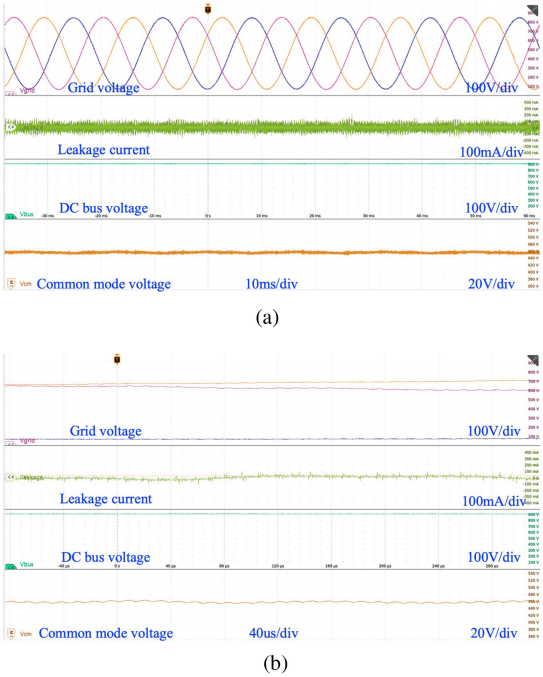


Fig. 24. Common-mode waveforms of the proposed zero-sequence control. (a) Common-mode voltage and leakage current waveforms. (b) Zoomed common-mode voltage and leakage current waveforms.

terminal during CC charging/discharging modes. The entire cycle is recorded and plotted in Fig. 23.

D. Common-Mode Leakage Current Performance

The leakage current is attenuated with the proposed topology and zero-sequence voltage controller. According to the IEC 62955:2018, the leakage current should be within 30 mA for safety issue. Also, based on the UL requirement, the common-mode voltage rms values should be less than 5MIU at a specific frequency range of 20 Hz–1 MHz. Fig. 24 shows the common-mode voltage and leakage current waveforms at rated 900 V DC bus voltage and 20 kHz switching frequency. It can be seen from the bottom waveform that the common-mode voltage has been stabilized by the zero voltage controller at half of DC bus voltage. The calculated rms common-mode voltage and leakage current are 2.27MIU and 15 mA, which are both lower

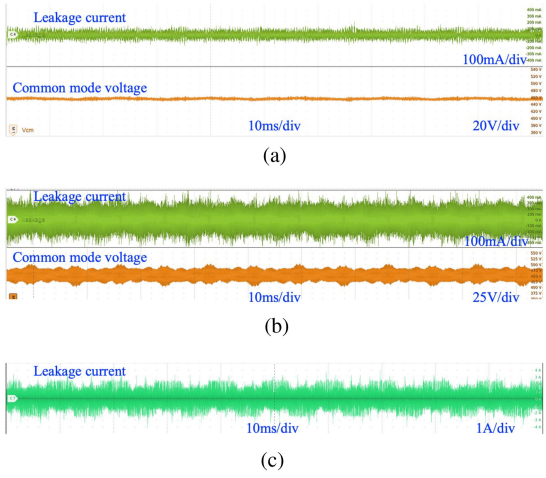


Fig. 25. Comparison of leakage current and common-mode voltage (a) for the proposed topology with zero-sequence voltage control, (b) for the proposed topology without zero-sequence voltage control, and (c) for the traditional topology without zero-sequence voltage control.

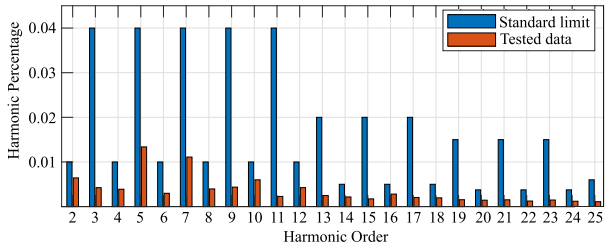


Fig. 26. Harmonic components compliance with standard.

than the standard limits of 5MIU and 30 mA, respectively. To further demonstrate the effectiveness of the proposed topology and control method for the attenuation leakage current, three cases of the leakage current and common-mode voltage waveforms are tested and shown in Fig. 25. Fig. 25(a) shows the leakage current and common-mode voltage for the proposed topology with the zero-sequence voltage control. Fig. 25(b) is the waveforms for the proposed topology without zero-sequence voltage control. Fig. 25(c) performs the leakage current of the traditional topology. The comparative results validate that the proposed topology with zero-sequence voltage achieves the minimum leakage current of 15 mA with the least common-mode voltage ripple of less than 10 V. The proposed topology without zero-sequence voltage control has 75 mA leakage current and 75 V common-mode voltage ripple which are both 5 times larger than the zero-sequence voltage controlled case. The traditional topology without zero-sequence voltage control has the maximum leakage current of 300 mA, which are 20 times larger than the zero-sequence voltage controlled case.

E. Harmonic Standard Compliance

For the compliance of UL standard in the aspect of EMI and harmonics, the grid current waveforms are captured to derive the different orders of harmonic components. The harmonics are compared with the standard requirement in Fig. 26, which

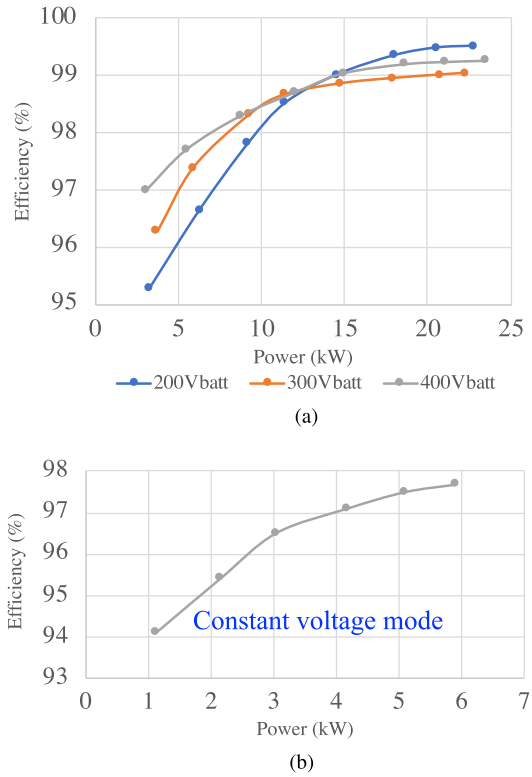


Fig. 27. Efficiency curves of the proposed charger (a) from 3 to 22 kW at battery voltages of 200, 300, and 400 V and (b) in CV charging mode of 400 V.

demonstrates that the proposed charger satisfies the standard requirement of harmonic components in every frequency order.

F. Efficiency

The efficiency of the proposed DC fast charger with power step of 3 kW from 3 to 22 kW are tested and measured in Fig. 27(a) at battery voltage of 200 V, 300 V, and 400 V, respectively. The peak efficiency of 99.51% is achieved at rated power, 200 V battery voltage condition. For all the battery voltage ranges, the peak efficiencies at rated power are all above 99%. Also, the efficiency in CV charging mode is tested with the battery voltage of 400 V. The curve is shown in Fig. 27(b). A detailed loss breakdown is analyzed in Fig. 28, which shows the power loss distribution of the proposed DC charger.

G. Comparison

1) Prototype Comparison With Commercial Products: The two versions of the proposed EV DC chargers are compared with the existing typical commercial products in Table III to show the merits in the aspects of efficiency, cost, volume, weight, grid service functions, and power density. ChargerPoint Express 100, Blink DCFC, and Delta EVHU503 are selected for benchmark. The proposed DC charger achieves the highest efficiency of 99% for version 1 and 98.5% for version 2 at rated power among the products. The efficiencies of the commercial ones are all below 95%. The cost and cost per watt of the proposed chargers

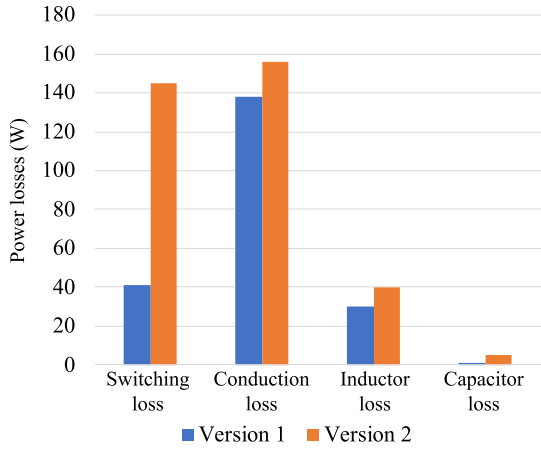


Fig. 28. Loss breakdown of the proposed chargers at rated power.

are all lower than the commercial ones. The volume of the proposed version 1 charger is 1.6, 6.8, and 9.7 times smaller than ChargerPoint Express 100, Blink DCFC, and Delta EVHU503, respectively. The weight of the proposed version 1 charger is 1.24, 3, and 5.3 times smaller than ChargerPoint Express 100, Blink DCFC, and Delta EVHU503, respectively. The power density of the proposed version 1 charger is 1.5, 3, and 4.3 times higher than ChargerPoint Express 100, Blink DCFC, and Delta EVHU503, respectively. The volume of the proposed version 2 charger is 2.7, 11.3, and 16 times smaller than ChargerPoint Express 100, Blink DCFC, and Delta EVHU503, respectively. The weight of the proposed version 2 charger is 2.83, 6.9, and 12.1 times smaller than ChargerPoint Express 100, Blink DCFC, and Delta EVHU503, respectively. The power density of the proposed version 2 charger is 2.5, 5, and 7.14 times higher than ChargerPoint Express 100, Blink DCFC, and Delta EVHU503, respectively.

2) Methodology Comparison With Other Solutions: The proposed control method and topology are compared with the existing solutions in the aspect of methodology. For the leakage current elimination literature of three-phase transformerless inverter, Guo *et al.* [19] and Sonti *et al.* [20] added extra DC or AC bypassing circuit to stabilize the common-mode voltage. Guo *et al.* [13] and Chee *et al.* [21] introduced a fourth switch phase leg and the corresponding *LC* filter to compensate for the common-mode voltage fluctuation. Ayano *et al.* [22] injected the zero-sequence voltage into the output voltage references to attenuate the leakage current.

Specifically, Guo *et al.* [19] added two switches on the positive and negative DC bus terminals. On the other hand, Sonti *et al.* [20] added a three-phase rectifying circuit on the AC side including six diodes and one switch. Both solutions are aimed at decoupling the DC and AC during null states to attenuate the common-mode voltage fluctuation by 2/3. However, extra switches will bring more modulation complexity and conduction losses. The current flows through two more switches in [19] during active states and two more diode plus one more switch in [20] during null states. The extra switching phase leg with the *LC* filter in [13] and [21] also results in more modulation

complexity and switching losses. The zero-sequence voltage injection solution in [22] reduced the leakage current in the aspect of modulation. The comparative testing results in Fig. 25 demonstrate that the proposed zero-sequence voltage control method can further reduce the leakage current and common-mode voltage fluctuation by a factor of 5 compared with the injection solution. Thus, the proposed control and topological solutions can attenuate the leakage current and common-mode voltage fluctuation without adding extra devices, which means less cost and power losses.

VI. Conclusion

This article proposes a high-efficiency low-leakage current nonisolated EV DC charger. A zero-sequence voltage control method is developed to stabilize the common-mode voltage and reduce the leakage current. The grid services and start-up functions are designed for smart charger application. Efficiency of more than 99% is achieved. The rms common-mode voltage and leakage current are all attenuated to satisfy the standard requirements. The experimental results have verified the proposed topology and control methods.

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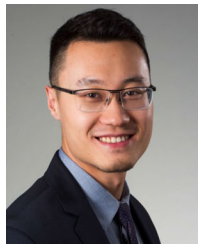

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