A Switched-Capacitor-Based Six-Level Inverter

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***Abstract*—This article introduces a new switched-capacitor-based multilevel inverter topology. The proposed structure consists of six switches with a single dc voltage source and three floating capacitors, and it is capable of producing a six-level output voltage waveform with voltage boosting gain of 2.5. Moreover, the voltages of the capacitors are constructively balanced because they are directly charged to fixed voltage by the input dc voltage source. The operating principles, circuit description, and pulsewidth modulation control technique for the proposed topology are presented, along with the selection of components. A comparative study between the proposed inverter and other existing multilevel inverter topologies is also discussed. The simulation results are provided to confirm the theoretical analysis. Furthermore, the experimental results obtained from a laboratory-built prototype under different conditions are presented as a comparison to assess the performance of the proposed inverter.**

***Index Terms*—Boost inverter, leakage current, multilevel inverters, switched-capacitor network.**

I. Introduction

THE research and application of multilevel voltage source inverters for renewable energy systems have recently been attracting increasing attention. This is because multilevel voltage source inverters [1], [2] have specific merits over conventional two-level voltage-source inverters, such as high-quality output waveforms, limited blocking voltage ratings of semiconductor devices, smaller filters, low electromagnetic interference, high efficiency, etc. However, the conventional multilevel voltage source inverters, including the neutral point clamped [3], [4], cascaded H-bridge (CHB) [5], [6], and flying-capacitor (FC) inverters [7], are only a buck conversion, where the output peak ac voltage is lower than the total input dc voltages. Further, a huge number of dc-link voltage sources or a large number of semiconductor devices are required to generate higher level output voltage waveforms. For applications in renewable energy systems wherein a low input voltage is inverted to a high dc output voltage, impedance networks [8] or dc–dc boost converters [9], [10] have been added to the conventional multilevel inverters to provide a boosting feature. As a result, these power circuits use more semiconductor devices and passive components, which are accompanied by higher loss and cost.

In recent years, numerous multilevel inverters have been developed with step-up capability and reduced component count [11], [12]. In [11], a hybrid multilevel inverter was introduced by integrating the switched-capacitor technique into the conventional cascaded H-bridge multilevel inverter. In this topology, a switched-capacitor network that consists of one capacitor, two switches, and one diode was used to step-up the input voltage. In [12]–[15], some types of switched-capacitor-based seven-level inverters have been introduced with output voltage levels that reach up to three times the input voltage. Moreover, all capacitors were charged directly from the input voltage source. Therefore, the voltage stress on the capacitors was the same, making the voltage balancing easily. As reported in [16], a boost switched-capacitor multilevel inverter with self-balancing was proposed by integrating an H-bridge with a novel switched-capacitor cell. This topology has the ability to provide up to nine voltage levels with a single dc source. However, the topology in [16] only provides a low voltage gain. In addition, enabling the charging of two capacitors connected in series was the profound contribution of the matter of unbalanced voltage, because the two capacitors have different discharging rates. A modified version of the topology reported in [16] was discussed in [17] to limit the voltage stress across semiconductor devices. However, this topology also exists with a low voltage gain and the matter of unbalanced voltage. Such as [16] and [17], a boost switched-capacitor multilevel inverter in [18] has the ability to provide up to nine voltage levels with a single dc source, and their maximum voltage level was achieved at two times the input voltage. As presented in [19], a new type of switched-capacitor nine-level inverter has been introduced with output voltage levels reaching up to four times the input voltage. However, as presented in [16], [17], and [19], the limitations of these topologies include the high-voltage stress on semiconductor devices and the use of numerous isolated dc sources for their three-phase configurations. Nevertheless, as presented in [11]–[19], the matter of leakage current in the solar photovoltaic (PV) system [20], [21] has yet to be considered. Therefore, there is a need for an effective approach for the reduction of the leakage current for these topologies before they can be suitable for PV applications.

More recently, several types of switched-capacitor multilevel inverters, which are based on the common ground [22]–[27]

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and the half-bridge capacitor concepts [28]–[31], have been discussed in the literature for reduction of the leakage current. Based on the CHB structure, a single-source switched-capacitor multilevel inverter with common ground in [22] was shown to be capable of eliminating the leakage current. This inverter has the ability to provide up to seven voltage levels with a single dc source, and their maximum voltage level was achieved at three times the input voltage. Nevertheless, similar to the conventional multilevel inverters, the use of numerous semiconductor devices and capacitors to produce a number of output voltage levels is the major disadvantage of this topology. Similar to [22], a switched-capacitor nine-level inverter with common ground was reported in [23]. In this case, the power circuit uses numerous semiconductor devices. In [24] and [25], two types of switched-capacitor five-level inverters with common ground have been discussed. In these topologies, the negative terminal of the PV and the grid neutral line are directly connected. As a result, the common-mode voltage is clamped to zero. However, these topologies lack voltage boosting capability, and their peak output voltage is lower than the input voltage. Similar to [24] and [25], a new type of switched-capacitor seven-level inverters with common ground was introduced in [26]. As presented in [26], this topology has the ability to provide up to seven voltage levels with a single dc source, and its maximum voltage level is achieved at three times the input voltage. Nevertheless, this topology contains an unbalanced voltage because four capacitors are charged with different level voltages. Unlike [26], a switched-capacitor nine-level inverter with leakage current limiting capabilities and reduced component count has been discussed in [27]. In this topology, the positive terminal of the PV and the grid neutral line are directly connected. As a result, the common-mode voltage is kept constant. Similar to [26], this topology also contained unbalanced voltage. Certain types of switched-capacitor seven-level inverters have been introduced in [28]–[30]; the midpoint of two decoupled dc-link capacitors was directly connected with the grid neutral line. Because of this, the common-mode voltage is kept constant. However, these topologies also contain low voltage gain. A switched-capacitor four-level inverter with leakage current-limiting capabilities and reduced component count has been introduced in [31]. Similar to the other switched-capacitor multilevel inverter topologies, this topology also suffers from low voltage gain, and the peak output voltage was limited to lower than 1.5 times the input voltage.

In light of the above, this article proposes a new switched-capacitor-based six-level inverter topology (SC-based SLI). The proposed topology is capable of generating a six-level output voltage waveform with the maximum voltage level of 2.5 times the input voltage, and also provides the self-balancing of capacitors voltage. In the proposed inverter, the midpoint of two decoupled dc-link capacitors and the grid neutral line is directly connected to eliminate leakage current.

The rest of this article is organized as follows. The operating principles and circuit description of the proposed inverter with a pulsewidth modulation (PWM) control technique are discussed in Section II. A comparative study between the proposed inverter and other existing multilevel inverter topologies and parameter selection are also addressed in Section II. The simulation and experimental results are provided in Section III. Finally, Section IV concludes this article.

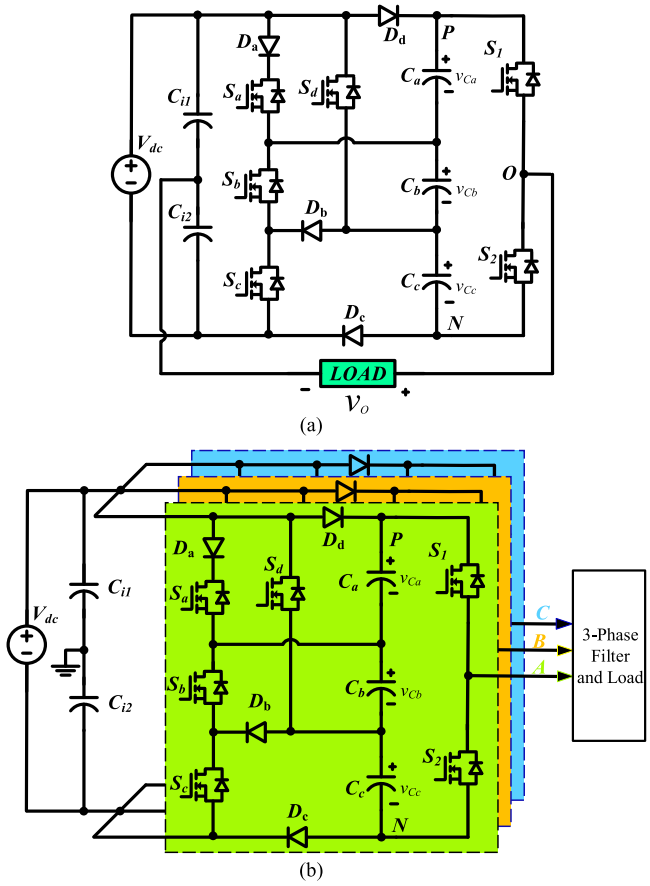

Fig. 1. Equivalent circuit of proposed SC-based SLI topology. (a) Single-phase configuration. (b) Three-phase configuration.

II. Proposed SC-Based SLI Topology

In this section, a single-phase hybrid six-level inverter with voltage boosting capabilities is first proposed by combining a traditional half-bridge inverter and the switched-capacitor-based network. The schematic diagram of the proposed single-phase SC-based SLI topology is shown in Fig. 1(a). As presented in this figure, the switched-capacitor-based network is composed of three floating capacitors C_a-C_b-C_c, two decoupled dc-link capacitors C_{i1}-C_{i2}, four power switches S_a-S_b-S_c-S_d, and four power diodes D_a-D_b-D_c-D_d. The structure of the proposed single-phase SC-based SLI topology in Fig. 1(a) can perform a buck-boost voltage conversion and provide up to six voltage levels of $\pm 2.5V_{\mathrm{DC}}$, $\pm 1.5V_{\mathrm{DC}}$, and $\pm 0.5V_{\mathrm{DC}}$ at the output voltage terminal. Fig. 1(b) presents the configuration of the proposed three-phase SC-based SLI. As depicted in Fig. 1(b), the proposed three-phase SC-based SLI topology can be configured by connecting three-module SC-based SLI in parallel across a single dc voltage source; each phase can generate six levels in the output side.

A. Operating Principle of the Proposed SC-Based SLI

The operating principle of the proposed single-phase SC-based SLI topology can be explained by the switching states,

TABLE I
STATE OF SEMICONDUCTOR DEVICES AND CAPACITORS OF THE PROPOSED SC-BASED SLI TOPOLOGY UNDER SIX SWITCHING STATES

Switching state	Switch state						Diode state				Capacitor state			Output voltage
	S_a	S_b	S_c	S_d	S_1	S_2	D_a	D_b	D_c	D_d	C_a	C_b	C_c	(V_o)
M1	Off	Off	Off	On	On	Off	Off	Off	On	Off	D	D	C	2.5V_{dc}
M2	On	Off	On	Off	On	Off	On	On	Off	Off	D	C	F	1.5V_{dc}
M3	Off	On	On	Off	On	Off	Off	Off	Off	On	C	F	F	0.5V_{dc}
M4	Off	Off	Off	On	Off	On	Off	Off	On	Off	F	F	C	-0.5V_{dc}
M5	On	Off	On	Off	Off	On	On	On	Off	Off	F	C	D	-1.5V_{dc}
M6	Off	On	On	Off	Off	On	Off	Off	Off	On	C	D	D	-2.5V_{dc}

"C": Charging mode; "F": floating mode; and "D": Discharging mode.

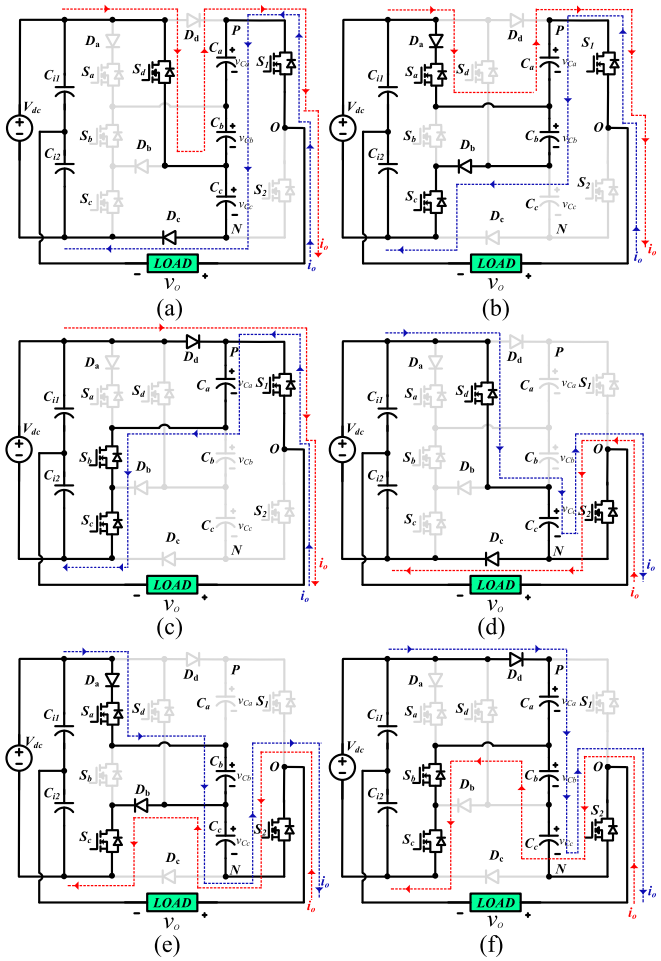

Fig. 2. Switching states of proposed SC-based SLI topology. (a) State M1. (b) State M2. (c) State M3. (d) State M4. (e) State M5. (f) State M6.

as given in Table I. The detailed description of each switching states is as follows.

1) *State M1 [see Fig. 2(a)]:* Two switches S_1 and S_d are turned ON while four switches S_a, S_b, S_c, and S_2 are turned OFF. As a result, diode D_c conducts and three diodes D_a, D_b, and D_d are blocked. In this state, the capacitor C_c is charged from the input dc source through a loop of $V_{\rm dc}$-S_d-C_c-D_c. Two capacitors C_a and C_b are used to step up the output voltage by releasing the energy stored in these capacitors to the load. The output voltage of the proposed inverter (v_o) is equal to the sum of the voltages on capacitors C_a, C_b, and C_{i1}, is given

$$\begin{cases} V_{Ci1} = 0.5V_{\rm dc} \\ V_{Cc} = V_{\rm dc} \\ v_o = V_{Ci1} + V_{Ca} + V_{Cb} = 2.5V_{\rm dc}. \end{cases} \tag{1}$$

2) *State M2 [see Fig. 2(b)]:* Three switches S_1, S_a, and S_c are turned ON, while three switches S_2, S_b, and S_d are turned OFF. Two diodes D_a and D_b conduct, while two diodes D_c and D_d are blocked. In this state, capacitor C_b is also charged from the input dc source through a loop of $V_{\rm dc}$-D_a-S_a-C_b-D_b-S_c. Capacitor C_c *is* floating, while capacitor C_a is used to step up the output voltage. In this case, the output voltage is equal to the sum of the capacitors C_a and C_{i1} voltage

$$\begin{cases} V_{Ci1} = 0.5V_{\rm dc} \\ V_{Cb} = V_{\rm dc} \\ v_o = V_{Ci1} + V_{Ca} = 1.5V_{\rm dc}. \end{cases} \tag{2}$$

3) *State M3 [see Fig. 2(c)]:* Three switches S_1, S_b, and S_c are turned ON, while four switches S_a, S_d, and S_2 are turned OFF. As a result, diode D_d conducts, while three diodes D_a, D_b, and D_c are blocked. In this state, capacitor C_a is charged by the input dc source. Two capacitors C_b and C_c are disconnected to the circuit, while capacitor C_{i1} is connected in parallel with the load. Therefore, the output voltage of the proposed inverter is the voltage of capacitor C_{i1}

$$\begin{cases} V_{Ci1} = 0.5V_{\rm dc} \\ V_{Ca} = V_{\rm dc} \\ v_o = V_{Ci1} = 0.5V_{\rm dc}. \end{cases} \tag{3}$$

4) *State M4 [see Fig. 2(d)]:* Two switches S_2 and S_d are turned ON, while four switches S_a, S_b, S_c, and S_1 are turned OFF. As a result, diode D_c conducts, while three diodes D_a, D_b, and D_d are blocked. It can be seen that capacitor C_c is charged from the input dc source and two capacitors C_a and C_b are floating. The output voltage of the proposed inverter is a negative and equal to the capacitor C_{i2} voltage

$$\begin{cases} V_{Ci2} = 0.5V_{\rm dc} \\ V_{Cc} = V_{\rm dc} \\ v_o = -V_{Ci2} = -0.5V_{\rm dc}. \end{cases} \tag{4}$$

5) *State M5 [see Fig. 2(e)]:* Three switches S_2, S_a, and S_c are turned ON, while three switches S_1, S_b, and S_d are turned OFF. Hence, two diodes D_a and D_b conduct while

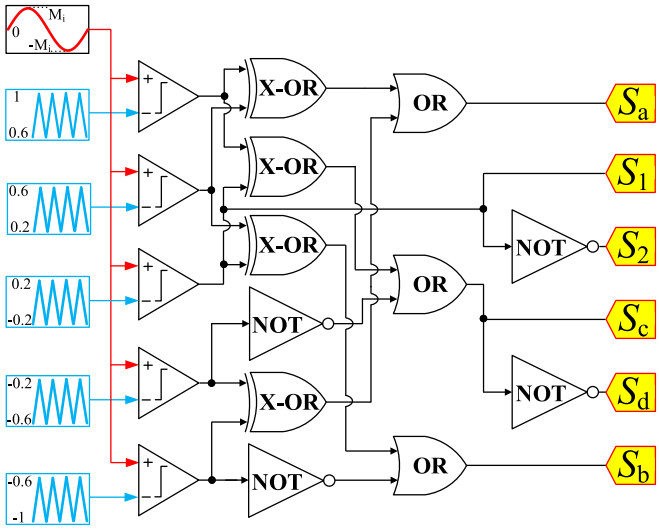

Fig. 3. Proposed PWM signal generation scheme for proposed SC-based SLI topology.

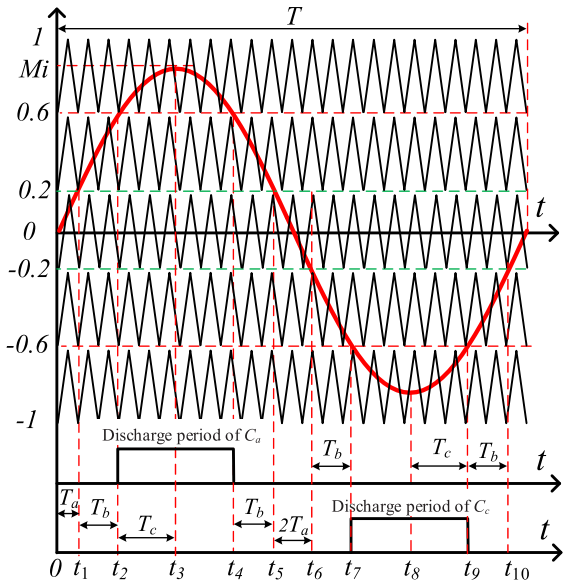

Fig. 4. Discharge period of two floating capacitors C_a and C_c.

two diodes D_c and D_d are blocked. In this state, capacitor C_b is charged from the input dc source through a loop of V_{dc}-D_a-S_a-C_b-D_b-S_c. Capacitor C_a *is* floating while capacitor C_c is discharged. The output voltage is equal to the sum of a negative capacitor C_c voltage and a negative capacitor C_{i2} voltage

$$\begin{cases} V_{Ci2} = 0.5V_{\rm dc} \\ V_{Cb} = V_{\rm dc} \\ v_o = -V_{Ci2} - V_{Cc} = -1.5V_{\rm dc}. \end{cases} \tag{5}$$

6) *State M6 [see Fig. 2(f)]:* Three switches S_2, S_b, and S_c are turned ON, while three switches S_a, S_d, and S_1 are turned OFF. Diode D_d is conducted while three diodes D_a, D_b, and D_c are blocked. Furthermore, capacitor C_a is charged from the input dc source. Two capacitors C_b and C_c are discharged. The output voltage of the proposed inverter is equal to the sum of a negative capacitor C_c voltage, a negative capacitor C_b voltage, and a negative capacitor C_{i2} voltage

$$\begin{cases} V_{Ci2} = 0.5V_{\rm dc} \\ V_{Ca} = V_{\rm dc} \\ v_o = -V_{Ci2} - V_{Cb} - V_{Cc} = -2.5V_{\rm dc}. \end{cases} \tag{6}$$

B. PWM Control Technique for the Proposed SC-Based SLI

Fig. 3 shows the proposed PWM control technique for the SC-based SLI. As depicted in Fig. 3, to generate PWM control signals for switches of the proposed SC-based SLI, a modulating sinusoidal control waveform is compared with five level-shifted high-frequency triangle waveforms. The proposed PWM control technique only uses logical relation-based operation to create the gate signals for all six switches.

C. Selection of Capacitors

Similar to existed single-phase switched-capacitor multilevel inverters, the proposed SC-based SLI topology also has a low-frequency ripple in each capacitor, which results in reducing efficiency and increasing THD of power conversion. From Fig. 1, we can see that the output current of the proposed SC-based SLI topology is equally splited into two decoupled dc-link capacitors C_{i1} and C_{i2}. As a result, the voltages of C_{i1} and C_{i2} are around half of input voltage. The maximum discharge amount of two capacitors C_{i1} and C_{i2} is presented by

$$Q_i = \frac{1}{2} \times \int_0^{T/2} i_o(t)\, dt \tag{7}$$

where T is the time period of the output voltage reference signal.

The optimal capacitance for C_{i1} and C_{i2} can be calculated

$$C_i \geq \frac{Q_i}{\Delta V_{Ci}} \tag{8}$$

where ΔV_{Ci} is the peak-to-peak voltage ripple of two decoupled dc-link capacitors C_{i1} and C_{i2}.

The longest discharging period of three capacitors C_a, C_b and C_c are taken into consideration for calculating their peak-to-peak voltage ripple. Due to symmetrical operation, the longest discharging time for C_a and C_c are same as highlighted in Table I. Furthermore, we can see that the longest discharging time of the capacitor C_a is from t_2 to t_4 (switching states M1 and M2) as highlighted in Fig. 4, where the time interval t_2 and t_4 are calculated as

$$\begin{cases} t_2 = \frac{\sin^{-1}(0.6/M_i)}{2\pi f_0} \\ t_4 = \frac{\pi - \sin^{-1}(0.6/M_i)}{2\pi f_0} \end{cases} \tag{9}$$

where f_0 and M_i are the fundamental frequency of output voltage and modulation index, respectively.

The maximum discharge amount of capacitors C_a and C_c can be expressed as

$$Q_{a,c} = \int_{t_2}^{t_4} i_o(t)\, dt. \tag{10}$$

From (9) and (10), the optimal capacitance for C_a is calculated as

$$C_a = C_c = \frac{Q_{a,c}}{\Delta V_{Ca}} = \frac{Q_{a,c}}{\Delta V_{Cc}} \tag{11}$$

where ΔV_{Ca} and ΔV_{Cc} are the peak-to-peak voltage ripple of capacitor C_a and C_c, respectively.

Capacitor C_b always repeats discharging and charging during the time interval from t_2 to t_4. The time duration (t'_3-t_3) is the longest discharging time of the capacitor C_b. So, the maximum discharge amount of capacitor C_b can be expressed as

$$\begin{cases} Q_b \approx \int_{t_3}^{t_3'} i_o(t)\, dt \\ t_3 = \frac{1}{4f_0} \\ t_3' = \frac{1}{4f_0} + \frac{5M_i - 3}{2f_{sw}} \end{cases} \tag{12}$$

where $f_{\rm sw}$ is the switching frequency.

Solved (12), the optimal capacitance for C_b is calculated as

$$C_b \geq \frac{Q_b}{\Delta V_{Cb}} \tag{13}$$

where ΔV_{Cb} is the peak-to-peak voltage ripple of capacitor C_b.

According to [32] and [33], for purely resistive load (R_L) condition, the maximum discharge amount for capacitors are calculated as

$$\begin{cases} Q_i = \frac{V_{\rm dc}}{4R_L}\left[2T_a + 6(T_b - T_a) + 10T_c\right] \\ Q_{a,c} = \frac{5V_{\rm dc}}{R_L}T_c \\ Q_b = \frac{5V_{\rm dc}(5M_i - 3)}{4R_L f_{\rm sw}} \end{cases} \tag{14}$$

where the time interval T_a is calculated as

$$T_a = \frac{\sin^{-1}(0.2/M_i)}{2\pi f_0}. \tag{15}$$

For resistive–inductive load condition, the output current of the proposed SC-based SLI topology is defined as

$$i_o(t) = I_p \sin\left(2\pi f_0 t - \Phi\right) \tag{16}$$

where I_p and Φ are the peak value of the output current, and phase difference between the output voltage and the output current, respectively.

The maximum discharge amounts for capacitors are calculated as

$$\begin{cases} Q_i = \frac{I_p}{2\pi f_0} \\ Q_{a,c} = \frac{I_p}{2\pi f_0}\left|\cos(2\pi f_0 t_2 - \Phi) - \cos(2\pi f_0 t_4 - \Phi)\right| \\ Q_b = \frac{I_p}{2\pi f_0}\left|\cos(2\pi f_0 t_3 - \Phi) - \cos(2\pi f_0 t_3' - \Phi)\right|. \end{cases} \tag{17}$$

It can be seen that the maximum discharge amount of capacitors is relative to the peak value of the output current and the phase difference between the output voltage and the output current. Fig. 5 shows the variation of optimum capacitance for capacitors with different resistive load conditions. Considering the allowable voltage ripple of capacitors is k percentage of capacitors voltage in steady-state, we can see that capacitance values of capacitors dropping with rising value of resistive load and k.

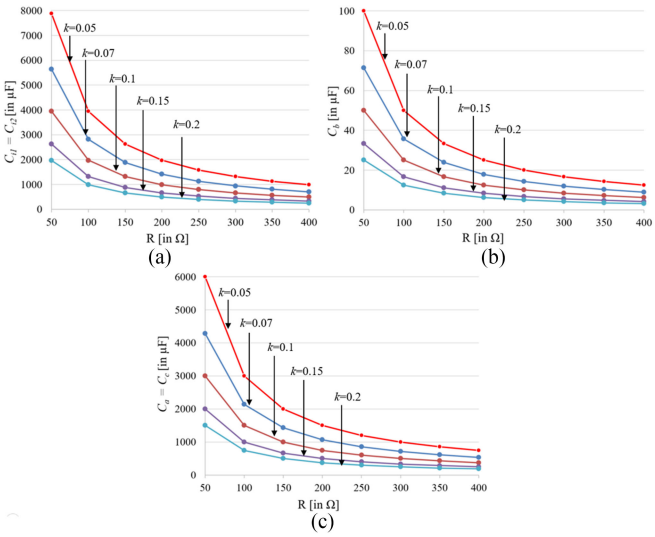

Fig. 5. Variation of optimum capacitance for different resistive load conditions. (a) Two decoupled dc-link capacitors C_{i1} and C_{i2}. (b) Capacitor C_b. (c) Two capacitors C_a and C_c.

D. Comparison With Other Multilevel Inverters

Table II compares the proposed SC-based SLI topology to other recent multilevel voltage source inverter topologies. The attributes for comparison are the count of devices, number of voltage levels, boosting capability, switch-per-level ratios, maximum number of switches in charging path, total standing voltage (TSV), maximum standing voltage (MSV), reported measured efficiency, capacitor ripple loss and three-phase configuration with single source ability as well as the capability to eliminate the leakage current. As given in Table II, the switched-capacitor nine-level inverter in [16], [17], and [19], which can provide the voltage boosting capability and generate nine levels at the output without eliminating the leakage current. Furthermore, multiple isolated dc sources are required for their three-phase counterparts, while the proposed SC-based SLI topology only requires a single dc voltage source in both single-phase and three-phase configuration, as given in Table II. As described in the table, the switched-capacitor seven-level inverter in [15] can achieve voltage boosting capability and generate seven levels at the output without eliminating the leakage current. Its switch-per-level ratio is also the highest. Multiple isolated dc sources are required for its three-phase counterpart. The TSV of topology in [15] is $16V_{\rm dc}$ while the TSV of the proposed inverter is $11V_{\rm dc}$. Compared with the article presented in [15], the MSV of the proposed inverter is higher than the MSV of the topology in [15]. Compared with the switched-capacitor nine-level inverter in [16], the proposed SC-based SLI topology uses three more diodes, four fewer switches, and three more capacitors. Compared with the topologies in [17] and [19], the

TABLE II
COMPARISON OF THE PROPOSED SC-BASED SLI TOPOLOGY WITH CONSIDERED TOPOLOGIES

Parameters	[15]	[16]	[17]	[19]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	Proposed
Number of voltage levels	7	9	9	9	9	7	5	5	7	9	7	7	7	6
Number of switches	16	10	12	12	17	13	8	6	6	9	9	8	10	6
Switch-per-level ratios	2.28	1.11	1.33	1.33	1.88	1.86	1.6	1.2	0.86	1	1.14	1.43	1.43	1
Maximum number of switches in charging path	4	2	4	4	8	2	4	2	1	4	2	4	4	2
Number of diodes	0	1	0	0	5	0	*0*	1	4	3	1	0	0	4
Number of capacitors	2	2	2	3	4	3	3	2	4	4	3	4	4	5
Boosting feature	yes	yes	yes	yes	yes	yes	no	no	yes	yes	yes	no	yes	yes
Voltage gain	3	2	2	4	4	3	1	1	3	4	1.5	1	1.5	2.5
TSV	$16V_{dc}$	$12V_{dc}$	$11V_{dc}$	$24V_{dc}$	$17V_{dc}$	$13V_{dc}$	$6.5V_{dc}$	$7V_{dc}$	$12V_{dc}$	$21V_{dc}$	$16V_{dc}$	$5V_{dc}$	$9V_{dc}$	$11V_{dc}$
$TSV_{P.U}$	5.33	6	5.5	6	4.25	4.3	6.5	7	4	5.25	10.66	5	6	4.4
MSV	V_{dc}	V_{dc}	V_{dc}	$4V_{dc}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	$1V_{dc}$	V_{dc}	$3V_{dc}$
Eliminating the leakage current	no	no	no	no	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes
Three-phase configuration with single source	no	no	no	no	yes	yes	no	yes	yes	yes	yes	yes	yes	yes
Reported measured efficiency [%]	92 @500W	96 @1kW	80.6 @16W	96 @50W	-	96.7 @500W	97 @1kW	96.3 @400W	97 @300W	95.2 @900W	96.7 @200W	97.5 @1kW	97@ 140W	95.8 @400W
Capacitors ripple loss*	9.1 W	-	-	-	-	10.3W	9.8 W	7.7 W	4.9 W	-	16.3 W	8.1 W	10.3 W	6.4 W

TSV: total standing voltage of switches; $TSV_{P.U}$: total standing voltage of switches in per unit; MSV: Maximum standing voltage of switches
* All mentioned inverters are operated at the parameters as $k = 0.1, f_{sw} = 10$ kHz, $f_0 = 50$ Hz, $P_o = 500$ W, and $V_{o-\max} = 250$ V.

proposed SC-based SLI topology uses four more diodes, six fewer switches, and two more capacitors. Table II gives that the multilevel voltage source inverter discussed in [22] requires 17 switches to produce nine levels at the output with eliminating the leakage current, while the proposed SC-based SLI topology only requires 6 switches. Therefore, the switch-per-level ratio of the proposed inverter is lower than the switch-per-level ratio of the topology detailed in [22].

As is made clear in Table II, the multilevel voltage source inverter discussed in [23] requires thirteen switches, while the proposed SC-based SLI topology only requires six switches. As presented in Table II, the topologies of [24], [25], and [29] require a lower number of active and passive components than the proposed SC-based SLI topology. However, these three topologies cannot provide voltage boosting capability. Furthermore, the multilevel voltage source inverter discussed in [24] requires multiple isolated dc sources for their three-phase counterparts. Similar to the multilevel voltage source inverter in [23], the topologies in [25]–[30] can eliminate the leakage current and only require a single dc voltage source in both single-phase and three-phase configuration. As given in Table II, the switch-per-level ratio of topology in [26] is the lowest, as it is only 0.86. The maximum number of switches in the charging path of topology in [26] is only one switch, while the maximum number of switches in the charging path of the proposed topology is two switches. Compared with [27], the TSV of the proposed topology is lower. Similar to the proposed topology, the topologies described in [26] and [27] require a single dc voltage source in both single-phase and three-phase configuration, as given in Table II. In addition, the proposed SC-based SLI topology can provide a voltage gain of 2.5, whereas the topologies of [28] and [30] can only provide a voltage gain of 1.5, as given in Table II. Compared with the switched-capacitor nine-level inverter in [30], the proposed SC-based SLI topology uses four more diodes, four fewer switches, and one more capacitor. The proposed SC-based SLI topology can also eliminate the leakage current like the topologies of [23]–[30]. In term of reported efficiency, the efficiency of the proposed SC-based SLI is found to be 95.8% at 400 W and is competent efficiency with other inverters. Nevertheless, the reported efficiency of the mentioned inverters in the literature employ difference semiconductor technologies and some difference switching frequencies. These characteristics may lead to not exactly comparison in terms of efficiency.

For the capacitor ripple loss comparison, the inverters in [15], [23]–[26], and [28]–[30] are considered comparing with the capacitors ripple losses of the proposed SC-based SLI topology. The eventual computed capacitors ripple losses are given in the last row of Table II. It can be observed that the multilevel voltage source inverter [26] has the lowest capacitor ripple loss. This is because they used four capacitors with low capacitance. Moreover, the proposed SC-based SLI topology has lower capacitor ripple loss than that of other inverters.

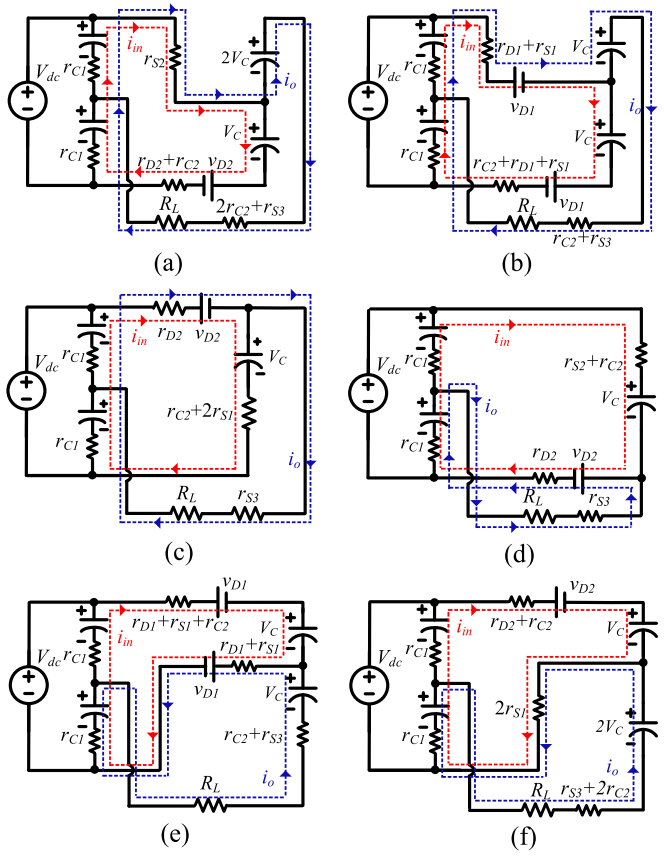

Fig. 6. Equivalent circuits of proposed SC-based SLI topology with parasitic components. (a) State M1. (b) State M2. (c) State M3. (d) State M4. (e) State M5. (f) State M6.

E. Power Loss Analysis

The power loss of the proposed SC-based SLI topology can be divided into the switches, diodes, and capacitors loss. The major power losses can also include the conduction losses, switching losses and capacitor ripple losses [32], [33]. For the conduction losses of different components in the proposed SC-based SLI topology, the equivalent circuits for power loss analysis have been shown in Fig. 6. It is assumed that the ON-state resistances of three switches (S_a, S_b and S_c), switch S_d, and two switches (S_1, S_2) are r_{S1}, r_{S2} and r_{S3}, respectively. The capacitors voltage: $V_{Ca} = V_{Cb} = V_{Cc} = V_C$, $V_{Ci1} = V_{Ci2} = V_{dc}/2$, and equivalent series resistance of two capacitors (C_{i1}, C_{i2}), three capacitors (C_a, C_b, C_c) are r_{C1} and r_{C2}, respectively. D_a and D_b diodes have same internal resistance (r_{D1}) and forward voltage drop (v_{D1}), D_c and D_d diodes have same internal resistance (r_{D2}) and forward voltage drop (v_{D2}). By applying Kirchhoff's voltage law to Fig. 6, the $i_{\rm in}$ and i_o can be calculated and given in Table III. The instantaneous and average conduction losses for the proposed SC-based SLI in each states have been evaluated as Table IV. Hence, the total conduction losses of the proposed inverter are the summation of average conduction losses in each states and can be derived as

$$P_{\rm Con\_Total} = \sum_{i=1}^{6} P_{i,\rm avg}. \tag{18}$$

TABLE III
CONDUCTING TIME AND CURRENT OF THE PROPOSED SC-BASED SLI

State	Conducting time	Conducting current
M1	T_c	$i_o = \frac{(2V_C + V_{dc}/2)(r_{S2}+r_{D2}+r_{C2}) - (V_{dc} - V_C - v_{D2})r_{S2}}{(R_L + r_{S2} + 2r_{C2} + r_{S3})(r_{S2}+r_{D2}+r_{C2}) - r_{S2}^2}$; $i_{in} = \frac{V_{dc} - V_C - v_{D2} - r_{S2}i_o}{r_{S2}+r_{D2}+r_{C2}}$
M2	$T_b + T_c$	$i_o = \frac{3V_C(r_{S1}+r_{D1}) + (V_{dc}/2 + V_C - v_{D1})r_{C2}}{(r_{S1}+r_{D1}+R_L+r_{C2}+r_{S3})(2r_{S1}+2r_{D1}+r_{C2}) - (r_{S1}+r_{D1})^2}$; $i_{in} = \frac{V_{dc} - V_C - 2v_{D1} - i_o(r_{S1}+r_{D1})}{2r_{S1}+2r_{D1}+r_{C2}}$
M3	$2T_a + T_b$	$i_o = \frac{(V_{dc}/2 - v_{D2})(2r_{S1}+r_{D2}+r_{C2}) - (V_{dc} - V_C - v_{D2})r_{D2}}{(R_L + r_{S3} + r_{D2})(2r_{S1}+r_{D2}+r_{C2}) - r_{D2}^2}$; $i_{in} = \frac{V_{dc} - V_C - v_{D2} - r_{D2}i_o}{2r_{S1}+r_{D2}+r_{C2}}$
M4	$2T_a + T_b$	$i_o = \frac{(V_{dc}/2 - v_{D2})(r_{S2}+r_{D2}+r_{C2}) - (V_{dc} - V_C - v_{D2})r_{D2}}{(R_L + r_{S3} + r_{D2})(r_{S2}+r_{D2}+r_{C2}) - r_{D2}^2}$; $i_{in} = \frac{V_{dc} - V_C - v_{D2} - r_{D2}i_o}{(r_{S2}+r_{D2}+r_{C2})}$,
M5	$T_b + T_c$	$i_o = \frac{3V_C(r_{S1}+r_{D1}) + (V_C + V_{dc}/2 - v_{D1})r_{C2}}{(R_L + r_{S3} + r_{C2} + r_{D1} + r_{S1})(2r_{S1}+2r_{D1}+r_{C2}) - (r_{S1}+r_{D1})^2}$; $i_{in} = \frac{V_{dc} - V_C - 2v_{D1} - (r_{S1}+r_{D1})i_o}{(2r_{S1}+2r_{D1}+r_{C2})}$
M6	T_c	$i_o = \frac{(2V_C + V_{dc}/2)(2r_{S1}+r_{D2}+r_{C2}) - 2r_{S1}(V_{dc} - V_C - v_{D2})}{(R_L + 2r_{S1} + r_{S3} + 2r_{C2})(2r_{S1}+r_{D2}+r_{C2}) - 4r_{s1}^2}$; $i_{in} = \frac{V_{dc} - V_C - v_{D2} - 2r_{S1}i_o}{2r_{S1}+r_{D2}+r_{C2}}$

TABLE IV
INSTANTANEOUS AND AVERAGE CONDUCTION LOSSES OF THE PROPOSED SC-BASED SLI

State M1	$p_1 = (r_{S2}+r_{C1})i_{in}^2 + (r_{D2}+r_{C1}+r_{C2})(i_{in}+i_o)^2 + (2r_{C2}+r_{S3})i_o^2$; $P_{1,avg} = \frac{T_c}{T}p_1$,
State M2	$p_2 = (r_{C1}+r_{D1}+r_{S1})i_{in}^2 + (r_{C2}+r_{S3})i_o^2 + (r_{C1}+r_{C2}+r_{D1}+r_{S1})(i_{in}+i_o)^2$; $P_{2,avg} = \frac{T_b+T_c}{T}p_2$,
State M3	$p_3 = (r_{C1}+r_{D2})i_{in}^2 + (r_{C1}+r_{C2}+2r_{S1})(i_{in}+i_o)^2 + r_{S3}i_o^2$; $P_{3,avg} = \frac{2T_a+T_b}{T}p_3$,
State M4	$p_4 = (r_{D2}+r_{C1})i_{in}^2 + (r_{S2}+r_{C1}+r_{C2})(i_{in}+i_o)^2 + r_{S3}i_o^2$; $P_{4,avg} = \frac{2T_a+T_b}{T}p_4$,
State M5	$p_5 = (r_{D1}+r_{C1}+r_{C2}+r_{S1})i_{in}^2 + (r_{C2}+r_{S3})i_o^2 + (r_{D1}+r_{S1}+r_{C1})(i_{in}+i_o)^2$; $P_{5,avg} = \frac{T_b+T_c}{T}p_5$,
State M6	$p_6 = (r_{D2}+r_{C1}+r_{C2})i_{in}^2 + (2r_{S1}+r_{C1})(i_{in}+i_o)^2 + (2r_{C2}+r_{S3})i_o^2$; $P_{6,avg} = \frac{T_c}{T}p_6$,

where $i_{\rm in}$ and i_o are the input current and load current.

The switching loss of the switches is given by the switches in the switched-capacitor leg (S_a, S_b, S_c and S_d) and the half-bridge leg (S_1, S_2). The power loss of each switch can be calculated as

$$P_{S\_\rm switching} = V_S \cdot I_S \cdot f_{\rm sw} \cdot \frac{(t_{\rm on} + t_{\rm off})}{2} \tag{19}$$

where I_S, V_s, t_{on}, and t_{off} are, respectively, the ON-state current passing through the switch, voltage across the switch, turn-ON delay time, and turn-OFF delay time.

The power loss of each diode can be given by

$$P_{D\_\text{switching}} = Q_{rr} \cdot V_D \cdot f_{\text{sw}} \tag{20}$$

where V_D and Q_{rr} are, respectively, voltage across the diode and reverse recovery charge of diode.

For the capacitor ripple loss calculation, the maximum voltage ripple of capacitor should be evaluated [32], [33]. The voltage ripple of each capacitor can be expressed

$$\Delta v_C = \frac{1}{C}\int_0^{t_k} i_C(t)dt \tag{21}$$

where $i_C(t)$ is the capacitor current in discharging state, and the duration t_k is the maximum discharging time period of capacitor.

Hence, the capacitor voltage ripple losses for capacitors are calculated as

$$\begin{cases} P_{Ci1\_\text{rip}} = P_{Ci2\_\text{rip}} = \frac{1}{4T}C_{i1}(\Delta v_{Ci1})^2 \\ P_{Ca\_\text{rip}} = P_{Ca\_\text{rip}} = \frac{1}{4T}C_a(\Delta v_{Ca})^2 \\ P_{Cb\_\text{rip}} = \frac{1}{2T}C_b(\Delta v_{Cb})^2. \end{cases} \tag{22}$$

Therefore, the total capacitor ripple loss of the proposed SC-based SLI can be derived

$$P_{C\_\text{rip\_total}} = 2P_{Ci1\_\text{rip}} + 2P_{Ca\_\text{rip}} + P_{Cb\_\text{rip}}. \tag{23}$$

III. Simulation and Experimental Results

A. Simulation Results

The performance and operating principle of the proposed SC-based SLI topology are verified in the PLECS simulation platform. In this simulation model, the ON-resistance of all power switches is 73 mΩ while the drop voltage of all power diodes is 1.6 V. All capacitors have the same value of 3300 μF, the reference frequency of 50 Hz, the switching frequency of 10 kHz, and the dc input voltage of 100 V.

Fig. 7 shows the simulation results of the proposed SC-based SLI topology under a resistive load of 40 Ω when an *LC* filter (500 μH + 10 μF) is used at the output terminal of the proposed SC-based SLI topology. In this case, the modulation index is set to 0.8. As shown in Fig. 7(a), the unfiltered output voltage waveform of the proposed SC-based SLI topology has six levels. From Fig. 7(b), we can see that the peak output voltage of the proposed inverter at the fundamental frequency is 190 V and the peak load current is 4.75 A. The THD values of the unfiltered output voltage and load current are 20.2% and 1.05%, respectively. In the steady-state, the average voltages of capacitors C_a, C_b, and C_c are 96.8, 96.3, and 97.2 V, respectively. Furthermore, the peak-to-peak voltages on capacitors C_a, C_b, and C_c are 6.8, 1.3, and 7 V, respectively, as highlighted in Fig. 7(c). As shown in Fig. 7(d), the capacitor C_{i1} voltage and capacitor C_{i2} voltage are around half of the input voltage ($V_{Ci1} = V_{Ci2} = 50$ V). The voltage stress on the power semiconductors is presented in Figs. 7(d)–(f). As shown in Fig. 7(d), the voltage stress on switches S_1 and S_2 is 293 V. From Fig. 7(e), we can see that the

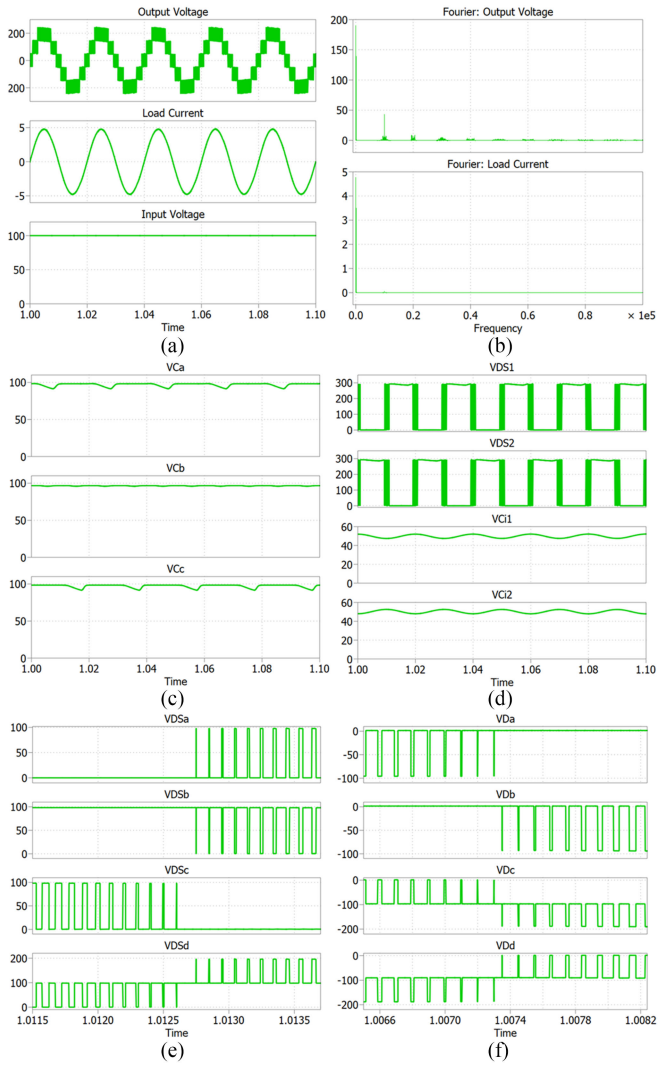

Fig. 7. Simulation results of proposed SC-based SLI topology under unity power-factor condition. From top to bottom. (a) Output voltage, output current, and input voltage. (b) FFT of load current and FFT of output voltage. (c) Voltage waveform across capacitors C_a, C_b, and C_c. (d) Voltage stress on switches S_1 and S_2 as well as capacitor C_{i1} voltage and capacitor C_{i2} voltage. (e) Voltage stress on switches S_a, S_b, S_c, and S_d. (f) voltage stress on diodes D_a, D_b, D_c, and D_d.

voltage stress on the three switches S_a, S_b, and S_c is 98V while the voltage stress on switch S_d is 196 V. As shown in Fig. 7(f), the voltage stress on the two diodes D_a and D_b is 98 V while the voltage stress on the two diodes D_c and D_d is 196 V.

Similar to Fig. 7, Fig. 8 shows the simulation results of the proposed SC-based SLI topology with a purely resistive load 40 Ω and an *LC* filter (500 μH + 10 μF) under various modulation indexes (Mi). In the case of Mi $>$ 0.6, the proposed SC-based SLI topology can produce a six-level voltage waveform at the output. Fig. 8(a) and (b) shows the unfiltered output voltage, load current, and the capacitor C_a voltage and capacitor C_c voltage waveforms of the proposed SC-based SLI topology at Mi = 1 and Mi = 0.7. The maximum voltage level in the output voltage was 245 V, which is approximately 2.5 times the input voltage source, as shown in Fig. 8(a). In the case of 0.2 $<$ Mi $\leq$ 0.6,

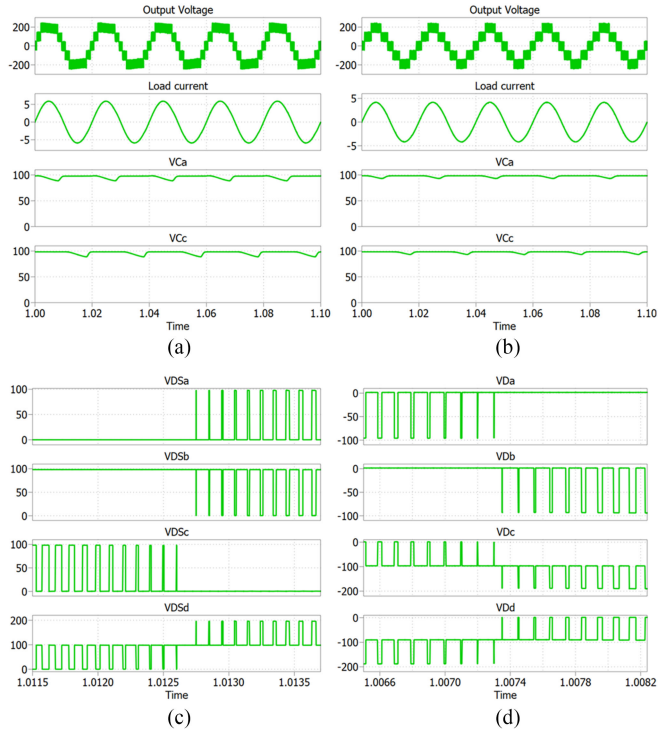

Fig. 8. Simulation results of the proposed SC-based SLI topology at different modulation indices. From top to bottom: output voltage, output current, capacitor C_a voltage, and capacitor C_c voltage. (a) Mi=1. (b) Mi=0.7. (c) Mi=0.5. (d) Mi=0.2.

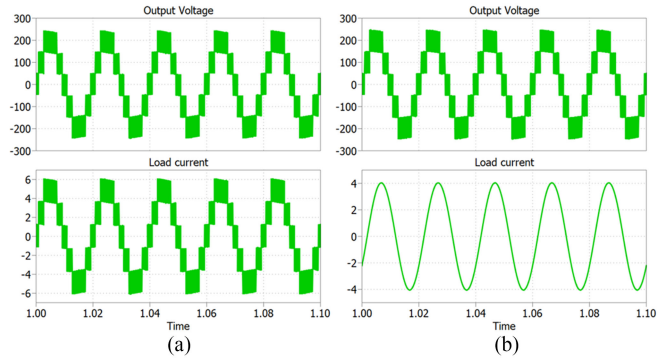

Fig. 9. Simulation results of proposed SC-based SLI topology for different loads. (a) Purely resistive load and (b) Resistive–inductive load.

the proposed SC-based SLI topology can produce a four-level voltage waveform at the output. Fig. 8(c) shows the unfiltered output voltage, load current, capacitor C_a voltage, and capacitor C_c voltage waveforms of the proposed SC-based SLI topology at Mi $= 0.5$.

When Mi is less than 0.2, the proposed SC-based SLI topology only produces two-level voltage waveform at the output. When the proposed SC-based SLI topology is used to power an inductive load (40 Ω + 85 mH) or purely resistive load (40 Ω), the output voltage and load current waveforms of the proposed SC-based SLI topology are highlighted in Fig. 9. As shown in Fig. 9(b), the proposed SC-based SLI topology provides the capability of delivering reactive power at the ac-side. For

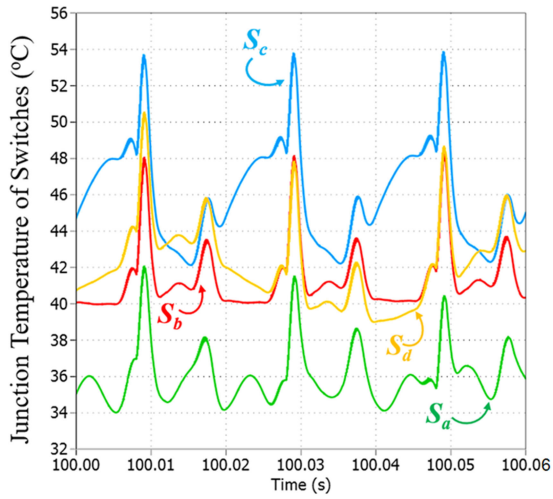

Fig. 10. Junction temperature profiles of switches in the charging path.

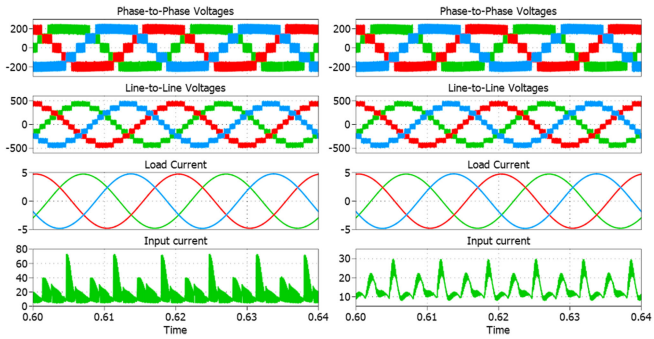

Fig. 11. Simulation results of three-phase SC-based SLI topology with resistive–inductive load. (a) Without using input filter. (b) With using input filter.

thermal analysis, a thermal model of the proposed SC-based SLI topology is built based on PLECS software. In this case, the ambient temperature was set to 25 °C. The output power of the proposed SC-based SLI topology is 800 W. Fig. 10 shows the junction temperature profiles of the switches in the charging path. The temperature of switch S_c is the highest while the temperature of switch S_a is the lowest. As shown in Fig. 10, the temperature of switch S_c reaches the maximum value of 53 °C.

Fig. 11 shows the phase-to-phase output voltage, line-to-line output voltage, and load current and input current of the proposed SC-based SLI topology under a resistive–inductive load of 40 Ω—100 mH/ phase. As indicated in Fig. 11, the RMS value of the load currents is 3.71 A_{rms}. Without using an input filter, as shown in Fig. 1(b), the input current stress of the proposed SC-based SLI topology is very high, as highlighted in Fig. 11(a). To limit the input current stress of the proposed SC-based SLI topology, a small LC input filter with 1 μH—1 μF is used. As shown in Fig. 11(b), the input current stress of the proposed SC-based SLI topology is significantly reduced.

B. Experimental Results

To prove the performance and practicality of the proposed SC-based SLI topology, a laboratory prototype of the proposed

TABLE V
SPECIFICATIONS OF THE EXPERIMENTAL SETUP

Parameters		Values
Input voltage, V_{dc}		100 V
Fundamental frequency		50 Hz
Switching frequency		10 kHz
Capacitors	C_a, C_b, and C_C	3300 μF
	C_{i1} and C_{i2}	2200 μF
Power switches		N-MOSFET, FCH47N60F
Power diodes		DSEI 30-06A
Controller		DSP TMS320F280049C
Output load	Resistive load Z_1	40 Ω
	Inductive load Z_2	40 Ω / 85 mH
Output filter	Filter inductor	500 μH
	Filter capacitor	10 μF

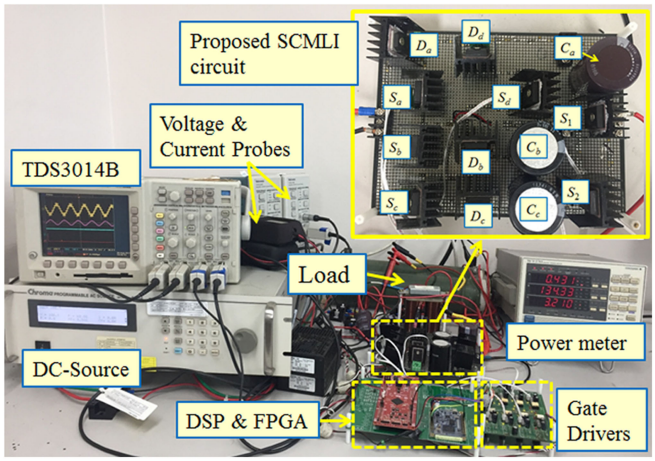

Fig. 12. Experimental setup of the proposed SC-based SLI.

SC-based SLI topology has been built. To limit the peak-to-peak voltage ripple of C_a and C_c to 13% and that of C_b to 3%, the capacitance of the selected capacitances of C_a, C_c and C_b is 3300 μF. The parameters of the proposed SC-based SLI topology used for the experiment are given in Table V. Fig. 12 depicts an experimental setup and zoomed version with switches, diodes and capacitors for the proposed SC-based SLI in the laboratory.

Fig. 13 shows the experimental waveforms when the proposed SC-based SLI topology powers a resistive load Z_1 and an LC filter is used at the output terminal; in this case, the modulation index is set to 0.81. From Fig. 13(a), we can see that the proposed SC-based SLI topology produces a six-level output voltage of 133 $V_{\rm rms}$ at the fundamental frequency from the input dc voltage of 100 V. The peak load current is 4.7 A. The THD value of load current is 0.9%. As shown in Fig. 13(b), the voltage stress on switches S_1 and S_2 is 290 V. As shown in Fig. 13(b), the capacitor C_{i1} voltage and capacitor C_{i2} voltage are around half of the input voltage ($V_{Ci1} = V_{Ci2} = 50$ V). The voltage stress on power semiconductors is presented from Fig. 13(b) and (d). Fig. 13(c) shows that the voltage stress on the three switches S_a, S_b, and S_c is 95 V, while the voltage stress on switch S_d is 191 V. As shown in Fig. 13(d), the voltage stress on two diodes D_a, and D_b is 96 V, while the voltage stress on two diodes D_c and D_d is 193 V. In the steady-state, the average capacitor C_a, C_b, and C_c voltages are 94.6, 94.1, and 95.3 V, respectively. In addition, the

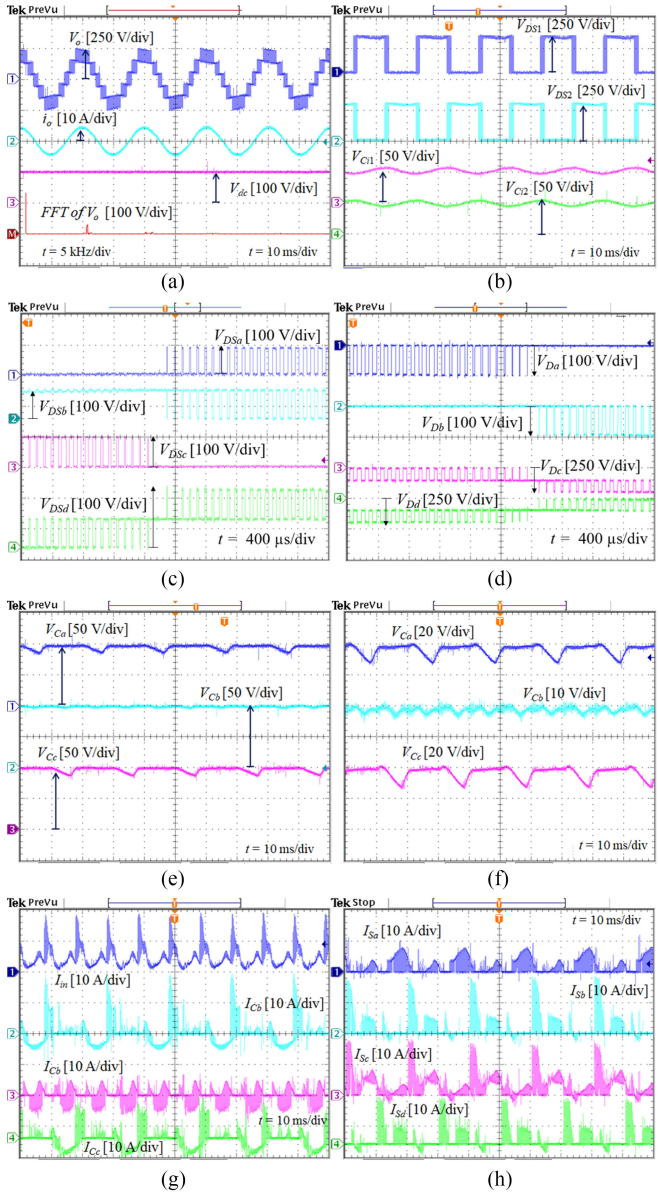

Fig. 13. Experimental results of proposed SC-based SLI topology under unity power-factor condition. From top to bottom. (a) Output voltage before the filter, load current, input voltage, and FFT of output voltage. (b) Voltage stress on switches S_1 and S_2, capacitor C_{i1} voltage and capacitor C_{i2} voltage. (c) Voltage stress on switches S_a, S_b, S_c, and S_d. (d) Voltage stress on diodes D_a, D_b, D_c, and D_d. (e) Voltage waveform across capacitors C_a, C_b, and C_c. (f) Enlarged view of (e). (g) Input current, current of capacitors C_a, C_b, and C_c. (h) Current stress on switches S_a, S_b, S_c, and S_d.

peak-to-peak voltage ripples on capacitors C_a, C_b, and C_c are 12.2, 3, and 12.5 V, respectively, as highlighted in Fig. 13(e) and (f). Moreover, the input current, capacitors current, and current across the switches are illustrated in Fig. 13(g) and (h).

When the Mi is set to 1 and 0.5, the experimental waveforms of the proposed SC-based SLI topology are shown in Fig. 14. Fig. 14(a) shows the six-level voltage waveform at the output, load current, capacitor C_a voltage, and input current waveforms of the proposed SC-based SLI topology at Mi = 1. The maximum voltage level in the output voltage is 236 V, which is approximately 2.5 times the input voltage source, as shown in

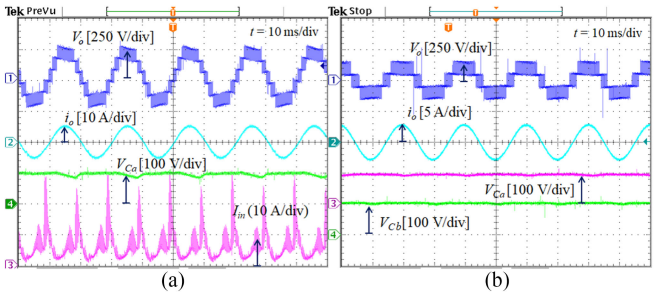

Fig. 14. Experimental results of proposed SC-based SLI topology at different modulation indexes. From top to bottom. (a) Output voltage before the filter, load current, capacitor C_a voltage, and input current when Mi = 1. (b) Output voltage before the filter, load current, and capacitor C_a and C_b voltage when Mi = 0.5.

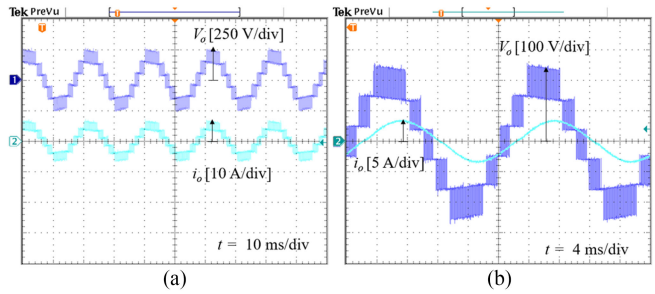

Fig. 15. Experimental results of proposed SC-based SLI topology for different loads. (a) Purely resistive load. (b) Resistive–inductive load.

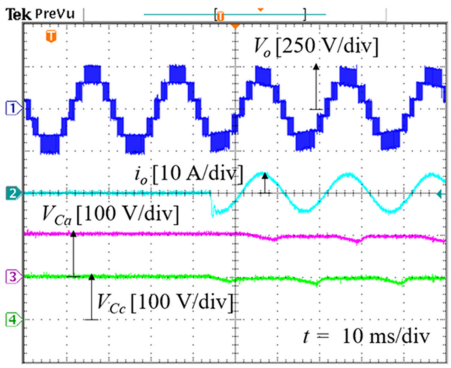

Fig. 16. Experimental waveforms of proposed SC-based SLI topology during load transient.

Fig. 14(a). In addition, Fig. 14(b) shows the four-level output voltage, load current, capacitor C_a voltage, and capacitor C_c voltage waveforms of the proposed SC-based SLI topology at Mi = 0.5.

When the proposed SC-based SLI topology powers the inductive load Z_2 or the resistive load Z_1 without an output filter, the output voltage and load current waveforms are highlighted in Fig. 15. As shown in Fig. 15(b), the proposed SC-based SLI topology provides the capacity of delivering reactive power at the ac-side like the simulation results shown in Fig. 9. The dynamic behavior of the proposed topology during load transient is provided in Fig. 16. We can see that when the load was suddenly switched from no load to 450 W, the load current quickly reached a sinusoidal current of 4.7 A.

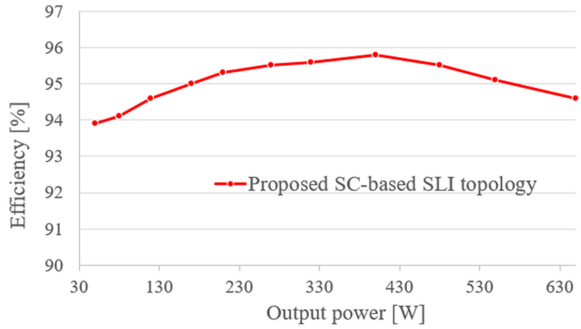

Fig. 17. Measured efficiency versus output power of the proposed SC-based SLI topology.

TABLE VI
PARAMETERS FOR POWER LOSS ANALYSIS

Parameters		Values
Capacitors	C_a, C_b, C_C	32 mΩ
	C_{i1} and C_{i2}	51 mΩ
Power switches		FCH47N60F (600 V, 47 A, R_{DSon} = 73 mΩ)
Power diodes		DSEI 30-06A (600V, 30A, VF=1.52V)

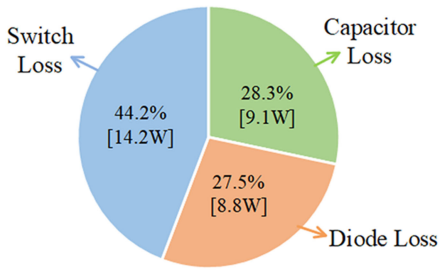

Fig. 18. Power loss for the proposed SC-based SLI topology.

A digital power meter Yokogawa WT230 is used to measure the efficiency of the proposed SC-based SLI topology. With varying output power, the efficiency of the proposed SC-based SLI topology was measured with various output power when $V_{\rm dc}$ = 100 V and output voltage of 135 $V_{\rm rms}$. As shown in Fig. 17, the highest efficiency of the laboratory prototype was 95.8% at 400 W.

Tables V and VI list the parameters of the proposed SC-based SLI topology for power loss calculation. Note that, to confirm the measured efficiency, the parameters for power loss analysis are selected based on the specifications of the experimental setup. Fig. 18 shows the power loss breakdown comparison between the two proposed methods when $V_{\rm dc}$ = 100 V, $f_{\rm sw}$ = 10 kHz, V_o = 135 $V_{\rm rms}$, and P_o = 600 W. As shown in Fig. 18, the power losses of switches, diodes, and capacitors are 44.2%, 27.4%, and 28.3%, respectively.

IV. CONCLUSION

In this article, the single-phase switched-capacitor-based six-level inverter topology and its three-phase counterpart are proposed. The proposed topology can be used to develop a six-level output voltage waveform, which leads to reduce the output filter size. Furthermore, the proposed topology possesses voltage

boosting capability with a maximum voltage level 2.5 times the input voltage. Similar to the single-phase configuration of proposed inverter, a single dc voltage source is used to charge all the capacitors in a three-phase configuration. The use of a single dc voltage source in both single-phase and three-phase configurations along with the self-balancing nature of the capacitor voltages is the other fascinating features of the proposed inverter. Furthermore, the leakage current, which is one of the key factors in PV applications, is effectively attenuated in the proposed inverter. However, the proposed inverter is not able to produce the zero voltage level. The operating principles and circuit description of the proposed inverter are provided. A comparative study with similar multilevel inverter topologies confirms the benefits of the proposed topology. Simulation and experimental tests associated with the efficiency measurement are presented to assess the feasibility of the proposed topology.

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