A Periodic-Steady-State Analysis Model in Time Domain for Dual Active Bridge Converter

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***Abstract*—This article forms a multitime-scale modeling method through a time-domain analysis, using both ideal steady-state processes and finite switching transient processes for increased accuracy of dual active bridge (DAB) converters. All possible operating modes and the corresponding state equations are derived from the switching transient process for a five-degrees-of-freedom-modulated DAB converter based on the unified equivalent circuit. The nonlinear parasitic capacitors are considered in this process. A periodic-steady-state analysis model is established to accurately predict the residual voltage under incomplete zero-voltage switching. This method is applicable for all phase-shift-modulated DAB converters, and the calculation time is reduced 28–61 times compared with LTspice simulation. Finally, the simulation and experimental results are compared to validate the effectiveness of the model.**

***Index Terms*—Dual active bridge (DAB), modulation scheme, periodic-steady-state model, zero-voltage switching (ZVS).**

I. INTRODUCTION

THE dual active bridge (DAB) converter is considered as a core power conversion unit for future smart energy systems due to its bidirectional power-flow capability, flexible control capability, and wide soft-switching range [1]–[3], and it is widely used in power electronic transformers (PETs) [4], [5], electric vehicles (EVs) [6], and energy storages (ESs) [7]. The topology of the DAB converter is illustrated in Fig. 1 where two active full-bridges are modulated to apply ac voltages (v_{ab} and v_{cd}) across the equivalent inductor L from the high-frequency transformer to control the current so does the power flow of the converter.

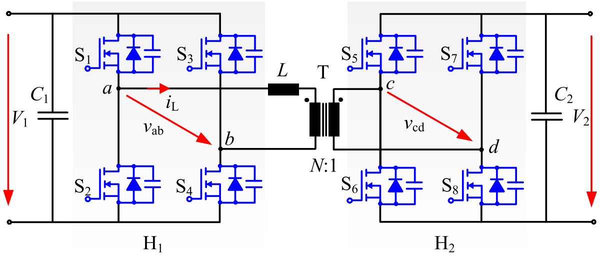

Fig. 1. Topology of DAB converter.

Mathematical modeling is the basis for the steady-state analysis and design of the DAB converter. In [8], a simple average power model for the phase-shift modulation (PSM) scheme was developed and used for hardware design. Although PSM is simple with only one degree of control freedom, a large amount of reactive power is generated and zero-voltage switching (ZVS) operation cannot be maintained when the input or output dc voltage of the converter varies a lot [1]. Many multidegrees-of-freedom modulation schemes have been developed to address this issue. However, the complexity increases with the increase of the degree of freedom (DOF). In [9], the model with triple-phase-shift (TPS) modulation scheme has been modeled into 12 operating modes by complete operating mode classification method in the time domain. In [10], a universal steady-state model for the high-frequency-link electrical quantities under TPS was developed by using Fourier series. In [11], a model-based superposition method having six operating modes was derived by analyzing the DAB converter full-bridge voltage and a complex inductor current waveform under TPS. In [12], 11 effective modes based on a five-degrees-of-freedom (5-DOF) modulation scheme were analyzed, and the expressions of the inductor peak-to-peak current and transmission power are established. In these models, power switches are considered ideal devices for simplicity without considering the nonlinear behavior of power switches during the finite transient time. However, this simplification fails to accurately evaluate optimizing design parameters and the dead time for different modulation schemes. For instance, it is impossible to determine if a complete ZVS has been achieved when the turn-ON time of the switch is neglected by the simplified method. Besides, it leads to an inaccurate prediction of the transmitted power and the inductor root-mean-square (rms) current [13]. Therefore, it is important to include the finite switching transient processes of power switches and to establish a complete mathematical model.

Manuscript received March 30, 2021; revised July 1, 2021, September 28, 2021, and November 7, 2021; accepted November 8, 2021. Date of publication November 15, 2021; date of current version December 31, 2021. Recommended for publication by Associate Editor A. Davoudi. *(Corresponding author: Quanming Luo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3127926.

Digital Object Identifier 10.1109/TPEL.2021.3127926

The accuracy and practicality are two critical requirements for the complete model [14]. In [13], a detailed switching transition model was incorporated with the traditional ideal frequency-domain modeling in an iterative fashion, and an improved modeling technique was proposed. The method is flexible and versatile, but it does not consider the influence of modulation schemes, which can alter the current loop in the transient process. When considering different current loops, the frequency-domain analysis (FDA) cannot meet the requirements, and only time-domain analysis (TDA) methods can be used. In [15], an improved DAB-based generalized power-flow model was derived, although the model takes the dead time and resonant commutation of the converter into account, the model is based on the simplest PSM modulation and cannot be well applied to other optimal modulation schemes, which restricts the application of this model. Various commercial power electronics simulation software (such as MATLAB, LTspice, and Saber) have been widely used for establishing a more accurate model of the converter. However, they require not only solving the system of ordinary differential equations (ODE) but also determining the operating timing and operation law of each power switch, as well as extracting nonideal model data, causing longer computing time. Therefore, these two conflicting performance tradeoffs in terms of accuracy and practicality still exist for the above models and methods.

In this article, an attempt is made to take the finite switching transition process into account in the analysis model. It is complex and difficult to model this multitime-scale containing both the behavior of power switches at the dead time (*n*s scale) and the conduction behavior of power switches at each modulation degree of freedom (μs scale). For the power devices, the transient process is described by fitting the law of nonlinear variation of the parasitic capacitance with the drain–source voltage according to the device datasheet, which is computationally inexpensive and accurately. Second, the analysis is discussed based on the most general 5-DOFs modulation scheme in order to consider all possible cases under multiple modulation DOF. It is worth mentioning that, to consider the effects of multiple loops, the TDA is the most appropriate approach. Therefore, a multitime-scale modeling method is formed by simultaneously considering the ideal steady-state process and finite transition process in the TDA for a 5-DOF modulation scheme. Finally, a periodic-steady-state analysis model (PSSAM) is developed in this article. Compared with previous methods and models, first it can accurately predict the residual voltage under incomplete ZVS; second, it is applicable for all phase-shift-modulated DAB since it is based on the 5-DOF modulation scheme for analysis; third, the calculation time is reduced by around 28–61 times when compared with LTspice simulation. It is worth noting that this model can be extended to other variants of the DAB converter structure with nothing more than a variation of the state equation. In summary, PSSAM is more accurate when compared with the current common methods, such as the FDA method, and faster than the numerical calculation iterative methods, such as circuit simulation.

The rest of this article is organized as follows. Section II presents the framework of the complete time-domain steady-state modeling approach based on the 5-DOF modulation scheme. The circuit analysis of the ideal steady-state process is carried out, and 16 situations are uniformly described in Section III. In Section IV, the operating modes in the finite transient process are discussed with considering the influence of the modulation scheme. The complete modeling steps are presented in Section V. Compared with the result of LTspice software, the validity and correctness of the proposed model are verified by the experiment in Section VI. Finally, Section VII concludes this article.

II. MODELING APPROACH

In this section, the basic structure of the DAB converter is introduced, and the 5-DOF modulation scheme and its relationship with other basic phase shift techniques are briefly discussed. The idea of its modeling may be changed after considering the switching transition process. Accordingly, a novel framework for a complete time-domain steady-state modeling approach is given.

A. Introduction of Topology and Its Modulation Scheme

The schematic diagram of the DAB converter is plotted in Fig. 1. Each device plays a different role in the converter. Specifically, S_1–S_8 are power devices that are controlled to simultaneously generate a specific power pulse or sequence according to certain combination rules. The inductor L determines the maximum power that can be transmitted by the converter. Capacitors C_1 and C_2 are used to filter and stabilize the port voltages, and the high-frequency transformer mainly undertakes the function of electrical isolation and voltage matching. In this article, it is assumed that input voltage V_1 is always greater than the equivalent output voltage NV_2, where N is the turns ratio of the high-frequency transformer. A similar analysis can be performed for the condition "$V_1 < NV_2$" due to the symmetrical structure [16].

Among multi-DOF modulation schemes, phase-shift techniques are the most common approach for DAB converter, which enables the generation of voltage square waves or quasi-square waves with relative phase shifts at the primary and secondary of an HF transformer, thus regulating the power flowing through the converter. This method is easy to be implemented and only needs to be modified at the software level without modifying the hardware. According to the number of DOF, it includes PSM with only 1-DOF, extended phase shift (EPS) [17], and dual phase shift (DPS) [18] modulation schemes with 2-DOF, TPS modulation scheme [19], and asymmetric duty modulation (ADM) [20] scheme with 3-DOF and 5-DOF modulation schemes. Fig. 2 shows the relationship between these modulation schemes, where the arrow indicates the containment relationship. It can be seen from Fig. 2 that PSM, EPS, DPS, TPS, and ADM are special cases of the 5-DOF. These modulation schemes are significantly different in terms of the extension of the soft-switching range and the reduction of inductor rms current. More DOF represents more potential optimization can be added. Therefore, the modeling is performed based on 5-DOF in this article as the general case.

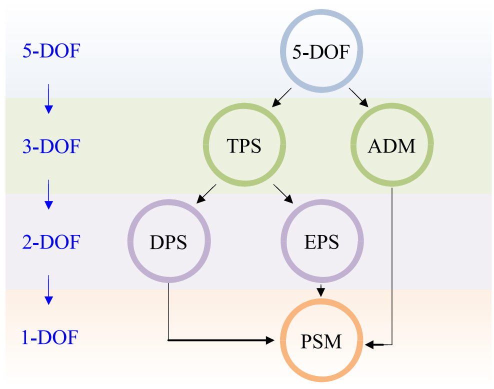


Fig. 2. Relationship between different modulation schemes.

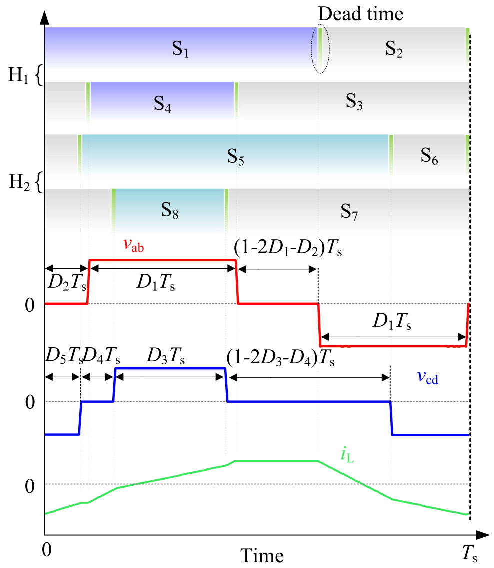
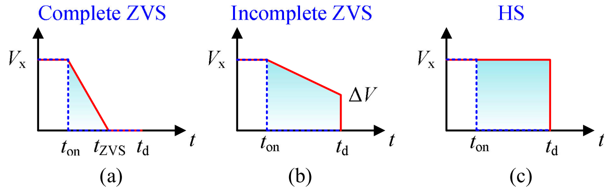


Fig. 3. Typical waveforms of the 5-DOF modulation scheme.

In 5-DOF, the transformer primary and secondary ac voltage waveforms consist of two voltage pulses of opposite polarity, with each switching period containing two unequal zero-voltage sections, as shown in Fig. 3. In Fig. 3, for the primary side, the duration of the high and low levels of v_{ab} is defined as $D_1 T_{\mathrm{s}}$, and $D_2 T_{\mathrm{s}}$ is the phase shift between switches S_1 and S_4. Similarly, for the secondary, the duration of the high and low levels of v_{cd} is defined as $D_3 T_{\mathrm{s}}$, and $D_4 T_{\mathrm{s}}$ is the phase shift between switches S_5 and S_6. Moreover, there is another independent DOF, that is, the phase shift between switches S_1 and S_5, which is defined as $D_5 T_{\mathrm{s}}$. These 5-DOF are used to jointly control the magnitude and direction of the power.

B. Switching Behavior in Finite Transition Process

A dead time (t_{d}) needs to be inserted between the complementary devices in the same leg (e.g., S1 and S2) to avoid shoot-through [21], as shown in Fig. 3. The switching transition behavior during the dead time needs to be modeled to achieve the expected ZVS. Several factors need to be considered specifically for a complete ZVS. 1) Current direction: Before the power switch is turned ON, the inductor current needs to flow through its body diode, which is the precondition to realize the complete ZVS. 2) Energy: The energy stored in the inductor should be greater than the total energy stored in the parasitic capacitor C_{oss} of the upper and lower arm switches [19], [22], [23]. When the transition process is over, the voltage across the turn-ON switch drops to zero, and the transition time is defined as the minimum complete ZVS time (t_{ZVS}) in this article. Therefore, when the complete ZVS occurs, the dead time is usually not less than this time. Fig. 4(a) gives the voltage variation across the power switch for the complete ZVS, where the voltage drops to zero before the dead time. Incomplete ZVS can occur either if the energy stored in L is too low or if the dead time is too short to accomplish the complete charging/discharging, as depicted in Fig. 4(b). The incomplete ZVS causes residual voltage ΔV across the turning ON a switch. When the direction of the current flowing through the power switch does not satisfy the prerequisites for complete ZVS, a hard switching (HS) turn-ON will occur, as shown in Fig. 4(c). In Fig. 4, the blue dashed line indicates the ideal transition and the actual voltage transition is shown in the red line. There are three possible behaviors of the power switches during the finite switching transition process as described above.



(a) (b) (c)

Fig. 4. Different switching behaviors of the power switch, the blue dashed line indicates the ideal transition and the actual voltage transition is shown in red. (a) Complete ZVS turn ON. (b) Incomplete ZVS turn ON. (c) HS turn ON.

C. Novel Time-Domain Steady-State Modeling Framework

In terms of power device models, there are mainly linear models [23], fitted models [24], and physical models [25]. The linear model uses linearized assumptions or lookup table method to describe the transient process of power switches, which is computationally less expensive but has lower adaptability and accuracy; the fitted model describes the transient process by fitting the nonlinear variation of the parasitic capacitor with the drain–source voltage in the power device datasheet, which is computationally less expensive and has improved accuracy relative to the linear model; the physical model is the precise mathematical modeling of the physical mechanism of the device transient process, which usually simulates the switching device in the form of a high-order nonlinear equivalent circuit, and can accurately describe the process of switching transient electromagnetic energy conversion, but the process is more complex and time-consuming to solve. In this article, the fitted model is used to build the power devices. The TDA is chosen to discuss and analyze the 5-DOFs modulation scheme.

Fig. 5 gives the framework for the complete modeling of the multitime-scale modeling approach, which mainly includes the design space and the operation space. The design space refers to the selection of device materials, circuit components, system parameters, etc., while the division and summarization

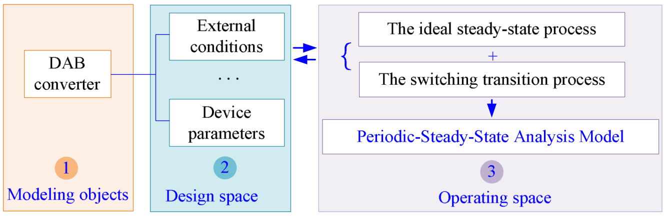


Fig. 5. Novel time-domain steady-state modeling framework.

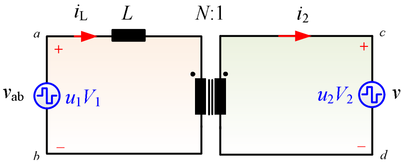


Fig. 6. Equivalent circuit of DAB converter in the ideal steady-state process.

of each process in the operation space is the focus of this article. Different state equations according to the ideal equivalent circuit of 5-DOF-modulated DAB are established first. Then possible operating modes in the finite transition process are considered. In order to synthesize a stable waveform, steady-state characteristics such as the initial value of inductor current and transmitted power need to be iterated repeatedly until the requirements are met. Before establishing the complete model, the waveform synthesis is simplified as follows: First, all devices are considered as lossless devices; second, electromagnetic and thermal coupling are ignored.

III. IDEAL STEADY-STATE MODELING

This section mainly introduces the ideal steady-state process and the equivalent circuit is shown in Fig. 6. Under 5-DOF, the waveforms of v_{ab} and v_{cd} are composed of the zero-voltage, high-voltage, and low-voltage portions. The high-voltage, low-voltage, and zero-voltage portions are represented by "1," "-1," and "0," respectively, during each switching period in the following. Considering the possible values of v_{ab} and v_{cd} in different switching states, u_1 and u_2 are used to define the relationship of ac voltage with their corresponding dc terminal voltage as shown in

$$\begin{cases} v_{\mathrm{ab}} = u_1 V_1 \left(u_1 = -1, 0, 1\right) \\ v_{\mathrm{cd}} = u_2 N V_2 \left(u_2 = -1, 0, 1\right) \end{cases} \tag{1}$$

where u_1 and u_2 mainly depend on the conduction state of the primary- and secondary-side power switches. For example, u_1 is "1" when switches S_1 and S_4 are in the conduction state; u_1 is "0" when switches S_1 and S_3 are in the conduction state; u_1 is "-1" when switches S_2 and S_4 are in the conduction state. Similarly, the state of u_2 can be obtained. According to the modulation rule of 5-DOF, 8 switches on the primary and secondary sides can form a total of 16 combinations, as shown in Table I. "1" indicates that the power switch is in the conduction state and "0" indicates that the switch is in the OFF state in Table I. Each case has its own expression, for example, λ_{1357} indicates that switches S_1, S_3, S_5, and S_7 are all in the conduction state while the other switches corresponding to the complementary bridge arms are in the OFF-state. In Fig. 3, with the conduction of switch S_1 as the zero-moment point, the conduction processes of its power switches in one switching period are sequentially λ_{1367}, λ_{1357}, λ_{1457}, λ_{1458}, λ_{1457}, λ_{1357}, λ_{2357}, λ_{2367}. Thus, for all possible steady-state processes in one switching period, there are no more than eight cases listed in Table I.

TABLE I
ALL COMBINATION OF SWITCH STEADY-STATE PROCESS IN 5-DOF

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	u_1	u_2
λ_{1357}	1	0	1	0	1	0	1	0	0	0
λ_{1457}	1	0	0	1	1	0	1	0	1	0
λ_{2457}	0	1	0	1	1	0	1	0	0	0
λ_{2357}	0	1	1	0	1	0	1	0	-1	0
λ_{1358}	1	0	1	0	1	0	0	1	0	1
λ_{1458}	1	0	0	1	1	0	0	1	1	1
λ_{2458}	0	1	0	1	1	0	0	1	0	1
λ_{2358}	0	1	1	0	1	0	0	1	-1	1
λ_{1368}	1	0	1	0	0	1	0	1	0	0
λ_{1468}	1	0	0	1	0	1	0	1	1	0
λ_{2468}	0	1	0	1	0	1	0	1	0	0
λ_{2368}	0	1	1	0	0	1	0	1	-1	0
λ_{1367}	1	0	1	0	0	1	1	0	0	-1
λ_{1467}	1	0	0	1	0	1	1	0	1	-1
λ_{2467}	0	1	0	1	0	1	1	0	0	-1
λ_{2367}	0	1	1	0	0	1	1	0	-1	-1

Combined with the equivalent circuit diagram of the ideal steady-state process, the equation can be calculated as

$$L\frac{di_L\left(t\right)}{dt} = u_1 V_1 - N u_2 V_2. \tag{2}$$

As shown in Fig. 3, the zero-moment point in this article is chosen as the moment of switch S_1 turn-ON, so its voltage initial value can be determined while the inductor current initial value needs to be calculated and its expressions for different modes are referred to the literature [12]. It is worth mentioning that the inductor current initial value is very important for the steady-state analysis of the DAB converter because it is directly related to the transmitted power, the inductor rms current, and the switching behavior. Given $i_{\mathrm{L}}(t = 0) = I_{\mathrm{L0}}$, following equation can be derived from (2):

$$i_L\left(t\right) = \frac{u_1 V_1 - u_2 N V_2}{L} \cdot t + I_{\mathrm{L0}}. \tag{3}$$

The solution of the inductor current of (3) can be used to uniformly represent the different cases of power switches in the ideal steady-state process, with some differences in the coefficients. On this basis, the circuit analysis and expression derivation of the ideal steady-state processes have been completed, and the analysis process is relatively simple. The details of the switching transition processes are discussed in the following sections.

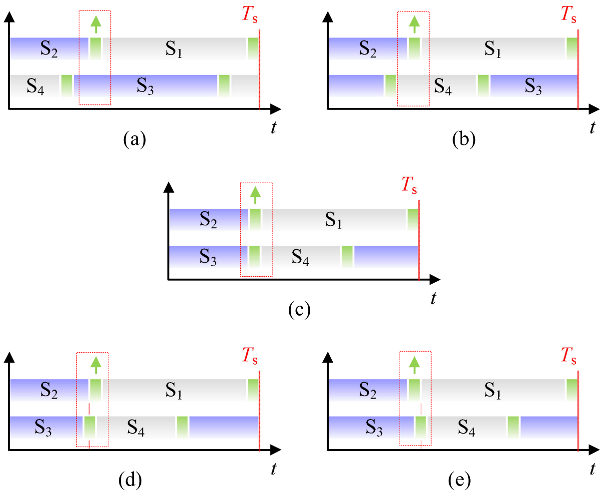


Fig. 7. When the switch S_1 is turned ON, the state of other switches is on the primary side. (a) S_3 is in the conduction state. (b) S_4 is in the conduction state. (c) S_4 is also turned ON at the same time. (b) S_4 is turned ON a little later, but the time is less than the dead time. (5) S_4 is turned ON a little later, but the time is less than the dead time.

IV. SWITCHING TRANSITION PROCESS MODELING

In the switching transition process, the power device model considers only the most critical physical process, i.e., the semiconductor parasitic capacitor varies with the drain–source voltage of the switch. As a result, the number of orders inside the circuit loop is reduced to accelerate the calculation while ensuring sufficient accuracy.

Section II shows that the power switches have different behavioral characteristics when the current direction and magnitude are different. When the power switch on one bridge arm is turned ON, the switch on the other bridge arm may be in a different state during the transition. Taking switch S_1 as an example, when S_1 is turned ON, there are following several cases.

1) S_3 is in the conduction state, as shown in Fig. 7(a).
2) S_4 is in the conduction state, as shown in Fig. 7(b).
3) S_4 is also turned ON at the same time, as shown in Fig. 7(c).
4) S_4 is turned ON earlier, but the time is less than the dead time, as shown in Fig. 7(d).
5) S_4 is turned ON later, but the time is less than the dead time, as shown in Fig. 7(e).

Combined with the three possible switching behaviors caused by the different magnitudes and directions of the inductor currents introduced in Section II, those five different switching processes would form 15 cases, and all of them have their own expressions. Assuming the primary and secondary power switches cannot be turned ON and OFF simultaneously, these cases are discussed in detail.

A. Current Meets the Precondition of ZVS

The direction of the inductor current i_L should be less than zero when it meets the precondition of ZVS in the case of power switch S_1 turned ON. At this moment, the switch S_1 either achieves complete ZVS or incomplete ZVS, depending on the magnitude of the inductor current.

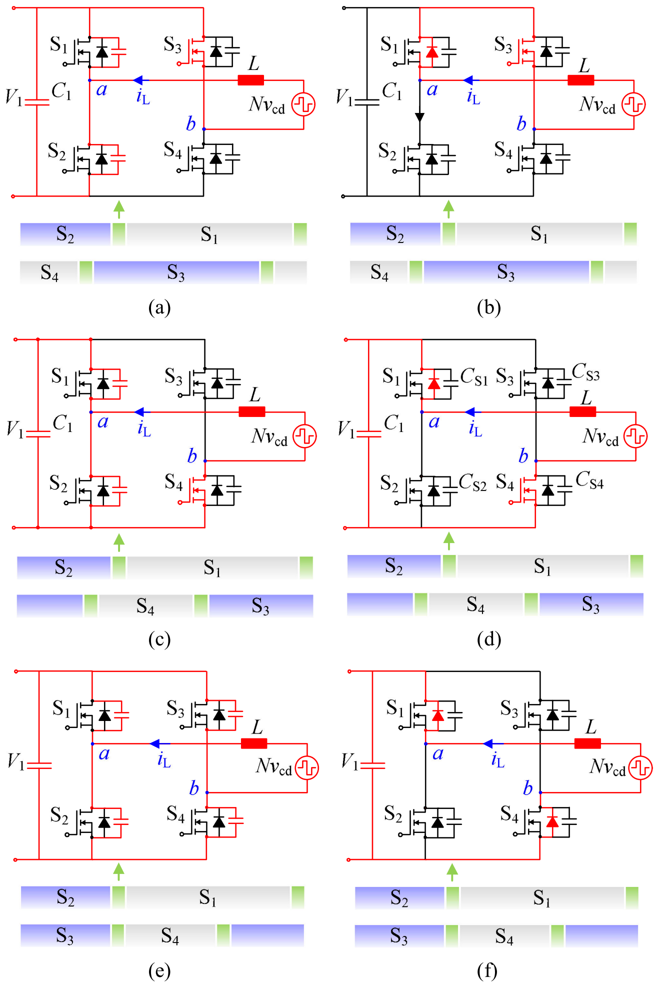


Fig. 8. Diagram of current flow in different cases when the inductor current satisfies the ZVS precondition when switch S_1 is turned ON. (a) Switch S_3 is in the conduction state, and switch S_1 realizes the incomplete ZVS or the first process of complete ZVS. (b) Switch S_3 is in the conduction state, and switch S_1 realizes the second process of complete ZVS. (c) Switch S_4 is in the conduction state, and switch S_1 realizes the incomplete ZVS or the first process of complete ZVS. (d) Switch S_4 is in the conduction state, and switch S_1 realizes the second process of complete ZVS. (e) Switch S_4 is also turned ON at the same time, and switch S_1 realizes the incomplete ZVS or the first process of complete ZVS. (f) Switch S_4 is also turned ON at the same time, and switch S_1 realizes the second process of complete ZVS.

The first of the above five cases, i.e., when the power switch S_3 is in the conduction state power switch and S_1 is turned-ON is discussed as follows. When the current is too low to release the energy of the parasitic capacitor, the switching behavior of the S_1 is incomplete ZVS, and its current flow diagram is shown in Fig. 8(a). Inductor current i_L transfers energy from the parasitic capacitor of S_1 to the parasitic capacitor S_2, thereby forming different current flow directions. The first case can be seen as the current flowing through a parasitic capacitor of S_2, input voltage V_1, inductor L, equivalent power supply on the secondary side Nv_{cd} and switch S_3. The second case can be seen as the current flowing through the parasitic capacitor of S_1, L, Nv_{cd}, and S_3. In order to accurately quantify this exchange of energy, the mathematical expression is established as

$$\begin{cases} V_1 - v_{\mathrm{S2}}(t) + L\dfrac{di_L(t)}{dt} + Nv_{\mathrm{cd}} = 0 \\ v_{\mathrm{S1}}(t) = v\, v_{\mathrm{S2}}(t) = V_1 - v \\ i_L(t) = C_{\mathrm{coss1}}(V_1 - v)\dfrac{dv_{\mathrm{S2}}(t)}{dt} - C_{\mathrm{coss1}}(v)\dfrac{dv_{\mathrm{S1}}(t)}{dt}. \end{cases} \tag{4}$$

In (4), the first equation is listed for the first case mentioned above. The second equation reveals the voltage relationship between the parasitic capacitors of power switches S_1 and S_2, whose sum is always equal to the input voltage. The third equation is listed based on node *a* that the sum of the currents flowing into node *a* is equal to the sum of the currents flowing out of node *a*, where *v* is defined as the voltage when the complementary switch is turned ON, and *v* in (4) shows the voltage across the switch S_2, where C_{oss1} is the parasitic capacitor of the switch on the primary side.

When the current is large enough to release the energy of the parasitic capacitor, the switching behavior of S_1 achieves complete ZVS. In addition to the process in Fig. 8(a), the second process, as shown in Fig. 8(b) exists. The current flow is relatively simple, flowing through the body diode of S_1, the power switch S_3, the inductor *L,* and equivalent power supply on the secondary side Nv_{cd}, which satisfies

$$L\frac{di_L(t)}{dt} + Nv_{\mathrm{cd}} = 0. \tag{5}$$

In summary, when the switch S_1 realizes incomplete ZVS, it has only one process, whereas when switch S_1 realizes complete ZVS, there is a second process in addition to the first one during the finite switching transition time, which is defined in this article as $\xi_{1\_3\mathrm{S}\_\mathrm{I}}$ and $\xi_{1\_3\mathrm{S}\_\mathrm{II}}$, respectively. The subscript "1" means power switch S_1 is ON; "3" means power switch S_3 is in the conduction state; "S" means that the switch may achieve soft switching; "H" means HS; "I" means the first process; "II" means the second process.

The second of the above five cases is discussed, that is, the power switch S_4 is in the conduction state when power switch S_1 is turned ON. Like the first case, it also has two processes $\xi_{1\_4\mathrm{S}\_\mathrm{I}}$ and $\xi_{1\_4\mathrm{S}\_\mathrm{II}}$ as shown in Fig. 8(c) and (d), respectively. The expression established in the first process is

$$\begin{cases} V_1 - v_{\mathrm{S1}}(t) - L\dfrac{di_L(t)}{dt} - Nv_{\mathrm{cd}} = 0 \\ v_{\mathrm{S1}}(t) = V_1 - v\, v_{\mathrm{S2}}(t) = v \\ i_L(t) = C_{\mathrm{coss1}}(V_1 - v)\dfrac{dv_{\mathrm{S1}}(t)}{dt} - C_{\mathrm{coss1}}(v)\dfrac{dv_{\mathrm{S2}}(t)}{dt}. \end{cases} \tag{6}$$

The expression established in the second process is

$$L\frac{di_L(t)}{dt} + Nv_{\mathrm{cd}} = V_1. \tag{7}$$

The third of the above five cases is discussed as follows. The power switch S_4 is turned ON at the same time when power switch S_1 is turned ON. The two corresponding processes are $\xi_{1\mathrm{a}4\mathrm{S}\_\mathrm{I}}$ and $\xi_{1\mathrm{a}4\mathrm{S}\_\mathrm{II}}$ as shown in Fig. 8(e) and (f). The subscript is different from the previous, where "a" means that switches S_1 and S_4 are ON at the same time. In the first process, the parasitic capacitors of all four switches are involved in resonance with the inductor *L*. The expression established in the first process is

$$\begin{cases} V_1 - 2v_{\mathrm{S1}}(t) - L\dfrac{di_L(t)}{dt} - Nv_{\mathrm{cd}} = 0 \\ v_{\mathrm{S2}}(t) = v\, v_{\mathrm{S1}}(t) = V_1 - v \\ i_L = C_{\mathrm{coss1}}(V_1 - v)\dfrac{dv_{\mathrm{S1}}(t)}{dt} - C_{\mathrm{coss1}}(v)\dfrac{dv_{\mathrm{S2}}(t)}{dt}. \end{cases} \tag{8}$$

The expression established in the second process is

$$V_1 - L\frac{di_L(t)}{dt} - Nv_{\mathrm{cd}} = 0. \tag{9}$$

For the latter two cases, they can be obtained by combining the first three with each other. For example, in the fourth case, first when switch S_4 is turned ON, switch S_2 is in the conduction state, then switch S_1 and S_4 are turned ON at the same time, and finally, switch S_1 is turned ON when switch S_4 is in the conduction state during the transition process. For other power switches that meet the preconditions of ZVS, the analysis is similar and many cases are formed. For practicality, the first and the second processes are summarized in a unified manner and the expression for the first process on the primary side is

$$\begin{cases} \dfrac{dv}{dt} = u_3 \cdot \dfrac{i_L}{C_{\mathrm{coss1}}(V_1 - v) + C_{\mathrm{coss1}}(v)} \\ \dfrac{di_L}{dt} = \dfrac{u_4 \cdot V_1 + u_5 \cdot v - nv_{\mathrm{cd}}}{L}. \end{cases} \tag{10}$$

The unified expression for the first process on the secondary side is

$$\begin{cases} \dfrac{dv}{dt} = u_3 \cdot \dfrac{Ni_L}{C_{\mathrm{coss2}}(v) + C_{\mathrm{coss2}}(V_2 - v)} \\ \dfrac{di_L}{dt} = \dfrac{u_4 \cdot NV_2 + u_5 \cdot Nv + v_{\mathrm{ab}}}{L} \end{cases} \tag{11}$$

where C_{oss2} indicates the parasitic capacitor of the switches on the secondary side. For the second process, the unified expression of the primary side is

$$\frac{di_L}{dt} = \frac{u_6 \cdot V_1 - Nv_{\mathrm{cd}}}{L} \tag{12}$$

and the unified expression of the secondary side is

$$\frac{di_L}{dt} = \frac{u_6 \cdot NV_2 + v_{\mathrm{ab}}}{L}. \tag{13}$$

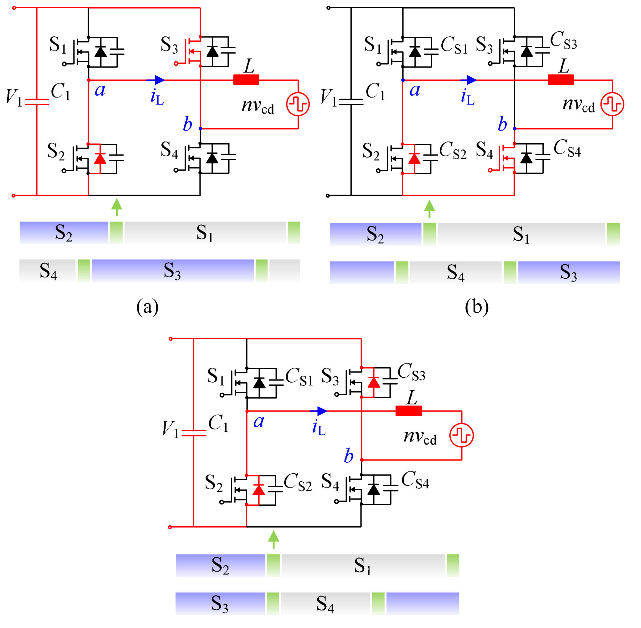
The specific values of u_3–u_6 in (10)–(13) are shown in Table II. It is worth noting that, when the primary-side power switches are in switching transition, it has been assumed that the secondary-side power switches are not in transition, but in some cases, simultaneous switching is a possible phenomenon, and the above formulas need to be coupled.

B. Current Does Not Meet the Precondition of ZVS

When the direction of the current flowing through the power switches does not satisfy the prerequisite for complete ZVS, the switching behavior is an HS turn-ON with current commutation from the complementary body diode. The circuits for the first three cases of HS behavior are shown in Fig. 9(a)–(c), corresponding to $\xi_{1\_3\mathrm{H}}$, $\xi_{1\_4\mathrm{H}}$, and $\xi_{1\mathrm{a}4\mathrm{H}}$.

TABLE II
ALL COEFFICIENTS OF SWITCH TRANSITION PROCESS

	u_3	u_4	u_5	u_6	u_7
$\xi_{1\_3S\_I}$/ $\xi_{1\_3S\_II}$/ ξ_{1_3H}/ $\xi_{4\_2S\_I}$/ $\xi_{4\_2S\_II}$/ ξ_{4_2H}	-1	-1	1	0	-1
$\xi_{2\_3S\_I}$/ $\xi_{2\_3S\_II}$/ ξ_{2_3H}/ $\xi_{3\_2S\_I}$/ $\xi_{3\_2S\_II}$/ ξ_{3_2H}	1	0	-1	-1	0
$\xi_{2\_4S\_I}$/ $\xi_{2\_4S\_II}$/ ξ_{2_4H}/ $\xi_{3\_1S\_I}$/ $\xi_{3\_1S\_II}$/ ξ_{3_1H}	1	1	-1	0	1
$\xi_{1\_4S\_I}$/ $\xi_{1\_4S\_II}$/ ξ_{1_4H}/ $\xi_{4\_1S\_I}$/ $\xi_{4\_1S\_II}$/ ξ_{4_1H}	-1	0	1	1	0
ξ_{1a4S_I}/ ξ_{1a4S_II}/ ξ_{1a4H}	-1	-1	2	1	-1
ξ_{2a3S_I}/ ξ_{2a3S_II}/ ξ_{2a3H}	1	-1	2	-1	1
$\xi_{5\_7S\_I}$/ $\xi_{5\_7S\_II}$/ ξ_{5_7H}/ $\xi_{8\_6S\_I}$/ $\xi_{8\_6S\_II}$/ ξ_{8_6H}	1	1	-1	0	1
$\xi_{6\_7S\_I}$/ $\xi_{6\_7S\_II}$/ ξ_{6_7H}/ $\xi_{7\_6S\_I}$/ $\xi_{7\_6S\_II}$/ ξ_{7_6H}	-1	0	1	1	0
$\xi_{6\_8S\_I}$/ $\xi_{6\_8S\_II}$/ ξ_{6_8H}/ $\xi_{7\_5S\_I}$/ $\xi_{7\_5S\_II}$/ ξ_{7_5H}	-1	-1	1	0	-1
$\xi_{5\_8S\_I}$/ $\xi_{5\_8S\_II}$/ ξ_{5_8H}/ $\xi_{8\_5S\_I}$/ $\xi_{8\_5S\_II}$/ ξ_{8_5H}	1	0	-1	-1	0
ξ_{5a8S_I}/ ξ_{5a8S_II}/ ξ_{5a8H}	1	1	-2	1	1
ξ_{6a7S_I}/ ξ_{6a7S_II}/ ξ_{6a7H}	-1	-1	2	-1	-1



(a)

(b)

(c)

Fig. 9. When the switch S_1 is turned ON with HS. (a) Switch S_3 is in conduction state. (b) Switch S_4 is in conduction state. (c) S_4 is also turned ON at the same time.

The expressions for all switches are standardized when an HS occurs. The unified expression of the primary side is as follows:

$$\frac{di_L}{dt} = \frac{u_7 \cdot V_1 - Nv_{\mathrm{cd}}}{L}. \tag{14}$$

The unified expression of the secondary side is as follows:

$$\frac{di_L}{dt} = \frac{u_7 \cdot NV_2 + v_{\mathrm{ab}}}{L}. \tag{15}$$

The specific value of u_7 in (14) and (15) is also shown in Table II. The above analysis provides a circuit analysis of all switching transition processes and establishes the unified equations. The detailed modeling is to insert each of these switching transition processes into the ideal steady-state process.

V. COMPLETE MODELING

Through the above analysis, the unified expressions of the ideal steady-state process and switching transition process based on 5-DOFs are obtained. This section mainly discusses the principle of waveform synthesis steps and some constraints and judgment conditions, forming complete mathematical modeling.

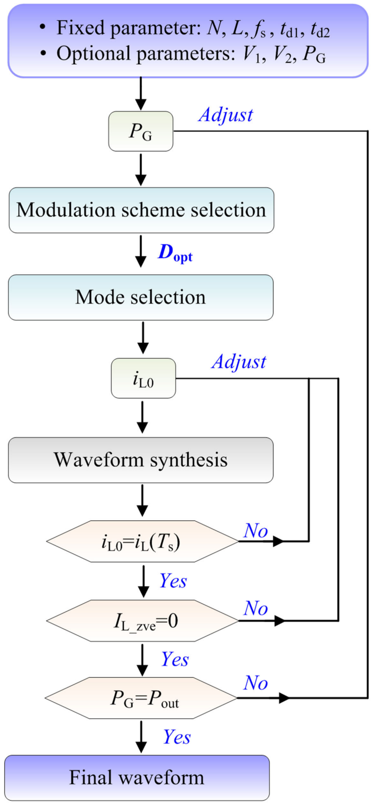


Fig. 10. Complete mathematical modeling steps of the PSSAM.

Fig. 10 shows the complete steps of modeling, thus forming the PSSAM by synthesizing the operating point-dependent waveforms. In the first step, a suitable modulation scheme is selected to generate the optimal DOF $\boldsymbol{D}_{\mathrm{opt}}$ when fixed and optional parameters are given. The fixed parameters mainly include transformer ratio N, inductor L, dead time t_{d1} and t_{d2} of primary and secondary power switches, switching frequency f_{s}, parasitic capacitor C_{oss1} and C_{oss2} of primary and secondary power switches, etc., whereas optional parameters include given power P_{G}, and input and output voltage V_1 and V_2.

In the second step, the mode is found, and its inductor current initial value is solved according to the literature [12] based on $\boldsymbol{D}_{\mathrm{opt}}$. It should be noted that since the inductor current initial value and the transmitted power for the synthesis of the waveforms in the previous steps do not take into account the effect of the transition, the obtained waveform has some deviations from the actual one. True values still need to be checked in the following steps.

In the third step, the inductor current initial value and the switching sequence obtained by $\boldsymbol{D}_{\mathrm{opt}}$ are employed to search for the corresponding equations and coefficients of the ideal steady-state process and the switching transition process at different time periods by the lookup table method. It is worth mentioning that the ODE45 numerical method with variable steps is used to solve the differential equations in this article. Besides, to obtain the steady-state waveforms, its transmitted

TABLE III
PARAMETERS OF DAB CONVERTER

Input voltage V_1	400V	Output voltage V_2	100V-200V
Auxiliary inductor L	190μH	Switching frequency fs	50kHz
Turn ratio N	2:1	Maximum power $P_{\max}$	1 kW

power, inductor current average value, and initial value need to be iterated until the requirements are satisfied. The specific iterative process for the three characteristic quantities is as follows.

1) For the iteration of the inductor current initial value, the initial value of the inductor current of the next switching cycle is always the average of the initial and final values of the inductor current of the previous switching cycle until the initial value end within a certain error range.
2) For the iteration of the average value of the inductor current, the average value of the inductor current is equal to zero. If it cannot be satisfied, the discussion is divided into two cases.
   a) When the average value of inductor current is greater than zero, the initial value of inductor current is appropriately reduced.
   b) When the average value of inductor current is less than zero, the initial value of inductor current is appropriately increased.
3) For the iteration of the transmitted power, the assignment of the transmitted power of the next switching cycle is always the average of the transmitted power of the previous switching cycle and the given value until the average value and the given value end within a certain error range.

In the fourth step, the obtained waveforms will need to be continuously adjusted until the initial value is equal to the end period value of the inductor current, the inductor current in a switching period meets the volt–second balance and the actual power matches the reference P_{out}. Through multiple cycles of these three conditions, stability is finally achieved with output waveforms.

The first two iterations continuously correct the initial value of the inductor current, whereas the second iteration continuously corrects the transmit power and finally synthesizes the waveforms through three iterations. The accuracy of its iterations then determines the time to be consumed by the calculation. This process is slightly more complicated, but it is a necessary process, and the algorithm can be considered in the future to reduce the number of iterations and speed up the computation.

VI. EXPERIMENTAL VERIFICATION

To validate the proposed PSSAM for the DAB converter, a hardware prototype as shown in Fig. 11 was built. The power level and switching frequency are 1 kW and 50 kHz, respectively. Other technical specifications are shown in Table III. The power devices on the primary and secondary sides of the converter were selected from Rohm's silicon carbide (SiC) MOSFET SCT3060 [21]. The dead time between primary switches was set as $t = 80$ *ns*, and the dead time between secondary-side power switches was set as $t = 60$ ns. The most important aspect of the proposed PSSAM is the analysis of the switching behavior during the finite switching transition process. The fitting of the parasitic capacitor is given ahead.

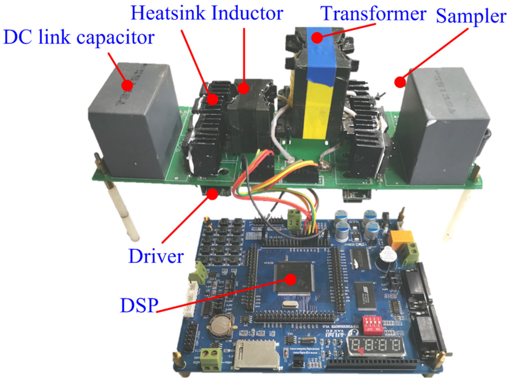


Fig. 11. Schematic diagram of the experimental prototype.

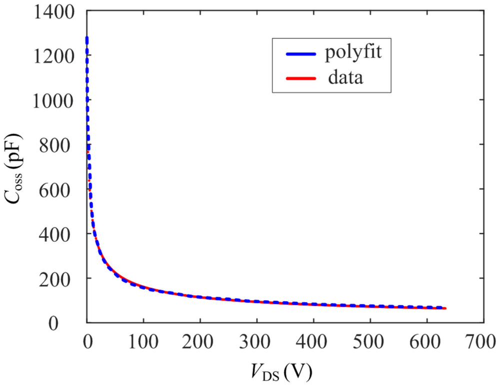


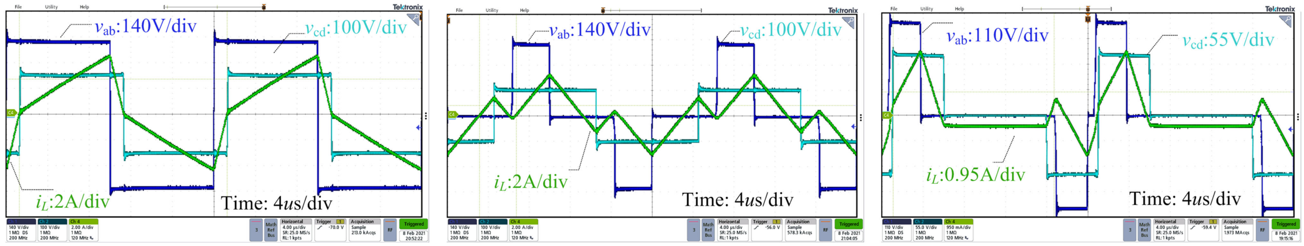
Fig. 12. Fit of the nonlinear behavior of the parasitic capacitor. Parasitic capacitor C_{oss} in function of the applied drain–source voltage V_{DS} as provided by the datasheet (SCH3060/ROHM).

A. Fitting of Power Switches Parasitic Capacitor

The relationship between the voltage across the power switches and the parasitic capacitor is extracted and fitted using the data from the datasheet of the device, as shown in Fig. 12. The relationship between C_{oss} and V_{DS} can be fitted according to the form proposed in [25], as shown in the following equation, where k_1 and k_2 are the coefficients to be fitted. $k_1 = 1025$ and $k_2 = 2.523$ can be obtained in this article:

$$C_{\mathrm{oss}}\left(V_{\mathrm{DS}}\right) = \frac{k_1}{\left(1 + \frac{V_{\mathrm{DS}}}{k_2}\right)^{\frac{1}{2}}}. \tag{16}$$

Next, in order to verify the uniformity and validity of the PSSAM, some more typical modulation schemes are selected below and verified under different operating conditions, respectively. It is worth mentioning that, in order to better demonstrate the effectiveness of the verification, the case with incomplete ZVS was selected as the most illustrative one.



(a) (b) (c)

Fig. 13. Experimental waveforms under different conditions. (a) $V_1 = 400$ V, $V_2 = 150$ V, and $P = 700$ W under PSM. (b) $V_1 = 400$ V, $V_2 = 100$ V, and $P = 200$ W under FDM. (c) $V_1 = 400$ V, $V_2 = 125$ V, and $P = 100$ W under O-5DOF.

TABLE IV
COMPARISON OF DIFFERENT SIMULATION AND DIFFERENT SOFTWARE

Software	Features
Saber	1. Support for importing SPICE models, and powerful and complex actual device modeling capabilities 2. Slow running speed of complex analysis 3. Very comprehensive complex analysis capabilities for real engineering
PSIM	1. Faster simulation speed under the ideal model 2. Support higher-order nonlinear behavior model of switching devices, and SPICE model of switching devices (embedded LTspice)
PLECS	3. Purely ideal components, but supports loss lookup functions based on voltage and current at the moment of switching, as well as magnetic component models based on magnetic circuits, and thermal analysis of thermally equivalent circuits
SIMULINK	1. Suitable for complex digital control, complex logic functions, and high-end algorithm implementation 2. Data interaction with external real systems, joint simulation
PsPice	1. Support importing SPICE models 2. Simulation speed is slow 3. Suitable for observing the real behavior under SPICE model, parasitic effects and other waveform details
SIMetrix/ SIMPLIS	1. Supports higher-order nonlinear behavior models and also supports importing SPICE models 2. Faster simulation speed
LTspice	1. Supports importing SPICE models 2. Optimized for switching conversion, faster simulation speed 3. Suitable for observing the real behavior of SPICE models, parasitic effects and other waveform details

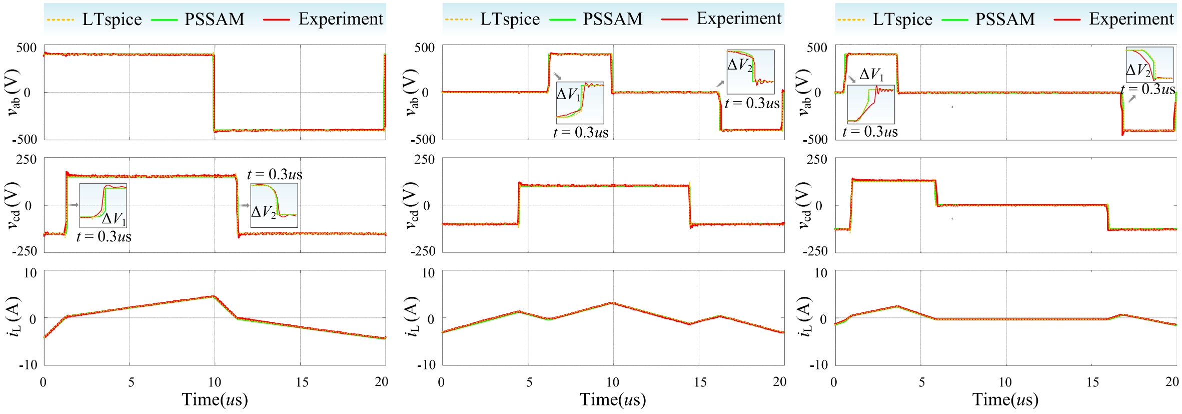
In this article, in order to better verify the proposed model, it is necessary to select suitable simulation software for comparison. Therefore, Table IV summarizes the characteristics of some commonly used simulation tools, including Saber, PISM, LTspice, etc. In comparison, LTspice simulation software supports the import of SPICE models, which can more accurately simulate and verify the behavior of power devices, and is suitable for observing the real behavior, parasitic effects, and other waveform details under SPICE models. Meanwhile, the software optimizes the switching conversion, and the simulation speed is relatively fast. Therefore, in the simulation comparison, an attempt was made to select the waveform obtained by LTspice as the comparison verification.

B. Validation of Different Modulation Schemes

Fig. 13 gives the waveforms of different modulation schemes under different operating conditions, containing the voltages v_{ab}, $v_{\mathrm{cd},}$ and the inductor current i_{L}. Fig. 13(a) gives the PSM waveforms at $V_2 = 150$ V, and $P = 700$ W. It can be seen from Fig. 13(a) that due to the absence of internal phase shift angle, v_{ab} and v_{cd} have a square wave shape, and in one switching period, the steady-state and transition processes, in this case, are λ_{1467}, $\xi_{\mathrm{5a8S\_I}}$, λ_{1458}, $\xi_{\mathrm{2a3S\_I}}$, $\xi_{\mathrm{2a3S\_II}}$, λ_{2358}, $\xi_{\mathrm{6a7S\_I}}$, λ_{2367}, $\xi_{\mathrm{1a4S\_I}}$, $\xi_{\mathrm{1a4S\_II}}$ in sequence. Comparison of the transmitted power, inductor rms current, etc., are shown in Table IV, showing characteristic quantities are also highly consistent. Furthermore, a detailed comparison of the residual voltages corresponding to each case was performed.

By extracting the LTspice and experimental waveform data, and then plotting the LTspice, PPSAM, and experimental data with the help of MATLAB, Fig. 14(a) was obtained. It can be seen from Fig. 14(a) that the waveforms obtained by PSSAM are highly consistent with the waveforms obtained by LTspice and experiments. Its current value is large enough to achieve complete ZVS when the primary-side switches are turned ON while the current is not large enough to transfer the energy of the parasitic capacitor when the secondary-side switches are turned ON, and incomplete ZVS is achieved. Besides, for the power switches S_5 and S_8, the residual voltages measured by PSSAM, LTspice, and experiment are -81.8 V, -79 V, and -76 V, respectively; for the power switches S_6 and S_7, the residual voltages measured by PSSAM, LTspice and experiment are 9.03 V, 20 V, and 14.9 V, respectively, which shows that the modeling accuracy is very high and the error is within $(81.8–76)/240 = 2.4\%$.

Fig. 13(b) gives the fundamental duty modulation (FDM) scheme waveforms at $V_2 = 100$ V and $P = 200$ W. In FDM, the phase shift between switches on the primary-side satisfies $D_1 + D_2 = 0.5$, whereas the secondary side satisfies $D_3 = 0.5$ and $D_4 = 0$, reflecting that the primary side is a quasi-square wave with two equal zero-voltage portions while the secondary side is a square wave, as shown in Fig. 13(b), with the given operating conditions of $V_2 = 100$ V and $P = 200$ W. In one switching period, the conduction and transition processes, in this case, are λ_{1367},



(a) (b) (c)

Fig. 14. Comparison of waveforms between PSSAM, LTspice, and experiments under different conditions. (a) $V_1 = 400$ V, $V_2 = 150$ V, and $P = 700$ W under PSM. (b) $V_1 = 400$ V, $V_2 = 100$ V, and $P = 200$ W under FDM. (c) $V_1 = 400$ V, $V_2 = 125$ V, and $P = 100$ W under O-5DOF.

TABLE V
COMPARISON OF PSSAM, LTSPICE, AND EXPERIMENTAL RESULTS UNDER DIFFERENT CONDITIONS

Test	PSSAM				LTspice				Experiment		
	P (W)	I_{rms} (A)	ΔV (V)	*Time* (s)	P (W)	I_{rms} (A)	ΔV (V)	*Time* (s)	P (W)	I_{rms} (A)	ΔV (V)
PSM (V_2=150V, P=700W)	696.02	2.635	ΔV_1=-81.8 ΔV_2=9.03	5.17	693.7	2.621	ΔV_1=-79 ΔV_2=20	149	696.3	2.63	ΔV_1=-76 ΔV_2=14.9
FDM (V_2=100V, P=200W)	200.9	1.51	ΔV_1=122.8 ΔV_2=-64.1	2.64	200.9	1.505	ΔV_1=80 ΔV_2=-70	144	201.1	1.50	ΔV_1=114 ΔV_2=-75.6
O-5DOF (V_2=125V, P=100W)	100.42	0.83	ΔV_1=250.9 ΔV_2=-161.2	3.45	97.9	0.82	ΔV_1=244.5 ΔV_2=-165.9	211	100.4	0.86	ΔV_1=239.8 ΔV_2=-180.5

$\xi_{\mathrm{5a8S\_I}}$, $\xi_{\mathrm{5a8S\_II}}$, λ_{1358}, $\xi_{\mathrm{4\_1S\_I}}$, λ_{1458}, $\xi_{\mathrm{2\_4S\_I}}$, $\xi_{\mathrm{2\_4S\_II}}$, λ_{2458}, $\xi_{\mathrm{6a7S\_I}}$, $\xi_{\mathrm{6a7S\_II}}$, λ_{2467}, $\xi_{\mathrm{3^{\cdot}2S\_I}}$, λ_{2367}, $\xi_{\mathrm{1\_3S\_I}}$, $\xi_{\mathrm{1\_3S\_II}}$ in sequence. The comparisons of the transmitted power, inductor rms current, etc., are shown in Table IV, which shows that these characteristic quantities are also highly consistent. In Fig. 14(b), switches S_3 and S_4 are not able to completely release the energy of the parasitic capacitor due to the relatively small current and incomplete ZVS turn ON is achieved. For the power switches S_3, the residual voltages measured by PSSAM, LTspice and experiment are -64.1 V, -70 V, and -75.6 V, respectively; for S_4, the residual voltages measured by PSSAM, LTspice, and experiment are 122.8 V, 80 V, and 114 V, respectively, which shows that the modeling accuracy is very high and the error is within (75.6–64.1)/400 = 2.8%. The rest of the power switches are able to complete ZVS.

Fig. 13(c) shows the waveforms of optimal five-degree-of-freedom (O-5DOF) at $V_2 = 125$ V, $P = 100$ W. It can be seen from Fig. 13(c) that v_{ab} contains two unequal zero-level sequences while v_{cd} contains only one zero-level sequence due to $D_4 = 0$. In one switching period, the conduction and transition processes, in this case, are λ_{1367}, $\xi_{\mathrm{4\_1S\_I}}$, λ_{1467}, $\xi_{\mathrm{6a7S\_I}}$, $\xi_{\mathrm{6a7S\_II}}$, λ_{1458}, $\xi_{\mathrm{3\_1S\_I}}$, $\xi_{\mathrm{3\_1S\_II}}$, λ_{1358}, $\xi_{\mathrm{7\_5S\_I}}$, $\xi_{\mathrm{7\_5S\_II}}$, λ_{1357}, $\xi_{\mathrm{6\_7S\_I}}$, $\xi_{\mathrm{6\_7S\_II}}$, λ_{1367}, $\xi_{\mathrm{2\_3S\_I}}$, λ_{2367}, $\xi_{\mathrm{1\_3S\_I}}$, $\xi_{\mathrm{1\_3S\_II}}$ in sequence. It is obvious that the O5-DOFs modulation scheme corresponds to more conduction and transition processes than the 3-DOFs FDM scheme and PSM scheme. Under this condition, switches S_2 and S_4 achieve incomplete ZVS and the other switches achieve complete ZVS, as shown in Fig. 14(c). For the power switch S_2, the residual voltages measured by PSSAM, LTspice, and experiment are -161.2 V, -165.9 V, and -180.5 V, respectively; for S_4, the residual voltages measured by PSSAM, LTspice, and experiment are 250.9 V, 244.5 V, and 239.8 V, respectively. It can be concluded that these residual voltages are accurately predicted.

PSSAM is much faster than LTspice for modeling as shown in Table V. PSSAM can speed up evidently compared to LTspice by about 28–61 times. This acceleration is mainly due to two reasons. First, in the finite switching transition process, PSSAM only considers the nonlinear variation of the parasitic capacitance with the drain–source voltage while in LTspice power devices are modeled with consideration of many other factors, such as the influence of temperature and stray inductance on output characteristics. Second, the equations of state under different loops are summarized, and the difference only lies in the coefficients. When the DAB converter works in different modes, a lookup table is used for giving coefficients only by judging the direction and value of the current. On the contrary, LTspice needs to create individual expressions for each process, and the equation for each is in higher order.

C. Discussion

First, the scalability aspect of the model is discussed. Currently, although many powerful simulation tools have been developed by many power electronics designers, it is still of great practical value to develop accurate analytical models for converter steady-state operation alone. Obviously, the multitime-scale modeling approach can also be applied to other DAB topologies, because the power switches of these converters need to be turned ON and OFF. With the modulation of each DOF, an ideal steady-state process is formed when the power device is in the ON-state. And a finite transition process is formed during the dead time of the power device is turned ON. Then, a more accurate and complete analytical model can be constructed by considering these processes in segments and solving them iteratively in turn within a switching period.

Next, the usefulness of the analysis model is discussed. On the one hand, PSSAM is obtained based on MATLAB numerical calculations, and its model of power switches considers only the nonlinear variation of the most central parasitic capacitor, and the speed of obtaining the final synthesized waveform has certain advantages. Therefore, the designer can rely on this model to consider different cases under the whole load and thus obtain the results quickly. In contrast, parameter scans are provided in most simulation tools, but this requires the designer to independently derive and subsequently analyze each steady-state result. On the other hand, with PSSAM, it is possible to build more accurate loss models, especially switching and conduction losses under incomplete ZVS conduction, to better predict the efficiency and optimize the design of each main circuit parameter. Overall, with the future trend of power electronics to operate converters at higher switching frequencies, the proposed approach is essential for the accuracy of steady-state modeling of DAB-based converters.

VI. CONCLUSION

In this article, a PSSAM is developed. To obtain this model, a time-domain steady-state modeling method is developed based on piecewise operating-mode analysis in one switching period. The operating modes in the switching transient process are included, and the influence of the nonlinear parasitic capacitors is considered. All possible operating modes are analyzed, and the corresponding state equations are derived and unified in the ideal steady-state and switching transient processes considering the influence of the modulation scheme. At the methodological level, the approach is based on the analysis of the most general 5-DOF modulation of DAB converters, which can incorporate all phase-shift modulation schemes. In addition, the modeling idea can be applied to the analysis of other DAB topologies. At the effect level, the model is able to accurately predict its steady-state characteristics including transmitted power, inductor rms current, etc. Meanwhile, PSSAM is able to accurately model switch device behaviors including residual voltages for incomplete ZVS. Compared with the existing commercial software, this scheme can greatly increase the simulation speed and reduce the calculation time by about 28–61 times. Therefore, PSSAM proposed in this article can provide good balance of accuracy and practicality.

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