A Novel Synchronous Rectifier Driving Scheme for *LLC* Converter Based on Secondary Rectification Current Emulation

Haiming Yu, Xiaogao Xie, *Member, IEEE*, Sen Xu, and Hanjing Dong

***Abstract*—In conventional synchronous rectifier (SR) driving schemes, the drain to source voltage of SR is detected to generate its driving signal. However, the driving signal by this method will lose a portion of duty cycle due to the parasitic inductance in SR package and on-board parasitic inductance. This phenomenon is severe under heavy load and deteriorates the efficiency of the converter. In this article, a novel *LLC* SR driving scheme based on secondary rectification current emulation is proposed. An auxiliary winding of the transformer and an auxiliary winding of the resonant inductor located on the secondary side are in series to generate a superposed voltage signal. The secondary rectification current is emulated out according to the superposed voltage signal by an integration circuit. After that the SR driving signal, which is not affected by parasitic inductance, is generated with a logic circuit. Detailed theoretical analysis and circuit implementation have been presented. Finally, a 400 V input and 12 V/20 A output half-bridge *LLC* resonant converter prototype has been built up to verify the feasibility of the proposed SR driving scheme.**

***Index Terms*—*LLC* resonant converter, secondary rectification current emulation, synchronous rectification (SR).**

I. Introduction

With the development of consumer electronics and IT equipment, the demand for the converters with low voltage and high output current keeps increasing. *LLC* resonant converter is becoming more and more popular for its high efficiency, which is benefit from both zero-voltage switching for the primary side switches and zero-current switching for the secondary side rectifiers [1]–[4]. For further improving the efficiency, the synchronous rectifiers (SRs) are employed due to their conduction loss is much lower than that of the diode rectifiers. The driving signal of SR is critical factor to reduce the conduction loss of SR [5], [6].

In resonant converters, unlike in PWM switching converters, the turn-ON/OFF times of primary switches and SRs are not exact identical in phase [7]. Therefore, it cannot use the same driving signals to control them.

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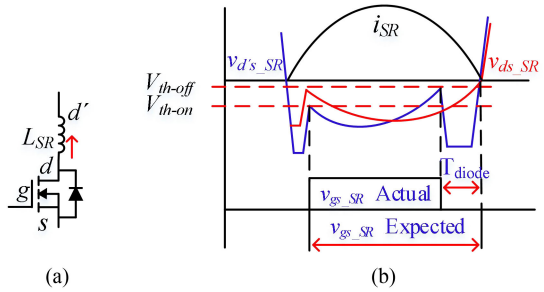

Fig. 1. (a) Model of SR with parasitic inductance. (b) v_{ds_SR} affected by SR parasitic inductance.

Driving the SRs in *LLC* resonant converter with the commercial SR driving ICs, which are commonly realized by detecting the drain-source voltage of *SR* [8], [9], is a very simple way but exists some inherent drawbacks. Due to MOSFET parasitic inductance in package and on-board parasitic inductance from the SR driver to the gate of SR, the duty cycle of SR driving signal is lost. This phenomenon becomes extremely severe in high-frequency *LLC* converters especially under heavy load conditions [10].

The model of MOSFET with parasitic inductance and key waveforms for generating the driving signal of SR is shown in Fig. 1(a) and (b), respectively. Where L_{SR} is the parasitic inductance of SR, including package inductance and on-board parasitic inductance. At the beginning, the SR is in the off-state and the body diode is conducted to carry the secondary current. The forward voltage of the body diode results in a large forward voltage drop in v_{ds_SR}, which is lower than the turn-ON threshold voltage V_{th_on} inside the SR control IC so that the SR control IC turns ON the SR. In the *LLC* converter, during on-time of SR, the secondary rectification current i_{SR} will first increase and then decrease to zero. As i_{SR} is close to zero, v_{ds_SR} is also close to zero. When v_{ds_SR} is higher than the turn-OFF threshold voltage V_{th_OFF} inside the SR control IC, SR turns OFF. However, the induced voltage on L_{SR} reverses when the SR current i_{SR} drops, which results in actual $v_{d's\_SR}$ arrives $V_{th\text{-}OFF}$ earlier than in ideal condition. Thus, the actual SR on time is shorter than the expected value, as shown in Fig. 1(b).

To resolve this problem, some new SR driving schemes for *LLC* resonant converters have been studied in the past years [11]–[20].

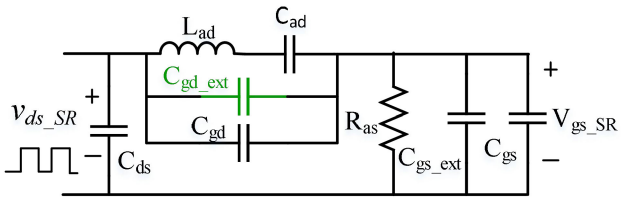

Fig. 2. Equivalent circuit of the self-driven gate driver [11].

To overcome the stray inductance effect and increase SR conduction time, a self-driven gate driver is introduced in [11]. As shown in Fig. 2, The auxiliary passive components including inductor L_{ad} and capacitor C_{ad} create a resonant tank to extract the first harmonic of v_{ds_SR} with a 180° phase shift to create the gate signal v_{gs_SR}. This scheme is simple in control method, but v_{gs_SR} is influenced by the parasitic capacitance C_{ds}, C_{gs}, and C_{gd} of SR, which are greatly affected by packaging, temperature, and the voltage across SR. Therefore, this scheme is preferable to be used for dc transformers and not suitable for batch production, which makes the application range of this method restricted.

The self-driven SR drain-to-source voltage sensing circuit introduced in [12] can provide a low-impedance bypassing path for the displacement current induced by the high *dv/dt* of semiconductor components. Based on the proposed SR drain-to-source voltage sensing circuit, an adaptive SR on-time tuning algorithm is implemented, which avoids the influence from the loop stray inductance and the propagation delay in the path. This scheme can obtain high accurate SR driving signal with small dead time. But SR drain-to-source voltage sensing circuit is very complex and four switches including a high-voltage switch are required.

The dead time regulation method based on SR drain-to-source voltage (v_{ds}) sensing introduced in [13] is an improvement on conventional SR drain-to-source voltage detecting methods [8], [9]. The dead time of v_{gs_SR} can be regulated to a small value by adjusting the inner voltage reference for turning OFF the driving signal. To avoid inversion SR current, a certain dead time (margin) larger than a preset value should be left. Therefore, the dead time cannot to be reduced to very small value due to the noise consideration. Besides, there exists a tradeoff between the conduction loss of SR and dead time because SR with lower on-state resistor will cause larger dead time. Under high-frequency applications, the lost portion of duty cycle of SR will be more obviously and the conduction losses will further increase. Therefore, this scheme is more suitable for low-frequency applications.

In [14], the SR driving signal is obtained by comparing and integrating large voltage signals including resonant capacitor voltage, input voltage, and output voltage. The driving signal is not sensitive to the noise, but the calculation and analysis process is very complicated, which needs a micro-controller to realize the function. The SR driving signals are on primary side, which needs additional isolated components such as high-speed optocoupler or transformer to transfer the signals from primary side to the secondary side. Therefore, the cost is increased and power density is deteriorated.

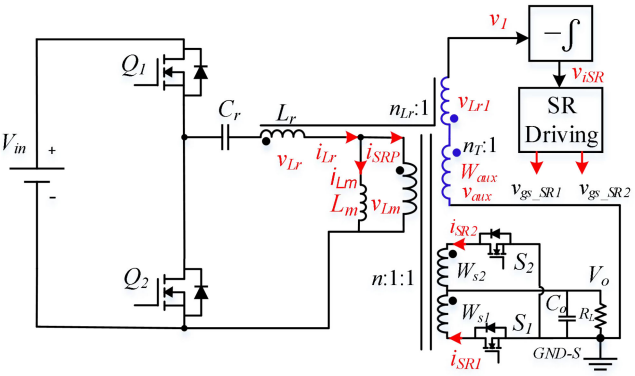

Fig. 3. Schematic of the proposed SR driving scheme for *LLC* resonant converter.

In other research, the digitally implemented adaptive control methods are presented [15]–[18]. By adaptively tuning the SR on-state duration based on the body diode conduct period in the last switching cycle, the body diode conduction time can be minimized after a few of switching cycles. However, during the fast transient process of load or input voltage, these methods may induce inversion SR current because the SR driving signal may not adjust in time by microcontroller unit.

SR driving schemes based on current-sensing transformer (CT) [19], [20] can achieve accurate SR driving signals, but it requires the bulky CT and complicated signal processing circuit. The cost and size of the converter have been sacrificed, which does not meet the development trend of high power density.

In this article, a new driving scheme for SRs in *LLC* resonant converter which based on secondary rectification emulation is proposed. The proposed SR driving signals can be simply achieved by using an auxiliary winding of the transformer and an auxiliary winding of the resonant inductor. And the signal processing circuit is also very simple and can be easily integrated into one IC. Thus, the size of the *LLC* converter will not increase, which ensures high power density of the converter. Moreover, the proposed scheme is not affected by parasitic inductance and the on-state resistor of SR. Meanwhile, accurate SR gate driving signal over the whole load range and wide input/out range can be achieved.

The rest of this article is organized as follows. Section II describes theory of the proposed SR driving scheme. Design on some key parameters and analysis on deviation due to components tolerances are presented in Section III. Experimental results based on a 12 V/20 A *LLC* converter are presented in Section IV. Finally, Section V concludes this article.

II. Basic Operation Principle of the Proposed SR Driving Scheme

Fig. 3 shows the schematic of the proposed SR driving scheme for *LLC* resonant converter. An auxiliary winding of the resonant inductor L_r and an auxiliary winding of the transformer are connected in series on the secondary side. v_{aux} and v_{Lr1} represent the voltages across the auxiliary winding of the transformer and the auxiliary winding of the resonant inductor, respectively. The

superposed voltage v_1 of v_{Lr1} and v_{aux} is sent to the reverse integrator and outputs a voltage signal v_{iSR}.

According to the basic operation principle of *LLC* and circuit theory, the following equations can be easily obtained.

$$i_{Lr} - i_{Lm} = i_{SRP} = i_{SR}/n \tag{1}$$

$$v_{Lr1} = \frac{v_{Lr}}{n_{Lr}} = \frac{1}{n_{Lr}} L_r \frac{di_{Lr}}{dt} \tag{2}$$

$$v_{aux} = \frac{v_{Lm}}{n_T} = \frac{1}{n_T} L_m \frac{di_{Lm}}{dt} \tag{3}$$

where L_m is the magnetizing inductance of transformer, i_{Lr} is resonant inductor current, i_{Lm} is the magnetizing inductor current and i_{SR} is the secondary rectification current, v_{Lr} and v_{Lm} represent the voltages across the resonant inductor L_r and the magnetizing inductance L_m, n_T, and n_{Lr} are the auxiliary winding turns ratios of the transformer and the resonant inductor, respectively.

The superposed signal v_1 can be achieved according to v_{aux} and v_{Lr1}

$$v_1 = -(v_{Lr1} - v_{aux}) = -\left(\frac{L_r}{n_{Lr}}\frac{di_{Lr}}{dt} - \frac{L_m}{n_T}\frac{di_{Lm}}{dt}\right). \tag{4}$$

The output signal v_{iSR} of the reverse integrator can be obtained according to

$$v_{iSR} = -\int v_1 dt. \tag{5}$$

By combining (2)–(5), v_{iSR} can be obtained as follows:

$$v_{iSR} = \int \left(\frac{L_r}{n_{Lr}}\frac{di_{Lr}}{dt} - \frac{L_m}{n_T}\frac{di_{Lm}}{dt}\right) dt. \tag{6}$$

If the parameters of L_r, n_{Lr}, L_m, and n_T are designed to satisfy the relationship $L_r / n_{Lr} = L_m / n_T = k$, (6) can simplified as follows:

$$v_{iSR} = \mathrm{k}\,(i_{Lr} - i_{Lm})\,. \tag{7}$$

Obviously, the waveform of $|v_{iSR}|$is similar to i_{SR}. Thus, v_{iSR} can be used for SR driving signal generation instead of v_{ds_SR}.

Fig. 4 shows the key waveforms of the proposed SR driving scheme for *LLC* resonant converter in discontinuous conduction mode (DCM) and continuous conduction mode (CCM), respectively.

The implementation circuit of the proposed SR driving scheme for *LLC* resonant converter is shown in Fig. 5. In Fig. 5, the reverse integrator consists of an operational amplifier, resistor R_1, resistor R_2, and capacitor C_1. The signal v_{iSR} is obtained by integrating the difference between the auxiliary winding voltage of the transformer and the auxiliary voltage of the resonant inductor. In addition, the action of integration also filters out the high-frequency noise, which further enhances the noise immunity.

Two RS flip-flops are used to generate the driving signal of SR. The SET signals are generated by comparing the DS voltage of SR with the preset negative threshold voltage V_{th_on}, which is similar to the conventional SR drain-to-source voltage detecting methods [8], [9]. When there is current flow through the body

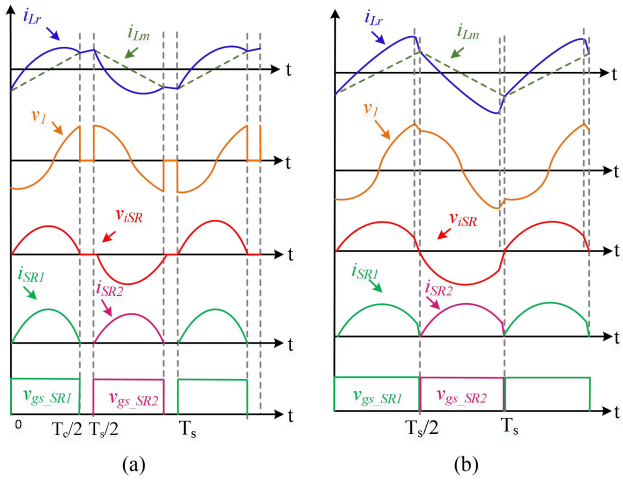

Fig. 4. Key waveforms of the proposed SR driving scheme for *LLC* resonant converter. (a) DCM (f_s<f_r). (b) CCM (f_s>f_r).

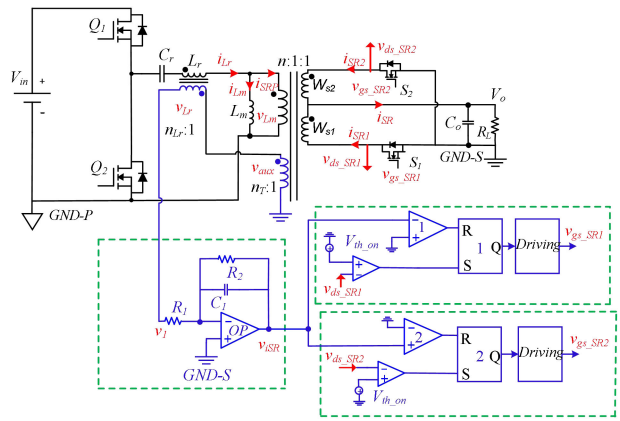

Fig. 5. Implementation circuit of the proposed SR driving scheme for *LLC* resonant converter.

diode of SR, the DS voltage of SR will be lower than V_{th_on}, which forces the output signals of the comparators to flip from low level to high level. The RESET signals are generated by comparing v_{iSR} with zero. For v_{gs_SR1}, the RESET signal is generated when v_{iSR} falls across zero, while for v_{gs_SR2}, the RESET signal is generated as v_{iSR} arises across zero.

In real application, some additional circuits such as minimum on-time circuit after the SET signals generation circuit and blank circuit after the RESET signals generation circuits are necessary for improving the noise immunity [8], [9]. These techniques are well-developed and not discussed in this article for simplicity.

III. Design Consideration

According to the integrator circuit shown in Fig. 6, it can be derived in the following:

$$V_1(s) = -(V_{Lr1}(s) - V_{aux}(s)) \tag{8}$$

$$V_{iSR}(s) = -\frac{R_2}{R_1}\frac{1}{SR_2C_1 + 1}V_1(s). \tag{9}$$

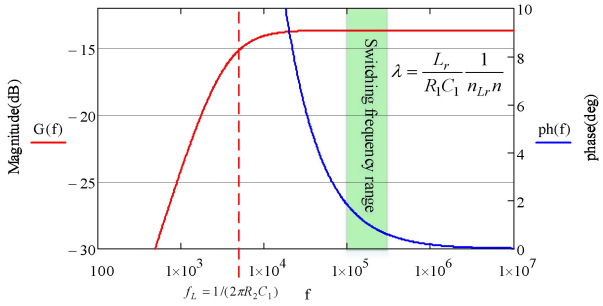

Fig. 6. Bode diagram of the gain G(s) of integrator.

By combining (2), (3), (8), and (9), the transfer function from i_{SR} to v_{iSR} can be obtained.

$$G(s) = \frac{V_{iSR}(s)}{I_{SR}(S)} = \frac{R_2}{R_1}\frac{SL_r}{SR_2C_1+1}\frac{1}{n_{Lr}n} = \frac{R_2}{R_1}\frac{SL_r}{\frac{f}{f_L}+1}\frac{1}{n_{Lr}n} \tag{10}$$

where $f_L = 1/(2\pi R_2 C_1)$. With appropriately selected parameters of R_1, R_2, and C_1, the Bode diagram of G(s) is drawn as shown in Fig. 6. It shows that the transfer function gain λ is constant and the phase shift is less than 2° when $f_s/f_L >> 1$. Under this condition, (10) can be simplified as follows:

$$G(s) \approx \lambda = \frac{L_r}{R_1 C_1}\frac{1}{n_{Lr}n}. \tag{11}$$

Then,

$$V_{iSR}(s) \approx \lambda I_{SR}(s). \tag{12}$$

In real applications, the turns ratio of transformer and resonant inductor can be precisely controlled during batch production so that no error will be brought by them. However, there exists about ±10% tolerance of inductance during batch manufacture. According to (6), the tolerance of L_r and L_m will cause the waveform of v_{iSR} deviated from the waveform of i_{SR} and lead to deviated turn-OFF point of SR driving signal. Therefore, the influence of these tolerances needs to be taken account.

When the actual magnetizing inductance value L'_m and actual resonant inductance L'_r are deviated from the rated magnetizing inductance L_m and the rated resonant inductance L_r, (6) and (7) are modified as follows:

$$v'_{iSR} = \int \left(\frac{\mathrm{L'_r}}{\mathrm{n_{Lr}}}\frac{di_{Lr}(t)}{dt} - \frac{\mathrm{L'_m}}{\mathrm{n_T}}\frac{di_{Lm}(t)}{dt} \right) dt \tag{13}$$

$$v'_{iSR} = k' i_{Lr} - k'' i_{Lm} \tag{14}$$

where v'_{iSR} is the actual output of integrator considering the tolerance of inductor, $k' = L'_r/n_{Lr}$ and $k'' = L'_m/n_T$. Therefore, if L'_m is larger than L_m, $|v_{iSR}|$will falls to zero ahead of the point that i_{SR} falls to zero. This condition makes SR driving signal turning OFF earlier than the expected, as is shown in Fig. 7(a). On the contrary, when L'_m is smaller than L_m, the SR driving signal will turn OFF later than the expected, as shown in Fig. 7(b).

The influence of the resonant inductance tolerance on SR driving signal is opposite to L_m, as shown in Fig. 8(a) and (b).

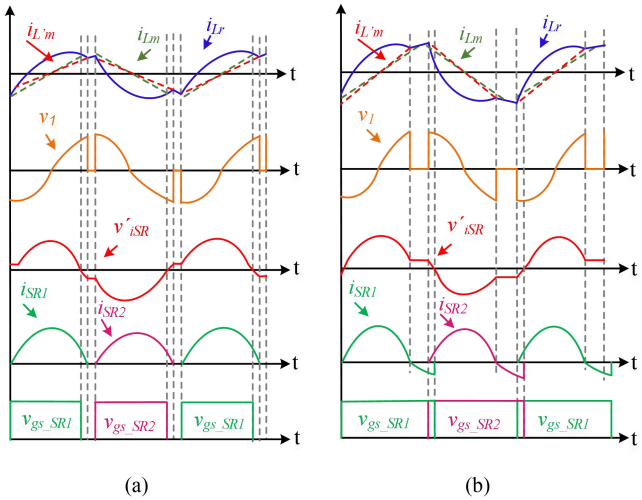

Fig. 7. Key waveforms of the *LLC* resonant converter with the proposed SR driving scheme considering the tolerance of L_m. (a) Actual $L'_m > L_m$. (b) Actual $L'_m < L_m$.

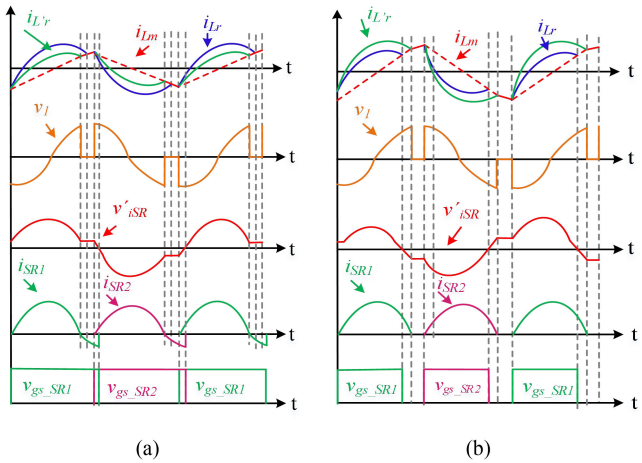

Fig. 8. Key waveforms of the *LLC* resonant converter with the proposed SR driving scheme considering the tolerance of L_r. (a) Actual $L'_r > L_r$. (b) Actual $L'_r < L_r$.

L'_m and L'_r are defined as $L_m + \Delta L_m$ and $L_r + \Delta L_r$, respectively. Where, ΔL_m and ΔL_r are deviations of the actual inductance from the rated parameters, respectively. Then, (14) can be rewritten as follows:

$$v'_{iSR} = \mathrm{v}_{iSR} + \left(\frac{\Delta L_r \cdot i_{Lr}}{n_{Lr}} - \frac{\Delta L_m \cdot i_{Lm}}{n_T} \right). \tag{15}$$

According to the relationship $i_{Lr} = i_{Lm} + i_{SR}/n$, (15) can be rewritten as follows:

$$v'_{iSR} = v_{iSR} + \left(\frac{\Delta L_r}{n_{Lr}} - \frac{\Delta L_m}{n_T} \right) i_{Lm} + \frac{\Delta L_r}{n_{Lr}}\frac{i_{SR}}{n}. \tag{16}$$

To simplify the calculation, the secondary rectification current is approximately regarded as half-sinusoidal waveform, as shown in Fig. 9. Thus, v_{iSR} during a half-resonant period can be described as follows:

$$v_{iSR}(t) = k\left[(\, i_{Lr}(t) - i_{Lm}(t) \right] = \frac{Lr}{n_{Lr}}\frac{\pi I_o}{2n}\sin(\omega t). \tag{17}$$

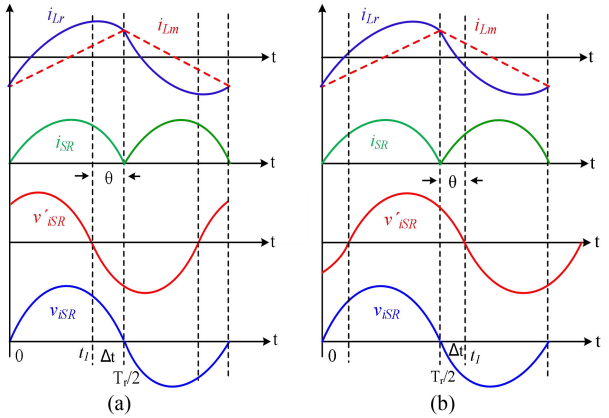

Fig. 9. Approximate diagram of deviation between v'_{iSR} and i_{SR} caused by the tolerances of inductors (a) $\Delta L_r/L_r<0$, $\Delta L_m/L_m>0$. (b) $\Delta L_r/L_r>0$, $\Delta L_m/L_m<0$.

Suppose v'_{iSR} falls to zero at time t_1, as shown in Fig. 9, (18) can be derived by combining (16) and (17)

$$\left(1+\frac{\Delta L_r}{L_r}\right)\sin(\omega t_1)=\left(\frac{\Delta L_m}{L_m}-\frac{\Delta L_r}{L_r}\right)i_{Lm}(t_1)\frac{2n}{\pi I_o} \tag{18}$$

where $i_{Lm}(t_1)$ is the magnetizing current i_{Lm} at time t_1. In order to calculate the $i_{Lm}(t_1)$, an error coefficient $\delta=\theta/180°$ is introduced, where θ is deviation angle between the crossing zero points of $v'_{iSR}(t)$ and $i_{SR}(t)$ due to the tolerances of inductance.

Because the resonant inductor current i_{Lr} and the magnetizing inductor current i_{Lm} with rated parameters are equal at $T_r/2$, the following equation can be derived as:

$$i_{Lr}\,(T_r/2)=i_{Lm}\,(T_r/2)=\frac{nV_o}{4f_r(L_m+\Delta L_m)}. \tag{19}$$

Based on (19), $i_{Lm}(t_1)$ can be obtained according to

$$\begin{aligned} i_{Lm}(t_1)&=-i_{Lm}\left(\frac{T_r}{2}\right)+\frac{nV_o(1-\delta)}{2f_r(L_m+\Delta L_m)}\\ &=\frac{nV_o(1-2\delta)}{4f_r(L_m+\Delta L_m)} \end{aligned} \tag{20}$$

where V_o is the output voltage and f_r is the resonant frequency. The deviation angle θ can be resolved by combining (18) and (20).

$$\theta=\arcsin\left[\left(\frac{\Delta L_m}{L_m}-\frac{\Delta L_r}{L_r}\right)\frac{n^2R_L(1-2\delta)}{2\pi f_r(L_m+\Delta L_m)}\frac{L_r}{L_r+\Delta L_r}\right]. \tag{21}$$

After that the deviation time $\Delta t=\theta/360f_r$ can also be obtained. The curve of deviation angle θ and deviation time Δt are shown in Fig. 10(a) and (b), respectively. It can be seen that in the worst case, i.e., $\Delta L_r/L_r=+10\%$ and $\Delta L_m/L_m=-10\%$ or $\Delta L_r/L_r=-10\%$ and $\Delta L_m/L_m=+10\%$, the deviation angle θ is about 5° and the deviation time Δt is about 95 ns.

The calculated Δt provides a basis to design v_{gs_SR} with maximal pulsewidth when the tolerance of inductor is taken account. To avoid shoot-through conditions between the primary switches and SR, the actual turn-OFF time of the SR driving

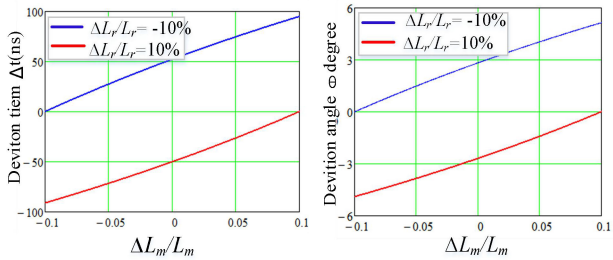

Fig. 10. Deviation between the zero-crossing points *of* v_{iSR} and v'_{iSR}. (a) Deviation angle θ. (b) Deviation time Δt.

TABLE I
ELECTRICAL SPECIFICATIONS AND COMPONENTS PARAMETERS OF PROTOTYPE

Parameters	Values
Input Voltage	380V-420V
Output Voltage/Current	12V/20A
Resonant Capacitor C_r	33nF
Resonant Inductance L_r	Core: RM8, L_r=37uH, n_{Lr}=2
Transformer	Core: PQ3230, Turn ratio 34:2:2, L_m=320uH, n_T=17:1
Output Capacitance	2×1000uF/25V&2×220uF/25V
Primary MOSFET	IPAN60R210PFD7S
Synchronous rectifier	BSC010N04LS6
Parameters of integrator	R_1=10kΩ, R_2=100kΩ, C_1=510pF

signal should be at least Δt earlier than crossing point of i_{Lr} and i_{Lm} obtained by rated parameters. During batch production, the accurate driving signal pulse of SR can be obtained with the rated parameters first. Then, a margin of Δt is left for v_{gs_SR} based on the calculation value. In this way, the inversion secondary current can be avoid even under the condition of maximal tolerances of inductor while the maximal pulsewidth of v_{gs_SR} can be obtained.

To verify the theoretical analysis, the proposed SR driving scheme for *LLC* resonant converter with the parameters shown in Table I in the experimental section is simulated with software PSIM. The simulated waveforms of v_{gs_SR}, v_{ds_SR}, and i_{SR} under full load are shown in Fig. 11. It can be seen that a margin of about 100 ns is left for v_{gs_SR} under the rated parameters according to the aforementioned design rule, as shown in Fig. 11(a). The maximal dead time of one driving signal of SR is about 150 ns under one of the maximal tolerance condition with $\Delta L_r=-10\%$ and $\Delta L_m=+10\%$, as shown in Fig. 11(b). While under another maximal tolerance condition with $\Delta L_r=+10\%$ and $\Delta L_m=-10\%$, the dead time of one driving signal of SR is close to zero and there is no inversion secondary current, as shown in Fig. 11(c).

Simulated waveforms of v_{gs_SR}, v_{ds_SR}, and i_{SR} under light load are shown in Fig. 12. It can be seen that the dead time of one SR driving signal has increased to 182 ns under the

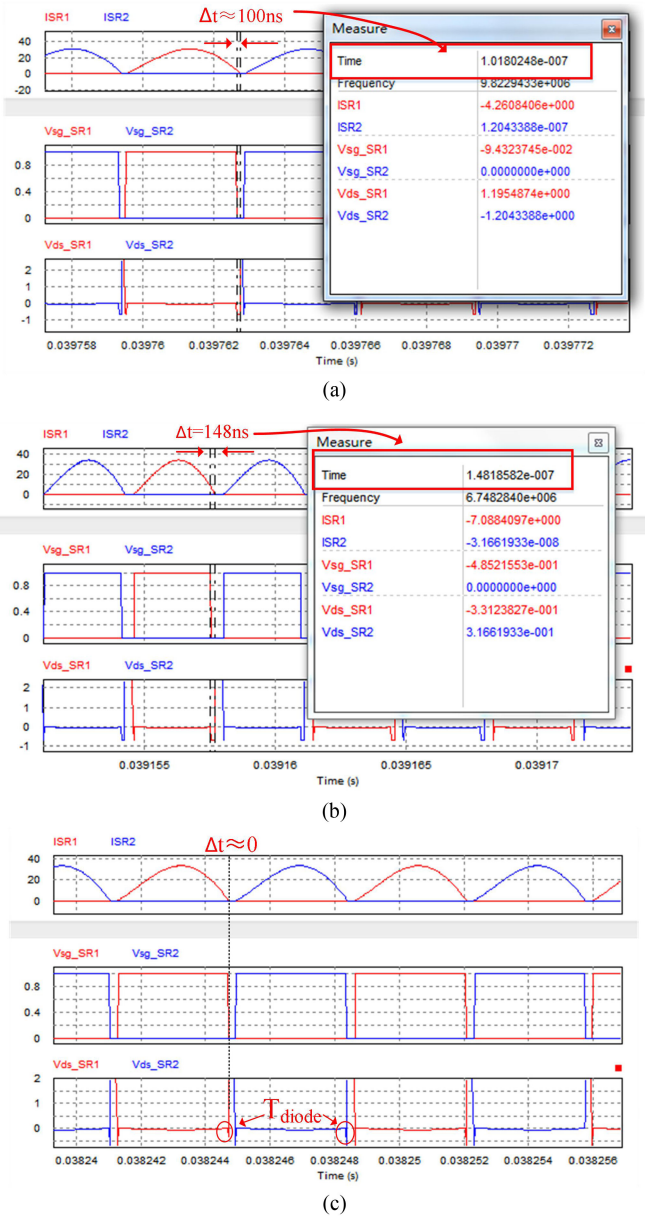

Fig. 11. Simulated secondary waveforms of *LLC* resonant converter with the proposed SR driving scheme under full load. (a) $\Delta L_r = \Delta L_m = 0$. (b) $\Delta L_r/L_r = -10\%$, $\Delta L_m/L_m = +10\%$. (c) $\Delta L_r/L_r = +10\%$, $\Delta L_m/L_m = -10\%$.

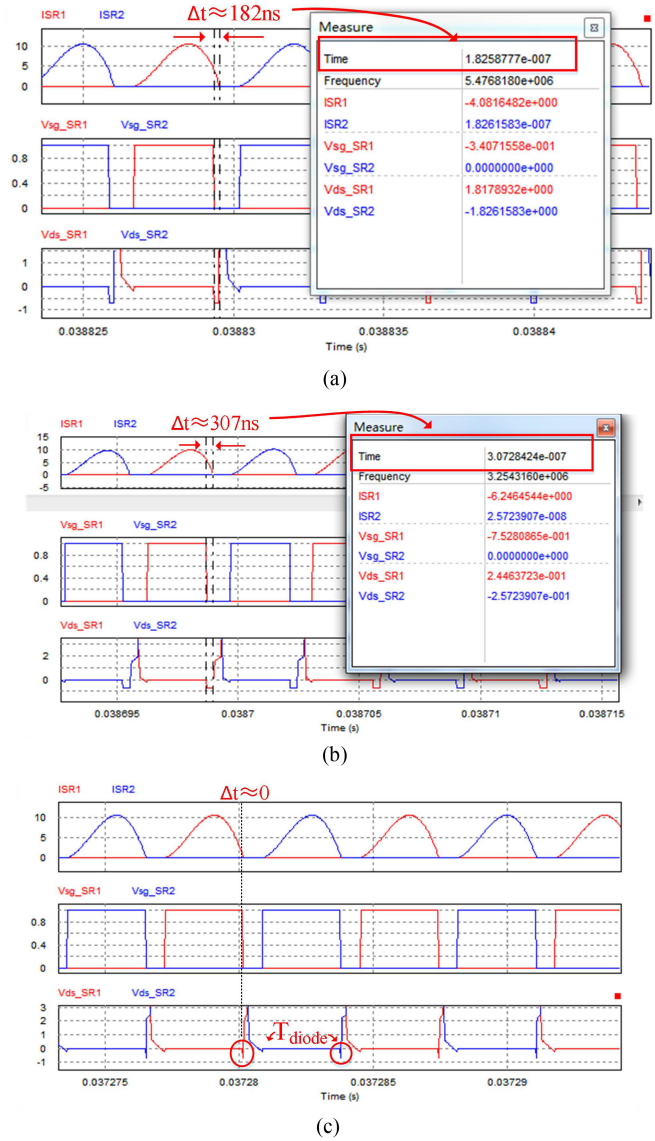

Fig. 12. Simulated secondary waveforms of *LLC* resonant converter with proposed SR driving scheme @ $I_o = 6$ A. (a) $\Delta L_r = \Delta L_m = 0$. (b) $\Delta L_r/L_r = -10\%$, $\Delta L_m/L_m = +10\%$. (c) $\Delta L_r/L_r = +10\%$, $\Delta L_m/L_m = -10\%$.

rated parameters, as shown in Fig. 12(a). The maximal dead time of one driving signal of SR has increased to 307 ns under the maximal tolerance condition with $\Delta L_r = -10\%$ and $\Delta L_m = +10\%$, as shown in Fig. 12(b). While under another maximal tolerance condition with $\Delta L_r = +10\%$ and $\Delta L_m = -10\%$, the dead time of one driving signal of SR is still close to zero and there is no inversion secondary current, as shown in Fig. 12(c).

The increase of dead time under light load condition lies in that the deviation angel θ is related to the load resistor, as shown in (21). Luckily, the current decreases as dead time increases, which means the increased dead time has slight influence on the efficiency of the converter.

Simulation results of the secondary waveforms of the *LLC* resonant converter with the proposed driving scheme during the load transient process from 6 to 20 A and vice versa are shown in Fig. 13. Similarly, margin of 100 ns has been left for the driving signal of SR. It can be seen that there is no inversion current on the secondary current during the transient process, which means the proposed driving scheme is very reliable.

IV. Experimental Result

The proposed *LLC* SR driving scheme is verified on a laboratory *LLC* converter prototype shown in Fig. 14. The conventional *LLC* controller L6599 is used as the controller. The electrical specifications and main components parameters of the prototype are listed in Table I. For convenience, a part of the inner

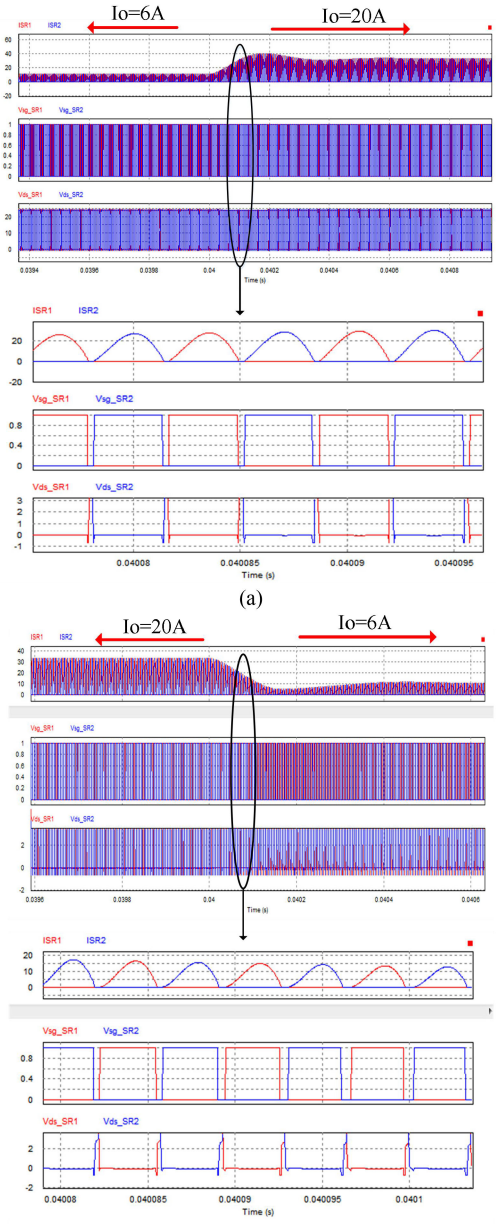

Fig. 13. Simulated waveforms of i_{SR} V_{gs_SR}, and V_{ds_SR} of SRs under load transient process. (a) Load step-up. (b) Load step-down.

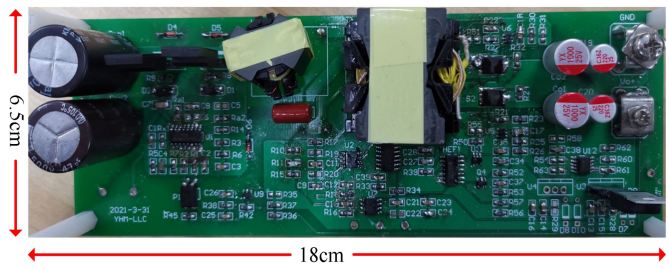

Fig. 14. Photograph of the experimental prototype of *LLC* converter with the proposed SR driving scheme.

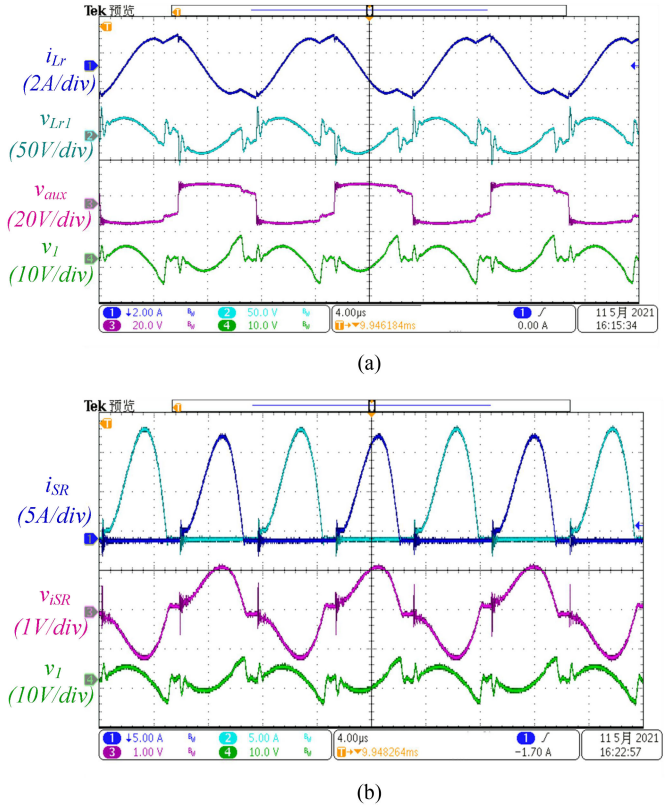

Fig. 15. Measured waveforms *LLC* resonant converter with the proposed SR driving scheme in DCM. (a) v_{iSR},v_{Lr1}, v_{aux}, and v_1. (b) v_{iSR}, v_1, i_{SR1}, and i_{SR2}.

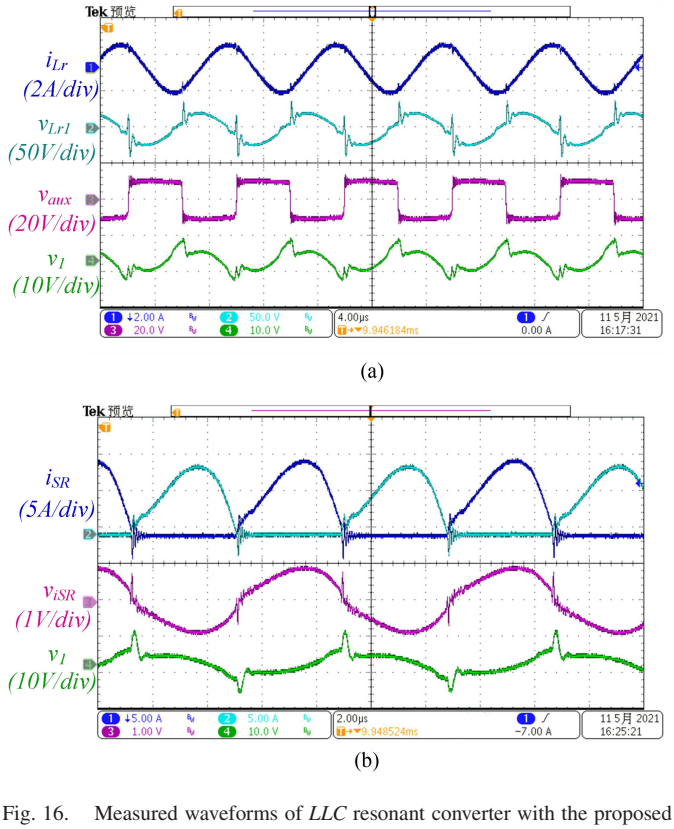

Fig. 16. Measured waveforms of *LLC* resonant converter with the proposed SR driving scheme in CCM. (a) v_{iSR},v_{Lr1}, v_{aux}, and v_1. (b) v_{iSR}, v_1, i_{SR1}, and i_{SR2}.

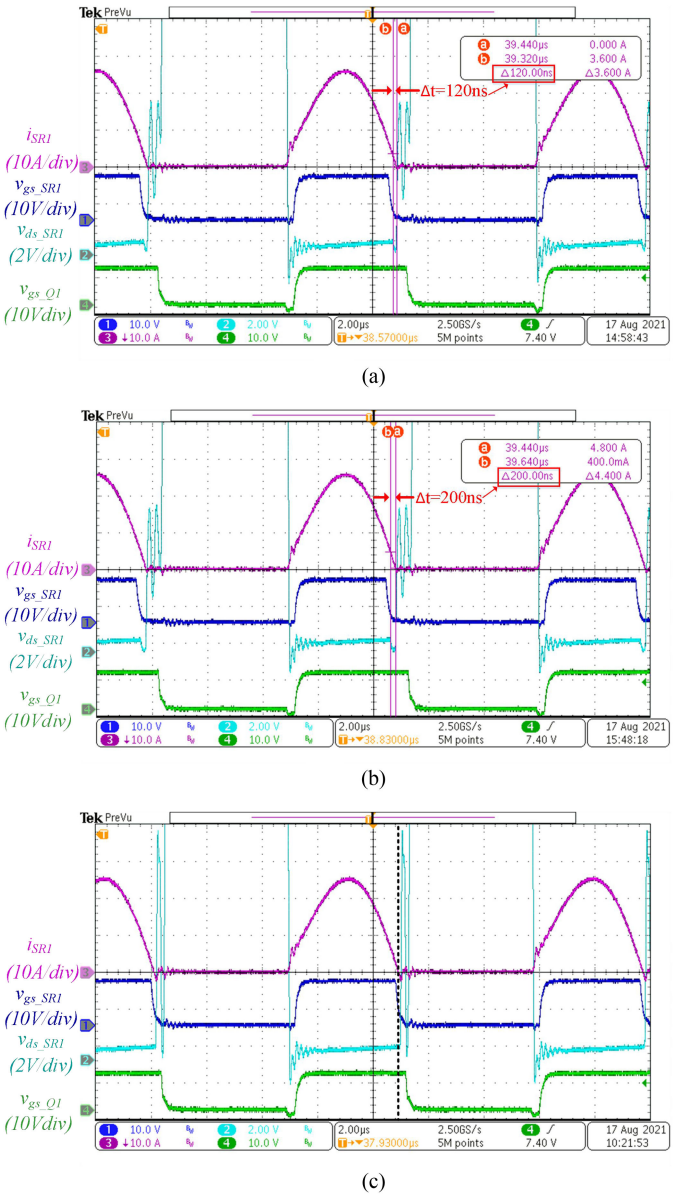

Fig. 17. Measured waveforms of i_{SR1}, v_{gs_SR1}, v_{ds_SR1}, and v_{gs_Q1} with the proposed SR driving scheme under full load. (a) $\Delta L_r = \Delta L_m = 0$. (b) $\Delta L_r/L_r = -10\%$, $\Delta L_m/L_m = +10\%$. (c) $\Delta L_r/L_r = +10\%$, $\Delta L_m/L_m = -10\%$.

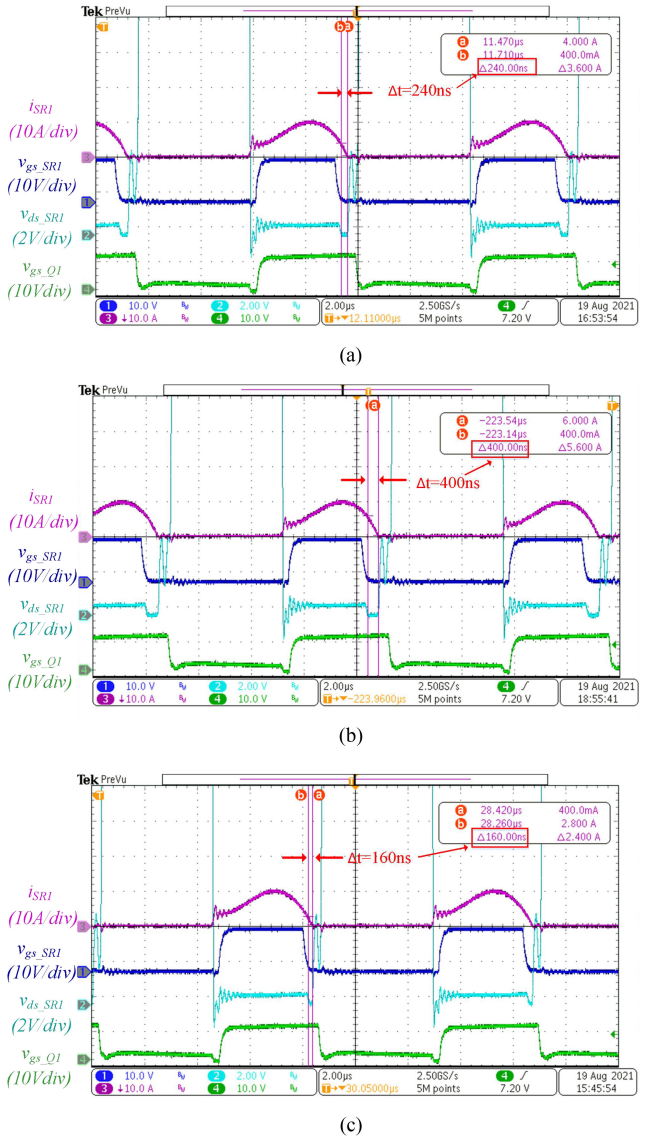

Fig. 18. Measured waveforms of i_{SR1}, v_{gs_SR1}, v_{ds_SR1}, and v_{gs_Q1} with the proposed SR driving scheme @ $I_o = 6$ A (a) $\Delta L_r = \Delta L_m = 0$. (b) $\Delta L_r/L_r = -10\%$, $\Delta L_m/L_m = +10\%$. (c) $\Delta L_r/L_r = +10\%$, $\Delta L_m/L_m = -10\%$.

circuit of the commercial SR driving IC NCP4306 is utilized as the SET signals generation circuit shown in Fig. 5.

Key waveforms of the converter with the proposed SR driving scheme operating in DCM and CCM are shown in Figs. 15 and 16, respectively.

It can be seen that v_{iSR} arises and falls synchronously with i_{SR} no matter in CCM mode or DCM mode. When i_{SR} of the SR drops to zero, v_{iSR} also drops to zero, which is consistent with theoretical analysis. Therefore, it is feasible to turn OFF SRs by detecting the zero-crossing point of v_{iSR} instead of detecting DS voltage of SRs.

Fig. 17 shows the measured waveforms of i_{SR1}, v_{gs_SR1}, v_{ds_SR1}, and v_{gs_Q1} under full load with/without inductance tolerances. To guarantee there is no inversion current under $\Delta L_r/L_r = +10\%$ and $\Delta L_m/L_m = -10\%$ as shown in Fig. 17(c), the dead time margin-left for v_{gs_SR1} is set to be 120 ns under the rated parameters as shown in Fig. 17(a), which is a little larger than the calculated value and simulation results. The maximal dead time has increased to 200 ns as shown in Fig. 17(b). The reason for the increase of dead time is induced by the time delay in the driving signal generation circuit, which is about 20 ns and has not been included in the calculation model and simulation circuit.

Fig. 18 shows the measured waveforms of i_{SR1}, v_{gs_SR1}, v_{ds_SR1}, and v_{gs_Q1} under light load with/without inductance tolerances. It can be seen that the dead time is about 240 ns under the rated parameters as shown in Fig. 18(a). The maximal dead time has increased to 400 ns under the condition of $\Delta L_r/L_r = -10\%$ and $\Delta L_m/L_m = +10\%$ as shown in Fig. 18(b), while the

TABLE II
COMPARISON ON THE PERFORMANCE OF SR DRIVING SCHEMES FOR *LLC* RESONANT CONVERTER

Schemes	Location	Implementation complexity	SR driving accuracy	Signal sensitivity	Cost	Range of application
Ref. [7]	Primary	High/digital+analog	Moderate	Low	High	Preferred for high power applications
Ref. [11]	Secondary	Low/analog	High	Low	Low	Preferred for dc transformers
Ref. [12]	Secondary	High/digital	High	Moderate	High	Preferred for high power applications
Ref. [13]	Secondary	High/analog	High	High	Low	Not suitable for high frequency applications
Ref. [14]	Primary	High/digital	Moderate	Low	High	Preferred for high power applications
Ref. [18]	Secondary	Moderate/digital	High	Low	High	Preferred for high power applications
Proposed scheme	Secondary	Low/analog	High	Low	Low	No limitation

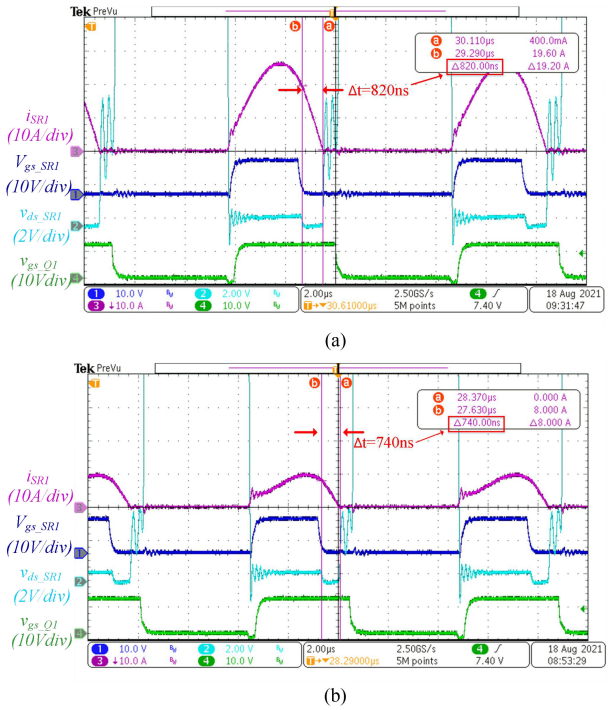

Fig. 19. Measured waveforms of i_{SR1}, v_{gs_SR1}, v_{ds_SR1}, and v_{gs_Q1} with commercial SR driving IC NCP4306. (a) $I_o = 20$ A. (b) $I_o = 6$ A.

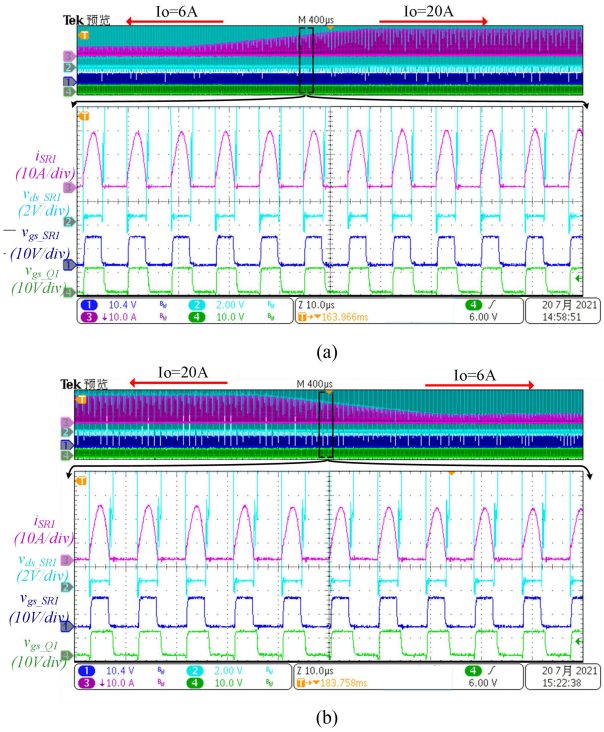

Fig. 20. Measured waveforms of i_{SR1}, v_{gs_SR1}, v_{ds_SR1}, and v_{gs_Q1} with the proposed SR driving scheme during load transient. (a) Load step-up. (b) Load step-down.

minimal dead time is 160 ns with $\Delta L_r/L_r = +10\%$ and $\Delta L_m/L_m = -10\%$. The actual values of dead time are a little larger the simulation results shown in Fig. 12 due to the time delay in the driving signal generation circuit.

For comparison, Fig. 19 shows the SR driving waveforms the commercial SR driving IC NCP4306, which generates SR driving signal by detecting the DS voltage of SR. It can be found that the dead time is about 820 ns under full load and 740 ns under light load, which are much larger than using the proposed SR driving scheme due to the influence of the parasitic inductance in package and on-board parasitic inductance from the SR driver to the gate of SR.

Experimental results of the *LLC* resonant converter with the proposed driving scheme during the load transient process from 6 to 20 A and vice versa are shown in Fig. 20. Similarly, margin of 120 ns has been left for the driving signal of SR. It can be seen that there is no inversion current flowing through SR during the

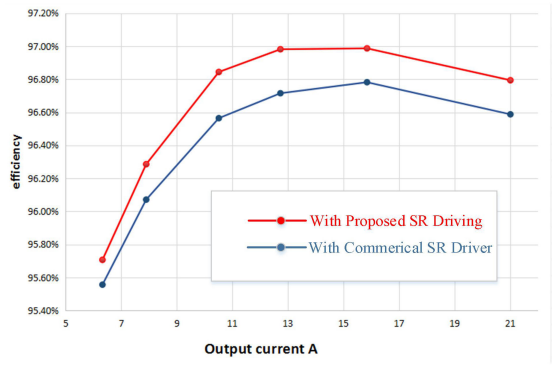

Fig. 21. Efficiency comparison between the *LLC* resonant converters with the proposed SR driving scheme and commercial SR driving IC.

transient process, which means the proposed driving scheme is very reliable.

Fig. 21 shows the measured efficiency curves between of the *LLC* prototype with the proposed SR driving scheme and with commercial SR driving IC NCP4306, respectively. It shows the efficiency of *LLC* resonant converter can be improved over a wide load range with the proposed SR driving scheme.

Furthermore, a comparison on the performance of the proposed SR driving scheme with previous works published in recent IEEE Journals is listed in Table II. It can be seen that the proposed SR driving scheme can achieve comprehensively better performance than most of the existing techniques.

V. Conclusion

In this article, a new SR driving scheme for *LLC* resonant converter based on secondary rectification current emulation is proposed. This scheme is realized with two auxiliary windings of magnetic components and some simple logic components. Furthermore, all logic components can be easily integrated into an IC. Thus, this scheme almost not increases the cost and size of the converter. The proposed SR driving scheme is not affected by the parasitic inductance and the on-state resistance of SR so that high precise SR driving signal can be achieved. Therefore, it is especially suitable for high frequency application. The feasibility of the proposed SR driving scheme has been verified by experimental results based on a laboratory experimental prototype. The load transient waveforms indicate that the proposed SR driving scheme can track the actual SR current period cycle-by-cycle so that inversion SR current can be avoided.

References

[1] Y. Wei, Q. Luo, Z. Wang, and H. A. Mantooth, "A complete step-by-step optimal design for LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3674–3691, Apr. 2021.

[2] H. Dong, X. Xie, and D. Yu, "Primary-side regulation scheme for LLC resonant converter with improved resonant current sampling circuit," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1242–1246, Feb. 2021.

[3] U. Ahmad, H. Cha, and N. Naseem, "Integrated current balancing transformer based input-parallel output-parallel LLC resonant converter modules," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5278–5289, May 2021.

[4] O. Kirshenboim and M. M. Peretz, "Combined multilevel and two phase interleaved LLC converter with enhanced power processing characteristics and natural current sharing," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5613–5620, Jul. 2018.

[5] K.-W. Kim, H.-S. Youn, J.-I. Baek, Y. Jeong, and G.-W. Moon, "Analysis on synchronous rectifier control to improve regulation capability of high-frequency LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7252–7259, Aug. 2018.

[6] Y. Wei, Q. Luo, and H. Alan Mantooth, "Synchronous rectification for LLC resonant converter: An overview," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7264–7280, Jun. 2021.

[7] M. Mohammadi and M. Ordonez, "Synchronous rectification of LLC resonant converters using homopolarity cycle modulation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1781–1790, Mar. 2018.

[8] NCP4306, "Secondary side synchronous rectifiation driver for high efficiency SMPS topologies," 2019. [Online]. Available: https://www.onsemi.cn/pdf/datasheet/ncp4306-d.pdf

[9] NCP4305, "Secondary side synchronous rectifiation driver for high efficiency SMPS topologies," 2016. [Online]. Available: https://www.onsemi.cn/pdf/datasheet/ncp4305-d.pdf

[10] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.

[11] M. Li, Z. Ouyang, M. A. E. Andersen, and B. Zhao, "Self-driven gate driver for LLC synchronous rectification," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 56–60, Jan. 2021.

[12] Z. Zhang, M. Wang, C. Liu, Y. Si, Y. Liu, and Q. Lei, "High-dv/dt-immune fine-controlled parameter-adaptive synchronous gate driving for GaN-based secondary rectifier in EV on-board charger," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi: 10.1109/JESTPE.2020.3034036.

[13] S. C. Moon, C. S. Chen, and R.-J. Wang, "A new dead time regulation synchronous rectification control method for high efficiency LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10673–10683, Sep. 2021.

[14] J.-D. Hsu, M. Ordonez, W. Eberle, M. Craciun, and C. Botting, "LLC synchronous rectification using resonant capacitor voltage," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10970–10987, Nov. 2019.

[15] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3775–3781, Aug. 2012.

[16] M. Sato, G. M. Dousoky, and M. Shoyama, "Improved digital control scheme of synchronous rectification for resonant converter at light load conditions," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 2015, pp. 1–5.

[17] F. Wang, B. A. McDonald, J. Langham, and B. Fan, "A novel adaptive synchronous rectification method for digitally controlled LLC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 334–338.

[18] C. Fei, Q. Li, and F. C. Lee, "Digital implementation of adaptive synchronous rectifier (SR) driving scheme for high-frequency LLC converters with microcontroller," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5351–5361, Jun. 2018.

[19] X. Wu, G. Hua, J. Zhang, and Z. Qian, "A new current-driving synchronous rectifier for series-sarallel resonant (LLC) DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 289–297, Jan. 2011.

[20] J. Zhang, W. Jianfeng, G. Zhang, and Z. Qian, "A hybrid driving scheme for full-bridge synchronous rectifier in LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4549–4561, Nov. 2012.

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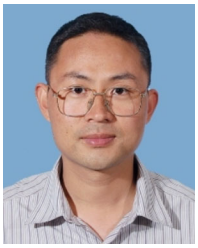

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