A Novel Approach to Model and Analyze Uneven Temperature Distribution Among Multichip High-Power Modules and Corresponding Method to Respecify Device SOA

Jianpeng Wang, *Student Member, IEEE*, Wenjie Chen, *Senior Member, IEEE*, Jin Zhang, *Student Member, IEEE*, Meng Xu, *Student Member, IEEE*, Laili Wang, *Senior Member, IEEE*, Jinjun Liu, *Fellow, IEEE*, and Yongmei Gan, *Member, IEEE*

***Abstract*—As the most widely used power semiconductor devices, insulated gate bipolar transistor (IGBT) modules are normally composed of parallel IGBT chips to achieve the desired current capability. However, the electrothermal behavior of each chip is significantly different due to the asymmetric layout, increasing the overheating risk of single chip. Therefore, this article proposes a novel approach to describe the thermal safe operation area of multichip IGBT modules in the inverter application, considering the uneven temperature distribution among parallel chips. The novelty of the approach is that it applied the proposed analytical model describing the uneven electrothermal behavior, thus avoiding the traditional averaging process. Comprehensive investigation has been made to reveal the deep mechanism of the inconsistent temperature distribution, which are the uneven dynamic current sharing and thermal cross-coupling effects. Correspondingly, the analytical model of the uneven switching loss and the standard form of thermal resistance matrix related to cooling performance are proposed and further verified, respectively. Based on the proposed approach, the recommended operation area of different rated devices is fully described. The contribution of this article enables more well-founded device selection to achieve a safe and cost-efficient design for the inverter application.**

***Index Terms*—Finite element method (FEM), insulated gate bipolar transistor (IGBT), thermal model, thermal safe operation area (TSOA).**

I. Introduction

THE power semiconductor module is considered as the core of power converters, which greatly determines the critical performance of the entire system, such as efficiency, cost, and reliability [1]–[4]. As the most widely used power semiconductor devices, insulated gate bipolar transistor (IGBT) modules are normally composed of parallel IGBT chips to achieve the desired current carrying capability. However, the electrothermal behavior of each chip cannot be completely consistent due to the asymmetric layout, increasing the overheating risk of a single chip [5]. Therefore, the accurate calculation on the power loss and junction temperature of each chip in multichip IGBT modules is important for the safe and efficient inverter design. The electrothermal simulation is the accurate method to calculate the power loss and thermal loading of power module according to the electrical profiles of the converter. Common electricity models of devices, such as Hefner model [6]–[7], lumped-charge model [8]–[10], and Fourier-based IGBT model [11], can be used to predict the electrical behavior of IGBT modules, especially the switching behavior. Besides, a series of thermal models, such as 3-D lumped thermal model [12], [13] and finite element (FE) model [14], [15], have been established and cosimulated with the device electricity model. However, the mentioned simulation method is not suitable for the rapid initial design, due to the complicated parameter extraction process [16]–[18], and low simulation efficiency.

To support the device selection in the initial design stage, manufacturers, such as Infineon [19] and SEMIKRON [20], have provided online power simulation programs for fast power loss and thermal calculation of their power modules. Furthermore, some fast batch calculation methods used to guide the initial inverter design have been presented in the previous literature. Ma *et al*. [21] proposed a more complete loss and thermal model considering not only the electrical loading but also the device rating as input variables, which greatly improved the freedom of converter design. Zhang *et al*. [22] proposed simplified thermal modeling for IGBT modules according to the operation condition characteristics of modular multilevel converters. Merkert *et al*. [23] presented a characterization and scalable loss and thermal modeling approach of power semiconductors. In the above methods [21]–[23], the average device power loss model based on a lookup table or data fitting is used to replace the device electricity model and co-simulated with the conventional

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The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: wangjackmvp@stu.xjtu.edu.cn; cwj@mail.xjtu.edu.cn; z062626@stu.xjtu.edu.cn; xmlemon@stu.xjtu.edu.cn; llwang@mail.xjtu.edu.cn; jjliu@mail.xjtu.edu.cn; ymgan@mail.xjtu.edu.cn).

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1-D *RC* lumped thermal model to achieve faster calculation efficiency. However, the resulting calculation error would increase significantly under certain operation conditions for the following two reasons. The first one is the uneven current distribution among parallel chips in the power module, caused by the asymmetric layout [24]. Especially at high switching frequency, the uneven transient current can cause large switching loss differences among chips. Therefore, the average power loss model might result in the underestimation of the power loss of the specific chip among parallel chips. The second one is the thermal cross-coupling effect among parallel chips, which means that the junction temperature of a chip is not only affected by its own power losses but also that of neighboring chips [25]. The conventional 1-D thermal model ignoring this effect might cause the underestimation of the predicted junction temperature. The misleading results are not conducive to the design of converters, since too small margin increases the risk of thermal failure.

To deal with these issues in the fast junction temperature calculation for more accurate estimation results, this article proposes an approach to evaluate the thermal safe operation area (TSOA) of multichip IGBT modules in the inverter application, considering the inconsistent junction temperature distribution among parallel chips. The novelty of the evaluation approach is twofold.

1) An analytical model of the uneven switching loss is proposed, thus the difference of power loss among chips can be expressed.
2) A standard form of the element in the thermal resistance matrix is proposed considering the cooling condition, which can fully reflect the influence of the cooling system on the junction temperature distribution of parallel chips.

Owing to the above contribution, the maximum thermal stress of a single chip is focused on rather than the average value of the entire module. Therefore, the proposed evaluation approach can provide a well-founded and fast device selection scheme to achieve the safe and cost-efficient initial design for the inverter application.

The rest of this article is organized as follows. In Sections II and III, comprehensive investigation has been made to reveal the deep mechanism of inconsistent junction temperature, where two key influencing factors, i.e., uneven dynamic current sharing and thermal cross-coupling effects, are introduced from the three aspects of experimental findings, qualitative analysis and quantitative calculation, respectively. The analytical relationship between the switching loss of each chip and operating conditions, the thermal resistance matrix and the cooling performance, are established and further verified by the experiment and FEM simulation. In Section IV, the calculation process of junction temperature based on the above models is introduced and compared with commercial software, and further verified by the inverter experimental prototype. Then, the complete evaluation approach of TSOA is presented and the TSOA of standard 1200-V half-bridge IGBT modules with EconoDUAL housing are fully evaluated under different operation conditions. Correspondingly, the recommended operation area of different rated devices is also described. Finally, Section V concludes this article.

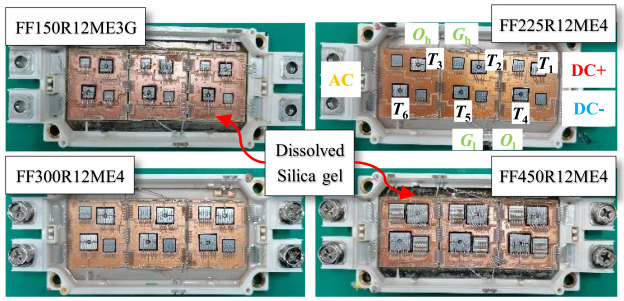


Fig. 1. Layout of researched IGBT modules with the housing of EconoDUAL.

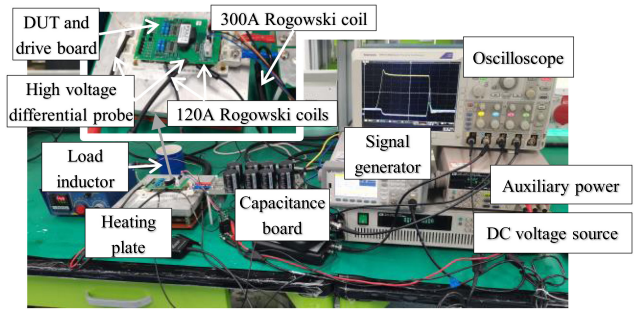


Fig. 2. DPT platform.

II. Modeling and Calculation of Uneven Switching Losses for Parallel Chips

A. Experimental Findings

The phenomenon of uneven dynamic current sharing among parallel chips has been reported and researched for several years [26]–[30], and it is considered to be a major problem affecting the performance of multichip power modules. However, few articles researched the quantitative relationship between the imbalance ratio of switching loss and various operating conditions for a specific package structure. In the article, 1200-V half-bridge IGBT modules with the housing of EconoDUAL are selected for modeling and experimental verification, as shown in Fig. 1.

First, the experimental study on module FF225R12ME4 is presented. Double pulse test (DPT) is carried out to obtain the switching behaviors, as shown in Fig. 2. In the platform, the Rogowski coil rated at 300 A is used to measure the switching current of the IGBT module, and which rated 120 A is used to measure the switching current of each IGBT chip. The test results are shown in Fig. 3, where the chip number refers to Fig. 1. The corresponding switching losses are also calculated and shown in the figure. According to Fig. 3, the following qualitative conclusions can be obtained.

1) The differences of turn-ON energy losses are much larger than that of turn-OFF energy losses, whatever among high-side or low-side parallel chips.
2) The differences of the turn-ON energy losses among low-side parallel chips are much greater than that of the high-side chips.
3) The chip close to dc negative terminal (T_4 in the figure) withstands the largest switching loss among all the chips.

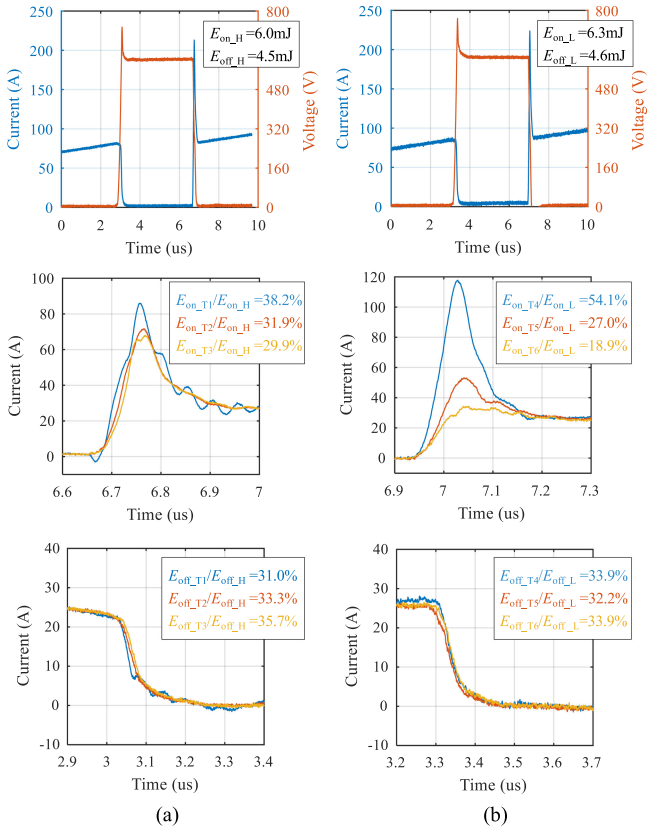


Fig. 3. Measured switching waveforms and energy losses of (a) high-side parallel chips and (b) low-side parallel chips.

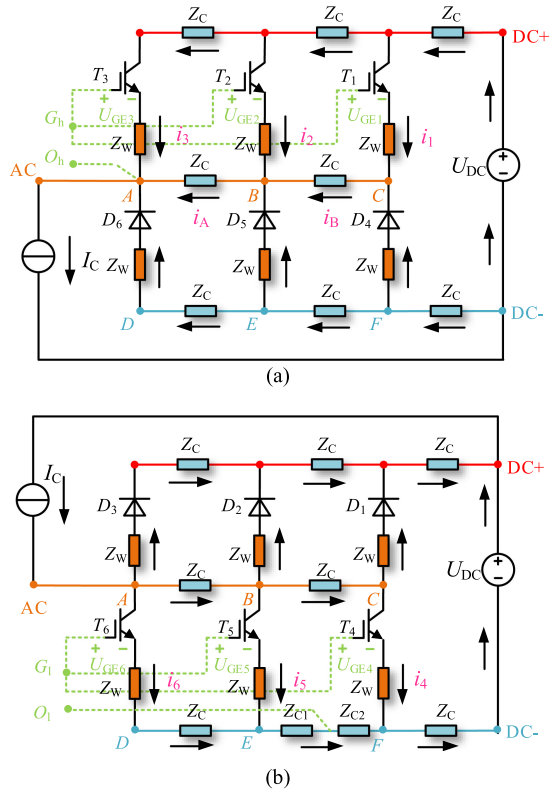


Fig. 4. Equivalent circuit diagrams at turn-ON transient of (a) high-side parallel chips and (b) low-side parallel chips.

B. Qualitative Analysis

Fig. 4 shows the equivalent circuits of turn-ON transient of the high-side and low-side parallel chips, respectively. Z_C is the stray impedance of the copper layer among parallel chips, and Z_W is the stray impedance of the bond wires-connected chips and copper layers. The following equation is applied to simplify the expression for the qualitative analysis:

$$\begin{cases} Z_W = Z_C = Z_{C1} = sL \\ Z_{C2} = 0 \end{cases} \tag{1}$$

where s is the Laplace operator. Besides, the uneven stray impedance of the gate is ignored in this article since the unbalanced dynamic current is more sensitive to the mismatched power source stray impedance as discussed in [24], [29], and [30]. Moreover, the mutual inductances among different commutation loops are also ignored in the quantitative analysis [29], [30].

When the chips turn ON, the current of each chip i_k can be expressed as follows:

$$i_k = g_m(u_{GEk} - U_{th}) \tag{2}$$

where $k = 1$ to 6. g_m and U_{th} are the transconductance and threshold voltage of IGBT chip, respectively. u_{GEk} is the gate–emitter voltage of the kth chip.

For high-side parallel chips, u_{GE1}, u_{GE2}, and u_{GE3} can be expressed as the following formula, according to Fig. 4(a):

$$\begin{cases} u_{GE1} = u_{GO\_h} - L\dfrac{di_1}{dt} - L\left(\dfrac{di_A}{dt} + \dfrac{di_B}{dt}\right) \\ u_{GE2} = u_{GO\_h} - L\dfrac{di_2}{dt} - L\dfrac{di_A}{dt} \\ u_{GE3} = u_{GO\_h} - L\dfrac{di_3}{dt} \end{cases} \tag{3}$$

where i_A is the current flowing from B to A, i_B is the current flowing from C to B, and $u_{\mathrm{GO\_h}}$ is the voltage between G_h and O_h, as shown in Fig. 4(a). According to Kirchhoff's laws, the voltage relationship among point A to F can be expressed by

$$\begin{cases} L\frac{di_A}{dt} + L\left(\dfrac{di_A}{dt} - \dfrac{di_2}{dt} - \dfrac{di_B}{dt}\right) \\ -2L\left(\dfrac{dI_C}{dt} - \dfrac{di_A}{dt} - \dfrac{di_3}{dt}\right) = 0 \\ L\left(\dfrac{di_A}{dt} - \dfrac{di_2}{dt} - \dfrac{di_B}{dt}\right) + L\left(\dfrac{dI_C}{dt} - \dfrac{di_3}{dt} - \dfrac{di_2}{dt} - \dfrac{di_B}{dt}\right) \\ -L\dfrac{di_B}{dt} - L\left(\dfrac{di_B}{dt} - \dfrac{di_1}{dt}\right) = 0 \end{cases} \tag{4}$$

where I_C is the total load current of the module, which can be considered a steady variable since it changes little during the fast turn-ON transient. Therefore, the above formula can be

transformed into

$$\begin{cases} 4L\dfrac{di_A}{dt} - L\dfrac{di_B}{dt} - L\dfrac{di_2}{dt} + 2L\dfrac{di_3}{dt} = 0 \\ L\dfrac{di_A}{dt} - 4L\dfrac{di_B}{dt} + L\dfrac{di_1}{dt} - 2L\dfrac{di_2}{dt} - L\dfrac{di_3}{dt} = 0. \end{cases} \tag{5}$$

Therefore, the following formula can be reached after rearranging:

$$\mathbf{di_x} = \mathbf{A^{-1}B di_{n\_H}} \tag{6}$$

where $\mathbf{A} = \begin{bmatrix} 4L & -L \\ L & -4L \end{bmatrix}$, $\mathbf{B} = \begin{bmatrix} 0 & L & -2L \\ -L & 2L & L \end{bmatrix}$, $\mathbf{di_x} = \left[\frac{di_A}{dt}, \frac{di_B}{dt}\right]^T$, $\mathbf{di_{n\_H}} = \left[\frac{di_1}{dt}, \frac{di_2}{dt}, \frac{di_3}{dt}\right]^T$. Substituting (2) and (6) into (3), the following formula can be obtained as:

$$\begin{aligned} \frac{1}{g_m}\mathbf{E i_{n\_H}} &= (u_{GO\_h} - U_{th})\mathbf{I} - L\mathbf{E di_{n\_H}} - \mathbf{C di_x} \\ &= (u_{GO\_h} - U_{th})\mathbf{I} - (L\mathbf{E} + \mathbf{CA^{-1}B})\mathbf{di_{n\_H}} \end{aligned} \tag{7}$$

where $\mathbf{i_x} = [i_A, i_B]^T$, $\mathbf{i_{n\_H}} = [i_1, i_2, i_3]^T$, $\mathbf{C} = \begin{bmatrix} sL & sL \\ sL & 0 \\ 0 & 0 \end{bmatrix}$, $\mathbf{E}$ is a third-order identity matrix, and $\mathbf{I} = [1,1,1]^T$. According to the differential properties of Laplace transform, the Laplace transform of $\mathbf{di_{n\_H}}$ can be expressed as the following formula since the initial value of $\mathbf{i_{n\_H}}$ is equal to zero:

$$L(\mathbf{di_{n\_H}}) = s\mathbf{i_{n\_H}}(s) - \mathbf{i_{n\_H}}(0-) = s\mathbf{i_{n\_H}}(s). \tag{8}$$

Therefore, the Laplace transform of (7) can be expressed as

$$\begin{aligned} \frac{1}{g_m}\mathbf{E i_{n\_H}}(s) = &\left(u_{GO\_h}(s) - \frac{U_{th}}{s}\right) \\ &\mathbf{I} - (sL\mathbf{E} + s\mathbf{CA^{-1}B})\mathbf{i_{n\_H}}(s). \end{aligned} \tag{9}$$

According to (9), $\mathbf{i_{n\_H}}(s)$ can be calculated by

$$\begin{aligned} \mathbf{i_{n\_H}}(s) &= \left(u_{GO\_h}(s) - \frac{U_{th}}{s}\right)\left[\left(\frac{1}{g_m} + sL\right)\mathbf{E} + s\mathbf{CA^{-1}B}\right]^{-1}\mathbf{I} \\ &= \begin{bmatrix} \dfrac{g_m\left(42L^2{g_m}^2s^2 + 52Lg_ms + 15\right)\left(u_{GO\_h}(s) - \frac{U_{th}}{s}\right)}{(23L^3{g_m}^3s^3 + 60L^2{g_m}^2s^2 + 52Lg_ms + 15)} \\ \dfrac{g_m\left(30L^2{g_m}^2s^2 + 43Lg_ms + 15\right)\left(u_{GO\_h}(s) - \frac{U_{th}}{s}\right)}{(23L^3{g_m}^3s^3 + 60L^2{g_m}^2s^2 + 52Lg_ms + 15)} \\ \dfrac{g_m\left(u_{GO\_h}(s) - \frac{U_{th}}{s}\right)}{(Lg_ms + 1)} \end{bmatrix}. \end{aligned} \tag{10}$$

Therefore, the ratio of current among chip T_1, T_2, and T_3 can be expressed as

$$\begin{cases} \xi_{12} = \dfrac{\mathbf{i_{n\_H}}_{(1)}(s)}{\mathbf{i_{n\_H}}_{(2)}(s)} = \dfrac{42L^2{g_m}^2s^2 + 52Lg_ms + 15}{30L^2{g_m}^2s^2 + 43Lg_ms + 15} > 1 \\ \xi_{23} = \dfrac{\mathbf{i_{n\_H}}_{(2)}(s)}{\mathbf{i_{n\_H}}_{(3)}(s)} = \dfrac{30L^2{g_m}^2s^2 + 43Lg_ms + 15}{23L^2{g_m}^2s^2 + 37Lg_ms + 15} > 1 \\ \xi_{13} = \dfrac{\mathbf{i_{n\_H}}_{(1)}(s)}{\mathbf{i_{n\_H}}_{(3)}(s)} = \dfrac{42L^2{g_m}^2s^2 + 52Lg_ms + 15}{23L^2{g_m}^2s^2 + 37Lg_ms + 15} > 1. \end{cases} \tag{11}$$

According to (11), the order of turn-ON current and loss among high-side parallel chips are

$$i_1 > i_2 > i_3 \tag{12}$$

$$E_{ON\_1} > E_{ON\_2} > E_{ON\_3}. \tag{13}$$

While for the low-side parallel chips, u_{GE4}, u_{GE5}, and u_{GE6} can be expressed as the following formula (14), according to Fig. 4(b):

$$\begin{cases} u_{GE4}(s) = u_{GO\_l}(s) - Z_W i_4(s) + Z_{C2} i_5(s) + Z_{C2} i_6(s) \\ u_{GE5}(s) = u_{GO\_l}(s) - (Z_W + Z_{C1}) i_5(s) - Z_{C1} i_6(s) \\ u_{GE6}(s) = u_{GO\_l}(s) - Z_{C1} i_5(s) - (Z_W + Z_C + Z_{C1}) i_6(s) \end{cases} \tag{14}$$

where u_{GO_l} is the voltage between G_l and O_l, as shown in Fig. 4(b). Substituting (2) into (14), the following formula can be reached after rearranging:

$$\frac{1}{g_m}\mathbf{E i_{n\_L}}(s) = \left(u_{GO\_l}(s) - \frac{U_{th}}{s}\right)\mathbf{I} - \mathbf{D i_{n\_L}}(s) \tag{15}$$

where $\mathbf{D} = \begin{bmatrix} sL & 0 & 0 \\ 0 & 2sL & sL \\ 0 & sL & 3sL \end{bmatrix}$. $\mathbf{i_{n\_L}} = [i_4, i_5, i_6]^T$, and its calculation result is

$$\begin{aligned} \mathbf{i_{n\_L}}(s) &= \left(u_{GO\_l}(s) - \frac{U_{th}}{s}\right)\left[\frac{1}{g_m}\mathbf{E} + \mathbf{D}\right]^{-1}\mathbf{I} \\ &= \begin{bmatrix} \dfrac{g_m\left(u_{GO\_l}(s) - \frac{U_{th}}{s}\right)}{(Lg_ms + 1)} \\ \dfrac{g_m\left(2Lg_ms + 1\right)\left(u_{GO\_l}(s) - \frac{U_{th}}{s}\right)}{(5L^2{g_m}^2s^2 + 5Lg_ms + 1)} \\ \dfrac{g_m(Lg_ms + 1)(u_{GO\_l}(s) - \frac{U_{th}}{s})}{(5L^2{g_m}^2s^2 + 5Lg_ms + 1)} \end{bmatrix}. \end{aligned} \tag{16}$$

Then, the ratio of current among chip T_4, T_5, and T_6 can be expressed as

$$\begin{cases} \xi_{45} = \dfrac{\mathbf{i_{n\_L}}_{(4)}(s)}{\mathbf{i_{n\_L}}_{(5)}(s)} = \dfrac{5L^2{g_m}^2s^2 + 5Lg_ms + 1}{2L^2{g_m}^2s^2 + 3Lg_ms + 1} > 1 \\ \xi_{56} = \dfrac{\mathbf{i_{n\_L}}_{(5)}(s)}{\mathbf{i_{n\_L}}_{(6)}(s)} = \dfrac{2Lg_ms + 1}{Lg_ms + 1} > 1 \\ \xi_{46} = \dfrac{\mathbf{i_{n\_L}}_{(4)}(s)}{\mathbf{i_{n\_L}}_{(6)}(s)} = \dfrac{5L^2{g_m}^2s^2 + 5Lg_ms + 1}{L^2{g_m}^2s^2 + 2Lg_ms + 1} > 1. \end{cases} \tag{17}$$

According to (17), the order of turn-ON current and loss among high-side parallel chips are as follows:

$$i_4 > i_5 > i_6 \tag{18}$$

$$E_{ON\_4} > E_{ON\_5} > E_{ON\_6}. \tag{19}$$

Furthermore, the ratio of the imbalanced current between the high-side and low-side parallel chips can be characterized

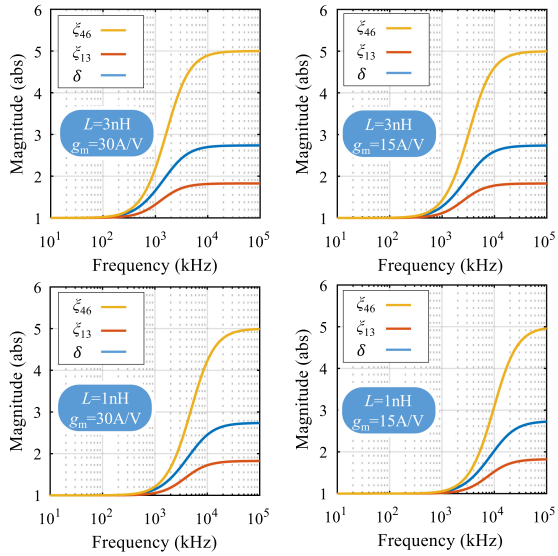


Fig. 5. Magnitude–frequency characteristic curves of uneven current ratio with variable parameters.

by

$$\delta = \frac{\xi_{46}}{\xi_{13}} = \frac{115L^4{g_m}^4s^4+300L^3{g_m}^3s^3+283L^2{g_m}^2s^2+112Lg_ms+15}{42L^4{g_m}^4s^4+136L^3{g_m}^3s^3+161L^2{g_m}^2s^2+82Lg_ms+15} > 1. \quad (20)$$

According to formulas (11), (17), and (20), the magnitude–frequency characteristic curves of uneven current ratio are described as Fig. 5. It indicates that the imbalance of current of the low-side chips is much greater than that of the high-side chips. What is more, the uneven current ratio would increase as the current rise time decreases (as the frequency increases). Besides, the decrease of g_m and L can delay the responses in the frequency domain, thereby improving the current imbalance ratio.

Different from turn-ON current, turn-OFF current is less influenced by the inconsistent parasitic inductance caused by asymmetrical layout [31], [32]. Therefore, the current sharing at turn-OFF transient is more balanced, regardless of high-side or low-side chips.

The above qualitative analysis results are consistent with the DPT results shown in Fig. 3. It can be concluded that among all switching processes, the uneven turn-ON losses of low-side chips are the most severe, which cannot be ignored at high-frequency inverter applications.

C. Quantitative Calculation

According to the results of qualitative analysis in Section II-B, an accurate quantitative calculation model for the uneven turn-ON losses of the low-side parallel chips need to be proposed. Therefore, some ideal assumptions and simplifications in Section II-C are not adopted in this section to ensure calculation accuracy.

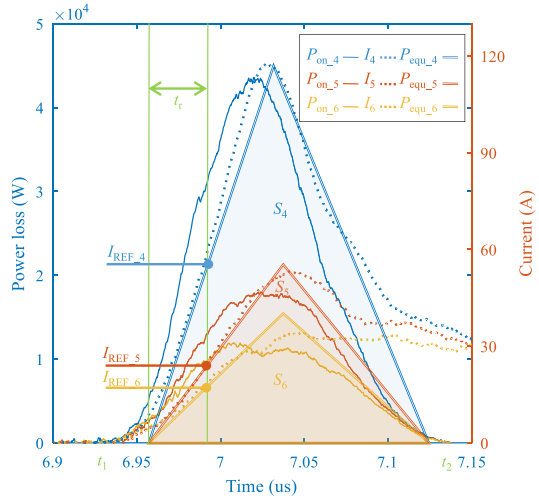


Fig. 6. Schematic diagram of equivalent turn-ON losses.

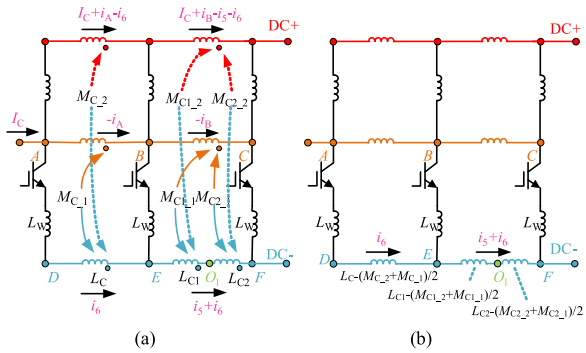


Fig. 7. Schematic diagram of parasitic inductance inside the IGBT module. (a) Circuit considering mutual inductances. (b) Decoupled circuit.

To simplify the calculation process, the concept of equivalent turn-ON losses P_{equ} is proposed, as shown in Fig. 6. The form of P_{equ} is a series of triangles with the same base side, and the slope of the left side is proportional to that of the current within rise time t_r. The rise time t_r is defined by power semiconductor manufacturers, that is, the rise time of the power module from 10% I_C to 90% I_C during the turn-ON transient. The rise time can be obtained by datasheet or DPT for the power module. In this way, the area of the geometry formed by P_{ON} and the abscissa axis is similar to the area of the triangle formed by P_{equ} and the abscissa axis. Therefore, the ratio of each chip's turn-ON loss to the total turn-ON losses can be simplified as follows:

$$n_k = \frac{\int_{t_1}^{t_2} P_{on\_k}\,dt}{\sum_{k=4}^{6}\int_{t_1}^{t_2} P_{on\_k}\,dt} \approx \frac{S_k}{\sum_{i=4}^{6} S_k} = \frac{I_{REF\_k}}{\sum_{i=4}^{6} I_{REF\_k}} \quad (21)$$

where $k = 4$, 5, or 6. Moreover, the mutual inductances among different commutation loops should be considered in the quantitative calculation. The symbols of mutual inductance refer to Fig. 7. Correspondingly, (14) can be rewritten in time-domain

form as the following formula:

$$\begin{cases} u_{GE4} = u_{GO\_l} - L_W\dfrac{di_4}{dt} + L_{C2}\left(\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) - M_{C2\_1}\dfrac{di_B}{dt} \\ -M_{C2\_2}\left(-\dfrac{di_B}{dt}+\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) \\ u_{GE5} = u_{GO\_l} - L_W\dfrac{di_5}{dt} - L_{C1}\left(\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) + M_{C1\_1}\dfrac{di_B}{dt} \\ +M_{C1\_2}\left(-\dfrac{di_B}{dt}+\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) \\ u_{GE6} = u_{GO\_l} - (L_W+L_C)\dfrac{di_6}{dt} + M_{C\_1}\dfrac{di_A}{dt} \\ +M_{C\_2}\left(-\dfrac{di_A}{dt}+\dfrac{di_6}{dt}\right) \\ -L_{C1}\left(\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) + M_{C1\_1}\dfrac{di_B}{dt} + M_{C1\_2} \\ \left(-\dfrac{di_B}{dt}+\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right). \end{cases} \tag{22}$$

When M_{C2_1}, M_{C1_1}, and M_{C_1} are close to M_{C2_2}, M_{C1_2}, and M_{C_2}, respectively, (20) can be approximately reached

$$\begin{cases} M_{C2\_1}\dfrac{di_B}{dt} + M_{C2\_2}\left(-\dfrac{di_B}{dt}+\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) \\ \approx \dfrac{M_{C2\_1}+M_{C2\_2}}{2}\left(\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) \\ M_{C1\_1}\dfrac{di_B}{dt} + M_{C1\_2}\left(-\dfrac{di_B}{dt}+\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) \\ \approx \dfrac{M_{C1\_1}+M_{C1\_2}}{2}\left(\dfrac{di_5}{dt}+\dfrac{di_6}{dt}\right) \\ M_{C\_1}\dfrac{di_A}{dt} + M_{C\_2}\left(-\dfrac{di_A}{dt}+\dfrac{di_6}{dt}\right) \\ \approx \dfrac{M_{C1\_1}+M_{C1\_2}}{2}\left(\dfrac{di_6}{dt}\right). \end{cases} \tag{23}$$

In this way, the mutual inductances can be decoupled, as shown in Fig. 7(b).

According to Fig. 6, the slope of the current within the rise time can be approximately considered as constant, which is

$$\frac{di_k}{dt} \approx \frac{I_{REF\_k}}{t_r}. \tag{24}$$

Furthermore, considering the nonlinearity of g_m, (2) can be rewritten in quadratic form and then linearized at $I_C/3$, as

$$\begin{aligned} u_{GEk}(i_k) &= \sqrt{\frac{i_k}{\beta}} + U_{th} \\ &\approx \sqrt{\frac{I_C}{3\beta}} + U_{th} + \frac{\sqrt{3}}{2\sqrt{\beta I_C}}\left(i_k - \frac{I_C}{3}\right) \end{aligned} \tag{25}$$

where β is a constant determined by device structure and doping concentration. Therefore, the expression of U_{GEk} at I_{REF_k} can be simplified as

$$U_{GEk} \approx \sqrt{\frac{I_C}{3\beta}} + U_{th} + \frac{\sqrt{3}}{2\sqrt{\beta I_C}}\left(I_{REF\_k} - \frac{I_C}{3}\right). \tag{26}$$

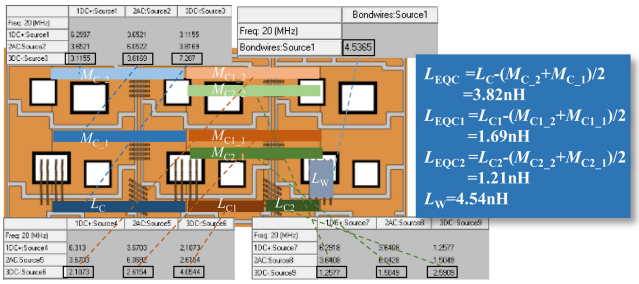


Fig. 8. Extraction process of parasitic inductance inside FF225R12ME4 by Q3D Extractor.

Substituting (23)–(26), (22) can be rewritten as

$$\frac{\sqrt{3}}{2\sqrt{\beta I_C}}\mathbf{EI_{REF}} = \left(u_{GO\_l} - U_{th} - \sqrt{\frac{I_C}{12\beta}}\right)\mathbf{I} - \mathbf{FI_{REF}} \tag{27}$$

where

$$\mathbf{F} = \begin{bmatrix} L_W/t_r & -L_{EQC2}/t_r & -L_{EQC2}/t_r \\ 0 & (L_{EQC1}+L_W)/t_r & L_{EQC1}/t_r \\ 0 & L_{EQC1}/t_r & (L_{EQC1}+L_W+L_{EQC})/t_r \end{bmatrix}$$

in which $L_{EQC2} = L_{C2}$-(M_{C2_2}+M_{C2_1})/2, $L_{EQC1} = L_{C1}$-(M_{C1_2}+M_{C1_1})/2, and $L_{EQC} = L_C$-(M_{C_2}+M_{C_1})/2. $\mathbf{I_{REF}} = [I_{REF\_4}, I_{REF\_5}, I_{REF\_6}]^T$, and its calculation result is

$$\mathbf{I_{REF}} = \left(u_{GO\_l} - U_{th} - \sqrt{\frac{I_C}{12\beta}}\right)\left(\frac{\sqrt{3}}{2\sqrt{\beta I_C}}\mathbf{E} + \mathbf{F}\right)^{-1}\mathbf{I}. \tag{28}$$

Therefore, the calculation result of (21) is

$$n_k = \frac{\mathbf{I_{REF}}(k)}{\sum_{k=4}^{6}\mathbf{I_{REF}}(k)} = \frac{\mathbf{G}(k)}{\sum_{k=4}^{6}\mathbf{G}(k)} \tag{29}$$

where $\mathbf{G}(k) = (\frac{\sqrt{3}}{2\sqrt{\beta I_C}}\mathbf{E} + \mathbf{F})^{-1}\mathbf{I}$.

To verify the accuracy of above quantitative relationship, a series of DPTs under different load currents, bus voltages, junction temperatures, and gate resistances are carried out. The parasitic inductances of module FF225R12ME4 under test are extracted by ANSYS Q3D Extractor, as illustrated in Fig. 8. The quantitative relationship between β and junction temperature can be established according to the transfer characteristic curve in the datasheet [33], which is

$$\beta = \alpha_1 {T_{jav}}^2 + \alpha_2 T_{jav} + \alpha_3 \tag{30}$$

where T_{jav} is the average temperature among parallel IGBT chips, and α_1, α_2, and α_3 are the temperature coefficients.

The comparison between the proposed analytical model and the experiment is shown in Fig. 9, which verifies the accuracy of the model under various operation conditions. Furthermore, introducing the influence of temperature difference among chips, the uneven switching loss model of an individual chip can be

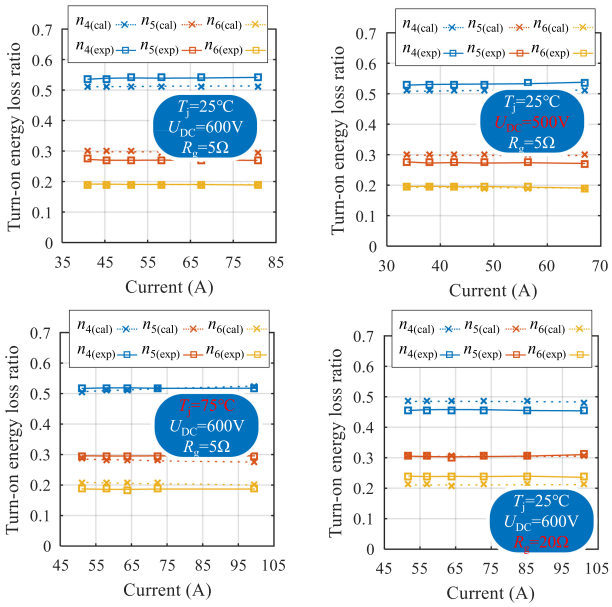


Fig. 9. Comparison results between experimental and proposed analytical models.

expressed as

$$E_{\mathrm{ON\_k}} = \begin{cases} \dfrac{1}{3}[E_{\mathrm{ON\_ref}}(I_C, R_g, U_{DC}, T_{jav}) + k_T \Delta T_{j\_k}], \\ \qquad k = 1, 2, 3 \\ n_k \cdot [E_{\mathrm{ON\_ref}}(I_C, R_g, U_{DC}, T_{jav}) + k_T \Delta T_{j\_k}], \\ \qquad k = 4, 5, 6 \end{cases} \tag{31}$$

$$E_{\mathrm{OFF\_k}} = \frac{1}{3}[E_{\mathrm{OFF\_ref}}(I_C, R_g, U_{DC}, T_{jav}) + k_T \Delta T_{j\_k}], \quad k = 1, \cdots, 6 \tag{32}$$

$$E_{\mathrm{rr\_k}} = \frac{1}{3}[E_{\mathrm{rr\_ref}}(I_C, R_g, U_{DC}, T_{djav}) + k_T \Delta T_{dj\_k}], \quad k = 1, \cdots, 6 \tag{33}$$

where $E_{\mathrm{ON\_ref}}$, $E_{\mathrm{OFF\_ref}}$, and $E_{\mathrm{rr\_ref}}$ are the total turn-ON, turn-OFF, and reverse recovery losses of power modules, ignoring the temperature difference among chips. In this article, the three expressions of switching loss are derived from the PLECS model by the manufacturer, which can also be replaced by the experimental test results. $\triangle T_{j\_i}$ is the difference between the junction temperature of the individual IGBT chip T_{j_i} and the average temperature T_{jav} of parallel IGBT chips. $\triangle T_{dj\_i}$ is the difference between the junction temperature of the individual diode chip T_{dj_i} and the average temperature T_{djav} of parallel diode chips. k_T is the temperature coefficient of $E_{\mathrm{ON\_ref}}$, $E_{\mathrm{OFF\_ref}}$, or $E_{\mathrm{rr\_ref}}$, which is expressed as

$$k_T = \frac{\partial E_{\mathrm{ON\_ref}}}{\partial T_{jav}}, \frac{\partial E_{\mathrm{OFF\_ref}}}{\partial T_{jav}}, or \frac{\partial E_{\mathrm{rr\_ref}}}{\partial T_{djav}}. \tag{34}$$

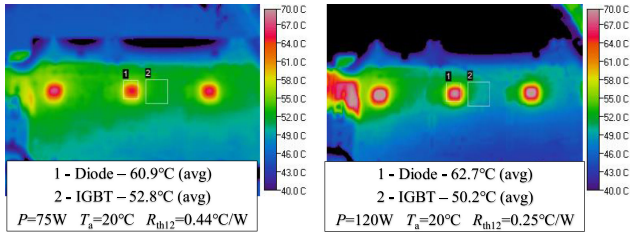


Fig. 10. Thermal images of IGBT module without fan (left) and with fan (right).

III. Modeling Thermal Coupling Among Parallel Chips and Corresponding Calculation

A. Experimental Findings

The thermal cross-coupling of parallel chips is another important effect influencing the calculation of junction temperature inside multichip modules, which has been fully considered in [13], [25], and [34]. However, few references focus on the impact of cooling performance on the thermal coupling effect, and the standard form of the thermal resistance network has not been proposed. In [12], the influence of boundary conditions on the thermal model is introduced by the fitting on a large number of FE simulation results. However, the selection of fitting formula and the correlation of fitting coefficients are unclear due to the lack of a theoretical basis. Only based on a series of FE method simulations and data processing, the modeling process in [12] is inefficient.

Fig. 10 shows the thermal images of black-painted open IGBT module under different cooling conditions by IR camera. The diode chips are actively heated by dc current and the IGBT chips are passively heated by the thermal cross-coupling effect. The expression of a thermal resistance network is

$$R_{thm,n} = \frac{T_{jn} - T_a}{P_m} \tag{35}$$

where m and n are the serial numbers of actively and passively heated chips, respectively, and T_a is the ambient temperature. Especially, $R_{thm,m}$ represents the self-thermal resistance. According to (35), the coupling thermal resistance without fan is much greater than that with the better cooling condition. The experimental phenomenon illustrates that the parameters of the thermal resistance network are closely related to the cooling performance.

B. Qualitative Analysis

Fig. 11 shows the 2-D schematic diagram of heat conduction inside multichip IGBT modules, where the solder layers are ignored. Since the cooling condition greatly affects the heat spreading angle θ [12], a 2-D FE simulation as Fig. 11 is carried out to investigate the distribution of θ. According to the simulation results shown in Fig. 12, θ can be ideally expressed by

$$tan\theta = g(h)l(x) = \frac{-k_{Cu} dT_x/dx}{h(T_x - T_a)} \tag{36}$$

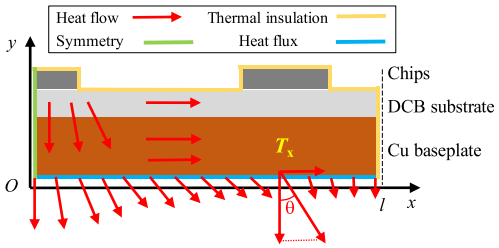


Fig. 11. Schematic diagram of heat conduction inside multichip IGBT modules.

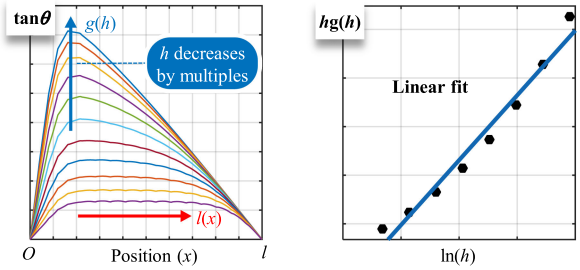


Fig. 12. Two-dimensional FE simulation results according to the boundary conditions shown in Fig. 11 (a) tanθ versus position. (b) $hg(h)$ versus ln(h).

where $g(h)$ and $l(x)$ are the components of tan θ related to h and abscissa x, respectively. Besides, h is convective heat transfer coefficient at lower boundary, k_{Cu} is the thermal conductivity of copper, and T_x is the temperature at lower boundary, which can be expressed by

$$T_x - T_a = e^{-\frac{hg(h)}{k_{Cu}}L(x)} \tag{37}$$

where

$$L(x) = \int l(x)dx. \tag{38}$$

Correspondingly, (35) can be rewritten as

$$R_{thx0} = \frac{T_x - T_a}{P_0} = \frac{T_x - T_a}{2h\int_0^l (T_x - T_a)dx} = \frac{e^{-\frac{hg(h)}{k_{Cu}}L(x)}}{2h\int_0^l e^{-\frac{hg(h)}{k_{Cu}}L(x)}dx}. \tag{39}$$

According to the first mean value theorem for definite integrals, the following formula can be reached:

$$\int_0^l e^{-\frac{hg(h)}{k_{Cu}}L(x)}dx = le^{-\frac{hg(h)}{k_{Cu}}L(\xi)} \tag{40}$$

where ζ is a constant between 0 and l. Therefore, (39) can be simplified as

$$R_{thx0} = \frac{e^{-\frac{hg(h)}{k_{Cu}}L(x)}}{2h\int_0^l e^{-\frac{hg(h)}{k_{Cu}}L(x)}dx} = \frac{e^{-\frac{hg(h)}{k_{Cu}}L(x)}}{2hle^{-\frac{hg(h)}{k_{Cu}}L(\xi)}} = \frac{e^{-\frac{hg(h)}{k_{Cu}}[L(x)-L(\xi)]}}{2lh}. \tag{41}$$

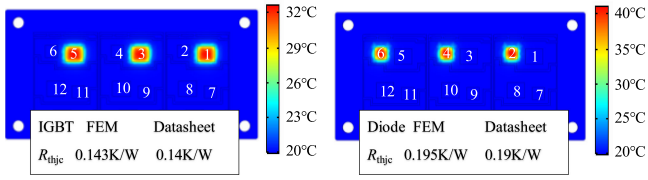


Fig. 13. Comparison results of R_{thjc} between FEM model and datasheet.

As shown in Fig. 12(b), $hg(h)$ can be approximately linearized as follows:

$$hg(h) \approx p_1 ln(h) + p_2 \tag{42}$$

where p_1 and p_2 are the fitting coefficients. Therefore, (39) can be rewritten as

$$R_{thx0} \approx \frac{e^{-\frac{p_1 ln(h)+p_2}{k_{Cu}}[L(x)-L(\xi)]}}{2lh} = a \times h^b \tag{43}$$

where

$$a = \frac{e^{-\frac{p_2}{k_{Cu}}[L(x)-L(\xi)]}}{2l} \tag{44}$$

$$b = \frac{-p_1}{k_{Cu}}[L(x) - L(\xi)] - 1. \tag{45}$$

Since x is at the lower boundary, the coupling thermal resistance of the upper chip can be expressed by

$$R_{thm,n} = R_{thx0} + c = a \times h^b + c \tag{46}$$

where c represents the thermal coupling resistance inside the module, only related to the property of the module.

The formula (46) can be considered as a standard form of thermal resistance network. According to Fig. 12(b), the fitting coefficient p_1 is positive and L(x) is an increasing function. Therefore, the qualitative laws of b and c about the module layout can be concluded as follows.

1) The value of b decreases as the distance between parallel chips increases. Generally, b is greater than -1 when the distance between chips is close, and less than -1 when the distance is far, which depends on the size of x and ζ in (45).
2) The value of c decreases as the distance between parallel chips increases since the thermal coupling effect decreases. Especially, c is close to zero if the two chips are not on the same direct copper bonding (DCB).

C. Quantitative Calculation

To solve the 3-D temperature field of the proposed IGBT module, finite element method (FEM) is applied for the extraction of the thermal resistance network. First, the accuracy of the material parameters and geometric structure of the FEM model need to be verified. The comparison results are shown in Fig. 13. For the FEM model using the material parameters shown in Table I, its simulation results of junction-case thermal resistance are almost consistent with datasheet. Then, based on the verified FEM

TABLE I
MAJOR MATERIAL PROPERTIES OF THE IGBT MODULE

Layers	Materials	ρ (kg/m^3)	k (W/(m·°C))	c_p (J/(kg·°C))
Chip	Si	2330	130	700
Solder	SnAgCu	7404	64	232
DCB copper	Cu	8700	400	385
Ceramic	Al_2O_3	3900	27	776
Baseplate	Cu	8700	400	385

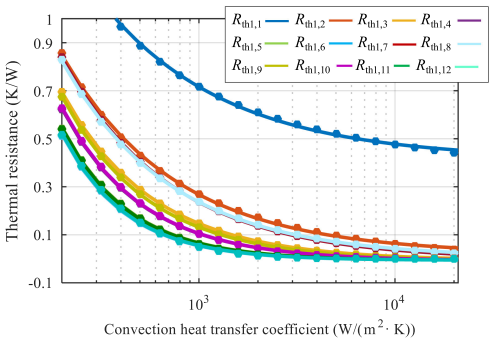


Fig. 14. Fitting results of the thermal resistance network of chip 1 based on (40).

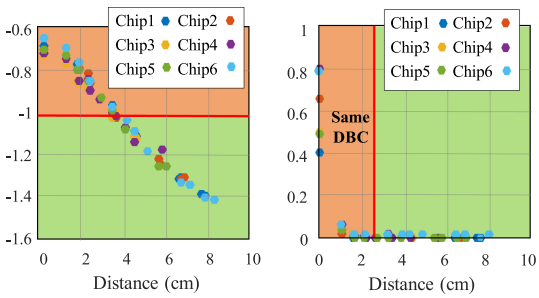


Fig. 15. Fitting parameter distribution: (a) b and (b) c.

model, the parametric sweep of variable h from 20 W/(m^2·K) to 20 000 W/(m^2·K) is carried out. Finally, the thermal resistance network can be obtained according to the standard fitting form as (40). The fitting results are shown in Fig. 14 and Table II. It can be seen that the standard equation has high fitting accuracy, as the goodness of fit (R in Table II) of all the chips are close to 1. Moreover, according to Table II, the relationship between fitting coefficients (b and c) and chip distance is established, as shown in Fig. 15. Based on the result of quantitative calculation in the figure, the conclusions of qualitative analysis can be fully verified. According to (40), fewer FEM simulations can be used to obtain the thermal resistance network related to cooling conditions, thereby speeding up the modeling efficiency.

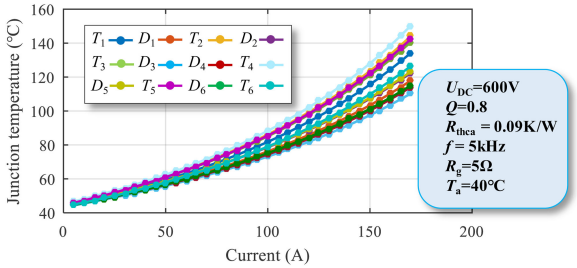


Fig. 16. Junction temperature of each chip at different root-mean-square of the output current.

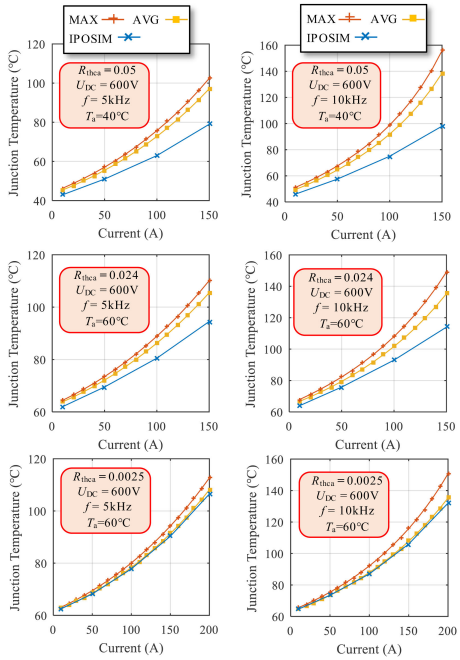


Fig. 17. Comparison results between the proposed calculation method and Infineon IPOSIM at different operation conditions ($R_g = 5\ \Omega$).

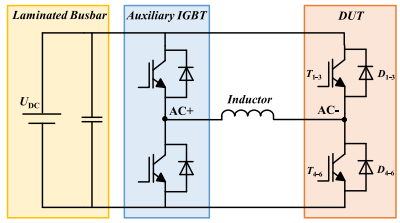


Fig. 18. Topology of the experimental setup.

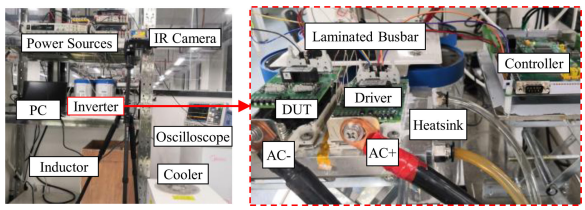


Fig. 19. Inverter experimental setup.

TABLE II
FITTING COEFFICIENT OF THERMAL RESISTANCE NETWORK

Thermal resistance	Coefficient a	b	c	R	Thermal resistance	Coefficient a	b	c	R	Thermal resistance	Coefficient a	b	c	R
$R_{th1,1}$	32.3	-0.68	0.50	0.999	$R_{th2,1}$	43.8	-0.75	0.02	0.999	$R_{th3,1}$	154.6	-1.03	0	0.999
$R_{th1,2}$	43.8	-0.75	0.02	0.999	$R_{th2,2}$	34.2	-0.70	0.67	0.998	$R_{th3,2}$	80.43	-0.89	0	0.999
$R_{th1,3}$	121.1	-0.97	0	0.999	$R_{th2,3}$	57.6	-0.82	0	0.999	$R_{th3,3}$	36.91	-0.73	0.51	0.997
$R_{th1,4}$	234.3	-1.12	0	0.999	$R_{th2,4}$	135.4	-1.00	0	0.999	$R_{th3,4}$	45.03	-0.773	0.05	0.998
$R_{th1,5}$	566.2	-1.31	0	0.999	$R_{th2,5}$	377.9	-1.22	0	0.999	$R_{th3,5}$	127.6	-0.99	0	1
$R_{th1,6}$	847.7	-1.40	0	0.998	$R_{th2,6}$	592.6	-1.32	0	0.999	$R_{th3,6}$	234.4	-1.12	0	0.999
$R_{th1,7}$	54.73	-0.79	0	1	$R_{th2,7}$	74.9	-0.86	0	1	$R_{th3,7}$	188.9	-1.07	0	0.999
$R_{th1,8}$	48.51	-0.77	0	1	$R_{th2,8}$	51.7	-0.79	0	1	$R_{th3,8}$	100.4	-0.94	0	0.999
$R_{th1,9}$	156.3	-1.03	0	0.999	$R_{th2,9}$	102.6	-0.94	0	0.999	$R_{th3,9}$	68.27	-0.86	0.01	1
$R_{th1,10}$	235.0	-1.12	0	0.999	$R_{th2,10}$	152.5	-1.03	0	0.999	$R_{th3,10}$	64	-0.85	0.02	0.999
$R_{th1,11}$	600.8	-1.32	0	0.998	$R_{th2,11}$	427.8	-1.25	0	0.998	$R_{th3,11}$	168.5	-1.0	0	0.999
$R_{th1,12}$	808.3	-1.39	0	0.998	$R_{th2,12}$	581.9	-1.31	0	0.999	$R_{th3,12}$	242.8	-1.13	0	0.999
$R_{th4,1}$	270.2	-1.148	0	0.999	$R_{th5,1}$	659	-1.34	0	0.998	$R_{th6,1}$	911.6	-1.41	0	0.998
$R_{th4,2}$	61.6	-1.0	0.02	0.999	$R_{th5,2}$	451	-1.26	0	0.999	$R_{th6,2}$	644.4	-1.34	0	0.999
$R_{th4,3}$	40.59	-0.75	0.07	0.998	$R_{th5,3}$	126.4	-0.99	0	1	$R_{th6,3}$	210.8	-1.09	0	0.999
$R_{th4,4}$	34.79	-0.72	0.81	0.997	$R_{th5,4}$	65.8	-0.85	0	1	$R_{th6,4}$	125.3	-0.98	0	1
$R_{th4,5}$	63.66	-0.84	0.01	0.999	$R_{th5,5}$	34.9	-0.70	0.50	0.999	$R_{th6,5}$	34.52	-0.69	0.05	0.999
$R_{th4,6}$	128.6	-0.99	0	0.999	$R_{th5,6}$	39.5	-0.73	0.04	0.999	$R_{th6,6}$	28.77	-0.65	0.78	0.999
$R_{th4,7}$	311.5	-1.18	0	0.999	$R_{th5,7}$	687.9	-1.35	0	0.998	$R_{th6,7}$	936.3	-1.416	0	0.998
$R_{th4,8}$	185.8	-1.07	0	1	$R_{th5,8}$	454.8	-1.262	0	0.999	$R_{th6,8}$	637.9	-1.168	0	0.999
$R_{th4,9}$	127.5	-0.99	0	0.999	$R_{th5,9}$	199.6	-1.084	0	1	$R_{th6,9}$	299.4	-0.99	0	0.999
$R_{th4,10}$	64.66	-0.85	0.01	0.999	$R_{th5,10}$	99.55	-0.935	0	1	$R_{th6,10}$	167.1	-1.04	0	0.999
$R_{th4,11}$	103	-0.94	0	0.999	$R_{th5,11}$	55.21	-0.803	0	1	$R_{th6,11}$	73.18	-0.85	0	1
$R_{th4,12}$	146.9	-1.02	0	1	$R_{th5,12}$	54.91	-0.80	0.01	1	$R_{th6,12}$	49.07	-0.76	0	1

Due to the central symmetry of the module layout, the complete thermal resistance network can be expressed as

$$\mathbf{R_{th}} = \begin{bmatrix} R_{th1,1} & \cdots & R_{th1,n} & \cdots & R_{th1,12} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ R_{thm,1} & \cdots & R_{thm,n} & \cdots & R_{thm,12} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ R_{th6,1} & \cdots & R_{th6,n} & \cdots & R_{th6,12} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ R_{th13-m,12} & \cdots & R_{th13-m,13-n} & \cdots & R_{th13-m,1} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ R_{th1,12} & \cdots & R_{th1,13-n} & \cdots & R_{th1,1} \end{bmatrix}. \tag{47}$$

IV. METHOD TO RESPECIFY DEVICE SOA

A. Calculation Method of the Maximum Junction Temperature

In this section, the two-level voltage-source dc–ac converter (2L-VSC) is selected to introduce the TSOA description approach. Above all, two ideal assumptions need to be made: one is that the current is considered constant during one switching cycle; the other is that the junction temperature is also considered constant during one fundamental cycle. Based on the above assumptions, the current I_C at the ith switching cycle can be expressed as

$$I_C(i) = \sqrt{2} \times I \times sin\left(2\pi \times \frac{f_{OUT} \times i}{f_W} - arccos(Q)\right) \tag{48}$$

where f_{OUT} is the fundamental frequency, f_W is the switching frequency, and Q is the power factor. Therefore, the conduction energy loss in one switching cycle can be expressed as

$$E_{CON\_H}(i) = \begin{cases} I_C(i) \times V_{CE}(I_C(i), T_{jav}) \\ \qquad \times T_{ON}(i), I_C(i) > 0 \\ 0, I_C(i) \le 0 \end{cases} \tag{49}$$

$$E_{DCON\_H}(i) = \begin{cases} -I_C(i) \times V_F(-I_C(i), T_{djav}) \\ \quad \times T_{ON}(i), I_C(i) < 0 \\ 0, I_C(i) \ge 0 \end{cases} \tag{50}$$

$$E_{CON\_L}(i) = \begin{cases} -I_C(i) \times V_{CE}(-I_C(i), T_{jav}) \\ \qquad \times (\frac{1}{f_W} - T_{ON}(i)), I_C(i) < 0 \\ 0, I_C(i) \ge 0 \end{cases} \tag{51}$$

$$E_{DCON\_L}(i) = \begin{cases} I_C(i) \times V_F(I_C(i), T_{djav}) \\ \quad \times (\frac{1}{f_W} - T_{ON}(i)), I_C(i) > 0 \\ 0, I_C(i) \le 0 \end{cases} \tag{52}$$

TABLE III
PARAMETERS OF EXPERIMENTAL SETUP

Parameter	Value
Power source	1.2 kV /5A
IR camera	FLIR T650sc
Cooling system	Water, 6L/min
DUT (IGBT)	FF225R12ME4
DC link capacitor	6.8mF 1200V
Load inductor	0.5 mH, 400A
Switching frequency	10 kHz
Output frequency	100 Hz

TABLE IV
COMPARISON RESULTS BETWEEN IR CAMERA, PROPOSED METHOD, AND IPOSIM

Conditions	Value	T_1	T_2	T_3	T_4	T_5	T_6	D_1	D_2	D_3	D_4	D_5	D_6
Test I:	IR	43.9°C	44.2°C	42.8°C	44.8°C	43.5°C	41.7°C	44.3°C	44.2°C	42.8°C	43.5°C	43.5°C	42.7°C
U_{DC}=250V	P	43.4°C	44.5°C	44.1°C	45.5°C	44.2°C	42.3°C	43.2°C	44.0°C	43.0°C	43.3°C	44.0°C	43.0°C
I_{peak}=100A	I	41.5°C	41.5°C	41.5°C	41.5°C	41.5°C	41.5°C	40.4°C	40.4°C	40.4°C	40.4°C	40.4°C	40.4°C
R_g=5Ω	E_1	-1.1%	0.7%	3.0%	1.5%	1.6%	1.4%	-2.5%	-0.5%	0.5%	-0.5%	1.1%	0.7%
T_a=33°C	E_2	-5.5%	-6.1%	-1.6%	-7.4%	-4.6%	-0.5%	-8.8%	-8.6%	-5.6%	-7.1%	-7.1%	-5.4%
R_{thca}=0.0165K/W													
Test II:	IR	59.1°C	60.1°C	58.5°C	61.3°C	58.8°C	54.5°C	58.8°C	58.3°C	55.0°C	58.3°C	58.0°C	55.5°C
U_{DC} =250V	P	57.1°C	59.5°C	58.7°C	61.2°C	59.1°C	55.1°C	56.7°C	58.5°C	56.3°C	56.8°C	58.5°C	55.1°C
I_{peak}=200A	I	53.0°C	53.0°C	53.0°C	53.0°C	53.0°C	53.0°C	49.5°C	49.5°C	49.5°C	49.5°C	49.5°C	49.5°C
R_g=5Ω	E_1	-3.4%	-1.0%	0.3%	-0.2%	0.3%	1.1%	-3.6%	0.3%	2.3%	-2.6%	0.9%	-0.7%
T_a=33°C	E_2	-10.3%	-11.8%	-9.4%	-13.5%	-9.9%	-2.8%	-15.8%	-15.1%	-10.0%	-15.1%	-14.7%	-10.8%
R_{thca}=0.0165K/W													

*IR: IR camera, P: proposed method , I: IPOSIM, E_1=(P−IR)/IR×100%, E_2=(I−IR)/IR×100%.

where V_{CE} and V_F are the output characteristic of parallel IGBT and diode chips, respectively, which can be obtained from datasheet. $T_{ON}(i)$ is the conduction time of the high-side IGBT chips in the ith switching cycle, which can be expressed as

$$T_{ON}(i) = \frac{0.5 \times (1+K \times \sin(2 \times \pi \times i \times f_{OUT}/f_W))}{f_W} \tag{53}$$

where K is the modulation index, which is set to 0.8 in this article. Substituting (31)–(33), the average power loss of an individual chip in one fundamental cycle can be expressed as

$$P_{IGBT\_k} = \begin{cases} f_{OUT} \sum_{i=1}^{f_W/f_{OUT}} \left(\frac{E_{CON\_H}(i)}{3} + E_{ON\_k}(i) + E_{OFF\_k}(i) \right), k = 1,2,3 \\ f_{OUT} \sum_{i=1}^{f_W/f_{OUT}} \left(\frac{E_{CON\_L}(i)}{3} + E_{ON\_k}(i) + E_{off\_k}(i) \right), k = 4,5,6. \end{cases} \tag{54}$$

$$P_{Diode\_k} = \begin{cases} f_{OUT} \sum_{i=1}^{f_W/f_{OUT}} \left(\frac{E_{DCON\_H}(i)}{3} + E_{rr\_k}(i) \right), k = 1,2,3 \\ f_{OUT} \sum_{i=1}^{f_W/f_{OUT}} \left(\frac{E_{DCON\_L}(i)}{3} + E_{rr\_k}(i) \right), k = 4,5,6. \end{cases} \tag{55}$$

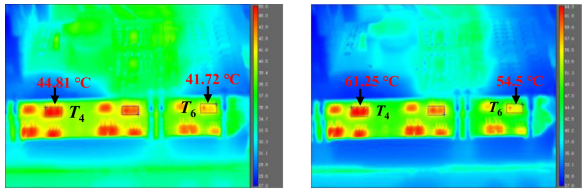
Furthermore, substituting (47), the junction temperature of each chip can be expressed as

$$\mathbf{T} = \mathbf{P} \times \mathbf{R_{th}} + T_a \mathbf{I} \tag{56}$$

where $\mathbf{P} = [P_{IGBT\_1}, P_{Diode\_1}, P_{IGBT\_2}, P_{Diode\_2}, \ldots, P_{IGBT\_6}, P_{Diode\_6}]$, and $\mathbf{T} = [T_{j\_1}, T_{dj\_1}, T_{j\_2}, T_{dj\_2}, \ldots, T_{j\_6}, T_{dj\_6}]$. Moreover, h can be obtained according to the information of the cooling system, which is

$$h = \frac{1}{R_{thca} \times A} \tag{57}$$

where R_{thca} is the thermal resistance of the cooling system. A is the heat exchange area of the IGBT module, that is, the area of the bottom surface of the substrate. For the considered modules in this article, A is 7561 mm^2. Since power loss is closely related to junction temperature, the iterative calculation is carried out until the relative error ε is lower than the setting reference,



(a) (b)

Fig. 20. Temperature distribution by IR camera at (a) Test I and (b) Test II.

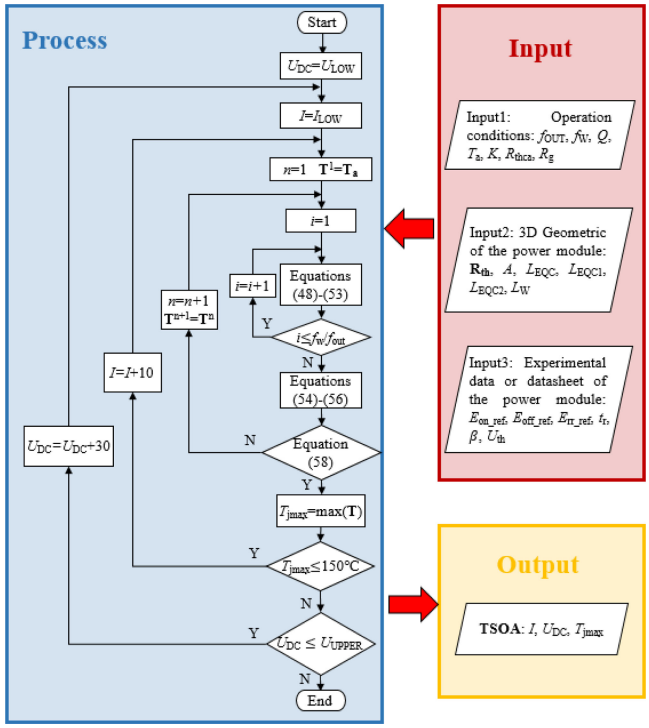


Fig. 21. Description process of TSOA.

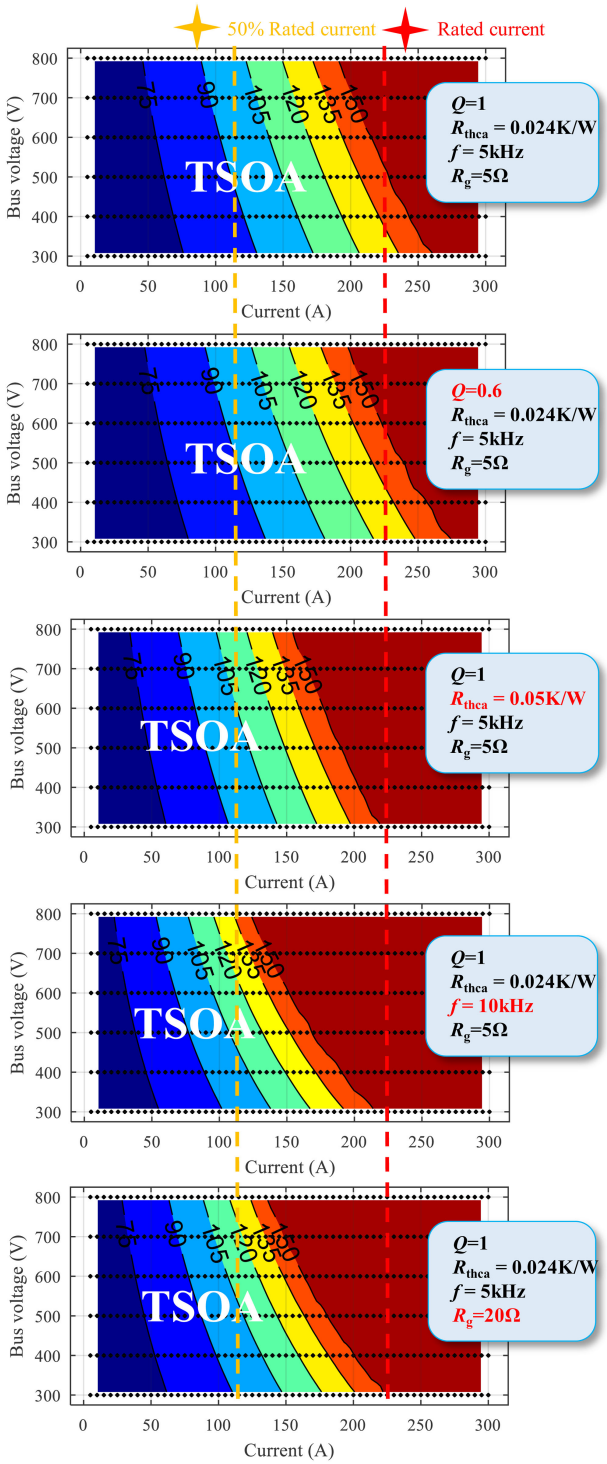


Fig. 22. TSOA of module FF225R12ME4 under different operation conditions (T_a = 60 °C).

which is

$$\varepsilon = \frac{\left\|\mathbf{T}^{n+1} - \mathbf{T}^{n}\right\|}{\left\|\mathbf{T}^{n}\right\|} < 0.001 \tag{58}$$

where n is the number of iterations.

Due to the employment of uneven power loss and thermal resistance model, the junction temperature of each chip can be calculated, thus the chip with the highest temperature can be discovered and used to evaluate the thermal safety of the IGBT module, as shown in Fig. 16. It can be seen that the junction temperatures among parallel chips are different, and the chip T_4 usually has the highest junction temperature due to the highest ratio of turn-ON loss. To evaluate the effectiveness of the model, a series of simulations at different operation conditions have been carried out by Infineon IPOSIM. The comparison results are shown in Fig. 17. Since the measurement conditions of thermal resistance in the datasheet and IPOSIM are using a water-cooling bar [35], the thermal cross-coupling effect is poor (shown in Fig. 14). Therefore, the calculation results between the average junction temperature and IPOSIM are almost the same when the cooling performance is good. However, as the cooling performance decreases, the calculated junction temperature is gradually higher than IPOSIM due to the greater thermal cross-coupling effect. In this case, the conventional 1-D RC lumped thermal model by IPOSIM could lead to the underestimation of the maximum junction temperature in the IGBT module, increasing the risk of thermal failure of the device. Additionally, the difference between the maximum junction temperature and the average junction temperature increases as the switching frequency increases at the same current, due to the uneven dynamic current effect. The comparison results show that the proposed calculation method is more effective than the traditional one in calculating the maximum junction temperature.

To verify the accuracy of the proposed method, an experimental setup was established, as shown in Figs. 18 and 19. The setup consists of an H-bridge inverter, a water cooling system, and an infrared thermal camera, and the setup parameters are presented in Table III. Moreover, an opened and black-painted IGBT module was used for the test of temperature distribution under the high-frequency inverter condition for each chip. In the experiment, two different operation conditions were tested as shown in Fig. 20, and the comparison results are shown in Table IV. From the test results, it can be seen that the temperature distribution among parallel IGBT chips is quite uneven due to the imbalanced switching loss and the uneven thermal resistance distribution, and chip T4 has the highest junction temperature. Compared with IPOSIM, the proposed calculation method can describe the uneven temperature distribution among chips to a certain extent, as shown in Table IV. The errors come from the simplified processing of the method itself, such as the averaging processing of power loss in parallel diode chips. However, the maximum temperature inside the IGBT module can be accurately calculated by the method, thereby providing strong support for the safe design of inverters.

B. Description Process of TSOA

The detailed description process of TSOA is shown in Fig. 21, where U_{LOW} and U_{UPPER} are the lower and upper limits of U_{DC} respectively, and I_{LOW} is the low limit of I. The complete process considers both operation conditions and the information of power modules. Owing to the proposed analytical model of uneven power loss and thermal distribution in (29) and (47), the description process can be performed within a few seconds,

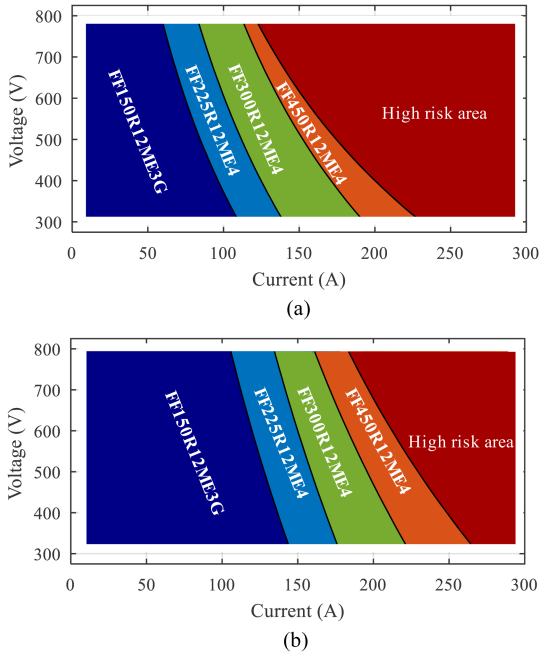


Fig. 23. Recommended area of different types of IGBT modules under inverter applications. (a) $R_{thca} = 0.024$ K/W, $T_a = 60$ °C, and $f = 10\,000$ Hz. (b) $R_{thca} = 0.06$ K/W, $T_a = 40$ °C, and $f = 5000$ Hz.

including the several hundred junction temperature calculations under different current and voltage. Therefore, the approach is a more efficient tool in the initial design phase of the power electronic system, compared with the traditional circuit simulation software. Fig. 22 shows the TSOA of module FF225R12ME4 under different operation conditions. It can be seen that the area of TSOA is sensitive to R_{thca}, f and R_g, while less sensitive to Q. Moreover, the 50% current margin (based on experience) still cannot meet the thermal safety requirements of the power module under certain operation conditions. Therefore, can be regarded as a supplement to the datasheet, which enables more well-founded margins design to achieve the safe application of power modules in the inverter application.

With the proposed approach, the TSOA of standard 1200-V half-bridge IGBT modules from 150 to 450 A with EconoDUAL housing can be fully described. According to [21], 100 °C can be considered as the optimized junction temperature since the device achieves good tradeoff between cost and thermal safety. Correspondingly, Fig. 23 shows the recommended area of different types of IGBT modules under inverter application (R_{g} is the recommended value on the respective datasheet), which represents the lowest design cost when the maximum junction temperature is lower than 100 °C. It illustrates that the proposed approach can guide the cost-efficient device selection for the power electronics system.

V. Conclusion

This article proposes a description approach for the TSOA of multichip power modules. The superiority of this approach is to consider the uneven distribution of junction temperature among parallel chips while ensuring the efficiency of the calculation. The two key influencing factors, i.e., uneven dynamic current and thermal cross-coupling effects, have been fully investigated and modeled. The proposed uneven power loss and thermal resistance model are verified by experiments and FEM simulation, and further applied in the TSOA evaluation process. Compared with the traditional circuit simulation software, the proposed approach has higher calculation efficiency and accuracy, especially suitable for initial device selection and system design. Moreover, although for IGBT module and 2L-VSC in this article, the method is also applicable to other multichip parallel high-power devices and circuit topologies.

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Jianpeng Wang (Student Member, IEEE) was born in Heilongjiang, China, in 1995. He received the B.S. degree in electrical engineering in 2017 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include packaging and reliability of power semiconductor modules.

Wenjie Chen (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1996, 2002, and 2006, respectively.

Since 2002, she has been a member of the Faculty of School of Electrical Engineering, Xi'an Jiaotong University, where she is currently a Professor. From January 2012 to January 2013, she was a Visiting Scholar with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN, USA. She then joined Xi'an Jiaotong University, where she was engaged in the teaching and research works in power electronics. Her main research interests include electromagnetic interference, active filters, and power electronic integration.

Jin Zhang (Student Member, IEEE) was born in Hebei, China, in 1998. He received the B.S. degree in electrical engineering in 2020 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include packaging and reliability of power semiconductor modules.

Meng Xu (Student Member, IEEE) was born in Sichuan, China, in 1997. He received the B.S. degree from Chongqing University, Chongqing, China, in 2017, and the M.S. degree from Xi'an Jiaotong University, Xi'an, China, in 2021, both in electrical engineering.

His research interests include online monitoring technology of power semiconductor modules.

Laili Wang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with Electrical Engineering Department, Queen's University, Kingston, ON, Canada. From 2014 to 2017, he was an Electrical Engineer with Sumida, Canada. In 2017, he joined Xi'an Jiaotong University as a Full Professor. His research interests include package and integration, wireless power transfer, and energy harvesting.

Dr. Wang is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is the Vice-Chair for TC2 (Technical committee of Power Conversion Systems and Components) in PELS, the Co-Chair for System Integration and Application in the International Technology Roadmap for Wide Band-Gap Power Semiconductor, and the Chair for IEEE CPSS&PELS joint Chapter in Xi'an, China.

Jinjun Liu (Fellow, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University (XJTU), Xi'an, China, in 1992 and 1997, respectively.

He then joined XJTU Electrical Engineering School as a faculty. From late 1999 to early 2002, he was a Visiting Scholar with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. In late 2002, he was promoted to a Full Professor and then the Head of the Power Electronics and Renewable Energy Center, XJTU, which now comprises more than 20 faculty members and more than 200 graduate students and carries one of the leading power electronics programs in China. From 2005 to early 2010, he was an Associate Dean of Electrical Engineering School, XJTU, and from 2009 to early 2015, the Dean for Undergraduate Education, XJTU. He is currently an XJTU Distinguished Professor of power electronics. He coauthored 3 books (including one textbook), authored or coauthored more than 500 technical papers in peer-reviewed journals and conference proceedings, holds more than 50 invention patents (China/US/Europe), and delivered for many times plenary keynote speeches and tutorials at IEEE conferences or China national conferences in power electronics area. His research interests include modeling, control, and design methods for power converters and electronified power systems, power quality control and utility applications of power electronics, and microgrids for sustainable energy and distributed generation.

Dr. Liu served the IEEE Power Electronics Society Region 10 Liaison and then China Liaison for 10 years, an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS for 13 years, and 2015–2019 Executive Vice-President and 2020–2021 Vice President for membership of IEEE PELS. He is on the Board of China Electrotechnical Society 2012–2020 and was elected the Vice-President in 2013 and the Secretary General in 2018 of the CES Power Electronics Society. Since 2013, he has been the Vice-President for International Affairs, China Power Supply Society (CPSS), and since 2016, the inaugural Editor-in-Chief for CPSS Transactions on Power Electronics and Applications. Since 2013, he has been the Vice-Chair of the Chinese National Steering Committee for College Electric Power Engineering Programs. He was the recipient of eight governmental awards at national level or provincial/ministerial level for scientific research/teaching achievements. He was also the recipient of the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, the 2016 State Council Special Subsidy Award, the IEEE Transactions on Power Electronics 2016 Prize Paper Award, and the Nomination Award for the Grand Prize of 2020 Bao Steel Outstanding Teacher Award.

Yongmei Gan (Member, IEEE) was born in 1971. She received the B.S. and M.S. degrees in control engineering from the Xi'an University of Technology, Xi'an, China, in 1993 and 1996, respectively, and the Ph.D. degree in control theory and control engineering from Northwestern Polytechnical University, Xi'an, China, in 1999.

Since 2000, she has been with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, where she is currently an Associate Professor. From February 2008 to February 2009, she was a Visiting Scholar of Electrical and Computer Engineering Department, University of Toronto, Toronto, ON, USA. Her research interests include package and integration and energy harvesting and supervisory control of discrete-event systems.