A Highly Integrated PCB Embedded GaN Full-Bridge Module With Ultralow Parasitic Inductance

Zhiyuan Qi, *Student Member, IEEE*, Yunqing Pei, *Member, IEEE*, Laili Wang, *Senior Member, IEEE*, Qingshou Yang, *Student Member, IEEE*, and Kangping Wang, *Member, IEEE*

***Abstract*—To fully take the high-frequency advantage of gallium nitride (GaN) devices, this article presents a face-up integrated power module based on the printed circuit board embedding technology to tackle the challenges caused by the conventional discrete solutions. The proposed GaN module highly integrates a GaN-bare-dies-based full bridge, driving circuits, and decoupling capacitors, in which the advanced bismaleimide-triazine material is used as the packaging material and the copper-filled laser microvias are used for low-parasitic-inductance and high-thermal-conductivity interconnection. Careful electro-thermal codesign and optimization of power loop is conducted to make the tradeoff between power loop inductance and thermal performance. The proposed full bridge power module achieves the lowest power loop inductance of about 0.305 nH in power modules with the same power level. The maximum thermal resistances from the embedded GaN bare dies to top and bottom surface are 3.39 and 0.42 °C/W, respectively. Benefitting from the ultralow power loop parasitic inductances, the switching speed of GaN devices reaches to 57.5 V/ns, while the voltage overshoot is not higher than 5.35% of the dc bus voltage. The superior performance of the proposed integrated GaN module makes it a promising application prospect in high frequency high power density converters.**

***Index Terms*—Finite-element analysis (FEA) simulation, gallium nitride high electron mobility transistors (GaN HEMTs), high frequency, parasitic inductance, PCB embedding technology, thermal resistance.**

I. Introduction

EFFICIENCY and power density are two key drivers and metrics for the advancement of power conversion technologies. As the silicon (Si) device is approaching its theoretical limit [1]–[3], it cannot meet the future demands for higher efficiency and power density. The emergence of gallium nitride high electron mobility transistors (GaN HEMTs), as the representative of wide bandgap (WBG) devices, gives the potential to break the bottleneck. Compared with Si and silicon carbide (SiC) materials, GaN material has higher electron mobility, higher saturated electron velocity, and higher electric breakdown field [4]–[6], as shown in Fig. 1. These material superiorities can bring many benefits to GaN HEMTs, i.e., much higher switching speed and smaller ON-state resistance, which mean much higher switching frequency without increasing power loss [7]. By using GaN HEMTs, the switching frequency can be pushed up to multi megahertz easily. Thus, passive components with smaller size can be used, which can help to increase power density [8].

However, the ultrahigh switching speed of GaN HEMTs makes it susceptible to parasitic inductances. The superior high frequency advantages of GaN devices cannot be fully utilized by simple and direct drop-in replacement of Si devices [9]. It is because the widely used bonding wires in conventional Si discrete devices or power modules usually have large parasitic inductance above 10 nH [9]–[12], as shown in Fig. 2.

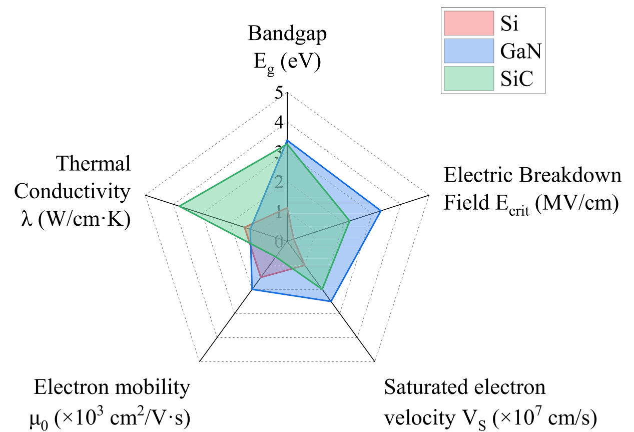

Fig. 1. Comparison of material properties among Si, GaN, and SiC materials.

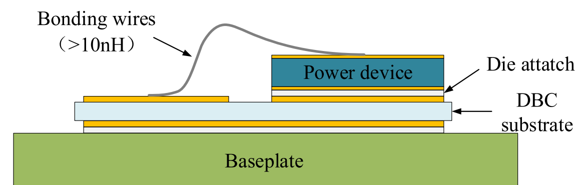

Fig. 2. Structure of the conventional power module based on DBC and bonding wires.

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The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: mambaqizhy@stu.xjtu.edu.cn; peiyq@mail.xjtu.edu.cn; llwang@mail.xjtu.edu.cn; qs_yang@stu.xjtu.edu.cn; wangkp@mail.xjtu.edu.cn).

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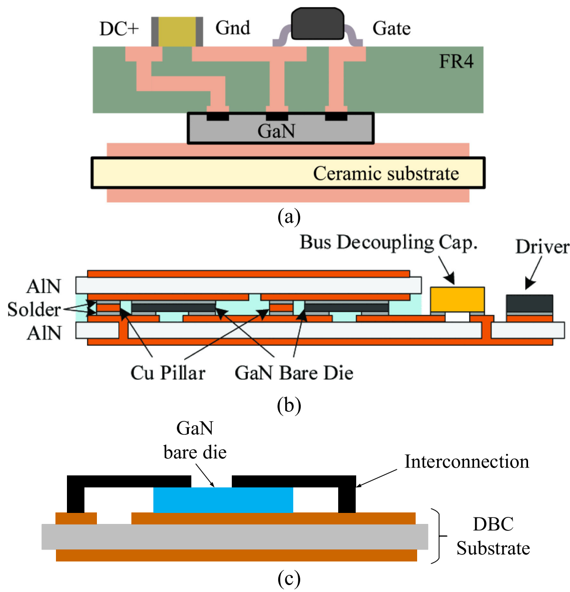


Fig. 3. (a) DBC/PCB hybrid GaN module [15]. (b) Double-sided DBC GaN module [16]. (c) GaN module with shaped interconnection [19].

For the high-speed GaN devices, it is very critical to modify the conventional packages or remove bonding wires from the package. Otherwise, serious voltage overshoot, parasitic ringing, electromagnetic interference (EMI) and reliability issues can be caused. With the efforts of device manufacturers, an advanced wire-bonded package (QFN package with parasitic inductance smaller than 1 nH) has been developed for GaN discrete devices [13]. Several advanced packages without bonding wires have also been developed, including GaNPX, PQFN, and LGA, etc. Based on the discrete GaN devices using these advanced packages, some power modules were proposed [14], [15]. In [15], a hybrid GaN power module based on printed circuit board (PCB) and direct bonded copper (DBC) was proposed, as shown in Fig. 3(a), in which the discrete GaN HEMTs GS66508T with GaNPX package were employed. The realized power loop inductance of 2.65 nH is still large for GaN devices.

It is preferred to directly integrate GaN bare dies into power module, and various wire-bondless power modules were proposed [9], [16]–[21]. In [16], the GaN bare dies were sandwiched between two DBC ceramic substrates to realize a double-sided cooling 650 V/30 A GaN module integrating the decoupling capacitors and gate drivers, as shown in Fig. 3(b), the power loop inductance was reduced to 0.95 nH. Seong *et al.* [19] proposed an interconnection having shaped contacts fit with the top metal of GaN bare dies, as shown in Fig. 3(c), but the decoupling capacitors were not integrated and the power loop inductance was not reported. As mentioned above, both the two modules in Fig. 3(b) and (c) use GaN bare dies, which are lateral device with all the electrodes on the same side, as shown in Fig. 4. The distances between drain and source electrodes, and between drain and gate electrodes are only 300 and 323 μm, respectively. Any slight misalignment with DBC and solder overflow during mounting and soldering process will inevitably further reduce the originally small distances. Thus, insulation issue will be incurred if no insulation measures are taken, which is not reliable for the used 650 V GaN bare dies. Filling with

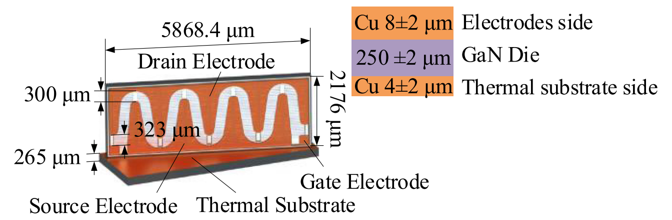


Fig. 4. Structure of the GaN bare die GS66508.

silicone gel is indispensable for the above two power modules to ensure enough insulation capabilities, while this will increase the manufacturing complexity.

There is an ideal packaging and integration solution for lateral GaN HEMTs [22], i.e., PCB embedding solution, which is inherently easy to realize good insulation [17]. Since the first PCB embedded power module emerged in Europe, it has attracted strong research interest of many researchers [23], because many benefits can be achieved by using PCB embedding technology. As embedding GaN bare dies into PCB, the space for GaN HEMTs on the surface of PCB are freed for the driving circuit and decoupling capacitors, and the interconnection can be realized by the copper-filled laser microvias [17]. Therefore, significant reduction of parasitic inductances can be realized due to the ultrasmall power loop area and the elimination of bonding wires. What is more, befitting from the quasi 3-D structure, the PCB embedded power modules have small form factor and light weight [9], [12], [23]–[33].

Up to now, there have been some PCB embedded power modules for SiC MOSFETs and insulated gate bipolar transistors (IGBTs) reported [9], [10], [24], [26], [28], [32]–[34], but the PCB embedded GaN modules (PEGMs) are still rare [17], [22], [35]. In [17], a three-phase inverter based on PCB embedded GaN HEMTs was realized, in which the power loop inductance is only 0.43 nH. But the thermal performance was not discussed, and the turn-OFF dv/dt is only 6 kV/μs, which cannot show the high frequency advantages of GaN HEMTs. Moench *et al.* [35] integrate gate and dc-link capacitors on the surface of a PCB-embedded GaN-on-Si half-bridge package. But the module is a two-layer design, and the power loop is in the horizontal plane, so the realized power loop parasitic inductance is 2.22 nH, still too large. In this article, the PCB embedding technology will be also employed for the packaging and integration of GaN HEMTs, and thus an ultrathin PEGM with surface mount package (SMP) structure is proposed. Benefitting from the high integration of a full bridge based on GaN bare dies, the main driving circuits based on isolated drivers, and decoupling capacitors, the external circuits can be greatly simplified. To achieve both small parasitic inductances and good thermal performance, careful electro-thermal codesign will be carried out.

The rest of this article is organized as follows. In Section II, the concept of the proposed PEGM is first introduced, and some design considerations are discussed. Then, two different PCB embedded structures based on face-up and face-down process flows respectively are compared to determine a better PCB embedding scheme. Then, the process flow of fabricating the proposed PEGM is given out. In Section III, based on finite-element analysis (FEA) simulation, the proposed PEGM is carefully

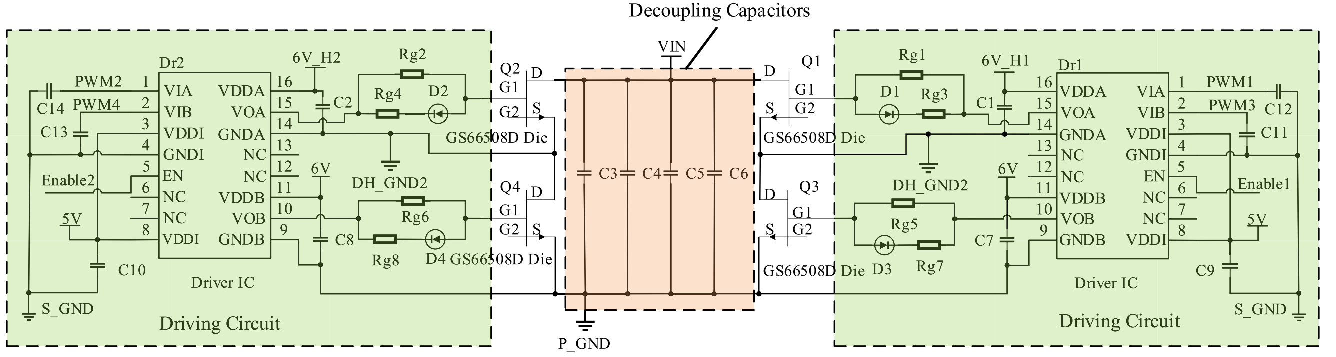


Fig. 5. Schematic of the circuit integrated in the proposed PCB embedded module.

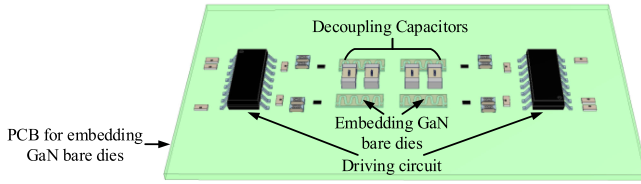


Fig. 6. Simplified 3-D view of the proposed PCB embedded module.

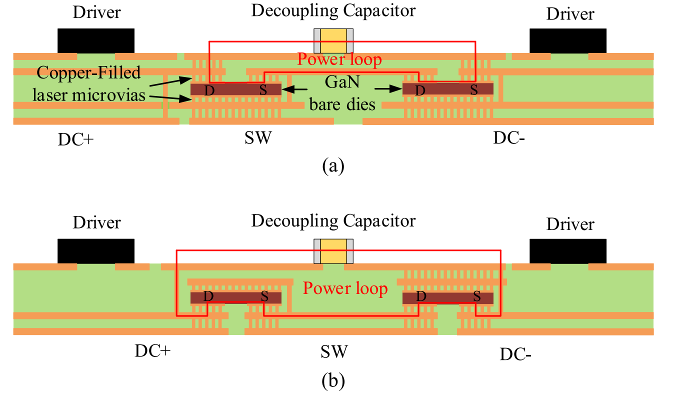


Fig. 7. Simplified structure schematic of (a) face-up PEGM and (b) face-down PEGM.

designed and optimized to make a tradeoff between thermal performance and power loop inductances (PLIs). Then, the optimized PLIs and thermal resistance are carefully extracted. In Section IV, the electrical performance, involving common source inductances (CSIs), driving loop parasitic inductances (DLIs), parasitic capacitances brought by PCB embedded package, and the insulation strength, are carefully designed and evaluated. In Section V, the double pulse test (DPT) experiment is carried out to demonstrate the low parasitic inductances of the proposed PCB embedded GaN full-bridge module. Finally, Section VI concludes this article.

II. Proposed PCB Embedded GaN Full-Bridge Module

A. *Concept of the Proposed Ultrathin PEGM*

As mentioned above, the circuits shown in Fig. 5 are highly integrated in the proposed PEGM, including a full bridge formed by four GaN bare dies, the main driving circuits, and decoupling capacitors, as shown in Fig. 6. In order to be compatible with PCB embedding technology, the GaN bare dies GS66508 (650 V, 30 A) from GaN Systems, Inc., are employed, both sides of which are copper, as shown in Fig. 4. The isolated half-bridge driver Si8273GBD-IS1 from Silicon Labs are used to drive the four GaN HEMTs, and four ceramic capacitors CGA5L1X7T2J473M160AE with the package of 1206 (630 V, 0.047 μF) are used as decoupling capacitors. To realize the high integration of the circuits in Fig. 5, a four-layer PCB design is required, in which the four GaN bare dies forming the full bridge are embedded in the middle core layer to realize a symmetrical structure, as shown in Fig. 7. The advanced bismaleimide-triazine (BT) material HL832NS from MITSUBISHI GAS CHEMICAL with better properties than conventional FR4 material is employed as the PCB material in this article, e.g., higher thermal conductivity, lower CTE (much

TABLE I
Properties Comparison Between BT Material HL832NS and FR4

Properties	BT (HL832NS)	FR4
Thermal conductivity (W/m·K)	0.6	0.288
CTE (ppm/°C)	7	13 ~ 17
T_g (°C)	255	170
Insulation resistance (Ω)	$10^{15\text{-}16}$	5×10^{8}

closer to the 3.5 ppm/°C of GaN material and the 2.6 ppm/°C of Si material as the substrate of GaN devices), higher T_g, etc., as listed in Table I. In addition to being used to integrate driving circuit and decoupling capacitors, the top surface of the proposed PEGM, with large-area exposed copper, is also intended for attaching to heat sink. The bottom surface is mainly used to lead out the power and signal pads to realize an SMP structure, which can be directly soldered on the motherboard. Through deliberate design of the proposed PEGM, the bottom-sided cooling can also be enabled, and thus, double-sided cooling can be realized.

The key to realize the proposed PEGM is the interconnection from the embedded GaN bare dies to outer layers to connect to driving circuit, decoupling capacitors, and the terminal pads. Since both the electrodes side and thermal substrate side of the employed GaN bare dies GS66508 have enough copper thickness for laser drilling process, which are 8 and 4 μm, respectively, as shown in Fig. 4, so the laser microvias filled

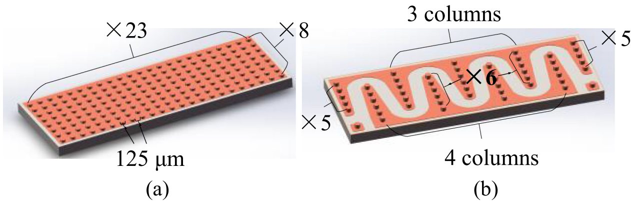


Fig. 8. Schematic of the formed copper pillars by laser microvais and electroplating copper on (a) thermal substrate side and (b) electrodes side of the GaN bare dies.

with electroplating copper are used to lead out the electrodes and thermal substrate of the embedded GaN bare dies to the inner copper layers [32], [36]. Combining with the redistribution layers (RDLs), the interconnection from the embedded GaN bare dies to driving circuit, decoupling capacitors and terminal pads can be realized. To minimize the parasitic inductances and thermal resistances, as many copper-filled laser microvias as possible need to be formed on both sides of the embedded GaN bare dies. According to the manufacturing level of the PCB manufacturers, the diameter of the laser microvias and the distance between two adjacent microvias are both 125 μm in this article. As shown in Fig. 8, there are 23 $\times$ 8 microvias formed on the thermal substrate side of each embedded GS66508 GaN bare die, and as many microvias as possible are also formed on the electrodes side. Note that, there is a unique phenomenon for lateral GaN devices, i.e., current collapse, the resultant dynamic resistance will increase conduction loss. To mitigate the current collapse phenomenon, it is recommended by manufacturers to connect thermal substrate to source pad [4], which is considered in this article.

B. Determination of the Proposed PEGM Based on Face-Up Process Flow

As shown in Fig. 7, the embedded GaN bare dies can be either face up or face down. Figs. 9 and 10 show the detailed structures of the two PEGMs based on face-up and face-down process flows, respectively. Although they have similar appearances, some differences still exist in the detailed packaging structures, resulting in some differences in the electrical and thermal performances. To determine a better PCB embedded structure, the two PEGMs are compared on the parasitic inductances and heat dissipation performance, in which the distances between the embedded GaN bare dies are kept the same, and the layouts are also kept consistent.

In order to accurately achieve the parasitic inductances of the two PEGMs, the simulation models are obtained by firstly exporting the two actual PCB layouts from Altium Designer to ODB++ files, and then using Ansys SIwave to convert the ODB++ files to the files readable by Ansys Q3D Extractor. By using Q3D Extractor, the power-loop parasitic inductances of both two bridge legs in the two structures are extracted at the simulation frequency of 100 MHz, as listed in Table II. It can be seen that the face-up PEGM has smaller PLIs than face-down PEGM, which is due to the smaller power loop area formed by top layer and the first inner layer below top layer than that of face-down PEGM formed by top layer and the second inner layer below top layer, as shown in Fig. 7(a) and (b).

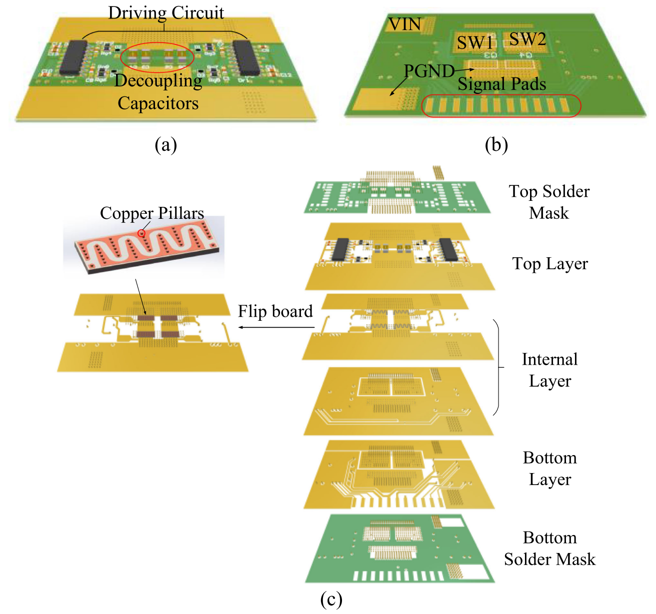


Fig. 9. Detailed structure schematic of the proposed face-up PEGM (a) top view, (b) bottom view, and (c) exploded view.

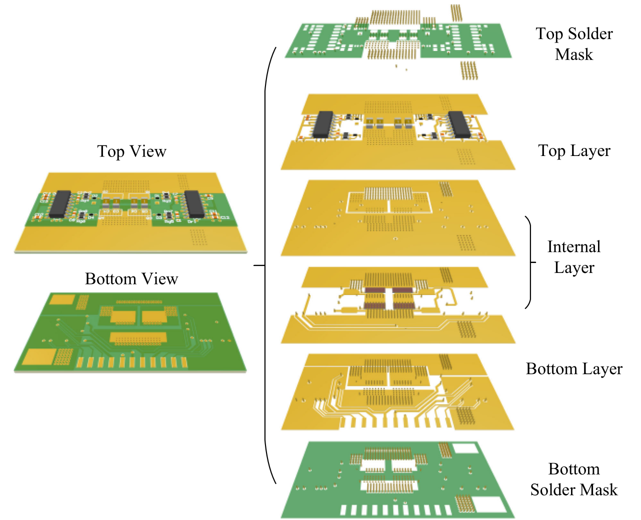


Fig. 10. Detailed structure schematic of the face-down PEGM.

TABLE II
COMPARISON OF POWER-LOOP PARASITIC INDUCTANCES BETWEEN FACE-UP AND FACE-DOWN MODULES

Parasitic inductance (nH)	Bridge Leg1 (Q_1 and Q_3)	Bridge Leg2 (Q_2 and Q_4)
Face-up module	0.305	0.305
Face-down module	0.462	0.462

Then, the thermal performances of the proposed two structures are simulated in Ansys Icepak, in which the power losses of the four GaN bare dies are set to 10 W, the ambient temperature is set to 40 °C, and the heat transfer coefficients of top side and bottom side are set to 1000 and 20 W/(K·m^2), respectively, representing water cooling and natural cooling. The temperature distributions of the two PEGMs are shown in Fig. 11(a) and (b), and the maximum temperatures of the four embedded GaN bare

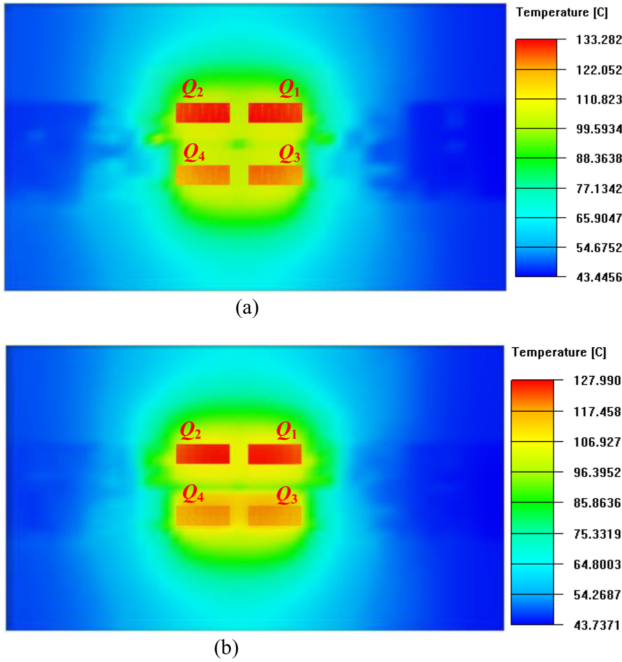


Fig. 11. Thermal distribution comparison between (a) face-up PEGM and (b) face-down PEGM.

TABLE III
COMPARISON OF MAXIMUM TEMPERATURES BETWEEN FACE-UP AND FACE-DOWN MODULES

Temperature (°C)	Q_1	Q_2	Q_3	Q_4
Face-up module	133.282	133.251	127.162	126.316
Face-down module	127.95	127.99	119.948	119.857

dies are listed in Table III. As we can see, the face-up PEGM has higher maximum temperature than face-down PEGM. However, as shown in Fig. 12, with the increase of the heat transfer coefficient of the bottom side, the maximum temperature of face-up PEGM decreases more than that of face-down PEGM. When the heat transfer coefficient of the bottom side is larger than 350 W/(K·m^2), the face-up PEGM has better heat dissipation performance than face-down PEGM. The reason is that the face-down PEGM has better top-sided heat dissipation capability while the face-up PEGM has better bottom-side heat dissipation capability. Due to the SMP structure of the proposed PEGM, the bottom-sided cooling can also be enabled by mounting the proposed PEGMs onto the motherboard having large amounts of thermal vias on the connection pads. By applying forced air cooling or water cooling on the bottom side of motherboard, the face-up PEGM can achieve better comprehensive performance than face-down PEGM, involving both parasitic inductances and the heat dissipation capability. Therefore, the proposed face-up PEGM is employed in this article. In Sections III and IV, electro-thermal codesign will be performed for the proposed PEGM to achieve the optimal performances.

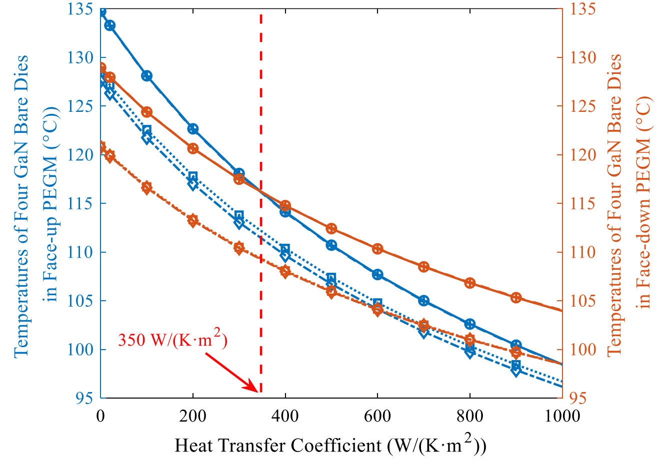


Fig. 12. Comparison of maximum temperatures between face-up PEGM and face-down PEGM versus heat transfer coefficient of bottom surface (solid line marked "o": Q_1, dashed line marked "+": Q_2, dotted line marked "□": Q_3, dash-dot line marked "◊": Q_4).

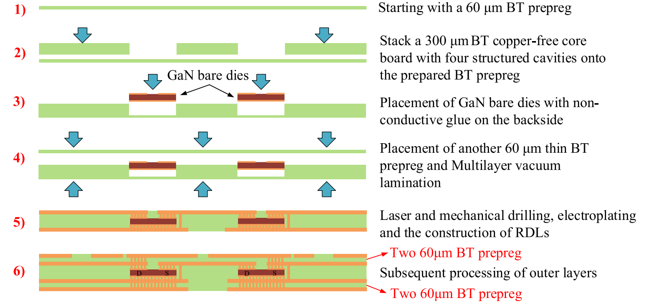


Fig. 13. Schematic of face-up process flow to realize the proposed PEGM.

C. Manufacturing Process Flow of The Proposed PEGM

The process flow to realize the proposed PEGM is shown in Fig. 13.

1) The fabrication of the proposed PEGM starts with a thin BT prepreg, the thickness of which is 60 μm to prevent resin starved as the following core board to embed GaN bare dies is thick.
2) Prepare a copper-free core board with four structured cavities for embedding GaN bare dies and stack it onto the prepared thin BT prepreg. The thickness of the copper-free core board should greater than the thickness of the embedded GaN bare dies to prevent them being crushed during lamination pressing process. As the thickness of GS66508 is 265 μm, thus the thickness of the copper-free core board is selected as 300 μm.
3) Place four GaN bare dies with nonconductive glue on the backside into the four structured cavities.
4) Put another 60 μm BT prepreg onto the above stack-ups, and laminate them in a vacuum lamination press to prevent air voids.
5) Drill microvias to the embedded GaN bare dies by laser, followed by via cleaning, activation and galvanic copper deposition to fill the microvias with copper.

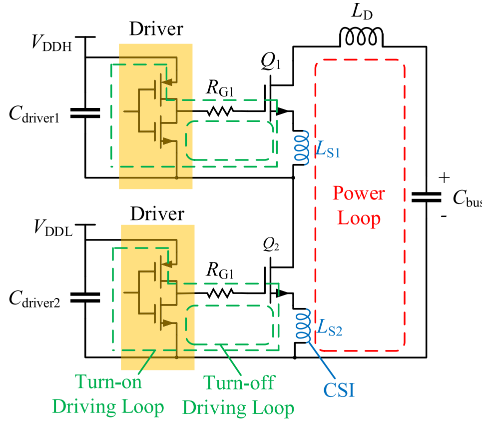


Fig. 14. Schematic of the three main parasitic inductances.

6) The rest process is the processing of outer layers, which is the same as the process flow of conventional PCB. Note that, as the thickness of the copper layer is 2 oz, to prevent resin starved, two 60 μm BT prepregs are needed between top layer and the first inner layer below, and between bottom layer and the first inner layer above.

III. Optimization of Power Loop Based on Electro-Thermal Codesign

As aforementioned, GaN devices have very high switching speed, thus very high dv/dt and di/dt can be caused during high frequency switching transients, which makes it very susceptible to parasitic inductances. There are three main parasitic inductances, i.e., CSI, PLI, and DLI, as shown in Fig. 14. With regard to the PLI, a voltage will be induced across it due to the negative di/dt during the turn-OFF process. The induced voltage has the same direction with bus voltage, and will be applied across the turn-OFF GaN device together with bus voltage. As GaN devices have very high di/dt, the induced voltage can be very high, resulting in a very high voltage overshoot across the turn-OFF GaN device. If the PLI is not optimized, the GaN devices must be only used under derated voltage, otherwise overvoltage breakdown may be caused. Therefore, the minimization of PLI is very essential for the high frequency operation of GaN devices.

Benefitting from the employed PCB embedding technology, the GaN bare dies are embedded in the PCB laminates, and the interconnection of copper-filled laser microvias can be enabled to replace the conventional bonding wires. More importantly, the space on top surface above the four embedded GaN bare dies is left for the integration of decoupling capacitors. Therefore, a vertical power loop formed by the top RDL and the first inner RDL below can be realized, which has very small loop area. Thus, the cancelling effect will take into effect to realize an ultrasmall PLI. However, during the optimization of PLI, there are several coupling parameters affecting the heat dissipation capability of the proposed PEGM, including the distances between power devices in the same bridge arm d and the distance between power devices in different bridge arms w. In this section, the electro-thermal codesign will be carried out to reveal their effects on PLI and the thermal performance, and further to achieve both small PLI and good heat dissipation performance.

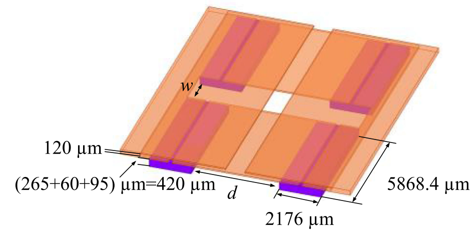


Fig. 15. Simplified model for PLI optimization.

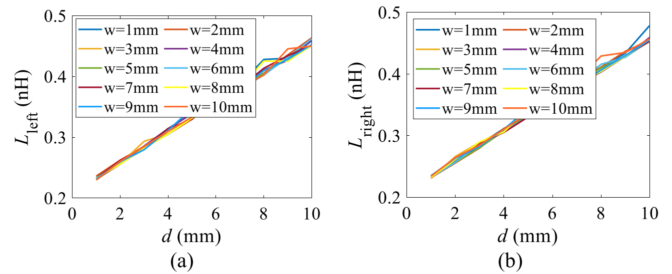


Fig. 16. PLI of (a) left bridge and (b) right bridge versus d and w.

A. Effects of d and w on Power Loop Inductance

To study the effects of d and w on PLI, the FEA simulation is carried out by using Ansys Q3D Extractor, in which d and w are swept from 1 to 10 mm at the frequency of 100 MHz. Since changing d and w will accordingly change the layout, which is time consuming. To facilitate research, the simulation model is simplified, in which the embedded GaN bare dies including the copper pillar arrays by laser microvias and copper electroplating on both sides are replaced by four boxes with the same size, and the layouts of power loop are regularized, as shown in Fig. 15. Through simulation, the curves of the PLIs of left and right bridge arms versus d at different w are plotted in Fig. 16. As we can see, both the PLIs of left and right bridge arms increase linearly with increase of d, with the same slope at different w. Therefore, to minimize the PLIs, the smaller d, the better.

B. Effects of d and w on Thermal Performance

However, reducing d will strengthen the thermal coupling between the embedded GaN bare dies, which will further bring challenge to the heat dissipation of the proposed PEGM. Therefore, by using the FEA simulation software Icepak, the thermal simulation of the proposed PEGM is carried out in this section, to investigate the effects of d and w on the thermal performance by sweeping d and w from 1 to 10 mm. Wherein, the power losses of the four GaN bare dies are all 10 W, the ambient temperature is 40 °C, and the heat transfer coefficients of both the top and bottom sides of the proposed PEGM are 1000 W/(K·m^2). The maximum temperatures of the four GaN bare dies versus d and w are plotted in Fig. 17(a)–(d). As we can see, with the increase of d and w, the maximum temperatures drop rapidly at the beginning, and then flatten out gradually. When d is larger than about 3 mm

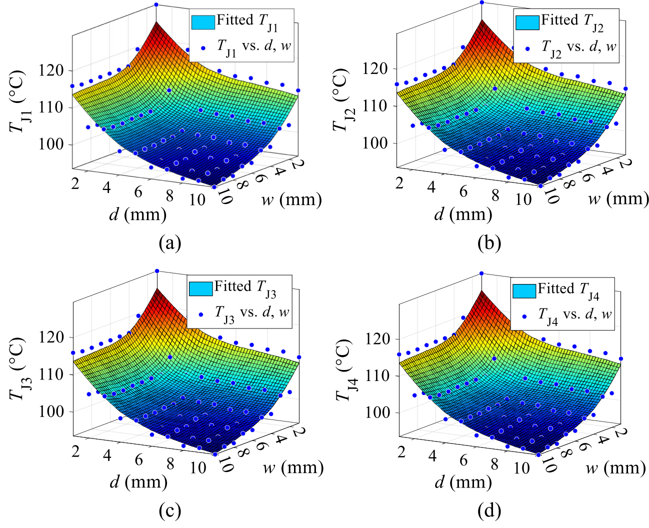


Fig. 17. Maximum junction temperature of (a) Q_1, (b) Q_2, (c) Q_3, and (d) Q_4 versus d and w.

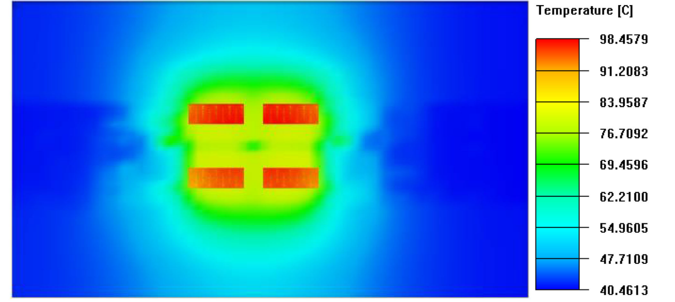


Fig. 18. Thermal distribution of the proposed PEGM with the thermal transfer coefficient of 1000 W/(K·m^2) on both sides.

TABLE IV
THERMAL RESISTANCES FROM JUNCTIONS OF THE EMBEDDED GAN BARE DIES TO TOP SURFACE

Maximum Junction Temperature (°C)		Thermal Resistance (°C/W)	
T_{J1}	73.92	$R_{th\text{-}JT1}$	3.39
T_{J2}	73.77	$R_{th\text{-}JT2}$	3.38
T_{J3}	67.65	$R_{th\text{-}JT3}$	2.77
T_{J4}	67.33	$R_{th\text{-}JT4}$	2.73

TABLE V
THERMAL RESISTANCES FROM JUNCTIONS OF THE EMBEDDED GAN BARE DIES TO BOTTOM SURFACE

Maximum Junction Temperature (°C)		Thermal Resistance (°C/W)	
T_{J1}	44.57	$R_{th\text{-}JB1}$	0.46
T_{J2}	44.3	$R_{th\text{-}JB2}$	0.43
T_{J3}	44.4	$R_{th\text{-}JB3}$	0.44
T_{J4}	44.24	$R_{th\text{-}JB4}$	0.42

and w is larger than about 2 mm, the decrease of the temperatures is no longer obvious. Considering that the space directly above the four embedded GaN bare dies is used to attached to heat sink to improve the thermal performance, In this article, to prevent the decoupling capacitors with the package of 1206 affecting the attachment of heatsink directly above the embedded GaN bare dies, the distance between the power devices in the same bridge arm d is set to about 4.3 mm considering the size, and the distance between the power devices in different bridge arms w is set to about 2 mm.

Based on the designed parameters, the PCB layout of the proposed PEGM is realized. From the actual layout, the simulation model for extracting parasitic inductance is established as aforementioned. The PLIs of both the two bridge arms in the proposed full-bridge PEGM are extracted by using Ansys Q3D Extractor, as listed in Table II. The PLIs of the left and right bridge arm are both about 0.305 nH, which are the lowest value in power modules with the same power level. Thus, the voltage overshoot across GaN device can be dramatically reduced to ensure that the GaN devices can work at a voltage much closer to their rated voltage. Then, the thermal performance of the proposed PEGM is evaluated by using Ansys Icepak, in which the heat transfer coefficients of both the top and bottom sides are set to 1000 W/(K·m^2). The simulated thermal distribution of the proposed PEGM is shown in Fig. 18. The maximum temperature of the proposed PEGM is about 98.46 °C, which benefits from the large amounts of copper-filled laser microvias on both sides of the embedded GaN bare dies, the advanced BT material, and the electro-thermal optimization.

To further quantify the thermal performance of the proposed PEGM, the thermal resistances of the proposed PEGM are extracted. By fixing the top side to ambient temperature and setting the other boundary walls to be adiabatic, the thermal resistances from the embedded GaN bare dies to top side of the module are achieved according to (1). In the same way, by fixing the bottom side to ambient temperature, the thermal resistances from the embedded GaN bare dies to bottom side of the module are achieved. The maximum junction temperatures of the embedded GaN bare dies and the calculated thermal resistances are listed in Tables IV and V. The maximum junction-to-top thermal resistance of the four embedded GaN bare dies is 3.39 °C/W, while the maximum junction-to-bottom thermal resistance is 0.46 °C/W.

$$R_{\rm th} = \frac{T_J - T_{\rm case}}{P}. \tag{1}$$

IV. ELECTRICAL PERFORMANCE OPTIMIZATION AND EVALUATION BESIDES PLI

In this section, the electrical performance of the proposed PEGM besides the PLI are carefully optimized and evaluated, including the CSI, DLI, the parasitic capacitances brought by the package, and the insulation strength, which are also very important for the reliable high-frequency operation of GaN devices.

A. Optimization of Common Source Inductance

The CSI is the part of parasitic inductance common to both power loop and driving loop, and has the most serious impact on

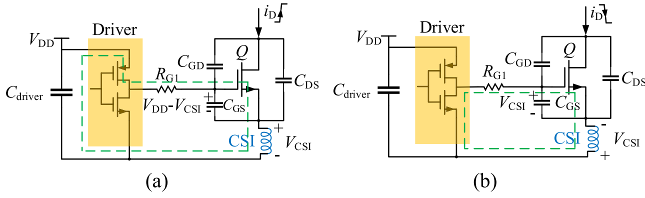


Fig. 19. Effect of CSI during (a) turn-ON process and (b) turn-OFF process.

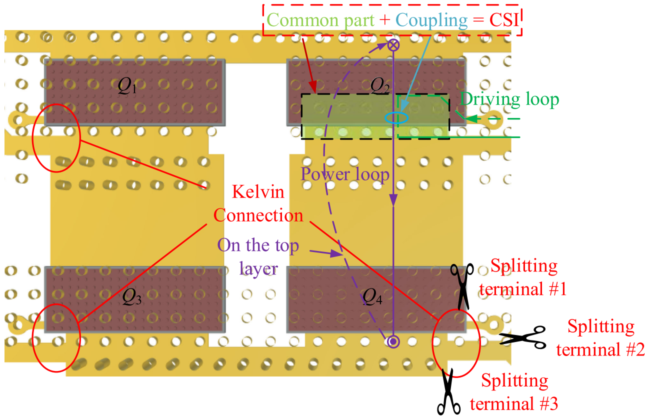


Fig. 20. Kelvin connections to reduce CSI.

the high-frequency operation of GaN devices, which is mainly brought by high d*i*/d*t* in power loop to driving loop during high-speed switching transient. For GaN devices, the driving threshold voltage is usually very small (1.3 V for GS66508), so it is sensible to the CSI. During the turn-ON process, the high positive d*i*/d*t* will induce a positive voltage across CSI, as shown in Fig. 19(a), which will counteract the driving voltage to turn OFF the device unintendedly. During the turn-OFF process, the high negative d*i*/d*t* will induce a negative voltage across CSI, as shown in Fig. 19(b), which will directly drive the GaN device to turn on unexpectedly. Hence, it is very important to minimize CSI for the high frequency operation of GaN devices. A well-acknowledged solution is to separate the driving and power loops to as close to the GaN device as possible, which is so-called Kelvin connection. In this article, the Kelvin connection is realized for all the four embedded GaN bare dies, as shown in Fig. 20.

To accurately evaluate the CSI, the FEA simulation considering the coupling between power loop and driving loop was carried out, during which the GaN bare dies, driving resistances and the decoupling capacitors are set to conductors. First, the simulation model for extracting the mutual inductance between power loop and driving loop was obtained by splitting driving loop and power loop because it is not allowed to apply more than one source-sink pairs to the same electrical nets. For the power loop, we applied the source to one terminal of the decoupling capacitors connecting to the positive terminal of dc bus voltage, and apply the corresponding sink to the other terminal of the decoupling capacitors connecting the ground terminal. For the driving loop, we applied a source to the output of the driver, and applied the corresponding sink to the splitting terminal #1. Then, we applied another source to the splitting terminal #3,

TABLE VI
EXTRACTED SELF-INDUCTANCE AND MUTUAL INDUCTANCE OF CSI

	Self-inductance (pH)	Mutual inductance (pH)
Q_1	24.83	-6.2 [a]
Q_2	24.81	-5.78 [a]
Q_3	24.59	-5.12 [a]
Q_4	28.27	-2.86 [a]

[a]Minus sign indicates the two applied terminals are not homonymous ends.

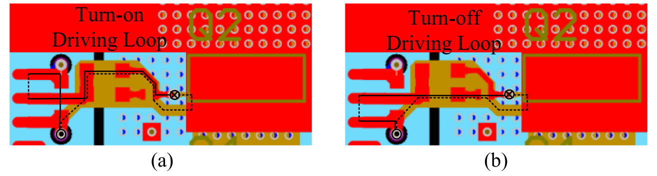


Fig. 21. Designed (a) turn-ON loop and (b) turn-OFF loop for Q_2.

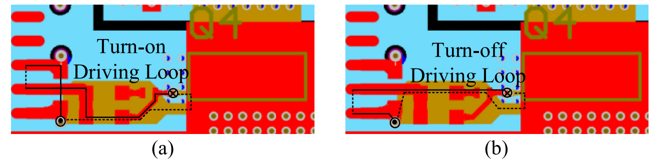


Fig. 22. Designed (a) turn-ON loop and (b) turn-OFF loop for Q_4.

and applied the corresponding sink to the terminal back to driver. Finally, we assigned the reduced matrix in Ansys Q3D Extractor to connect the first sink to the second source in series. By this way, the mutual-CSIs of the four GaN bare dies Q_1, Q_2, Q_3, and Q_4 can be extracted. The extraction of the self-CSIs is relatively simple, in which the source was applied to the source pad of the GaN bare die, and the sink was applied to the splitting terminal #2. Under the simulation frequency of 100 MHz, the self-CSIs and mutual CSIs by PSI of Q_1, Q_2, Q_3, and Q_4 were extracted, as listed in Table VI. As we see that the maximum self-CSI of the four GaN bare dies is only 28.27 pH, and the maximum mutual-CSI is 6.2 pH. The ultrasmall CSIs can greatly improve the switching characteristics of GaN devices.

C. Optimization of Driving-Loop Parasitic Inductance

The existence of DLI will bring ringing to the voltage across the gate-to-source capacitance of power device. For GS66508 GaN device, the maximum gate-to-source voltage is 7 V, while the recommended driving voltage is 6 V. The only 1 V margin of the gate-to-source voltage highly requires to minimize the DLI. In order to minimize the DLI, the driving circuit has been placed as close to the GaN device as possible. Besides, as shown in Figs. 21–23, an area of copper plane is intendedly placed below the driving circuit on top layer to form a vertical loop. The turn-ON and turn-OFF DLIs for Q_1, Q_2, Q_3, and Q_4 are extracted by using Ansys Q3D Extractor at the simulation frequency of 100 MHz, as listed in Table VII. Then, the turn-ON resistances are designed to ensure that the gate-to-source voltage of GaN devices has no much overshoot during turn-ON transient. According to (2), the turn-ON driving resistances can be calculated

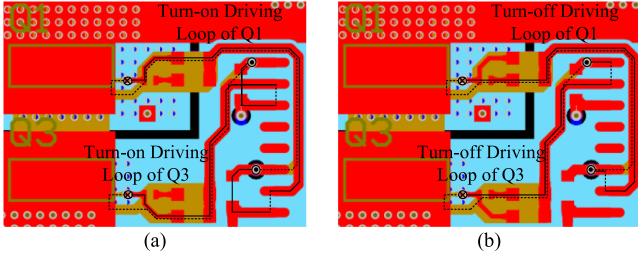


Fig. 23. Designed (a) turn-ON loop and (b) turn-OFF loop for Q_1 and Q_3.

TABLE VII
DRIVING LOOP PARASITIC INDUCTANCES AND THE CALCULATED EXTERNAL TURN-ON RESISTANCES

	Turn-on inductance (nH)	Turn-off inductance (nH)	External Turn-on resistance (Ω)
Q_1	6.93	5.5	2.6
Q_2	4.06	3.83	1.1
Q_3	4.93	4.45	1.6
Q_4	3.6	3.36	0.81

[15], [37]

$$R_{\text{Gon}} = 2\zeta\sqrt{\frac{L_{\text{Gon}}}{C_{\text{ISS}}}} \tag{2}$$

$$\text{Overshoot Voltage} = V_g \cdot e^{-\frac{\zeta\cdot\pi}{\sqrt{1-\zeta^2}}} \tag{3}$$

where ζ is the damping coefficient of the driving loop, L_{Gon} is the parasitic inductance of turn-ON loop, C_{ISS} is the input capacitance of the GS66508 (260 pF), and V_{g} is the driving voltage (6 V is recommended). To ensure the gate-to-source voltage smaller than 0.5 V with sufficient safety margin, according to (3), ζ should be greater than 0.62. As the employed isolated half-bridge driver Si8273GBD-IS1, the internal turn-ON resistance is 2.7 Ω, and the internal gate resistance of GS66508 GaN bare dies is 1.1 Ω. Therefore, the calculated minimum external resistances are listed in Table VI. In this article, all the four turn-ON resistances are selected as 2.7 Ω.

D. Optimization of the Parasitic Capacitances

By applying the PCB embedding technology to the packaging and integration of GaN devices, an ultrathin PEGM is realized. Due to the ultrathin profile, the distance between layout layers is very small so that ultrasmall parasitic inductances are achieved. However, the introduced parasitic capacitances by the ultrathin package cannot be ignored under this condition, because the capacitances are in inverse proportion to the distance between two conductors (layout layers), determined by (4)

$$C = \frac{\varepsilon_r \varepsilon_0 A}{t} \tag{4}$$

where ε_r is the relative permittivity of BT material, ε_0 is the permittivity of vacuum, A is the area of the copper foil, and t is the thickness of the dielectric material BT.

The introduced parasitic capacitances by the packaging structure, i.e., C_{DSP1}, C_{DSP2}, C_{DSP3}, and C_{DSP1} are paralleled

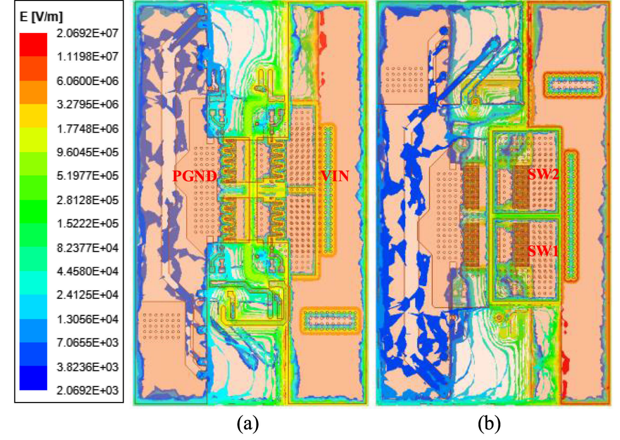


Fig. 24. Electric field distribution of the proposed PEGM. (a) Top view. (b) Bottom view.

TABLE VIII
PARASITIC CAPACITANCES BROUGHT BY THE PCB-EMBEDDED PACKAGE

	Parasitic Capacitance (pF)
C_{DSP1}	13.956
C_{DSP2}	13.546
C_{DSP3}	13.048
C_{DSP4}	11.46

with Q_1, Q_2, Q_3, and Q_4 in Fig. 5, respectively, which will be superimposed on the output capacitances of the four embedded GaN bare dies, affecting the switching characteristics together. To minimize the parasitic capacitances brought by the package, this article has carefully reduced the copper area of the nets of SW1 and SW2, as shown in Fig. 24. With the assumption that the lamination and filling of the BT prepreg is perfect, the electrostatic field simulation is conducted by using Ansys Maxwell, to extract the four paralleled parasitic capacitances brought by the packaging structure, as listed in Table VIII. The four simulated parasitic capacitances are 13.956, 13.546, 13.048, and 11.46 pF, respectively, which are comparable to the output capacitance of GS66508 (65 pF). Meanwhile, the electric field strength in package can also be achieved by the electrostatic field simulation, are simulated, in which 650, 0, and −650 V are applied to the nets of VIN, SW1 and SW2, and PGND, respectively. As shown in Fig. 24, the maximum electric field strength is about 20.7 MV/m, which is much smaller than the maximum electric field strength of BT material (usually above 40 MV/m) [38], [39]. Therefore, the proposed PEGM can meet the insulation requirement.

V. EXPERIMENTAL VERIFICATION

A. Experimental Setup

Based on the face-up process flow in Fig. 13, the proposed PEGM is fabricated. As shown in Fig. 25(a), (b), and (c), the size of the realized PEGM is 55.1 mm × 31.9 mm × 0.9 mm, which is an ultrathin package. The overall thickness of the proposed PEGM with soldered driving circuit and decoupling capacitors

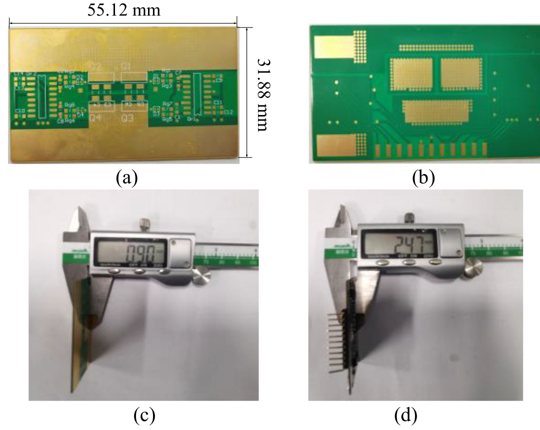


Fig. 25. Figure of the realized PEGM. (a) Top view, (b) bottom view, (c) side view without soldered components, and (d) side view with soldered components.

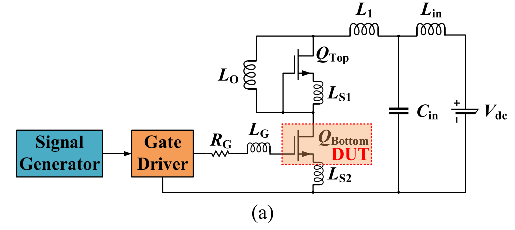
is 2.47 mm, as shown in Fig. 25(d). Due to the high integration of the GaN based full-bridge, four decoupling capacitors, and the driving circuits, the external circuit on motherboard can be simplified. To verify the ultralow parasitic inductances of the proposed PEGM, a DPT platform is established, in which an air core inductor of about 50 μH is used as the output inductor to prevent saturation under high current, as shown in Fig. 26. The signal generator DG4062 is used to generate the double pulse signal for gate driver, the auxiliary power is used to power the gate driver, and the power supply is used to provide the dc bus voltage. The 1-GHz high-bandwidth oscilloscope MSO64 6-BW-1000A and passive voltage probe TPP1000 are used to accurately measure the switching voltage waveforms, and the current probe TCP0030A is used to measure the current waveform of output inductor.

B. Experimental Results and Discussion

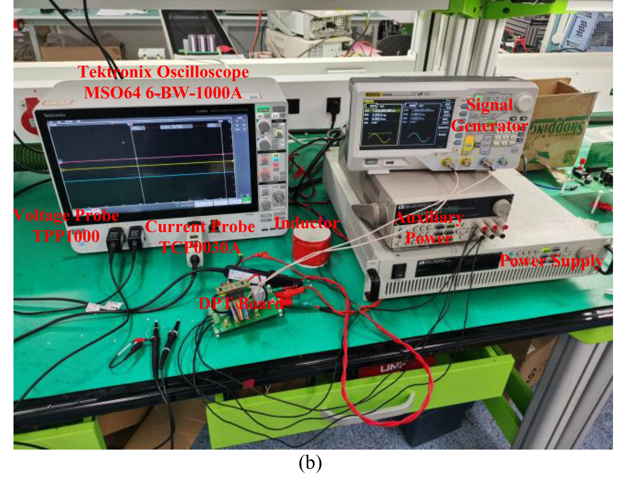
In this article, the DPT experiment is carried out for both the left (Q_2 and Q_4) and right (Q_1 and Q_3) bridge arms at the dc bus voltage of 200 V. The switching waveforms of both the left and right bridge arms are measured as shown in Fig. 27, including the drain-to-source voltage, gate-to-source voltage and output current waveforms of the device under test (DUT). As we can see, the current of output inductor rises to 19.4 A at the end of the first wide pulse, which is the turn-OFF current of DUT. The enlarged turn-OFF waveforms are replotted in Fig. 28. It can be seen that, for the left bridge arm, the dv/dt is 54.5 V/ns while the voltage overshoot is only 6.9 V, accounting for 3.45% of the dc bus voltage. For the right bridge arm, the dv/dt is 55.7 V/ns while the voltage overshoot is only 10.7 V, accounting for 5.35% of the dc bus voltage. Due to the ultralow PLIs, the turn-OFF waveform oscillation of the drain-to-source voltage is very small. For the left bridge arm, the oscillation period is about 1.45 ns, and for the right bridge arm, the oscillation period is about 1.44 ns, which are determined by

$$T_{\text{ring}} = 2\pi \cdot \sqrt{L_{\text{Loop}} \cdot (C_{\text{OSS}} + C_{\text{DSP}})} \tag{5}$$

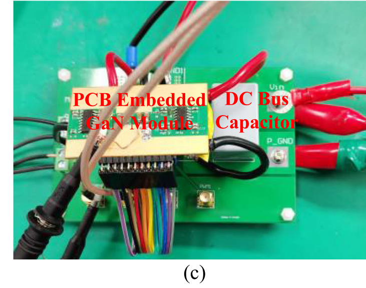
where L_{LOOP} is the power loop parasitic inductance, C_{OSS} is the output capacitance of GS66508 at 200 V (83.2 pF), and C_{DSP} is the parasitic capacitance brought by the package in



(a)



(b)



(c)

Fig. 26. (a) Schematic of DPT equivalent circuit, (b) DPT experimental platform, and (c) DPT experimental board.

parallel with DUT. Therefore, the PLIs of the left and right bridge arms can be calculated by using (6) and (7), respectively. The calculated PLIs of the left and right bridge arms are 0.553 and 0.555 nH, respectively, which are larger than the simulated value of 0.305 nH

$$\begin{aligned} L_{\text{Loop_Left}} &= \frac{T_{\text{ring}}^2}{4\pi^2 \left(C_{\text{OSS}} + C_{\text{DSP3}}\right)} \\ &= \frac{(1.45 \text{ ns})^2}{4\pi^2 \left(83.2 \text{ pF} + 13.05 \text{ pF}\right)} = 0.553 \text{ nH} \end{aligned} \tag{6}$$

$$\begin{aligned} L_{\text{Loop_Right}} &= \frac{T_{\text{ring}}^2}{4\pi^2 \left(C_{\text{OSS}} + C_{\text{DSP4}}\right)} \\ &= \frac{(1.44 \text{ ns})^2}{4\pi^2 \left(83.2 \text{ pF} + 11.46 \text{ pF}\right)} = 0.555 \text{ nH}. \end{aligned} \tag{7}$$

One main reason is that the parasitic inductance bought by the decoupling capacitors. In this article, four ceramic capacitors CGA5L1X7T2J473M160AE with the package of 1206 (630 V, 0.047 μF) are used as the decoupling capacitors. Fig. 29 shows the impedance characteristics curve

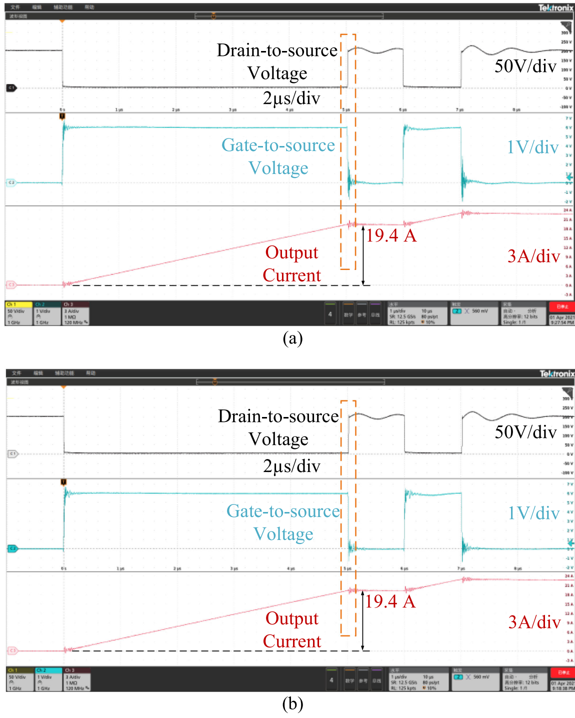


Fig. 27. Experimental switching waveforms of (a) left bridge arm and (b) right bridge arm.

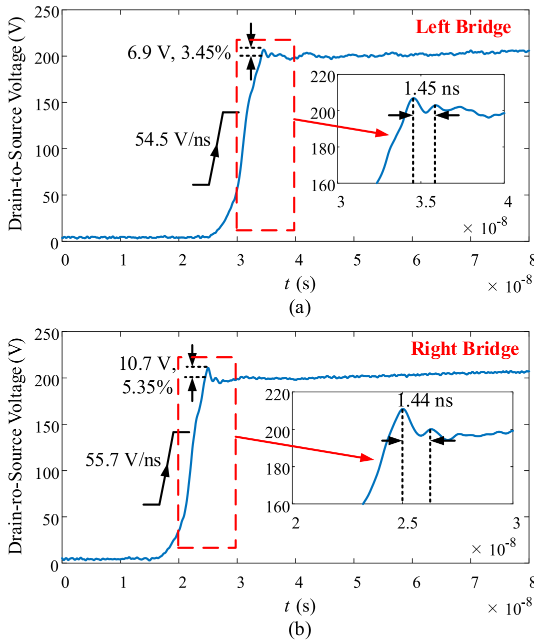


Fig. 28. Enlarged switching waveforms of (a) left bridge arm and (b) right bridge arm.

of CGA5L1X7T2J473M160AE from datasheet, which can be modeled by a series circuit consisting of a capacitor C_{dec}, an inductor ESL and a resistor ESR. Assuming C_{dec}, ESR and ESL are all frequency independent, their values can be obtained by curve fitting, as shown in Fig. 29. The obtained C_{dec}, ESR and ESL are 47.66 nF, 0.052 Ω, and 1.07 nH, respectively. Therefore,

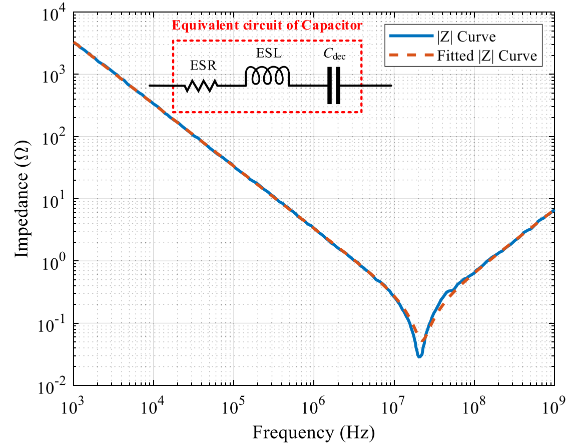


Fig. 29. Impedance characteristics curve of CGA5L1X7T2J473M160AE.

the parasitic inductance brought by the four paralleled decoupling capacitors is about 0.267 nH. By subtracting 0.267 nH from the calculated PLIs (0.553 nH and 0.555 nH), 0.286 nH and 0.288 nH are obtained, which are about 6.2% and 5.6% smaller than the simulated values (0.305 nH). It is because that there are differences in structural parameters between simulation model and the realized PEGM due to manufacturing error. The thickness of the realized PEGM is thinner than the designed thickness, which makes the actual parasitic inductances smaller than the simulated values. Nevertheless, the measurement results are sufficient to verify the ultralow parasitic inductance of the proposed PEGM.

VI. Conclusion

In order to promote the high frequency application of GaN devices, this article proposes an ultrathin GaN module with ultrasmall parasitic inductances based on the PCB embedding technology. The proposed PEGM highly integrates a full bridge, isolated driving circuit, and decoupling capacitors. Through comparing the parasitic inductances and thermal performance of the face-up and face-down based modules, the superiority of the proposed face-up based module was demonstrated. To make a tradeoff between PLI and the thermal performance, careful electro-thermal codesign was conducted by using FEA simulation. The simulated PLIs of the left and right bridge arms both reach to the lowest value of about 0.305 nH in power modules with the same power level. The maximum thermal resistances from the embedded GaN bare dies to top and bottom surface are 3.39 and 0.42 °C/W, respectively. Then, the electrical performance optimization, involving CSI, DLI, parasitic capacitances brought by package, and the insulation strength, was conducted. Finally, the DPT experimental platform is established to verify the ultralow PLIs of the proposed PEGM, and good results are shown. The dv/dt can be up to 55.7 V/ns, while the voltage overshoot is not higher than 5.35% of the dc bus voltage. The superiorities of the proposed PEGM will make it a promising application prospect in high frequency high power density converters.

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Zhiyuan Qi (Student Member, IEEE) was born in Henan Province, China, in 1989. He received the B.S. and M.S. degrees in electrical engineering and automation, in 2012 and 2015, respectively, from Harbin Engineering University, Harbin, China. He is currently working toward the Ph.D. degree in electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His research interests include the packaging and integration of wide bandgap power semiconductors and high-frequency power conversion technologies.

Yunqing Pei (Member, IEEE) was born in 1969. He received the B.S. and M.S. degrees, in 1991 and 1994, respectively, both in electrical engineering, and the Ph.D. degree in power electronics, in 1999, all from Xi'an Jiaotong University, Xi'an, China.

He became a Faculty Member with Xi'an Jiaotong University, where he is currently a Professor. From 2006 to 2007, he was a Visiting Scholar with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His research interests include the high-power inverters, switch mode power supply, and converters in distributed generation systems.

Laili Wang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with Electrical Engineering Department, Queen's University, Kingston, ON, Canada.

From 2014 to 2017, he was an Electrical Engineer with Sumida, Pointe Claire, QC, Canada. In 2017, he joined Xi'an Jiaotong University as a Full Professor. His research interests include package and integration, wireless power transfer, and energy harvesting.

Dr. Wang is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and the *IEEE Journal of Emerging and Selected Topics in Power Electronics.* He is the Vice Chair of TC2 (Technical committee of Power Conversion Systems and Components) in PELS, Cochair of System Integration and Application in ITRW (International Technology Roadmap for Wide Band-Gap Power Semiconductor), and Chair of IEEE CPSS&PELS joint Chapter in Xi'an, China.

Qingshou Yang (Student Member, IEEE) was born in Hebei, China, in 1993. He received the B.S. and M.S. degrees in electrical engineering and automation, in 2016 and 2019, respectively, from Yanshan University, Qinhuangdao, China. He is currently working toward the Ph.D. degree in electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His research interests include application of wide band gap devices and power electronic integration.

Kangping Wang (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2012 and 2018, respectively.

From 2016 to 2017, he was with the Department of ePOWER, Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, as a Visiting Scholar. Since 2018, he has been an Associate Professor with the School of Electrical Engineering, Xi'an Jiaotong University. His research interests include high-frequency power conversion technology and application and integration technology of wide bandgap devices.

Dr. Wang was the recipient of the Best Paper Award of the International Conference on Power Electronics–ECCE Asia in 2019.