Simultaneous Wireless Power and Data Transfer: A Comprehensive Review

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***Abstract*—Simultaneous wireless power and data transfer (SWPDT) is widely investigated because of the increasing requirement for real-time communication between the primary and secondary sides in wireless power transfer systems. This article classifies SWPDT systems into four categories according to the type and number of data channels and data carrier generation method. They are power carrier-based SWPDT system, high-frequency data carrier-based SWPDT system, multiple inductive channels SWPDT system, and inductive–capacitive hybrid channels SWPDT system, respectively. Four key issues, including cross-talk minimization, improvement of signal-to-noise ratio, modulation method for high data rate and low bit error rate, and special design to achieve full-duplex communication and improve misalignment tolerance, are discussed. The advantages, disadvantages, and applications of the four types of SWPDT systems are summarized. Finally, conclusions and outlook of the SWPDT system are given.**

***Index Terms*—Bit error rate (BER), cross-talk minimization, data channel gain maximization, data rate, misalignment tolerance, simultaneous wireless power and data transfer (SWPDT).**

I. Introduction

WIRELESS power transfer (WPT) has gained a large quantity of attention due to its advantages, such as convenience, safety, and reliability, when it is compared with the conventional wired power transfer system. This technique has been widely adopted in implantable biomedical devices, electrical vehicles, consumer electronics [1]–[6]. In these applications, the information is often required to be transferred simultaneously with power to achieve some special purposes, such as achieving maximum power transmission, online monitoring of battery status in electrical vehicle (EV) charging, and intracranial pressure detection from the implanted sensors [7]–[10]. Radio frequency (RF) based communication techniques such as Bluetooth, ZigBee, and Wi-Fi have been adopted to transfer forward or backward data in some WPT systems [11], [12]. However, the time delay of the RF-based communication techniques could be up to several milliseconds, which is not applicable to a real-time control system. With the increase of power level of the WPT system, the bit error rate (BER) of RF communication increases significantly [13], [14]. Thus, simultaneous wireless power and data transfer (SWPDT) is proposed and investigated [15].

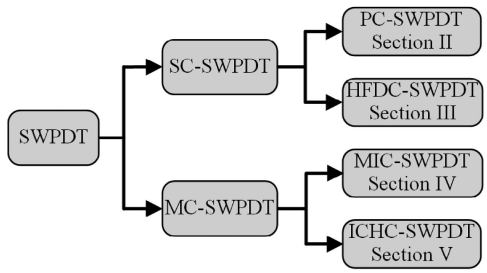

Fig. 1. Classification of SWPDT systems.

The reported SWPDT techniques can be mainly divided into two categories: power and data transfer through a single channel (SC-SWPDT) and multiple channels (MC-SWPDT). The SC-SWPDT can further be divided into two groups: power carrier-based SWPDT (PC-SWPDT) and high-frequency data carrier-based SWPDT (HFDC-SWPDT). In PC-SWPDT, the data signal is generated by directly modulating the power signal [16]–[18]. In HFDC-SWPDT, the modulated data signal is injected into the common channel by using frequency-division multiplexing (FDM) [19]–[24]. The MC-SWPDT can further be divided into two parts: multiple inductive channels SWPDT system (MIC-SWPDT) by adding extra coil pairs for data transfer [25]–[27] and inductive–capacitive hybrid channels SWPDT system (ICHC-SWPDT) by utilizing hybrid fields for SWPDT [28], [29]. Fig. 1 shows the classification of the WPDT system.

The introduction of a data transfer circuit may impair the constant output characteristic (COC) of the original WPT system. For example, in a PC-SWPDT system, it is difficult to achieve constant current output (CCO) or constant voltage output (CVO) owing to direct modulation of power signal [30]. In the HFDC-SWPDT system, the data signal may be incorrectly demodulated because of the low signal-to-noise ratio (SNR) when the transferred power is high. SNR is a concept widely employed in communication. However, up to now, there is not a standard method to calculate the SNR of an SWPDT system. In published papers, it is generally calculated using (1). $V_{\text{dd-data}}$

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represents the voltage at the data demodulation port (see Figs. 21, 22, and 26–29) resulting from the data signal. $V_{\text{dd-power-}m}$ stands for the voltage at the data demodulation port resulting from the mth harmonic of the power signal. The subscript m is the order of critical harmonics which can be obtained using (2). f_{data} and f_{power} are the fundamental frequencies of data and power signals, respectively. Odd is a function employed to calculate the most approximate odd number

$$\text{SNR}_{\text{SWPDT}} = 20\lg\left(\frac{V_{\text{dd-data}}}{V_{\text{dd-power-}m}}\right) \tag{1}$$

$$m = \text{odd}\left(\frac{f_{\text{data}}}{f_{\text{power}}}\right). \tag{2}$$

To obtain an SWPDT system with desirable performance, the following four requirements should be fulfilled. First, COC and power transfer efficiency (PTE) of the original WPT system should not be influenced. No overvoltage or overcurrent arises in passive components during data transfer and modulation. In other words, the cross talk from data transfer and power modulation should be well suppressed. Second, a high SNR is required. According to the Shannon–Hartley theorem summarized in (3), data channel capacity C_{dc}, i.e., theoretical maximum data rate, is related to data transfer power S, noise power N, and channel bandwidth W [31]. Apparently, a high SNR results in a high data rate. To achieve a high SNR, the cross talk from power transfer to data transfer should be minimized, and the data channel gain should be maximized to improve the cross-talk tolerance. Third, to realize real-time control and state detection, a full-duplex SWPDT system featuring a high data rate and low BER is required. Hence, special modulation methods and topologies for bidirectional telemetry are required. Fourth, in some special applications such as EV charging and cochlear implant, misalignment between the primary and secondary may arise due to parking position error and human tissue motion. Therefore, misalignment tolerance is a key performance indicator for the SWPDT system. It should be noted that in most scenarios, the above-mentioned four requirements cannot be satisfied simultaneously. They are just four targets to design an SWPDT system.

$$C_{\text{dc}} = W\log_2\left(1+\frac{S}{N+1}\right). \tag{3}$$

This article gives a comprehensive review of SWPDT systems. It focuses on the methods to achieve the above-mentioned four requirements in the four types of SWPDT systems, i.e., PC-SWPDT, HFDC-SWPDT, MIC-SWPDT, and ICHC-SWPDT, which are discussed in Sections II–V, respectively. The advantages, disadvantages, and applications of the four types of SWPDT systems are summarized and compared in Section VI. Finally, Section VII concludes this article.

II. PC-SWPDT System

This section will review the methods employed in PC-SWPDT systems for cross-talk minimization from power modulation, improvement of SNR, and special modulation methods for high data rate. To the best of our knowledge, no literature focuses on misalignment tolerance in PC-SWPDT systems.

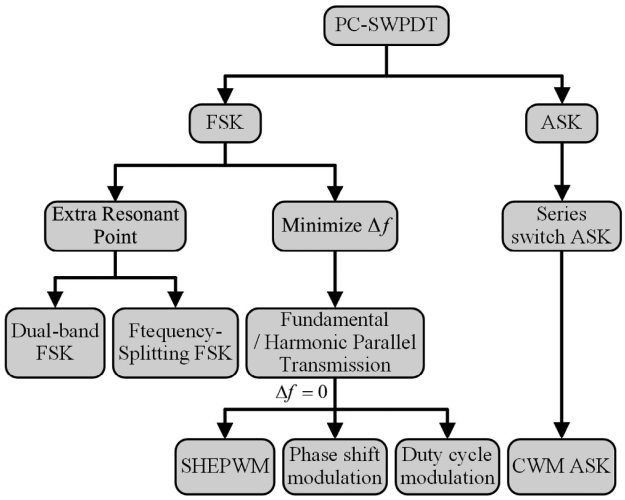

Fig. 2. Optimization design methods of modulation and compensation topology.

A. Cross-Talk Minimization From Power Modulation

Amplitude shift keying (ASK), ON–OFF keying (OOK), and frequency-shift keying (FSK) are widely adopted in PC-SWPDT systems for forward communication, and load-shift keying (LSK) is widely adopted for backward communication [15], [23], [24], [32]. Two methods are generally employed to minimize the crosstalk from power modulation. The first method is optimization design of modulation and compensation topology, while the second method is closed-loop control to achieve COC during power modulation. Fig. 2 shows the optimization design methods of modulation and compensation topology.

The block diagram of PC-SWPDT systems using different modulation methods is shown in Fig. 3. The common parts, including input voltage source, primary compensation topology, loosely coupled transformer, secondary compensation topology, uncontrolled rectifier, and load, are depicted with black line and words, while the different parts, primary and secondary modulation circuits, are highlighted with red line and words. The primary modulation circuit is for forward communication, while the secondary modulation circuit is for backward communication.

Fig. 4 shows the highlighted parts of the PC-SWPDT system shown in Fig. 3. The high-frequency inverter with variable frequency for PC-SWPDT system using FSK modulation is shown in Fig. 4(a). The binary FSK is adopted to achieve forward communication by simply changing the switching frequency of the inverter according to the bit stream [33]. However, the resonant state of the original WPT system will be changed and the PTE of the SWPDT system will be significantly reduced. In order to keep the resonant state, CVO, CCO, and PTE of the original WPT system unchanged, a 2FSK-PC-SWPDT system based on the frequency splitting phenomenon is introduced in [16], [17], and [34]. When the transfer distance of the WPT system is shortened, the WPT system will work from loose couple

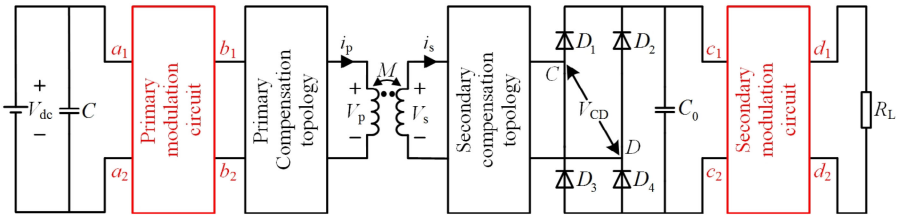

Fig. 3. Block diagram of PC-SWPDT systems using different modulation methods.

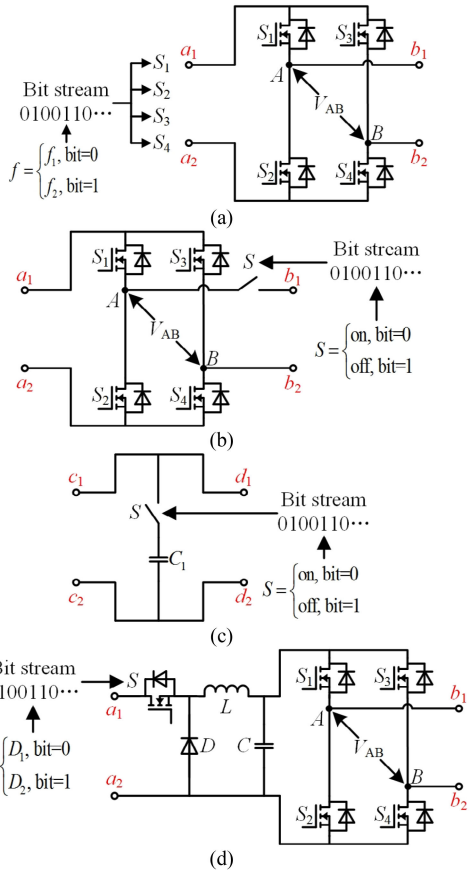

Fig. 4. Highlighted parts of the PC-SWPDT system shown in Fig. 3. (a) High-frequency inverter with variable frequency for PC-SWPDT system using FSK modulation. (b) Extra active switch in series with high-frequency inverter for PC-SWPDT system using OOK modulation. (c) Switching capacitor in parallel with rectifier for PC-SWPDT system using LSK modulation. (d) Boost converter with variable voltage gain and high-frequency inverter for PC-SWPDT system using ASK modulation.

region to strong couple region. The resonant frequency points will get two real solutions [35], [36]. The output power and PTE are proved to be the same at the two frequency splitting points in [37]. Therefore, directly modulating the power carrier using the 2FSK method will not influence the COC of the original WPT system. However, owing to the rapid decline of PTE as the coupling factor k increase, the PTE of the SWPDT system is not higher than 50%, which is relatively low compared to the WPT system working in the loose coupling region. Besides, the frequency splitting phenomenon only happens in strong coupling regions, which also limits the transfer distance of the SWPDT system.

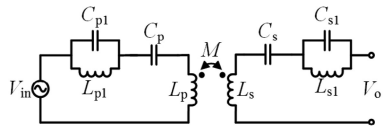

Fig. 5. Typical topology of the dual-band PC-SWPDT system.

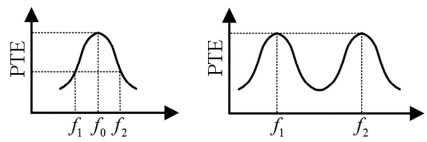

Fig. 6. PTEs of single-band and dual-band PC-SWPDT systems in [46].

To achieve a high PTE in 2FSK-PC-SWPDT, the dual-band WPT system is analyzed in [31] and [38]–[45]. As shown in Fig. 5, the composite resonant circuit-based WPT system is established by introducing the combined series-resonant networks ($C_{\rm p}$, $L_{\rm p}$, and $C_{\rm s}$, $L_{\rm s}$) and parallel-resonant networks ($C_{\rm p1}$, $L_{\rm p1}$ and $C_{\rm s1}$, $L_{\rm s1}$), achieving an extra resonant frequency point. By carefully designing the parameters, the quality factor Q of the resonant circuit can be maintained the same at the two resonant frequencies f_1 and f_2. Thus, the resonant state of the 2FSK-PC-SWPDT system will not be affected and the crosstalk from data transfer is eliminated [46]. As shown in Fig. 6, the PTE can be maintained as constant at the two resonant points and CCO is achieved with 20 kb/s data rate in [46]. However, the complexity of the SWPDT system will be increased with the introduction of the extra passive components.

To transfer power and data simultaneously without adding extra passive components and decreasing the PTE, another idea used in 2FSK modulation is to set the frequency deviation Δf as small as possible. Hence, the resonant state will not be significantly influenced during data transfer. However, owing to the limited accuracy of the demodulation circuit, Δf cannot be very small; otherwise, the BER will increase dramatically. To deal with this problem, the triangular current waveform-based SWPDT system is proposed in [47], as shown in Fig. 7. The key waveforms of the full-bridge inverter are shown in Fig. 8. The fundamental harmonic of the triangular current $i_{\rm p}$ is employed for power transfer, whereas the third-order harmonic of $i_{\rm p}$ is employed for data transfer. 2FSK is adopted for data modulation. When bit 0 is transferred, the fundamental frequency is f_0, and the frequency of the third-order harmonic is $3f_0$. The fundamental frequency shifts to f_1 when bit 1 is transferred, and the frequency of the third-order harmonic becomes $3f_1$. The frequency deviation of the fundamental and third-order

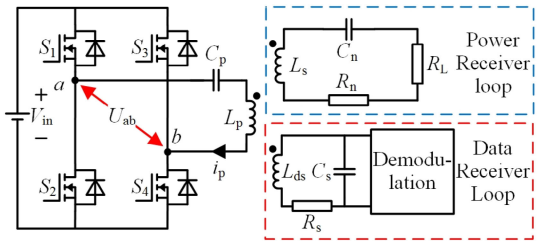

Fig. 7. Triangular current waveform-based SWPDT system proposed in [47].

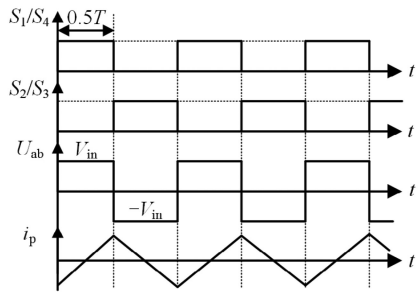

Fig. 8. Key waveforms of the full-bridge inverter in triangular current waveform-based SWPDT system [47].

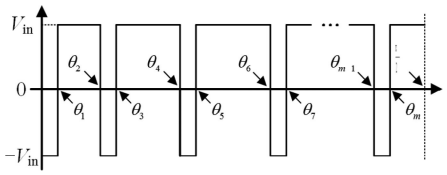

Fig. 9. Working principle of the PC-SWPDT system using SHEPWM within a quarter cycle [48].

harmonics are Δf and $3\Delta f$, respectively. The induced voltage over the signal winding is high when bit 0 is transferred and it is significantly reduced when bit 1 is transferred. Hence, the transferred data can be identified from the voltage envelope in the signal winding.

However, even a small Δf could spoil the PTE and output characteristics. To solve this problem, the selected harmonic elimination pulsewidth modulation (SHEPWM) is utilized in [48]. The Fourier expansion of output voltage of the GaN-based full-bridge inverter using SHEPWM can be obtained as follows [49], [50]:

$$\begin{cases} \frac{4V_{\text{in}}}{\pi}(1-2\cos\theta_1+2\cos\theta_2-\cdots+2\cos\theta_m)=V_{\text{LF}} \\ \frac{4V_{\text{in}}}{3\pi}(1-2\cos 3\theta_1+2\cos 3\theta_2-\cdots+2\cos 3\theta_m)=0 \\ \cdots\cdots \\ \frac{4V_{\text{in}}}{k\pi}(1-2\cos k\theta_1+2\cos k\theta_2-\cdots+2\cos k\theta_m)=V_{\text{HF}} \\ \cdots\cdots \\ \frac{4V_{\text{in}}}{n\pi}(1-2\cos n\theta_1+2\cos n\theta_2-\cdots+2\cos n\theta_m)=0. \end{cases} \tag{4}$$

Equation (4) indicates that the kth voltage harmonic can be designed to be zero or a certain value V_{HF}, while the other voltage harmonics are designed to be zero. By solving (4), switching angles θ_1 to θ_m can be obtained, as shown in Fig. 9. The amplitude of the kth current harmonic can be changed and employed for data transfer. The switching frequency is not changed when SHEPWM is adopted. Hence, the resonant state is not impaired and the PTE is maintained as a constant. However, solving the transcendental equation in (4) is very difficult. A total of 15 nonlinear equations and 15 switching angles need to be solved in [48].

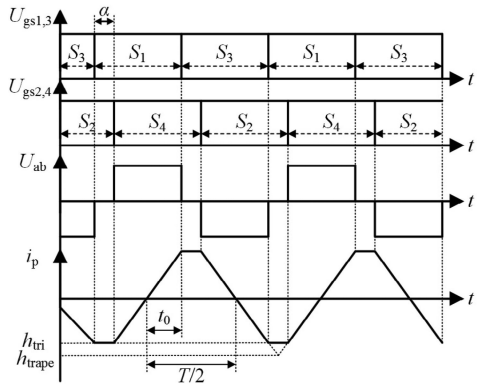

Fig. 10. Main working waveforms of the phase-shifted full-bridge inverter in PSM-PC-SWPDT system [51].

The phase-shift modulation (PSM) is proposed in [51] and [52] to simplify data modulation without increasing the calculation difficulty. The block diagram of the PSM-PC-SWPDT system is the same as in Fig. 7. The only difference between the PSM-PC-SWPDT system and the PC-SWPDT system proposed in [47] is the working principle of the full-bridge inverter, which is shown in Fig. 10. The triangularization rate of the trapezoidal wave σ is defined as (5) [51]. When the duty cycle equals 50%, the relationship between the phase shift time of S_1–S_4 and σ can be obtained, as shown in (6) and (7) [51]

$$\sigma=\frac{U_{\text{htrape}}}{U_{\text{htri}}}=\frac{4t_0}{T} \tag{5}$$

$$I_{\text{pk}}=\frac{4A_m}{k^2\omega t_0\pi}\sin k\omega t_0=\frac{8A_m}{k^2\sigma\pi^2}\sin\left(\frac{k\sigma\pi}{2}\right) \tag{6}$$

$$\sigma=1-\frac{\alpha}{180^\circ}. \tag{7}$$

On the basis of (6) and (7), the amplitude of the kth current harmonic can be designed to be zero or a certain value by changing the phase shift angle α. Thus, the forward data transfer can be achieved by using ASK demodulation, which is similar to the SHEPWM based SWPDT system. PTE of the SWPDT system using PSM is demonstrated the same as the original WPT system using nonphase shift control. Therefore, the interference from power carrier modulation is eliminated. The output power of the WPT system using PSM is larger than that using nonphase shift control.

However, changing the phase shift angle requires accurate clock synchronization. To simplify the modulation and lower the calculation difficulty, a novel active-clamped inverter (ACI) based SWPDT system is proposed in [53], as shown in Fig. 11. The working principle of the novel ACI is shown in Fig. 12. According to the article presented in [53], the kth current harmonic can be calculated as (8). It is obvious that by simply changing the duty cycle, the kth current harmonic can be controlled to zero or a certain value. The duty cycle is easy to calculate and

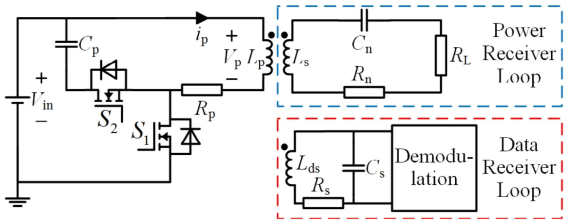

Fig. 11. ACI for PC-SWPDT system using duty-cycle modulation.

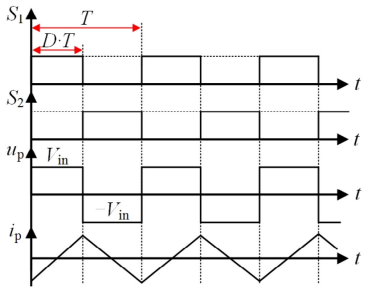

Fig. 12. Working principle of an ACI for PC-SWPDT system using duty-cycle modulation.

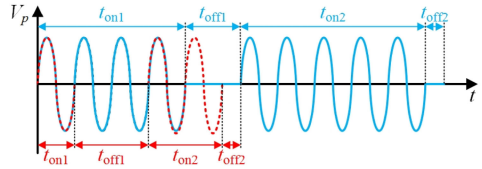

Fig. 13. CWM scheme for $n = 3$ (red dashed line) and $n = 6$ (blue line). n is the number of carrier cycles per data bit period [55].

the requirement of the clock synchronization is reduced. For the switching frequency is not changed, the dc/dc PTE is not influenced and less electromagnetic interference is introduced. The PTE is improved by 7% compared with the conventional H-bridge inverter and CCO is also achieved by a carefully designed transmitter coil because only the fundamental current is used for power transfer and two duty cycle points are selected to maintain a relatively close amplitude of the fundamental current.

$$I_{\mathrm{pk}}(D) = \frac{2V_{\mathrm{in}}}{k^2 L(1-D)\omega\pi} \sin kD\pi. \tag{8}$$

Apart from COC, the inner overvoltage and overcurrent generated by data modulation should be minimized as well. This phenomenon often happens in the series-switch SWPDT system using OOK, as shown in Fig. 4(b). When the switch is ON and OFF, the amplitude of the secondary-side current will be changed and ASK is adopted for demodulation. The lower amplitude of the data signal is directly controlled to zero, which is easier for data demodulation [54]. However, switching at the primary side will cause an overcurrent in the secondary coil. A novel carrier width modulation (CWM) is proposed in [55]–[57] to switch at the zero-crossing point of the secondary-side current. The working principle of CWM is shown in Fig. 13; the active switch is controlled ON and OFF at the zero-crossing point of the primary-side voltage V_{p}. Owing to the phase relationship of V_{p} and secondary-side current I_{s}, the overcurrent in the secondary

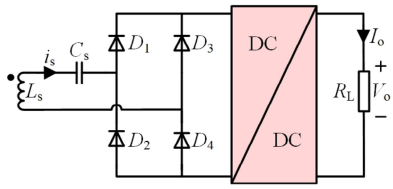

Fig. 14. Two-stage topology with a dc/dc converter for closed-loop control in [10].

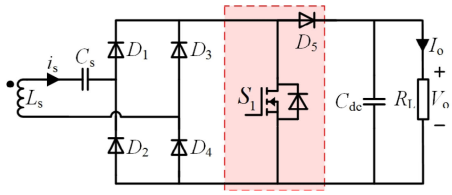

Fig. 15. Two-stage topology with a multiplexed inductor for closed-loop control in PC-SWPDT system in [48].

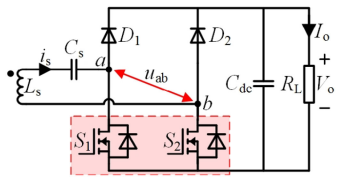

Fig. 16. Semibridgeless active rectifier proposed in [58] and [59] for closed-loop control.

side is eliminated and a 9.04 Mb/s forward communication is achieved. The CVO is also achieved in every fixed bit stream.

As shown in Fig. 4(c), LSK modulation is widely adopted in backward communication by controlling the switch S, which is connected with the output capacitor C_1 in series. However, this method results in overvoltage or overcurrent in the primary coil. Besides, the output current or voltage cannot be constant. The first solution is analyzing the relationship between the output power, PTE, and the switching capacitor C_0. The smaller value of C_0 is selected, the less impact on CVO can be obtained considering two main load ranges.

The second method utilizes a novel secondary-side topology and closed-loop control to maintain COC. As shown in Figs. 14 –16, three topologies have been employed in the PC-SWPDT system to achieve CVO or CCO. In [10], a Buck converter is added at the output side to achieve CVO or CCO when using ASK modulation by simply changing the input voltage of the inverter. As shown in Fig. 4(d), the duty cycle of the prestage dc/dc converter is changed according to the bit stream and the output voltage of the prestage boost converter can be changed. However, the PTE of the whole system may be lowered due to the introduction of the buck converter. As shown in Fig. 15, an inductor multiplexing method is adopted in [48] to combine the full-bridge rectifier and boost converter to achieve CVO. The passive components are reduced, leading to high power density and a high PTE. The backward communication is also achieved by simply changing the switching frequency of S_1. However, the extra switches still lower the power density and PTE of the original system that uses an uncontrolled full-bridge rectifier. In

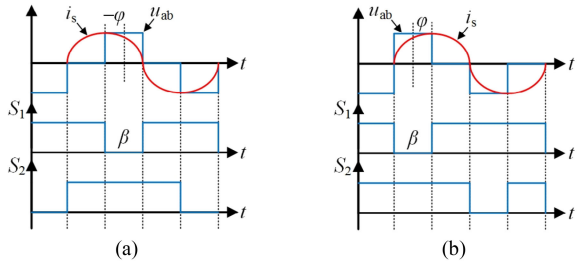

Fig. 17. Main working waveforms of S-BAR in (a) capacitive mode and (b) inductive mode.

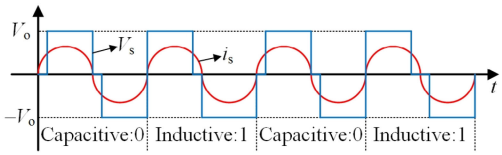

Fig. 18. Typical waveforms of S-BAR during constant bit stream 0101.

[58] and [59], a novel semibridgeless active rectifier (S-BAR) is proposed, as shown in Fig. 16. The CVO and CCO are achieved using phase shift control. The working principle of S-BAR and typical waveforms of S-BAR during constant bit stream 0101 are shown in Figs. 17 and 18. When the conduction angle of the rectifier is changed between capacitive and inductive modes, the phase of the primary-side current will be changed. By sampling the output current or voltage and using the PI controller, CCO and CVO are achieved. The backward communication is also achieved by the proposed dual-mode differential PSK (DDPSK) modulation and the interference from power carrier modulation is eliminated. However, ZVS can only be achieved when the inverter works under weak inductive mode. Thus, the backward data transfer cannot achieve ZVS all the time, leading to a low PTE. The three topologies can also be adopted to achieve CVO or CCO in forward communication, which enables the SWPDT system to achieve half-duplex communication [60].

B. Improvement of SNR

The cross talk from power transfer to data transfer mainly exists in fundamental and high-order harmonics parallel transmission systems, which utilize the fundamental component to transfer power and the high-order components to transfer data. The cross talk is mainly attributed to the following two factors. First, when the selected harmonic is designed to be zero or a certain value by changing the duty cycle or the phase shift angle of the inverter, the other order harmonics still exist, which have a significant impact on signal extraction. Second, in scenarios where two independent coils are employed to receive power and data signals, respectively, the cross coupling between power and data receiving coils could result in considerable cross talk.

To minimize the cross talk resulting from the first factor, SHEPWM can be adopted because the other order harmonics can be designed to be zero according to (4), but the calculation of conduction angles is difficult. To minimize the cross talk resulting from the second factor, the data receiving coil is designed to resonate with a capacitor at the selected harmonic

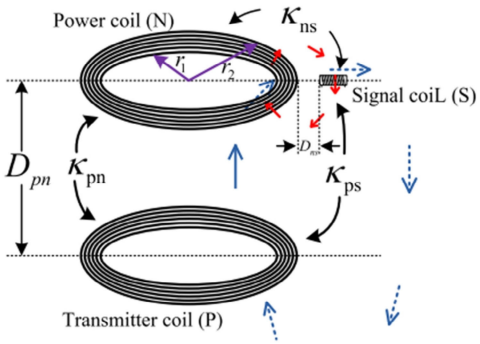

Fig. 19. Coil layout to minimize the cross talk from data transfer.

frequency with a high-quality factor. Thus, the amplitude of the selected harmonic which is employed for data transfer is much higher than the induced fundamental harmonic. Besides, the relative positions of the power and data receiving coils can be carefully designed to minimize the cross coupling. For example, the axis of the data receiving coil is perpendicular to the tangent of the power receiving coil in [47], as shown in Fig. 19. The cross coupling between power and data receiving coils can be neglected in this case.

C. Novel Modulation Method for High Data Rate and Low BER

In most SWPDT systems, ASK, FSK, and PSK modulation is adopted to transfer only one bit per time, which limits the data rate. Quadrature phase-shift keying (QPSK) is adopted in [61] to achieve forward communication at a high data rate. Two binary bits can be transmitted per time. The data rate is higher than 42 kb/s when the central switching frequency is only 110 kHz [62].

Sometimes, the SWPDT system may work in a strong coupling region. Qiu *et al.* [63] reveal that if the SWPDT system using LSK modulation and S/S compensation topology works in a strong coupling region, the data flipping phenomenon will arise. To overcome this disadvantage, the transmitter input voltage (sum of the voltage across transmitting coil and the voltage across primary compensation capacitor), rather than the voltage across transmitting coil, is adopted for demodulation. The data flipping phenomenon is eliminated by using this method, and very low BER is achieved. Reliable backward communication is achieved in the whole coupling range.

To the best of the authors' knowledge, the reported PC-SWPDT systems can only achieve half-duplex communication. This is unacceptable in applications such as spacecraft where ultralow delay is required. Hence, the SWPDT system that can transmit uplink and downlink data simultaneously is investigated.

III. HFDC-SWPDT System

Similar to PC-SWPDT, the cross talk both from data modulation and power transfer is analyzed in the HFDC-SWPDT system. The modeling and analysis method is illustrated in this

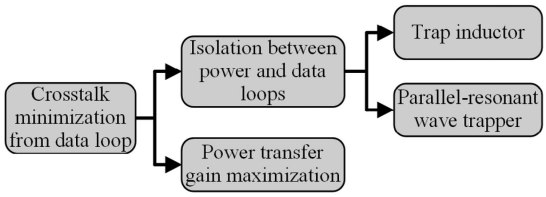

Fig. 20. Methods to minimize the cross talk from data transfer.

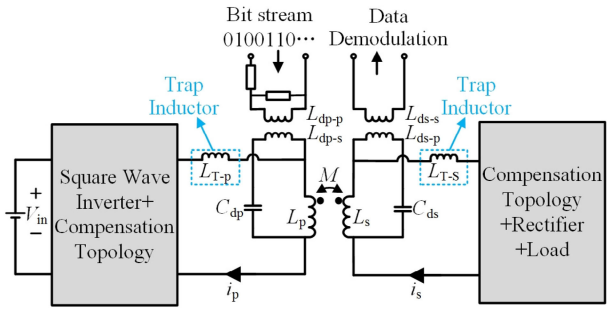

Fig. 21. Block diagram of the HFDC-SWPDT system using trap inductors.

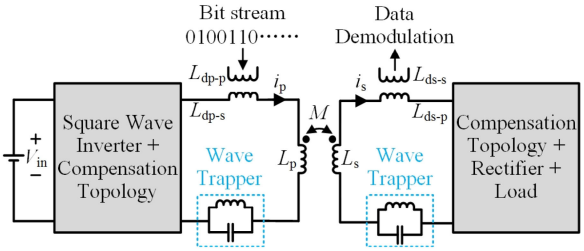

Fig. 22. Block diagram of the HFDC-SWPDT system using wave trappers.

section. Other special designs for achieving full-duplex and new modulation methods for high data rates are also introduced.

A. Crosstalk Minimization From Data Transfer

As shown in Fig. 20, two main methods to minimize the cross talk from data transfer have been proposed. The first method is to enhance the isolation between power and data loops. Adding extra passive components, i.e., trap inductors and wave trappers, is widely adopted in reported SWPDT systems. As shown in Fig. 21, the trap inductor is generally connected in series between the primary coupling coil and compensation topology [64]. The impedance of the trap inductor is high at the data carrier frequency. Hence, the trap inductor can be considered as an open circuit for the data carrier. Taking forward communication as an example, the data carrier will not flow into the circuit at the left hand of the trap inductor. A wave trapper is essentially a parallel resonance circuit that works as a notch filter. As shown in Fig. 22, the wave trapper is connected in series between the coupling coil and compensation topology [65]–[67]. The resonant frequency of the wave trapper is tuned at the data carrier frequency. Thus, the wave trapper acts as an open circuit for the data carrier. The isolation between data and power loops is achieved.

Power transfer gain maximization is the other method to minimize the cross talk from data transfer. Several methods, including adaptive frequency control and maximum power point tracking, have been proposed to increase output power and PTE of the WPT system and enhance noise immunity of the power transfer loop [68]–[70]. In fact, the data transfer power is less than 5 W in most HFDC-SWPDT systems. Compared with the transferred power which is generally as high as hundreds of watts, the impact of data transfer on PTE, CVO, or CCO characteristics can be neglected [71].

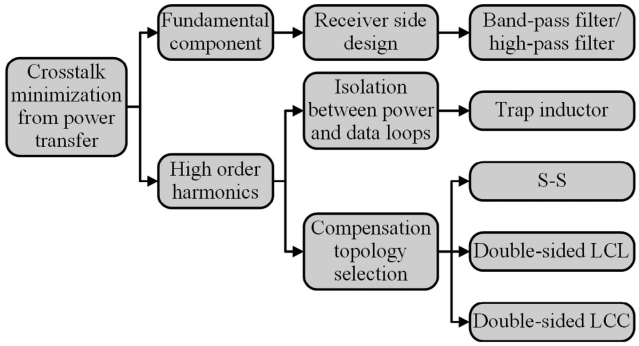

Fig. 23. Methods to minimize the cross talk from power transfer.

B. Improvement of SNR

Compared with the PC-SWPDT system, improvement of SNR is more important in the HFDC-SWPDT system. Two strategies to improve the SNR of an HFDC-SWPDT system have been proposed. The first strategy is to minimize the cross talk from power transfer. The second strategy is to maximize data channel gain.

Fig. 23 shows the methods to minimize the cross talk from power transfer. The cross talk from power transfer can be divided into two parts: fundamental component and high-order harmonics. The frequency of the fundamental component is generally one order lower than the frequency of the data carrier. Therefore, it is easy for the receiver to filter out the fundamental component using a band-pass or high-pass filter [64]. The high-order harmonics can be lowered by enhancing the isolation between power and data loops and selecting the optimal compensation topology. A trap inductor connected between data and power loops can be employed to achieve high impedance and isolate the two loops [64].

S–S, double-sided *LCC*, and double-sided *LCL* compensation topologies, as shown in Fig. 24, are compared in [72]. Taking forward communication as an example, u_{ab} can be regarded as the high-order harmonics resulting from the rectifier. S-S topology shows the worst high-frequency band-stop capability. *LCC* and *LCL* topologies perform better in cross-talk minimization owing to the high impedance of the series inductor and the low impedance of the parallel capacitor at high frequency. *LCL* topology shows the best high-frequency harmonic suppression performance because the primary (secondary) inductance L_p (L_s) equals L_1 (L_2). L_1 in *LCC* topology is less than L_1 in *LCL* topology because two series capacitors, C_{p2} and C_{s2}, are introduced. A larger L_1 (L_2) results in greater power loss. Hence, the PTE of *LCC* topology is generally higher than that of *LCL* topology. Taking high-order harmonic suppression capability

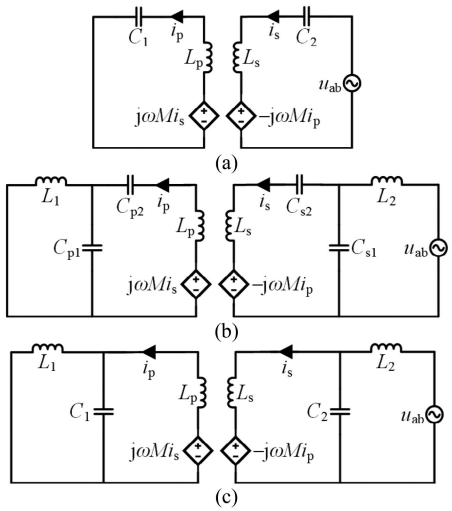

Fig. 24. Three symmetric compensation topologies used in full-duplex HFDC-SWPDT system. (a) S–S. (b) Double-sided *LCC*. (c) Double-sided *LCL* compensation topology.

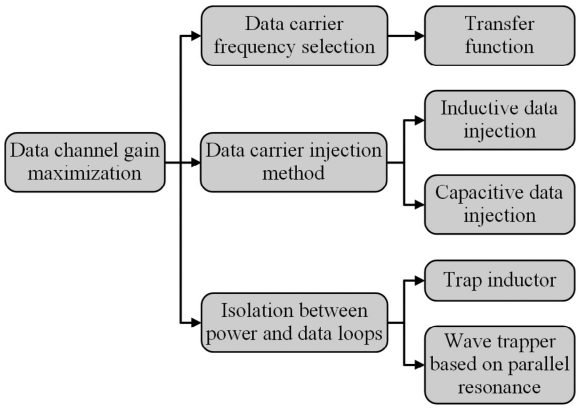

Fig. 25. Methods to maximize data channel gain.

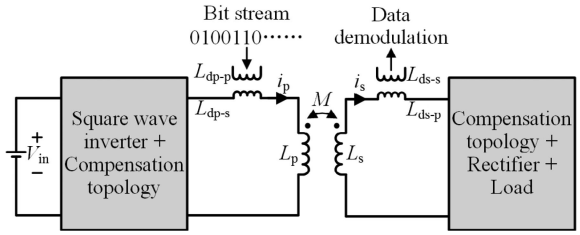

Fig. 26. Inductive-coupling-based HFDC-SWPDT system. The data carrier is injected and extracted using series transformers.

and system efficiency into consideration, double-sided *LCC* compensation topology is the optimal compensation topology.

Fig. 25 shows the methods to maximize data channel gain. The first method is to select the optimal data carrier frequency. The transfer function from a data transmitter to a data receiver is first established, based on which the highest channel gain can be obtained. Then, the optimal data carrier frequency can be selected [12], [65], [73].

The second method is to determine the best data carrier injection method. Figs. 26 and 27 show the circuit diagrams of inductive and capacitive injection. The data carrier is injected

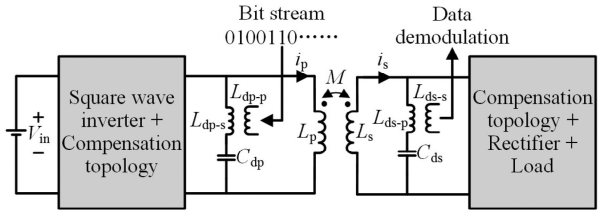

Fig. 27. Capacitive-coupling based HFDC-SWPDT system. The data carrier is injected and extracted using parallel transformers and capacitors.

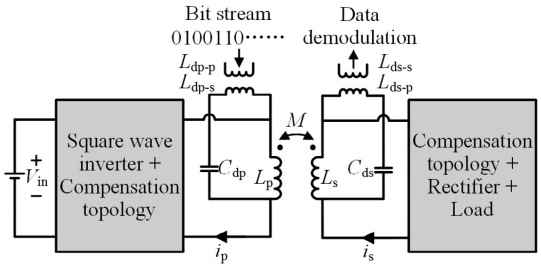

Fig. 28. Capacitive-coupling-based HFDC-SWPDT system with high SNR.

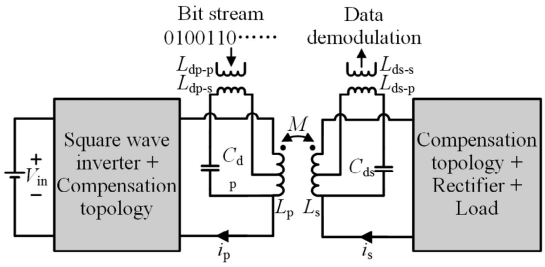

Fig. 29. Capacitive-coupling-based HFDC-SWPDT system with high data channel gain.

in the form of a high-frequency current in inductive injection. It is sensitive to the parameters of the passive components. By contrast, the data carrier is directly injected into the primary or secondary inductance in the form of voltage in capacitive injection. It is only sensitive to the value of the injection inductance [74]. In [75], the injection inductor $L_{\mathrm{dp\text{-}s}}$ is connected in series with a capacitance C_{dp}, as shown in Fig. 27, to achieve series resonance. However, $L_{\mathrm{dp\text{-}s}}$ only resonates with C_{dp}, resulting in a low channel gain. In [76], the primary and secondary coils L_{p} and L_{s}, as shown in Fig. 28, are multiplexed as injection inductors, which resonate with the whole compensation topology. Thus, a higher channel gain can be obtained. However, the cross talk from the power loop could be significant if the whole coupling coils are multiplexed as injection coils. To handle this problem, only parts of the coupling coils are multiplexed as injection inductors, as shown in Fig. 29. The turns ratio of the tapped coupler should be carefully designed to achieve high channel gain and high SNR [71].

Data channel gain also depends on the isolation between power and data loops. If the power and data signals are transferred through decoupled channels, the induced current in the power loop resulting from data transfer is nearly zero. As a consequence, the power loss of data transfer is minimized, and

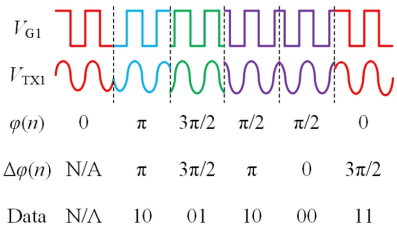

Fig. 30. Working principle of DQPSK modulation.

a high data channel gain is obtained. Therefore, the aforementioned isolation enhancement method, adding trap inductors and wave trappers, can be adopted to achieve a high channel gain.

C. Special Design for Full-Duplex

Different from the PC-SWPDT system, it is easy to achieve full-duplex using two different data carrier frequencies. For most full-duplex SWPDT systems, two main requirements should be maintained: first, backward and forward communication should achieve the same data rate and time delay with high SNR; second, the forward and backward data signals should be separately easily. First, in order to achieve full-duplex with high SNR, the transfer function method is adopted to obtain the bode diagram of the data channel gain–frequency plot and two frequency points with the same channel gain are selected as the data carrier frequency for forward and backward communication [65]. However, not only the amplitude–frequency characteristic but also the phase–frequency characteristic should also be paid attention to achieve the same time delay. The phase–frequency characteristic decides the time delay during data transfer. In [77], the two frequencies with the same phase delay and channel gain are selected to achieve the same time delay during full-duplex.

The isolation between two data carriers in full-duplex should also be designed specially. Similar to the wave trapper, the parallel-resonant circuit is added paralleled at the two receive sides to achieve bidirectional data carrier isolation in [66]. For most HFDC-SWPDT systems, the difference between two data carrier frequencies is larger than 1 MHz. Hence, it is simple to achieve isolation between bidirectional data carriers using a digital or analog band-pass filter [19], [71].

D. Novel Modulation Methods for High Data Rate and Low BER

Similar to the PC-SWPDT system, the QPSK can also be adopted for a high data rate. However, the conventional QPSK method may result in inaccurate problems and high dependence on the synchronism of the digital system. The differential quadrature phase-shift keying (DQPSK) is adopted and a novel analog demodulation circuit is proposed in [78]. Fig. 30 shows the working principle of DQPSK, the phase change between two adjacent symbols, namely, differential phase signals, are adopted to achieve more precise data modulation compared with the conventional QPSK.

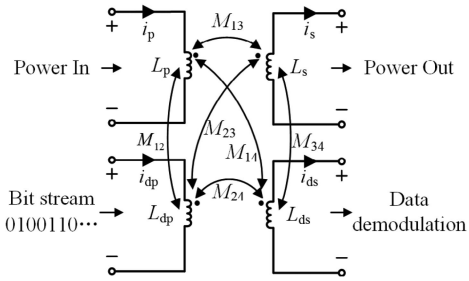

Fig. 31. Block diagram of MIC-SWPDT system with forward communication coils.

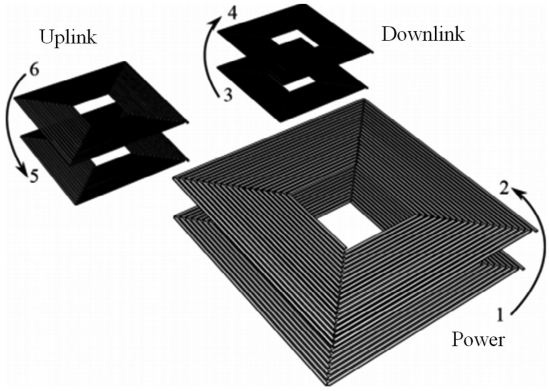

Fig. 32. Optimization design of coplanar coils to reduce cross coupling between power and data coils.

IV. MIC-SWPDT System

To simplify the passive component design and modulation method selection, the MIC-SWPDT is widely investigated. Different from the SWPDT system using a common channel, the bidirectional cross-talk minimization method is illustrated and compared in this section. The other special issues, including misalignment tolerance design and modulation method for low BER and high data rate, are also investigated.

A. Bidirectional Crosstalk Minimization

Taking two inductive channels SWPDT system as an example, the cross talk between power and data loops results from the cross coupling between the two coil pairs, as shown in Fig. 31. In the conventional hybrid couplers, which contain both power coils and data coils, the two or three coil pairs are placed in the same plane [79]–[83]. However, the cross coupling between data and power coils is considerable, especially in the case that the data coils are put near the power coils. In [26], the distance between the coplanar power and data coils is relatively large, as shown in Fig. 32. As a result, the mutual inductance M_{14} is small. However, the volume of the hybrid coupler is quite large.

To achieve zero cross coupling in theory and reduce the volume of the hybrid coupler, the first idea is to design the relative positions of power and data coils [27], [32], and [84]. Atluri and Ghovanloo [85] proposed the vertical coils, as shown in Fig. 33. The coils labeled by 1 and 2 are power transfer coils, and the coils labeled by 3 and 4 (5 and 6) are data coils for downlink (uplink) communication. Coils 1, 3, and 5 (2, 4,

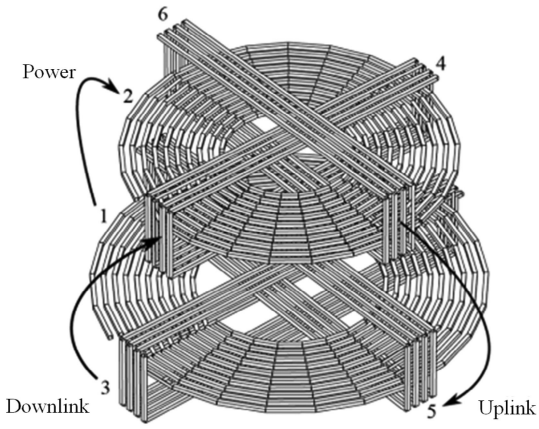

Fig. 33. Optimization design of vertical coils to reduce cross coupling between power and data coils with both uplink and downlink communication coils.

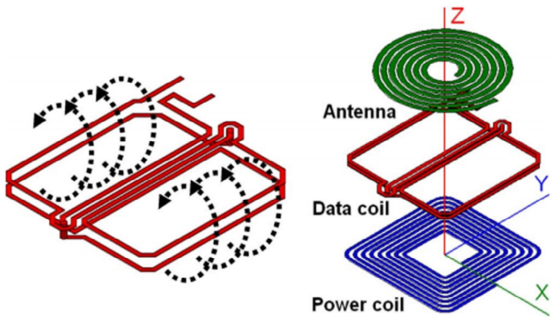

Fig. 34. Optimization design of Figure-8 type coils to reduce cross coupling between power and data coils.

and 6) are perpendicular to each other. Hence, the three coils are completely decoupled. The cross coupling between power and data coils is minimized to zero. However, the height of the vertical coils is increased, limiting its application in portable scenarios.

The second idea is to use multiple data coils. These data coils are carefully designed to make the sum of induced magnetic flux null. The Figure-8 coils shown in Fig. 34 are proposed in [86]. Two data coils are put in the same planar and wounded in the opposite direction. Therefore, the induced currents in the two coils are opposite in direction and identical in amplitude. The induced current in the Figure-8 coils is minimized to zero, and zero cross coupling is acquired. Barakat *et al.* proposed coexisting defected ground structure (DGS) resonators and Figure-8 inductors in [87], as shown in Fig. 35. The power coil (DGS resonator) and data coil (Figure-8 inductor) are put in the same plane. The two currents of a Figure-8 inductor loop are in opposite directions. Hence, the cross coupling between the Figure-8 inductor and DGS resonator is nearly zero as the Figure-8 inductor is placed symmetrically inside the DGS resonator. The electromagnetic simulation result indicates that the isolation between DGS and Figure-8 resonators is more than 37 dB.

Both DGS and Figure-8 coils are compensated by necessary capacitors to make the two inductor–capacitor networks resonate at the same frequency. Fig. 36 shows the equivalent circuit model of the coexisting DGS and Figure-8 resonant networks. Primary

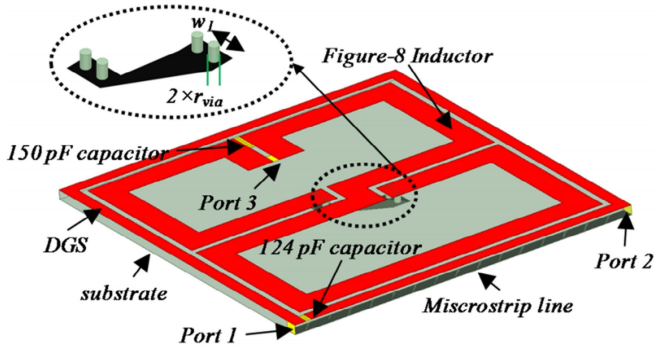

Fig. 35. Electromagnetic simulation model of coexisting DGS and Figure-8 type coils.

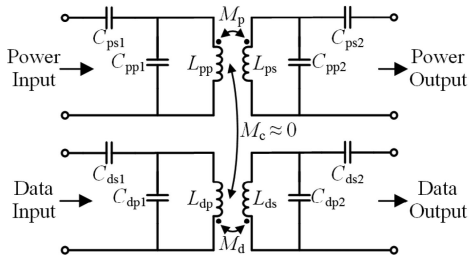

Fig. 36. Equivalent circuit model of coexisting DGS and Figure-8 type coils with compensation capacitors.

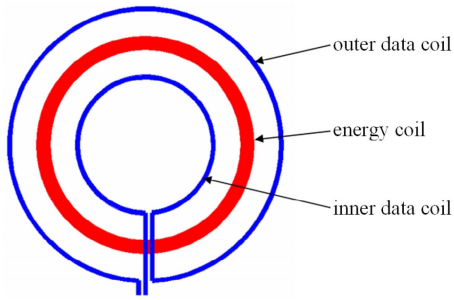

Fig. 37. Optimization design of coaxial coils to reduce cross coupling between power and data coils.

series–parallel secondary parallel–series (SP/PS) compensation topology is adopted. $C_{\rm ps1}$, $C_{\rm pp1}$, $C_{\rm ps2}$, and $C_{\rm pp2}$ are compensation capacitors in the power loop. $C_{\rm ds1}$, $C_{\rm dp1}$, $C_{\rm ds2}$, and $C_{\rm dp2}$ are compensation capacitors in data loop. The DGS resonator acts as a band-stop filter by setting the stop frequency as the data carrier frequency. Thus, a higher SNR can be acquired [88]. Owing to the flat design, the height and volume of the coexisting DGS resonators and Figure-8 inductors are reduced, making it very suitable for mobile device applications.

To reduce the coupler area, coaxial coils are widely utilized in WPT systems [89]–[91]. Following the same idea in Figure-8 coils, coaxial three coils are proposed in [92], as shown in Fig. 37. One of the three coaxial coils is utilized to transfer power, and the other two data coils (one inside the power coil and the other outside the power coil) are antiseries connected. The turns and radius ratio of the power and data coils and the distance between the inner and outer data coils are carefully designed. Then, zero cross coupling between data and power

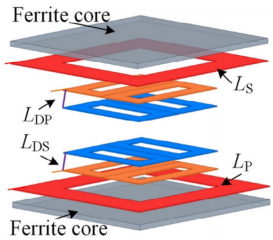

Fig. 38. Orthogonal DD coils designed for power and uplink data transfer.

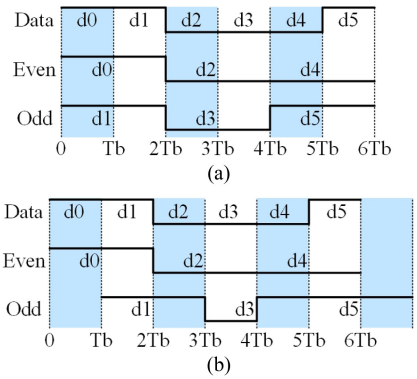

Fig. 39. Data stream using (a) QPSK and (b) OQPSK (di denotes one binary bit).

coils is achieved. The three coils are coaxial, leading to a reduced plane area, which is more suitable for portable applications.

As shown in Fig. 38, the planar square and orthogonal DD coils are utilized in [93]. The planar square coils are employed to transfer power, while the orthogonal DD coils are utilized to transmit data. The coils in different colors are decoupled from each other. Hence, the cross coupling between power and data coils is zero.

The second group is by adopting different carrier frequencies for power and data transfer. Similar to the HFDCI-SWPDT, the frequency difference between power and data carrier is selected as large as possible to avoid the cross talk. A 50 MHz and a 100 MHz frequency difference are selected in [87] to prevent the bidirectional cross talk. However, the harmonic voltage from the power loop is not considered in the reported literature.

B. Special Modulation Methods for High Data Rate and Low BER

Five carrier phase shift angles, 0°, ±90°, and ±180°, are employed in QPSK modulation. The phase shift angle of 180° is sensitive to the Gaussian noise. Thus, the offset quadrature phase-shift keying (OQPSK) is introduced in [26]. Fig. 39 shows the data streams using QPSK and OQPSK. The offset of T/2 between 2 bit streams is introduced to limit the phase shift angle between 0° and ±90°. This is optimum in terms of phase jitter immunity in the presence of additive Gaussian noise [94]. A novel demodulation circuit based on a square wave carrier is designed in [95] to achieve 8 Mb/s data rate with a 13.56 MHz carrier. It is more competitive than the conventional FSK and PSK modulation.

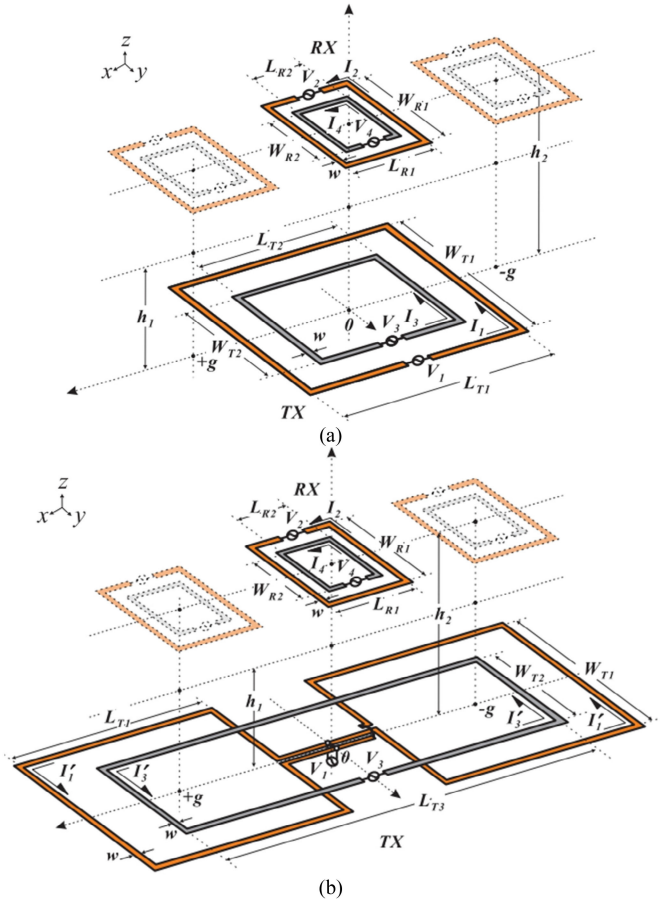

Fig. 40. Coil layout of SWPDT system. (a) Conventional coil layout. (b) Misalignment-insensitive coil layout in [25].

C. Misalignment-Tolerance Design

The second special issue in this section is antimisalignment performance. For wireless EV charging and online monitoring of animal behavior, the misalignment-tolerance performance is a requirement. However, the conventional EV charging system that consists of two coil pairs is placed in coaxial and shows weak antimisalignment characteristics, as shown in Fig. 40(a). Therefore, in [25], the longitudinally misalignment-intensive dynamic SWPDT system is proposed. A primary-side data coil in the shape of a long rail, as shown in Fig. 40(b), is adopted to achieve a high longitudinal antimisalignment performance. Also, in [96], to achieve online monitoring of the central neural system, cardiovascular functions, and neuropathological disorders, three orthogonal coils are adopted to achieve three-dimensional antimisalignment performance.

V. ICHC-SWPDT System

To fully utilize the parasitic parameters and combine the advantages of inductive and capacitive WPT, the ICHC-SWPDT is widely investigated in the reported literature. In this section, the methods for cross-talk minimization from data transfer and improvement of SNR are fully investigated. The misalignment-tolerance design and special modulation methods are also explored in this section.

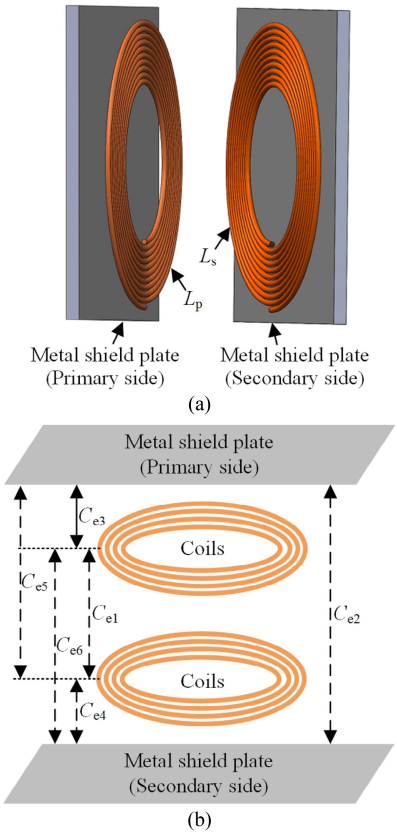

Fig. 41. Coupling structure of an ICHC-SWPDT system and its simplified model. (a) Coupling structure of a peer-to-peer ICHC-SWPDT system. (b) simplified model [28].

A. *Cross-Talk Minimization From Data Transfer*

ICHC-SWPDT systems can be divided into two groups. In the first group, the power and data are transferred via separate channels, and in the second group, the power and data are transferred via hybrid channels. Thus, the minimization from data transfer should be discussed separately.

Fig. 41(a) shows a typical coupling structure for the ICHC-SWPDT system that transfers power and data via separate channels [28]. The inductive channel is used to transfer power. The data are transferred through the electrical field generated by the capacitances of coils and metal shield plates, as shown in Fig. 41(b). The cross talk from data transfer to power transfer can be neglected due to the following two reasons. First, in most cases, the transferred power is at least an order higher than the power consumed by the data circuit. Second, the parasitic capacitances of coils and metal plates are very small, resulting in very large impedances. Hence, the induced current in the data circuit resulting from power transfer is very small.

The second group of the ICHC-SWPDT system is realized by utilizing a hybrid field. Similar to the PC-SWPDT system, binary FSK modulation can also be employed in the ICHC-SWPDT system for forward communication. However, the CVO or CCO characteristic and PTE could be impaired by the resonant frequency deviation resulting from the introduction of FSK. Following the idea in [97], the equivalent model of the

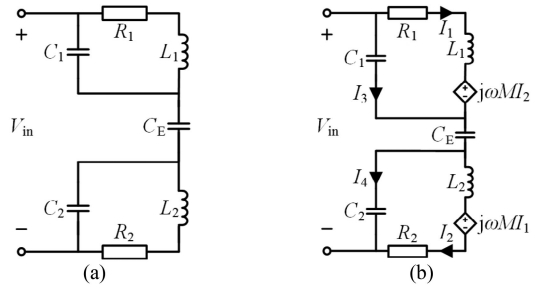

Fig. 42. (a) Equivalent circuit of ICHC-SWPDT system. (b) Equivalent circuit replacing the mutual inductance (M_s) between inner and outer coils with CCVS model.

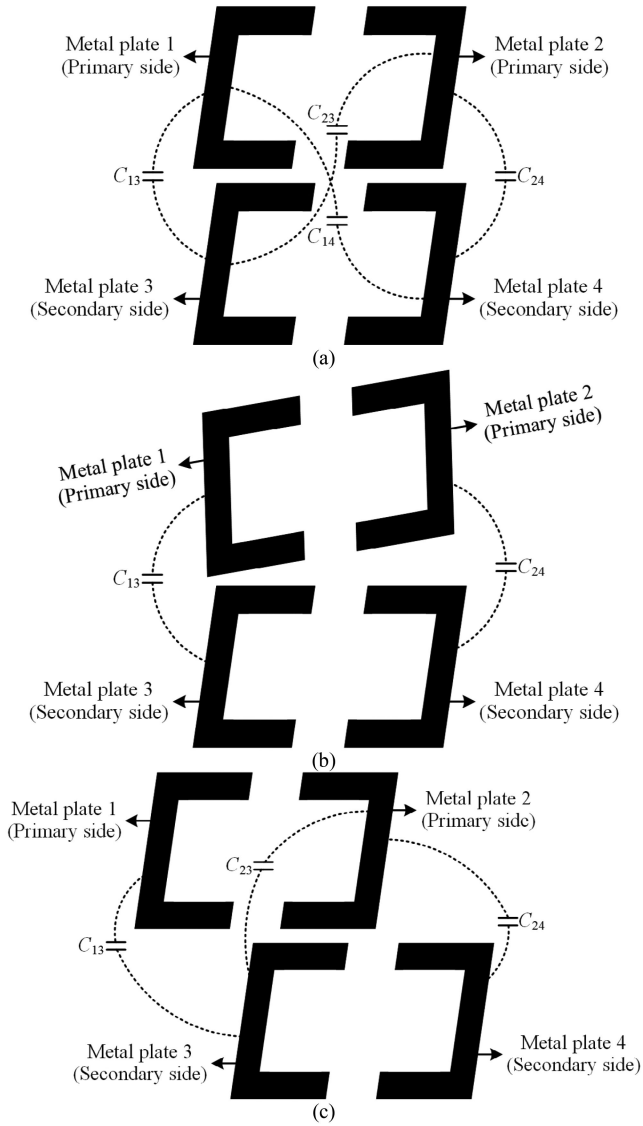

Fig. 43. Dual-frequency MCCs in (a) aligned, (b) angularly misaligned, and (c) laterally misaligned cases.

ICHC-SWPDT system considering capacitance and inductance can be obtained. The current control voltage source (CCVS) model, as shown in Fig. 42, is utilized to replace the mutual inductance between the inner and outer coils. Based on the proposed model, four resonant frequency points are calculated and

TABLE I
SUMMARIZED REPORTED AND PROPOSED SWPDT RESEARCH WORKS

Type	Reference	CCO/ CVO	Power level	PTE	Transfer distance/ Coupling factor (k)	Data rate	BER	Bidirectional/ unidirectional	Time delay
PC-SWPDT	[10]	NR	700W	92%	15-25mm	20kbps	15%	U	3μs
	[16]	CCO	3W	50%	0-120mm	15kbps	NA	U	NA
	[18]	NR	3W	58.1%	160mm	3.39Mbps	NA	U	NA
	[32]	CCO	1.568W	62.2%	7mm	3.57/5kbps	9/7%	B	NA
	[33]	NR	150mW	54%	8mm	170kbps	100ppm	U	NA
	[46]	CCO	5.5W	85%	50mm	20kbps	NA	U	NA
	[47]	NR	NA	84%	25mm	6kbps	NA	U	NA
	[48]	CVO	30W	81%	k=0.29	5/10kbps	NA	B	NA
	[51]	NR	NA	85%	25mm	6kbps	NA	U	NA
	[53]	CCO	30W	92%	30mm	NA	NA	U	NA
	[54]	NR	10W	30%	300mm	500kbps	NA	B	NA
	[55]	NR	55mW	NA	25mm	1.66Mbps	NA	U	NA
	[62]	NR	NA	81%	10-50mm	42kbps	0.1%	B	NA
	[99]	CVO	44mW	39%	10mm	50kbps	NA	U	NA
HFDC-SWPDT	[12]	CVO	500W	86%	75mm	20kbps	NA	B	NA
	[19]	CCO	100W	90.5%	NA	119kbps	NA	U	9.4μs
	[21]	NR	30W	86%	k=0.536	200kbps	0	B	NA
	[31]	NR	354W	51.977%	100cm	19.2kbps	11.6%	B	NA
	[43]	NR	2W	NA	28mm	100kbps	NA	U	NA
	[64]	CCO	290.1W	90.5%	47-267mm	150kbps	NA	B	5.2μs
	[65]	CVO	258W	83.2%	2-7mm	19.2kbps	NA	B	NA
	[66]	NR	600W	86%	NA	80kbps	NA	B	NA
	[67]	NR	NA	NA	NA	NA	NA	U	NA
	[71]	CCO	300W	90.1%	60mm	500kbps	NA	B	2μs
	[73]	NR	22.5W	70%	NA	115.2kbps	NA	U	NA
	[75]	NR	100W	84%	1mm	200kbps	0	B	NA
	[76]	CCO	30W	NA	10mm	80kbps	NA	U	NA
	[78]	CCO	3.3kW	NA	k=0.184	64kbps	NA	B	31.25μs
	[100]	CCO	19.88W	85%	20mm	1.25Mbps	NA	B	NA
MIC-SWPDT	[26]	NR	10.2mW	61%	5mm	4.16Mbps	2×10^{-8}	B	NA
	[27]	NR	58mW	NA	9mm	2.083Mbps	0	U	NA
	[33]	NR	1kW	NA	30mm	NA	NA	B	NA
	[93]	CVO	122W	87%	20mm	19.2kbps	NA	U	NA
	[101]	CVO	180W	90%	20mm	19.2kbps	NA	U	NA
ICHC-SWPDT	[28]	NA	40W	79.6%	50mm	230kbps	0	U	NA

the lowest two of those are selected for the series *LC* resonator. Therefore, the dual-band resonant topology is achieved and the cross talk from data modulation is minimized. However, only the capacitance formed by the primary and secondary metal plate is considered in the CCVS model, and the other parasitic capacitances are not considered in [29].

B. Improvement of SNR

In ICHC-SWPDT systems where the power and data are transferred through hybrid channels, the fundamental component of the power signal is generally employed for data transfer. In such systems, improvement of SNR is seldom investigated. Improvement of SNR is more important for ICHC-SWPDT systems where the power and data are transferred through separate channels. Two methods can be employed to improve the SNR. The first method is to minimize the cross talk from power transfer. The second method is to maximize the data channel gain.

The voltage difference between the primary and secondary resonant circuits is regarded as the interference resulting from power transfer [28]. To minimize the interference, the mutual inductance should be high, while the primary and secondary inductances and the operating frequency of the power circuit should be small. Although the interference resulting from high-order voltage harmonics generated by the inverter and rectifier is not analyzed in related literature, it can be analyzed using the method employed in [64], [75], and [76] to obtain a higher SNR.

To maximize the data channel gain, the transfer function should be first derived, followed by parameter optimization. In [98], the transfer function from data input voltage to data output voltage is derived considering the impedances of compensation capacitors and coupling inductors. Then, a high-frequency data carrier is chosen, and a high data transfer gain is achieved.

TABLE II
ADVANTAGES, DISADVANTAGES, AND APPLICATIONS OF PC-SWPDT, HFDC-SWPDT, MIC-SWPDT, AND ICHC-SWPDT SYSTEMS

Type	Advantages	Disadvantages	Applications
PC-SWPDT	1. No or few extra passive and active components are needed 2. No extra data carrier generation devices 3. Data demodulation is easy	1. CCO or CVO characteristic could be broken 2. Low power level and PTE 3. Low data rate 4. Complicated modulation method to maintain CCO or CVO 5. Half-duplex telemetry	Low power applications such as aerospace, medical implants, consumer electronics, and robotic arm joints
HFDC-SWPDT	1. High SNR and data rate 2. High power level and PTE 3. Simple modulation and demodulation method 4. Full-duplex telemetry can be achieved	1. Too much extra passive components for high data rate and SNR 2. Extra data carrier injection and extraction devices are needed	High power and high data rate applications such as vehicle charging
MIC-SWPDT	1. High power level and PTE 2. High SNR and data rate 3. Simple modulation and demodulation method 4. Full-duplex telemetry can be achieved	1. Complex magnetic coupler design for crosstalk minimization 2. Extra coil pair for data transfer results in large volume	Wide power level and high data rate applications such as vehicle charging
ICHC-SWPDT	1. The same as HFDC-SWPDT system when extra devices are employed to generate data carrier 2. The same as PC-SWPDT system when the power signal is directly modulated for data transfer 3. Difficult in system modeling and analysis		Low power level application such as Implantable medical or large power transfer level with metal shields

C. Misalignment-Tolerance Design

ICHC-SWPDT system is widely adopted in implanted medical applications, where reliable communication and excellent misalignment tolerance are required. The dual-frequency mixed-coupling coil (MCC) that combines two coils and four metal plates for SWPDT is proposed in [29] to achieve better lateral and angular misalignment tolerance. As shown in Fig. 43(a), the four metal plates form four capacitances, i.e., C_{12}, C_{14}, C_{13}, and C_{24}. When angular misalignment arises, as shown in Fig. 43(b), the distance between the metal plates is not even. C_{24} decreases and C_{13} increases, making the overall electrical field approximately unchanged. When lateral misalignment arises, as shown in Fig. 43(c), C_{13} and C_{24} decrease significantly, but C_{23} increases considerably. The overall electrical field remains nearly unchanged. Compared with the traditional printed spiral coil systems, MCC reduces the decline rate of S_{21} by 26.1% and 78.1% at 35 mm lateral and 90° angular misalignment.

D. Novel Modulation Methods for High Data Rate and Low BER

For the modulation and demodulation method issue, similar to the PC-SWPDT, the widely adopted dual-band topology is designed in [28] to achieve a 2FSK modulation. In [29], the ASK modulation is adopted to achieve half-duplex. Since the reported literature for ICHC-SWPDT is very few, there is no more modulation methods have been adopted to achieve SWPDT. But from the eyes of the authors, if the mixed coupling field analysis is adopted to achieve simultaneous power and data transfer, the mentioned data modulation method in PC-SWPDT can also be adopted to achieve forward and backward communication. On the contrary, if the independent coupling field analysis method is adopted, the same modulation method mentioned in the HFDC-SWPDT system can be adopted to achieve full-duplex.

VI. COMPARISON OF DIFFERENT TYPES OF SWPDT SYSTEMS

The main power transfer indices (power level, PTE, CCO or CVO characteristic, transfer distance or coupling factor k) and key data transfer indices (data rate, BER, bidirectional or unidirectional communication, and time delay) of the reported SWPDT systems are tabulated in Table I. U and B represent the unidirectional and bidirectional data transfer, respectively. NA and NR stand for not available and not realized, respectively. High power and high data rate can be achieved by HFDC-SWPDT and MIC-SWPDT systems. In contrast, the PC-SWPDT system shows moderate performance in power level and data rate, which is dependent on the switching frequency of the active components in the SWPDT system.

Table II summarizes the advantages, disadvantages, and applications of PC-SWPDT, HFDC-SWPDT, MIC-SWPDT, and ICHC-SWPDT systems. In the PC-SWPDT system, the power signal is multiplexed as the data signal. No extra passive component is required for data transfer. Only a few active components are added to the original WPT system resulting in little volume increase. The power signal in the PC-SWPDT system also acts as a data signal. Hence, the demodulation is much easier than the HFDC-SWPDT system, where the power of data transfer is very low. However, modulating the power signal for data transfer will break the CVO or CCO characteristic of the original WPT system. Several novel modulation methods and topologies such as SHEPWM modulation and dual-band compensation topology have been proposed to maintain CVO or CCO characteristics,

but the design of analog/digital controller and topology will be much more complicated.

Compared with the PC-SWPDT system, the HFDC-SWPDT system can achieve high power and high data rate simultaneously. Simple ASK, FSK, and PSK can be adopted to achieve a high data rate owing to a high data carrier frequency. Full-duplex telemetry can also be realized in the HFDC-SWPDT system. However, to transfer power and data through a common coil pair, several extra passive components are required to make up wave trappers and achieve high SNR and high data rate. In return, the cost and volume of the whole SWPDT system are increased. In addition, extra devices to generate data carriers also increase the system cost.

MIC-SWPDT system is able to achieve both high power and high data rate as well. Compared with the HFDC-SWPDT system, no extra passive component is needed for high SNR. Hence, the MIC-SWPDT system outperforms the HFDC-SWPDT system in volume and cost. However, the magnetic coupler should be designed carefully to achieve nearly zero cross-coupling between power and data coils, which prolongs the design process. What is worse, some types of coils, such as the vertical type coils, show poor misalignment tolerance and low power density. MIC-SWPDT system is mainly adopted in high power applications with low requirements on volume (for example, high power vehicle charging) or low power applications with high requirements on volume (for example, medical implants).

ICHC-SWPDT system is widely employed in medical implants. In the ICHC-SWPDT system, data can be transmitted by directly modulating power signals or using extra devices to generate the data carrier signal. As a result, the advantages and disadvantages of these two kinds of ICHC-SWPDT systems are the same as PC-SWPDT and HFDC-SWPDT systems, respectively. If the parasitic capacitance of the ICHC-SWPDT system is taken into consideration, the modeling and analysis of the ICHC-SWPDT system will be much more complicated. Fortunately, researchers in [28] and [29] have proposed two modeling and analysis methods that can be adopted in future studies.

VII. Conclusion

SWPDT has become widely used nowadays to achieve real-time control and online monitoring. This article presents a comprehensive review of the state-of-the-art SWPDT techniques. In terms of classification based on the type and number of channels and data carrier generation method, the SWPDT system is divided into PC-SWPDT, HFDC-SWPDT, MIC-SWPDT, and ICHC-SWPDT according to the channel types and data carrier generation method. Two main issues, including minimization cross talk from data transfer to power transfer and maximization of SNR, are talked about, and the corresponding solutions are given in the mentioned classification. Other special issues, including the novel modulation method and the antimisalignment, are also investigated. However, the reported SWPDT system still suffers from the following problems.

First, the switching noise of the semiconductor devices has a great influence on the SNR. Sending and receiving data during the nonswitching period can alleviate the impact of switching noise, but in return, the data rate is limited by switching frequency resulting in a low data rate. Therefore, optimization design to minimize the interference from switching noise should be deeply investigated in the future.

Second, the reported research works only achieve point-to-point communication and fixed bitstream transmission. When multiple receivers need to communicate, multiple-node communication is required and the communication protocol should be designed.

Third, some new techniques to achieve high SNR should be considered, such as the orthogonal frequency-division multiplexing adopted in wireless communication in [102]–[104] can be adopted in HFDC-SWPDT systems in the future to achieve naturally cross-talk minimization from power transfer, which can simplify the passive components design procedure in the reported literature.

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