Parallel Fixed Switching Frequency CRM and DCM Boost PFC Converter With High Power Factor

Kai Yao, *Member, IEEE*, Jiazhen Li, Fanguang Shao, and Bo Zhang

***Abstract*—Critical conduction mode (CRM) or discontinuous conduction mode (DCM) boost power factor correction (PFC) converter is widely used in low power applications for its advantages of zero-current turn-ON of the switch, no reverse recovery in diode, and simple control. The input current of fixed switching frequency control CRM boost PFC converter and the input current of constant duty-cycle control DCM boost PFC converter mainly contain third harmonic. Moreover, the phase of the third harmonics is opposite. This article proposes a harmonic elimination parallel control to connect these two converters in parallel. The input current third harmonic of the parallel converter can be eliminated completely so as to improve the PF to nearly unity in the whole input voltage range. This parallel method is an interesting way to extend power, and is different from the existing method of parallel DCM boost PFC converter or parallel CRM boost PFC converter. The experimental results verify the accuracy of the theoretical analysis.**

***Index Terms*—Boost, critical conduction mode (CRM), discontinuous conduction mode (DCM), harmonic elimination parallel (HEP) control, power factor correction (PFC).**

I. Introduction

For the improvement of grid power quality and the reduction of line current distortion, active power factor correction (PFC) is necessary in ac–dc conversion. Many topologies and control methods have been put forward for low total harmonics distortion and high power factor (PF) [1]–[3]. Among all kinds of power electronics circuit topologies, the boost converter is widely employed in commercial power supplies because of many advantages [4]–[6]. Based on whether the inductor current is continuous, the converter is divided into three operation modes: continuous conduction mode (CCM), critical conduction mode (CRM), and discontinuous conduction mode (DCM).

In low power applications, boost PFC converters usually operate in DCM mode or CRM mode due to many merits, such as zero-current turn-ON of the switch, no reverse recovery in diode, and simple control [7]–[13]. Whereas the input current of traditional constant duty-cycle (CDC) DCM boost PFC converter is distorted by the third harmonic with the phase difference of 180° from the fundamental one, especially at high input voltages. Theoretically, the unity PF of a DCM boost PFC converter can be achieved by the variable duty-cycle (VDC) control scheme [14], [15]. However, due to DCM, whether with CDC or VDC, there is always a period of zero inductor current in switching cycles, leading to a useless period in the whole switching cycle of the power transmission. As a result, the peak value and the root-mean-square (RMS) value of the inductor current as well as the power device current are large.

For CRM boost PFC converter, the power transmits in the whole switching cycle and the peak value and the RMS value of the inductor current as well as the power device current can be decreased, compared with that of DCM. However, with traditional constant on-time (COT) control, the switching frequency varies in a line cycle and the variation range increases with the increase of the RMS input voltage. Thus, the conducted EMI of a CRM boost PFC converter distributes in a wide frequency range, and finding the worst spectrum by repetitive measurements or interactive calculations under different input voltage and load conditions are time-consuming [16]–[18].

Generally, the power level of DCM or CRM boost PFC converter can be extended without sacrificing the advantages of the single-phase converter by paralleling multiple converters. As far as two channels are concerned, it is natural to have the following parallel architecture, i.e., DCM and DCM, VDCDCM and VDCDCM, CRM and CRM.

The performances comparison of the above-mentioned three parallel converters is given in Table I. It can be noticed that DCM boost PFC converter has fixed switching frequency and is easy to be paralleled. However, the peak current is high and the PF is low [19], [20]. As an improvement of parallel DCM and DCM, VDCDCM and VDCDCM can achieve a high PF and is easy to be interleaved, but the peak current is still high.

Compared with parallel DCM boost PFC converter, parallel CRM one can achieve a full usage rate of switching cycle and lower peak current envelope; however, the switching frequency is variable during line cycle. A lot of in-depth research on the control and performance optimization of interleaved parallel CRM boost PFC converter has been presented in [21]–[30]. Most of them are to deal with the challenge of interleaved parallel control caused by the continuous change of switching frequency. How to achieve accurate phase shift between each other in two-channels and multi-channels [21]–[24]? How does the open-loop mode ensure the current balance between circuits and the stable operation of CRM without falling into DCM or CCM [25]? How to compensate the conduction time of the

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TABLE I
PERFORMANCES OF THREE PARALLEL CONVERTERS

Parallel converter	Channel	Switching frequency	Usage rate of switching cycle	Peak current envelope	PF	Controllability of interleaving	Design complexity of magnetic components	Referenc es
DCM&DCM	DCM channel	Fixed	Low	Largest	Low	Easy	Simple	[19],[20]
	DCM channel	Fixed	Low	Largest				
VDCDCM& VDCDCM	DCM channel	Fixed	Low	Larger	High	Medium	Simple	
	DCM channel	Fixed	Low	Larger				
CRM&CRM	CRM channel	Variable	Full	Large	High	Difficult	Complex	[21]-[30]
	CRM channel	Variable	Full	Large				
HEP CRM&DCM	CRM channel	Fixed	Full	Large	High	Medium	Simple	
	DCM channel	Fixed	Low	Largest				

slave converter to improve the current distortion [26]? When the duty cycle of open-loop synchronous shutdown voltage mode control is lower than 0.5, the current of the slave converter will diverge due to frequency variation [27]. Whether the master–slave allocation of the converter can be determined adaptively so that the open-loop interleaving mode can also be adopted for voltage-type CRM control [28]? The closed-loop response of phase-shift disturbance is slow by using the closed-loop mode of phase-locked loop, low-pass filter, and *RC* compensation network [29]. How to carry out periodic phase-shift control on the slave converter to improve the dynamic response and solve the phase-shift error and non-CRM operation problems caused by inductance mismatch between the two channels [30]?

It is not difficult to find that the root of the problem lies in the frequency variation. To solve it, a certain control must be adopted to make CRM converter work at fixed frequency. This is likely to reduce the input PF and increase the harmonics. Obviously, it will not help if another fixed frequency CRM converter is connected in parallel. However, if another DCM converter is connected in parallel, what is the harmonic relationship between the two channels? Is there an appropriate control method to offset the main harmonics of the two channels?

In this article, a parallel FSF CRM and DCM boost PFC converter (FSFCRM&DCM) is studied. By analyzing the harmonic currents of two channels, we found that the third harmonic phases of two channels are opposite, and the amplitudes are related to the output power, input voltage, and output voltage of the corresponding channel, but the law is different. Then, a harmonic elimination parallel (HEP) control method is proposed to completely eliminate the third harmonic of the input current by adjusting the power distribution between the two channels under different input voltages. As a result, the converter achieves high PF and the switching frequency of both channels can be kept fixed in a half-line cycle, respectively.

The previous studies focused on the parallel connection of two or more CRM converters, focusing on overcoming the difficulties caused by frequency variation in line cycles. The work in this article studies the parallel connection of CRM and DCM converter, and solves the root problem of frequency variation in line cycle while maintaining a high PF, which is different from the previous work. The rest of this article is organized as follows. Section II derives the principle of FSF control, analyzes the input current harmonics of two channels, and discusses the optimal power distribution to eliminate third harmonic completely. In Section III, the control circuit of HEP is designed and the input current and PF are analyzed. A 120-W prototype has been built and tested, and the experimental results are presented in Section IV Finally, Section V concludes this article.

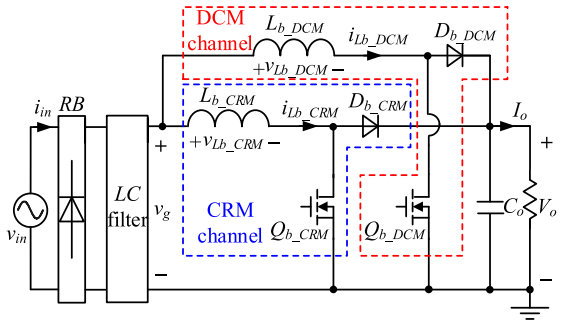

Fig. 1. Main circuit of FSFCRM&DCM.

II. OPERATION PRINCIPLE OF FSFCRM&DCM

The main circuit of FSFCRM&DCM is shown in Fig. 1. One channel (hereafter referred to as CRM channel) is operating in FSF CRM mode, and the other channel (hereafter referred to as DCM channel) is operating in CDC DCM mode.

Assuming the input voltage as a purely sinusoidal wave, the input voltage is expressed as follows:

$$v_{in} = V_m \sin \omega t \tag{1}$$

where V_m and ω are the amplitude and angular frequency of the input voltage, respectively.

In Fig. 1, i_{LB_DCM} and i_{LB_CRM} represent the inductor current of two branches in the process of converter operation, which includes the high-frequency component of switching signal and the low-frequency component of twice line frequency. However, i_{in_DCM} and i_{in_CRM} represent the average value of inductor current in each switching cycle, that is, the low-frequency component. Assuming that the filter can completely remove the high-frequency component, the input current i_{in} is the sum of i_{in_DCM} and i_{in_CRM}.

A. Principle of FSF Control and CRM Channel Harmonics Analysis

As shown in Fig. 2, the inductor current peak value of CRM channel is

$$i_{Lb\_CRM\_pk} = \frac{V_m \left|\sin \omega t\right|}{L_{b\_CRM}} t_{on\_CRM} \tag{2}$$

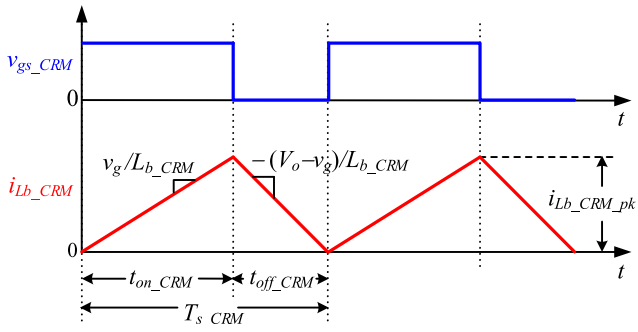

Fig. 2. Inductor current waveform of CRM channel.

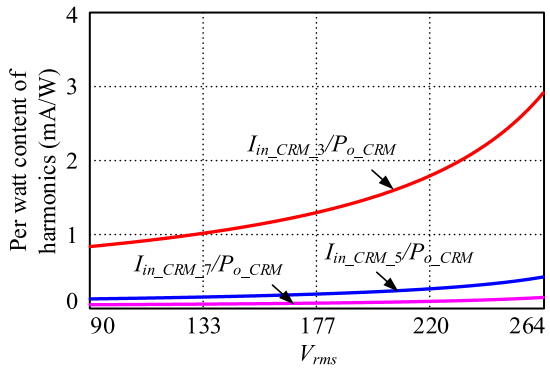

Fig. 3. Calculated third, fifth, and seventh harmonic curves of CRM channel average input current.

where L_{b_CRM} is the inductance value and t_{on_CRM} is the on-time, of the CRM channel, respectively.

The average input current of CRM channel is

$$i_{in\_CRM} = \frac{V_m \sin \omega t}{2L_{b\_CRM}} t_{on\_CRM}. \tag{3}$$

The switching frequency of CRM channel is calculated as follows:

$$f_{s\_CRM} = \frac{1}{t_{on\_CRM}} \frac{V_o - V_m |\sin \omega t|}{V_o}. \tag{4}$$

It can be observed from (4), if t_{on_CRM} varies as in (5), the switching frequency during a line cycle will be fixed.

$$t_{on\_CRM} = T_{s\_CRM} \left(1 - \frac{V_m}{V_o} |\sin \omega t|\right) \tag{5}$$

where T_{s_CRM} is an undetermined coefficient that will be calculated afterward.

Based on the power balance, (6) can be obtained from (1), (3), and (5)

$$T_{s\_CRM} = \frac{2P_{o\_CRM} L_{b\_CRM}}{V_m^2 \left(1/2 - 4V_m/3\pi V_o\right)} \tag{6}$$

where P_{o_CRM} is the output power of CRM channel.

Naturally, from (3), (5), and (6), the average input current of CRM channel is

$$i_{in\_CRM} = \frac{i_{Lb\_CRM\_pk}}{2} = \frac{P_{o\_CRM} \sin \omega t}{V_m \left(1/2 - 4V_m/3\pi V_o\right)} \left(1 - \frac{V_m}{V_o} |\sin \omega t|\right). \tag{7}$$

By Fourier analysis, the harmonics of CRM channel average input current is

$$i_{in\_CRM} = \frac{2P_{o\_CRM}}{V_m} sin\omega t + \sum_{n=3,5,\ldots} \frac{8P_{o\_CRM}}{(n^3-4n)(\pi V_o/2-4V_m/3)} sinn\omega t. \tag{8}$$

The rated voltage of power grids in different countries is not the same, such as 110 VAC/120 VAC and 220 VAC/230 VAC. Considering about 20% of the power grid fluctuation margin, 90–264 VAC is selected as the input voltage range. Thus, the design will be more general and universal. Because the output voltage is constant, the relation curves between the per-watt harmonics and RMS input voltage are depicted in Fig. 3, where the higher harmonics are ignored because of the very low value. In this way, it is more convenient to show the harmonic current under different input voltages. Obviously, all the harmonic contents increase with the increase of input voltage, and the third harmonic is dominant.

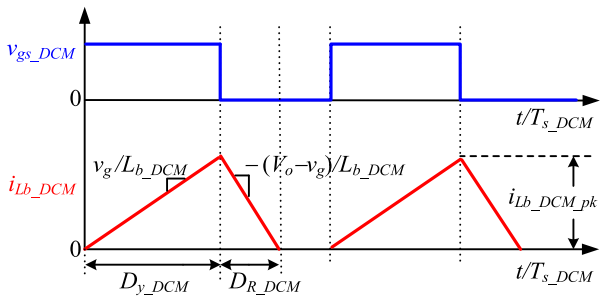

Fig. 4. Inductor current waveform of DCM channel.

B. DCM Channel Harmonics Analysis

As shown in Fig. 4, the inductor current peak value of DCM channel is

$$i_{Lb\_DCM\_pk} = \frac{D_{y\_DCM} V_m |\sin \omega t|}{L_{b\_DCM} f_{s\_DCM}} \tag{9}$$

where D_{y_DCM}, L_{b_DCM}, and f_{s_DCM} are the duty-cycle, inductance value, and switching frequency of DCM channel, respectively.

From Fig. 4, the volt-second balance yields the duty-cycle corresponding to the freewheeling falling period of inductor current

$$D_{R\_DCM} = \frac{V_m |\sin \omega t|}{V_o - V_m |\sin \omega t|} D_{y\_DCM}. \tag{10}$$

The average input current of DCM channel is expressed as follows:

$$i_{in\_DCM} = \frac{V_m D_{y\_DCM}^2}{2L_{b\_DCM} f_{s\_DCM}} \frac{\sin \omega t}{1 - V_m |\sin \omega t| / V_o}. \tag{11}$$

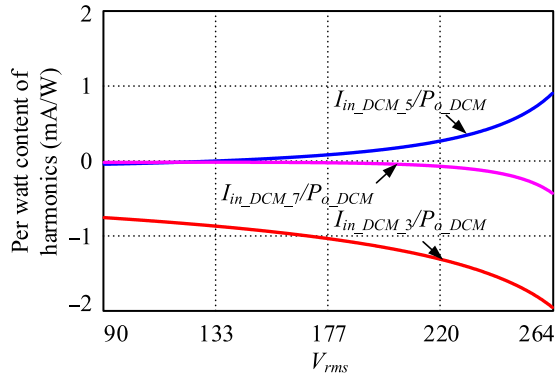

Fig. 5. Calculated third, fifth, and seventh harmonic curves of DCM channel average input current.

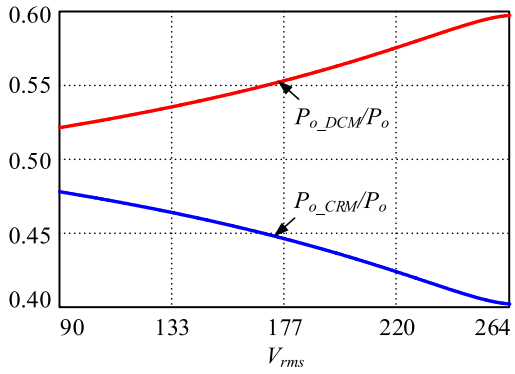

Fig. 6. Power distribution of two channels.

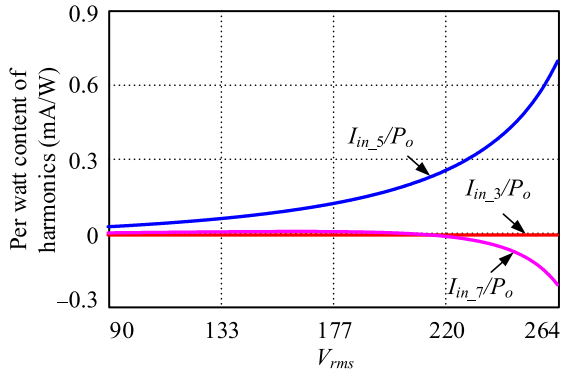

Fig. 7. Input current third, fifth, and seventh harmonic curves of the parallel converter.

Based on the power balance, the output power of DCM channel is formulated as follows:

$$P_{o\_DCM} = \frac{V_m^2 D_{y\_DCM}^2}{2\pi L_{b\_DCM} f_{s\_DCM}} \int_0^{\pi} \frac{\sin^2 \omega t}{1 - V_m \left|\sin \omega t\right| / V_o} d\omega t. \tag{12}$$

Substituting (12) into (11), and solving definite integral, the average input current of DCM channel is rewritten as follows:

$$i_{in\_DCM} = \frac{\pi \beta^2 P_{o\_DCM} \sin \omega t}{\alpha V_m \left(1 - \beta \left|\sin \omega t\right|\right)} \tag{13}$$

where $\beta = V_m/V_o$, $\alpha = \frac{\pi + 2\arctan(\beta/\sqrt{1-\beta^2})}{\sqrt{1-\beta^2}} - \pi - 2\beta$.

The harmonics of DCM channel average input current is expressed as follows:

$$i_{in\_DCM} = \frac{2P_{o\_DCM}}{V_m} \sin \omega t + \sum_{n=3,5,\ldots} \left(\frac{\beta^2 P_{o\_DCM}}{\alpha V_m} \int_0^{2\pi} \frac{\sin \omega t \sin n\omega t}{1 - \beta \left|\sin \omega t\right|} d\omega t \right) \sin n\omega t. \tag{14}$$

By solving definite integral, the third, fifth, and seventh harmonic contents are

$$I_{in\_DCM\_3} = \frac{\sqrt{2} P_{o\_DCM}}{V_m} \left[3 - \frac{4(\alpha - b)}{\alpha \beta^2} \right] \tag{15}$$

$$I_{in\_DCM\_5} = \frac{\sqrt{2} P_{o\_DCM}}{V_m} \left[5 - \frac{20(\alpha - b)}{\alpha \beta^2} + \frac{16(\alpha - b - c)}{\alpha \beta^4} \right] \tag{16}$$

$$I_{in\_DCM\_7} = \frac{\sqrt{2} P_{o\_DCM}}{V_m} \cdot \left[7 - \frac{56(\alpha - b)}{\alpha \beta^2} + \frac{112(\alpha - b - c)}{\alpha \beta^4} - \frac{64(\alpha - b - c - d)}{\alpha \beta^6} \right] \tag{17}$$

where $b = \frac{\pi \beta^2}{2} + \frac{4\beta^3}{3}$, $c = \frac{3\pi \beta^4}{8} + \frac{16\beta^5}{15}$, and $d = \frac{15\pi \beta^6}{48} + \frac{32\beta^7}{35}$. Equations (15)–(17) can be plotted in Fig. 5. Obviously, the third harmonic is the main component and increases with the increase of input voltage. The comparison between Figs. 3 and 5 indicate the phases of the third harmonic currents in the two channels are opposite. This gives us inspiration that the third harmonic in the total input current may be completely eliminated by paralleling DCM and CRM converters and adjusting the power distribution under different input voltages.

C. Power Distribution of Parallel Channels

It can be seen from (8) and (15), the third harmonic ratio of the two channels is related to P_{o_CRM}/P_{o_DCM} and V_m/V_o. Therefore, the third harmonic can be completely eliminated by controlling the power ratio P_{o_CRM}/P_{o_DCM} according to different V_m/V_o, as shown in the following:

$$\frac{P_{o\_CRM}}{P_{o\_DCM}} = \left(\frac{15\pi}{8\beta} - 5 \right) \left[\frac{4(\alpha - b)}{\alpha \beta^2} - 3 \right] = r(\beta). \tag{18}$$

In other words, if the total output power is P_o, the power of each converter is, respectively, as follows:

$$P_{o\_DCM} = \frac{1}{1 + r(\beta)} P_o \tag{19}$$

$$P_{o\_CRM} = \frac{r(\beta)}{1 + r(\beta)} P_o. \tag{20}$$

Thus, the power distribution of two channels over the wide input voltage range can be drawn in Fig. 6. From (8) and (15)–(18), the ratio of the input current third, fifth, and seventh harmonic content to the total output power over the wide input voltage range can be calculated and the curves are shown in Fig. 7. Compared with Fig. 3, the per watt content of third harmonic is reduced to 0 in the whole input voltage range. The seventh harmonic is also reduced and the fifth harmonic is slightly

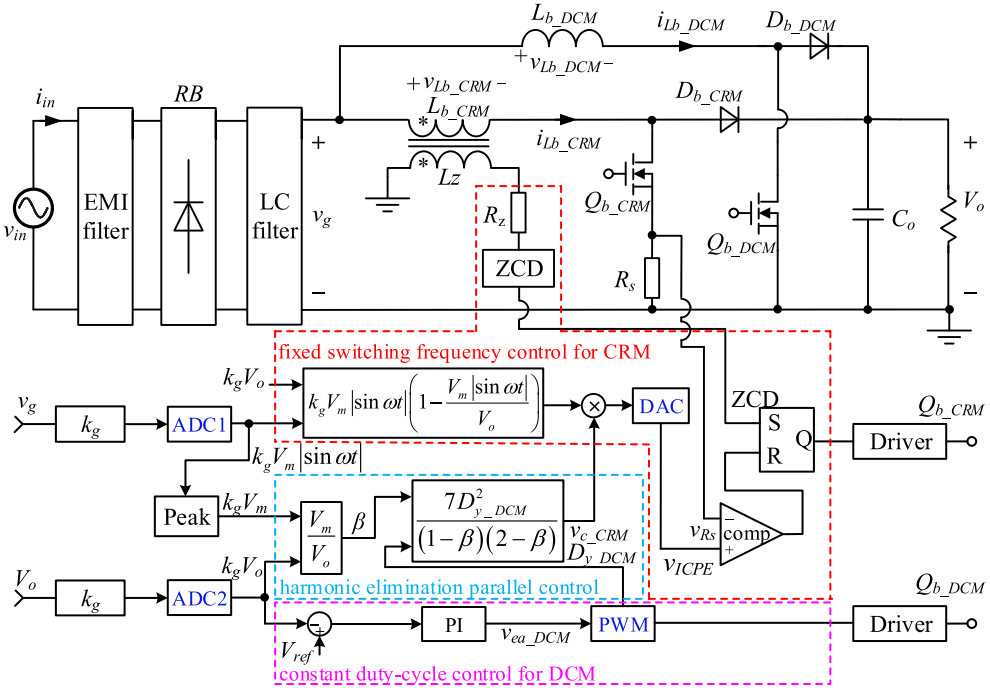

Fig. 8. Control circuit of FSFCRM&DCM with HEP.

increased. The reason for this is that the formulas of third, fifth, seventh, and higher harmonics are completely different, as expressed in (8) and (14)–(17). Consequently, further research is needed to eliminate all the harmonics, and, predictably, it is much more complex than the scheme presented here. Since the content of the fifth and higher order harmonics is far less than that of the third harmonic, whether it is necessary to eliminate them completely with more complex control depends on the application requirements.

III. Harmonic Elimination Parallel Control

A. Implementation of Control Circuit

The control circuit of HEP control method is shown in Fig. 8. The DCM branch adopts CDC control and the CRM branch adopts fixed switching frequency control. HEP is to achieve the coordinated power allocation between the two branches, and its essence is to transform the duty cycle information of DCM branch into the corresponding peak current information and provide it to CRM branch, so as to achieve the third harmonic elimination for the two branches operating in parallel.

For CRM channel, the ZCD signal controls the turn-ON of switch. The inductor current peak envelope signal v_{ICPE} and the sampled signal v_{Rs} are sent to the comparator. The output of the comparator determines the turn-OFF of switch. The analysis in Section II-A states clearly that, if the switching frequency is to be fixed for CRM operation, the peak value of inductor current should be $\frac{2P_{o\_CRM}\sin\omega t}{V_m(1/2-4V_m/3\pi V_o)}(1-\frac{V_m}{V_o}|\sin\omega t|)$.

Therefore, the given inductor current peak envelope reference signal in the control should contain the same information. The determination process of this signal includes two aspects, one is to obtain $k_gV_m|\sin\omega t|(1-V_m|\sin\omega t|/V_o)$by sampling the input and output voltage, where k_g is the voltage sensor gain. The other is to introduce the power information that needs to be transmitted by CRM branch, and the power must be proportional to that by DCM branch, and the coefficient is related to the ratio of input and output voltage, as shown in (18). Naturally, the duty cycle of DCM branch, which contains its power information, must be processed to construct a signal for generating the CRM branch power information, and such a signal is identified by v_{c_CRM}.

It can be seen from Fig. 8, under such control, the peak value of inductor current of CRM branch is

$$i_{Lb\_CRM\_pk}=\frac{v_{c\_CRM}k_gV_m|\sin\omega t|\,(1-V_m|\sin\omega t|/V_o)}{R_s} \tag{21}$$

where R_s is the sampling resistance of switch current.

Substitution of (7) into (21), the relationship between v_{c_CRM} and P_{o_CRM} is obtained as follows:

$$P_{o\_CRM}=\frac{v_{c\_CRM}k_gV_m^2\,(1/4-2V_m/3\pi V_o)}{R_s}. \tag{22}$$

For the control of DCM channel, the output voltage is compared with the reference, and the error signal v_{ea_DCM} is obtained through PI regulator. The duty cycle D_{y_DCM} is acquired by the intersection of the error signal and saw-tooth wave. The remaining problem is how to generate v_{c_CRM} from D_{y_DCM}.

The substitution of (12) and (22) into (18) yields the relationship between v_{c_CRM} and D_{y_DCM}

$$v_{c\_CRM}=\frac{15R_s}{8L_{b\_DCM}f_{s\_DCM}k_g}\left[\frac{8\,(\alpha-b)}{\beta^5}-\frac{6\alpha}{\beta^3}\right]D_{y\_DCM}^2. \tag{23}$$

It seems that this formula is complicated, which includes the inductance L_{b_DCM} and switching frequency f_{s_DCM} of DCM channel, the peak current sampling resistance R_s of CRM

branch, and the sampling coefficient k_g of input and output voltage of the converter, etc. In fact, there is no need to consider such complexity. If k_g is set to be $15\gamma R_s/8L_{b\_DCM}f_{s\_DCM}$, (23) can be simplified into the following, which is good for simplifying control:

$$v_{c\_CRM} = \frac{1}{\gamma}\left[\frac{8(\alpha-b)}{\beta^5} - \frac{6\alpha}{\beta^3}\right] D_{y\_DCM}^2 \tag{24}$$

where γ is a coefficient to be determined.

In terms of DCM branch, the inductance should meet (25a)

$$L_{b\_DCM} \le \left(1-\frac{V_m}{V_o}\right)^2 \frac{V_m^2}{2\pi f_{s\_DCM} P_{o\_DCM}} \int_0^{\pi} \frac{\sin^2\omega t}{1 - V_m\left|\sin\omega t\right|/V_o} d\omega t. \tag{25a}$$

Substituting (19) into (25a) leads to

$$L_{b\_DCM} f_{s\_DCM} = \frac{V_o^2}{2\pi P_o}\beta^2(1-\beta)^2\left[1+r(\beta)\right]\int_0^{\pi}\frac{\sin^2\omega t}{1-\beta\left|\sin\omega t\right|}d\omega t. \tag{25b}$$

It can be noticed from (25b), the inductance L_{b_DCM} and switching frequency f_{s_DCM} are not independent of each other, and they are in the form of products.

In terms of CRM branch, for achieving the inductor current shown in (7), the inductor current peak envelope signal v_{ICPE} should be

$$v_{ICPE} = v_{Rs\_pk} = R_s i_{Lb\_CRM\_pk} = \frac{2R_s P_{o\_CRM}\sin\omega t}{V_m\left(1/2 - 4V_m/3\pi V_o\right)}\left(1-\frac{V_m}{V_o}\left|\sin\omega t\right|\right). \tag{26a}$$

The substitution of (20) into (26a) results in

$$v_{ICPE} = v_{Rs\_pk} = \frac{2R_s P_o}{V_o}\frac{\frac{r(\beta)}{1+r(\beta)}}{\beta\left(1/2-4\beta/3\pi\right)}\sin\omega t\left(1-\beta\left|\sin\omega t\right|\right). \tag{26b}$$

The maximum voltage on the sampling resistor of inductor peak current should be limited, and this is marked as $v_{Rs\_pk\_\mathrm{limit}}$. Therefore, the sampling resistance R_s needs to be calculated in detail from 26(b).

It should be noted that when analyzing 25(b) and 26(b), we need to investigate their extremum about β and $\sin\omega t$. Here, the derivation process is ignored and only the result of k_g is given as follows (27):

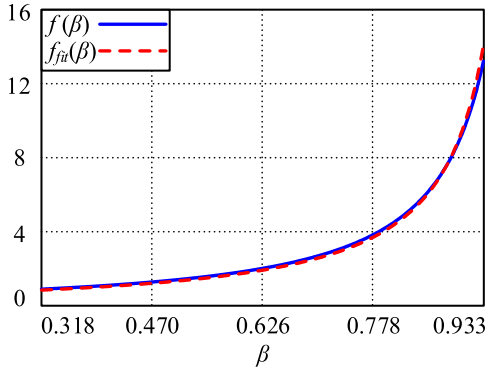

Fig. 9. $f(\beta)$ and $f_{fit}(\beta)$ curves.

$$k_g = \gamma\frac{15R_s}{8L_{b\_DCM}f_{s\_DCM}} = \gamma\frac{\frac{15V_o}{2P_o}\frac{v_{Rs\_pk\_limit}}{\left\{\frac{\frac{r(\beta)}{1+r(\beta)}}{\beta(1/2-4\beta/3\pi)}\sin\omega t(1-\beta|\sin\omega t|)\right\}_{\max}}}{\frac{4V_o^2}{\pi P_o}\left\{\beta^2(1-\beta)^2\left[1+r(\beta)\right]\int_0^{\pi}\frac{\sin^2\omega t}{1-\beta|\sin\omega t|}d\omega t\right\}_{\min}} = \gamma\frac{v_{Rs\_pk\_limit}}{0.037V_o}. \tag{27}$$

It can be seen from (27), not only the inductance L_{b_DCM} and switching frequency f_{s_DCM}, but also the output power P_o, have no effect on the setting of k_g. Actually, k_g needs to ensure that the high voltage sampling value of the main power circuit meets the input voltage range requirements of the control circuit. Furthermore, the purpose of the above-mentioned derivation is to determine how to select the value of γ, as described in the following.

Equation (27) can be written as follows:

$$\gamma = 0.037\frac{k_g V_o}{v_{Rs\_pk\_limit}}. \tag{28}$$

The input voltage range of DSP is 0–3.3 V. It is necessary to ensure that the sampling voltage is within this range and a certain margin should be considered, such as less than 2.7 V. In determining the value of $v_{Rs\_pk\_\mathrm{limit}}$, not only the input voltage range of DSP but also the dissipated power of sampling resistor should be considered. Here, the calculation process is ignored and the final value is 0.7 V. Then, $k_g = 2.7/400 \approx 1/150$ and $\gamma = 1/7$ can be figured out.

Substituting $\gamma = 1/7$ into (24) yields

$$v_{c\_CRM} = 7\left[\frac{8(\alpha-b)}{\beta^5} - \frac{6\alpha}{\beta^3}\right] D_{y\_DCM}^2. \tag{29}$$

There is no doubt that the calculation of $f(\beta) = \frac{8(\alpha-b)}{\beta^5} - \frac{6\alpha}{\beta^3}$ is too complicated. Further studies show that it can be fitted as $f_{fit}(\beta) = \frac{1}{(1-\beta)(2-\beta)}$, as shown in Fig. 9. Therefore, (29) is simplified into

$$v_{c\_CRM} = \frac{7}{(1-\beta)(2-\beta)} D_{y\_DCM}^2. \tag{30}$$

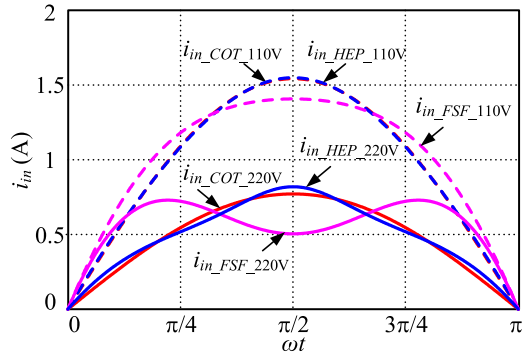

Fig. 10. Input current waveforms at 110 and 220 VAC.

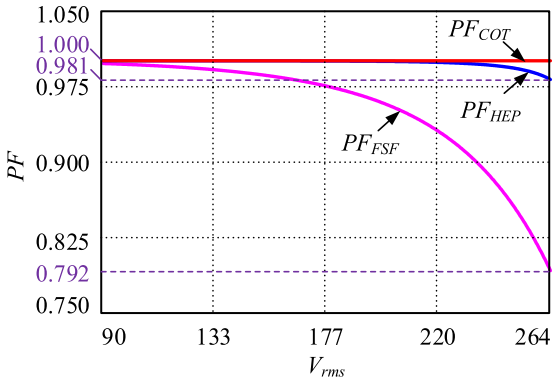

Fig. 11. Theoretical input current PF values.

B. Input Current and PF

Based on the above-mentioned analysis, the input current curves of single CRM boost PFC converter with COT and FSF, and the input current curves of FSFCRM&DCM with HEP are plotted in Fig. 10, at 110 VAC and 220 VAC, respectively. It can be recognized that the input currents with COT and HEP are purely sinusoidal and nearly sinusoidal, respectively. However, with FSF, the current is seriously distorted, especially at high input voltages. Accordingly, the PFs under the three controls can be calculated in (31a)–(31c) and plotted in Fig. 11.

$$PF_{COT} = 1 \tag{31a}$$

$$PF_{FSF} = \frac{\sqrt{2}}{\sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{\sin\omega t(V_o - V_m|\sin\omega t|)}{(V_o/2 - 4V_m/3\pi)}\right]^2 d\omega t}} \tag{31b}$$

$$PF_{HEP} = \frac{\sqrt{2}P_o}{V_m\sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{P_{o\_CRM}\sin\omega t(V_o - V_m|\sin\omega t|)}{V_m(V_o/2 - 4V_m/3\pi)} + \frac{\pi\beta P_{o\_DCM}\sin\omega t}{\alpha(V_o - V_m|\sin\omega t|)}\right]^2 d\omega t}}. \tag{31c}$$

IV. Simulated and Experimental Results

In order to verify the validity of the theoretical analysis, two prototypes of a single CRM boost PFC converter are built, with COT and FSF, respectively. Furthermore, a prototype of HEP FSFCRM&DCM converter is fabricated. The specifications are as follows. Input voltage: 90–264 VAC/50 Hz; output voltage: 400 VDC; and output power: 120 W.

The experimental and theoretically calculated waveforms of input voltage, input current, and inductor current in a line cycle are displayed in Figs. 12–15, at 220 VAC and 110 VAC, respectively. Obviously, the experimental results are almost consistent with the theoretical analysis, both in waveform shape and amplitude. For HEP, although the average inductor currents of CRM channel and DCM channel have their own distortion, the total input current is close to sine. The harmonic elimination effect under low input voltage is better than that under high input voltage.

The experimental and simulated waveforms of inductor current in switching cycles expanded around $\omega t = \pi/5$ and $\omega t = \pi/2$ are given in Figs. 16–23, with COT, FSF, and HEP, at 220 VAC and 110 VAC, respectively. It should be pointed out that the experimental results of frequency value are different from the simulation. The reason is that the simulation is ideal, but in experiments, the frequency will become lower due to the conversion efficiency. In addition, other factors such as the inductance deviation and so on should also be considered.

Obviously, the switching frequency of the converter with COT varies a lot in a half-line cycle. FSF can achieve a nearly constant switching frequency. In terms of DCM channel, the inductor current is discontinuous in switching cycles, and the duty cycle remains unchanged in a half-line cycle. Under different input voltages, the duty cycle is different, and so does the power. It can be seen from the sinusoidal degree of input current in Figs. 12(c) and 14(c), the third harmonic currents contained in DCM channel and CRM channel eliminate each other, which is consistent with the theoretical analysis.

The curves of PF versus different loads at 220 and 110 VAC are given in Figs. 24 and 25. Under different power, the HEP and COT control makes the converter achieve high PF. For the three kinds of control, PF almost decreases with the reduction of output power, especially when the input voltage is high. This is mainly because when the power is low, the influence of displacement factor and line frequency zero-crossing distortion is more prominent.

The efficiency curves are plotted in Figs. 26 and 27 for the three control methods, with different loads at 220 and 110 VAC. Compared to that with COT, the efficiency of converter with FSF is high, especially at light load and high input voltage, which is the case where the switching frequency of the converter with COT is larger. This shows that the switching loss can be greatly reduced by solving the problem of excessive switching frequency range.

Compared to those with COT and FSF, the efficiency of HEP controlled converter is lower. This is because only one converter is needed to verify COT and FSF, whereas two converters are paralleled for HEP control. However, the experiments in this article are only to verify the proposed concept of harmonic cancellation and its control method, as well as the effect of PF and fixed frequency. Based on this goal and considering fairness, the main power devices of two channels of HEP controlled converter are the same as those of COT and FSF. Obviously, this

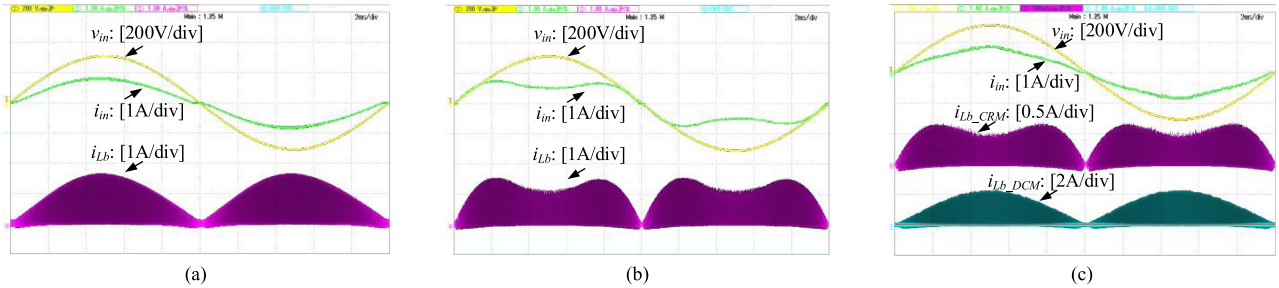

Fig. 12. Experimental waveforms in a line cycle at 220 VAC. (a) With COT. (b) With FSF. (c) With HEP.

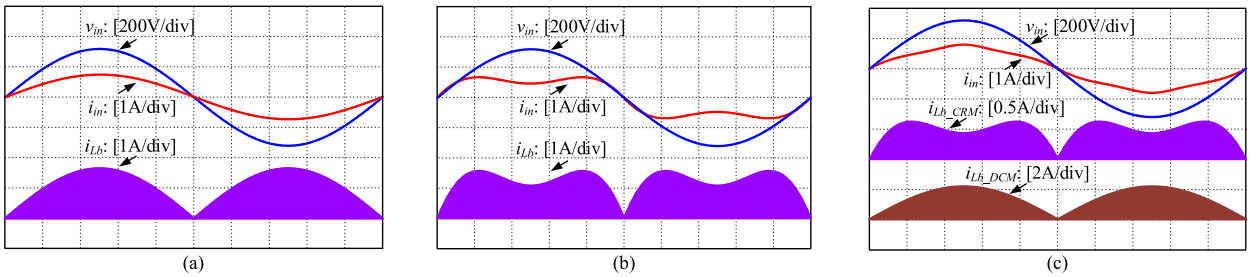

Fig. 13. Theoretical waveforms in a line cycle at 220 VAC. (a) With COT. (b) With FSF. (c) With HEP.

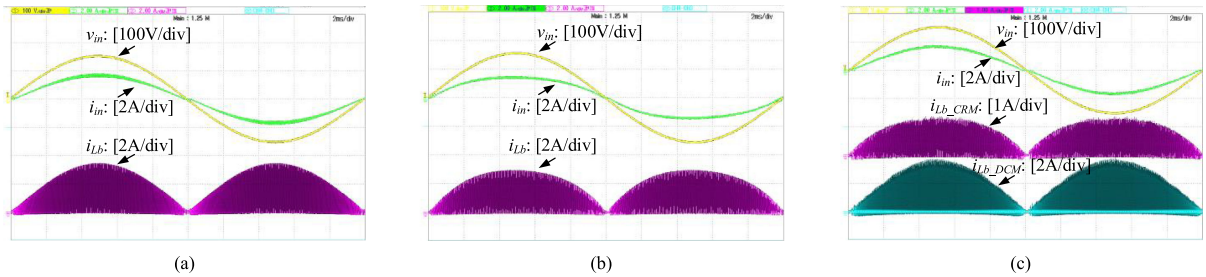

Fig. 14. Experimental waveforms in a line cycle at 110 VAC. (a) With COT. (b) With FSF. (c) With HEP.

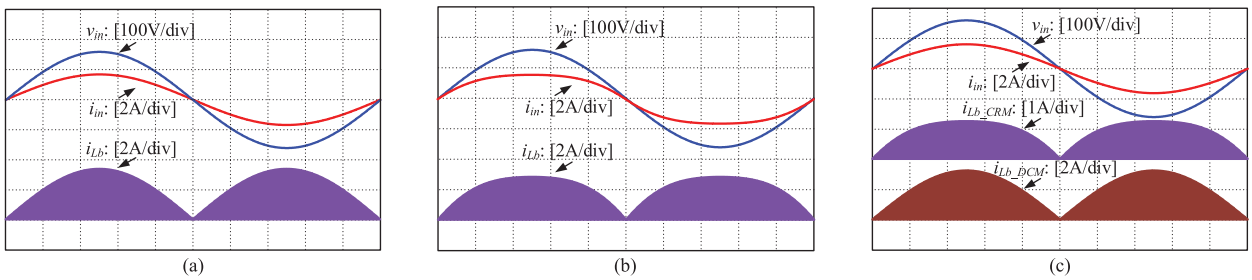

Fig. 15. Theoretical waveforms in a line cycle at 110 VAC. (a) With COT. (b) With FSF. (c) With HEP.

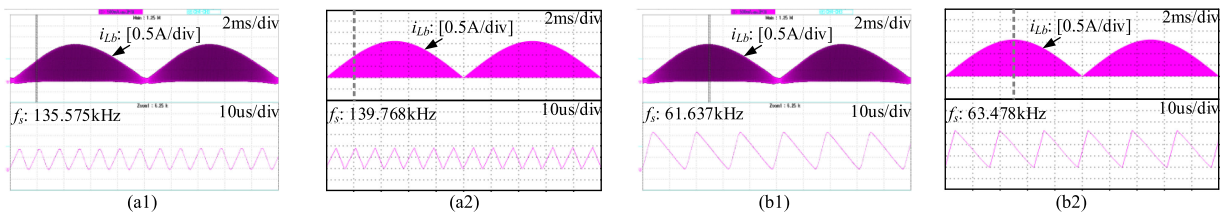

Fig. 16. Inductor current with COT in switching cycles at 220 VAC. (a1) Experiment at $\pi/5$. (a2) Simulation at $\pi/5$. (b1) Experiment at $\pi/2$. (b2) Simulation at $\pi/2$.

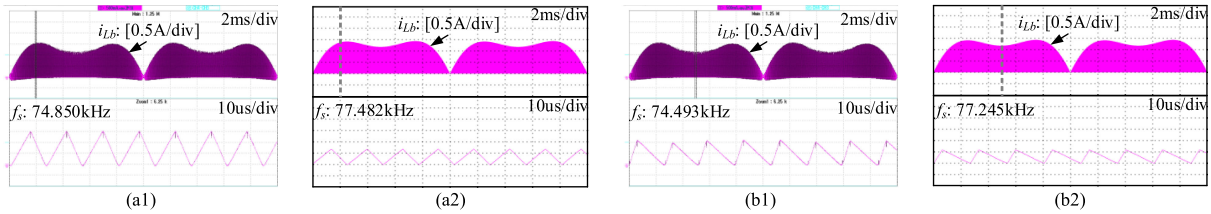

Fig. 17. Inductor current with FSF in switching cycles at 220 VAC. (a1) Experiment at $\pi/5$. (a2) Simulation at $\pi/5$. (b1) Experiment at $\pi/2$. (b2) Simulation at $\pi/2$.

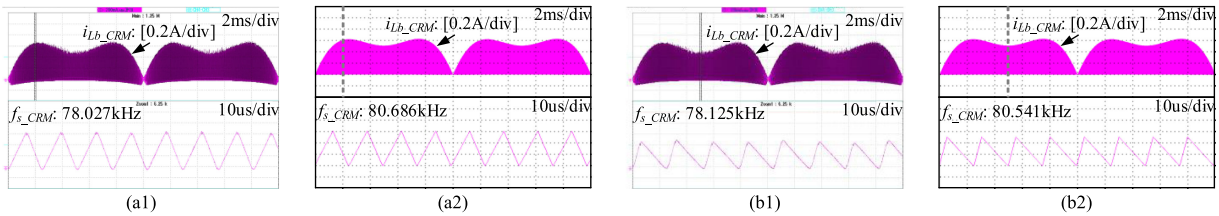

Fig. 18. CRM channel inductor current with HEP in switching cycles at 220 VAC. (a1) Experiment at $\pi/5$. (a2) Simulation at $\pi/5$. (b1) Experiment at $\pi/2$. (b2) Simulation at $\pi/2$.

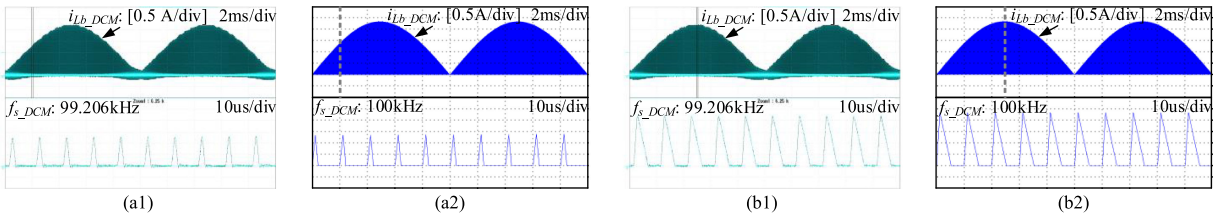

Fig. 19. DCM channel inductor current with HEP in switching cycles at 220 VAC. (a1) Experiment at $\pi/5$. (a2) Simulation at $\pi/5$. (b1) Experiment at $\pi/2$. (b2) Simulation at $\pi/2$.

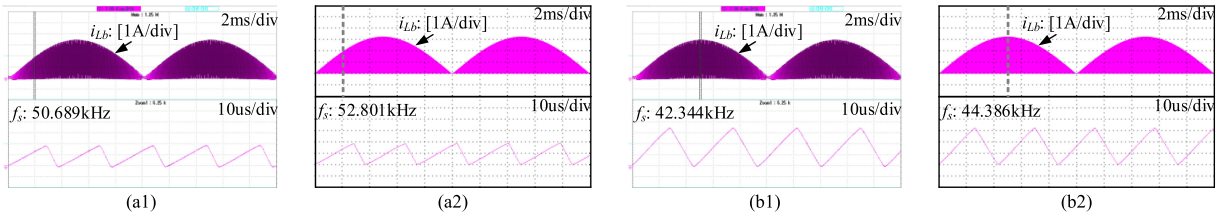

Fig. 20. Inductor current with COT in switching cycles at 110 VAC. (a1) Experiment at $\pi/5$. (a2) Simulation at $\pi/5$. (b1) Experiment at $\pi/2$. (b2) Simulation at $\pi/2$.

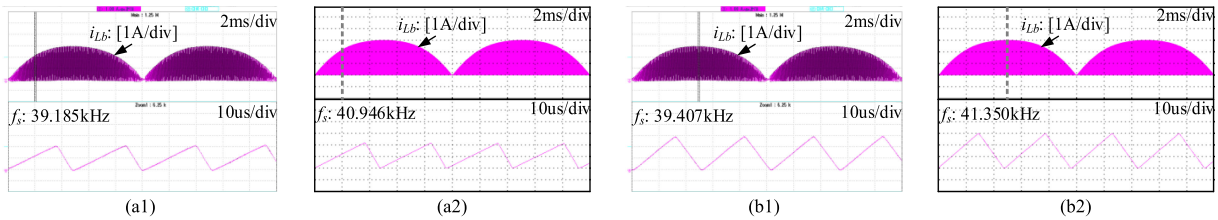

Fig. 21. Inductor current with FSF in switching cycles at 110 VAC. (a1) Experiment at $\pi/5$. (a2) Simulation at $\pi/5$. (b1) Experiment at $\pi/2$. (b2) Simulation at $\pi/2$.

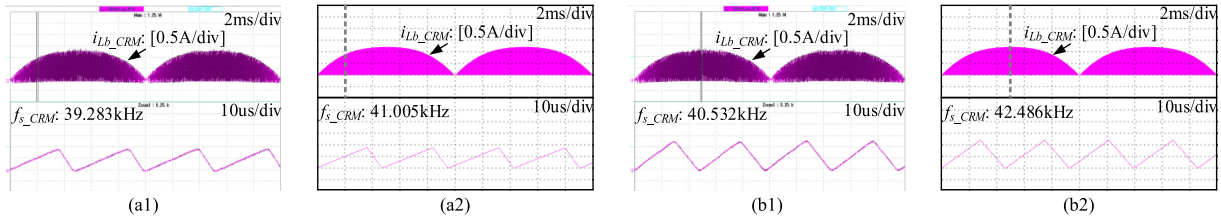

Fig. 22. CRM channel inductor current with HEP in switching cycles at 110 VAC. (a1) Experiment at $\pi/5$. (a2) Simulation at $\pi/5$. (b1) Experiment at $\pi/2$. (b2) Simulation at $\pi/2$.

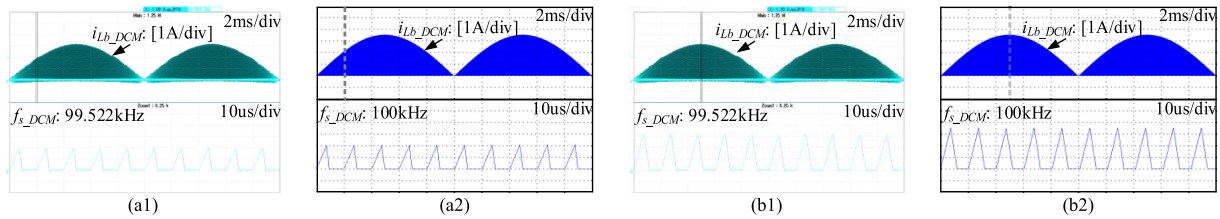

Fig. 23. DCM channel inductor current with HEP in switching cycles at 110 VAC. (a1) Experiment at $\pi/5$. (a2) Simulation at $\pi/5$. (b1) Experiment at $\pi/2$. (b2) Simulation at $\pi/2$.

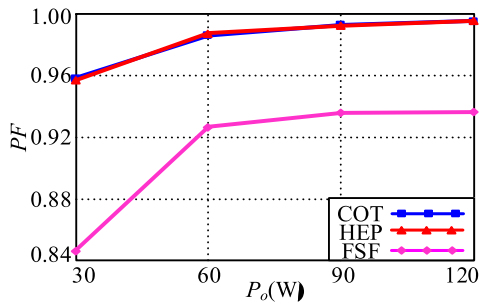

Fig. 24. Tested PF with different loads at 220 VAC.

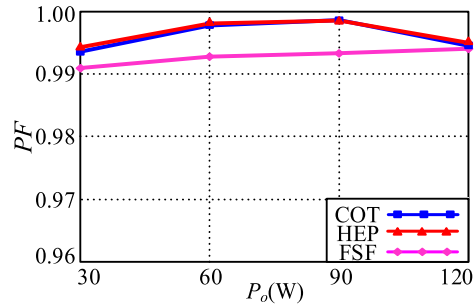

Fig. 25. Tested PF with different loads at 110 VAC.

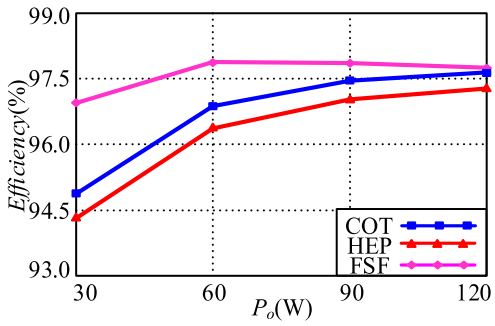

Fig. 26. Tested efficiency with different loads at 220 VAC.

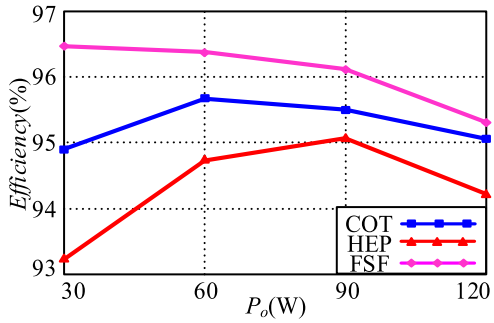

Fig. 27. Tested efficiency with different loads at 110 VAC.

reduces the efficiency of HEP controlled converter, because each channel only shares part of the power. In fact, compared with a single converter, the current rating of two parallel converters can be reduced to about half if they are designed at the same power. Or, if the components with the same current rating are selected, the power that two converters can handle is twice that of a single converter. In these two cases, whether the efficiency of HEP is lower or higher than that of COT and FSF is still a problem to be explored.

The measured and theoretical input current harmonics contents spectra are shown in Figs. 28 and 29. The experimental results nearly agree with the theory. The data fully illustrate that, with FSF, the harmonic contents of input current are very high, especially the third harmonic, while with COT and HEP, the harmonic contents are very low.

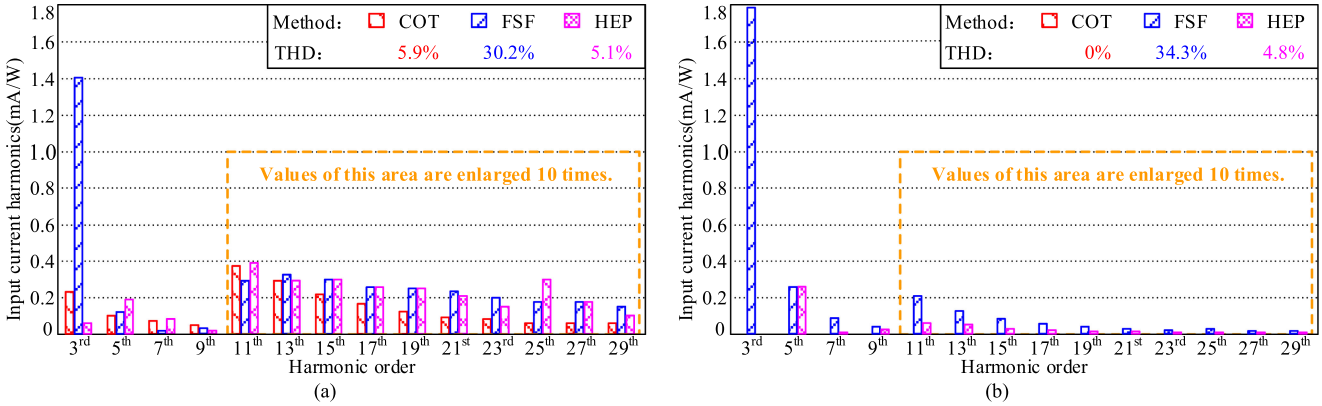

Fig. 28. Input current harmonics at 220 VAC. (a) Experiment. (b) Theory.

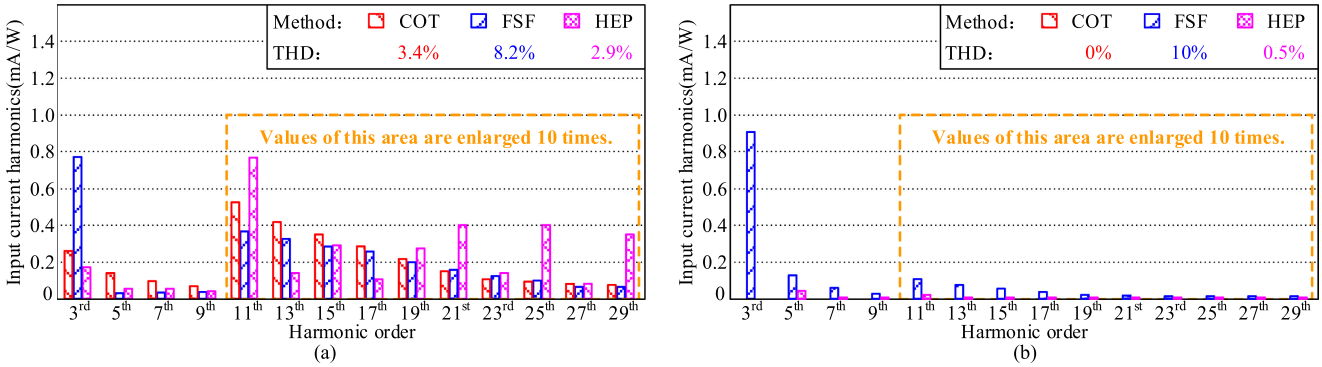

Fig. 29. Input current harmonics at 110 VAC. (a) Experiment. (b) Theory.

V. Conclusion

This article proposed a HEP control method of FS-FCRM&DCM. The detailed mathematical derivation and the implementation circuits were presented. The parallel converter is different from parallel CRM or parallel DCM boost PFC converter. Compared with parallel CRM converter, it has the advantage of fixed switching frequency of each channel in line cycles. While compared with parallel DCM converter, a higher PF and lower peak current can be achieved.

The feasibility of harmonic elimination is verified by adjusting the power distribution of two channels. In fact, this is the first part of the research work. Next, the following two aspects will be focused on. One is how to make the switching frequency of CRM channel consistent with DCM channel. The other is how to accurately control interleaving to achieve better converter performance.

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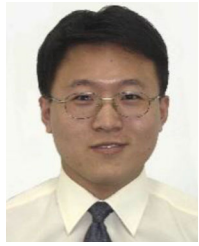

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