Investigation of Nonlinearities Introduced by Multi-sampled Pulsewidth Modulators

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***Abstract*—Multi-sampled pulsewidth modulator (MS-PWM) digital control is important for reduction of control and modulator delays as well as for noise suppression. To reduce aliasing and modulator nonlinearities, the MS-PWM is often implemented with switching ripple filtering, which limits the obtained dynamic improvements. This article analyzes the multi-sampled modulator nonlinearities in order to provide means for the optimal implementation of MS-PWM without ripple filtering. Depending on the types of intersections between the modulating waveform and the carrier, the nonlinearities are manifested as reduced-gain, zero-gain, and infinite-gain zones in the modulator transcharacteristic. For dc-type converters, the modulator nonlinearities can impair the transient response and give rise to limit cycle oscillations. For ac-type converters, it is shown that the modulator nonlinearities result in a stronger harmonic distortion compared to the aliasing effect. The nonlinear behavior is caused by the modulating waveform steps, whose pattern depends on switching ripple, controller gains, multi-sampling factor, and time delay of the control system. Particularly, the time delay is found to be a crucial factor that determines which nonlinearity is exhibited and to what extent. Discontinuity and nonlinearity graphs are proposed and exploited to adjust the time delay, so as to avoid specific nonlinearity zones and to, partially or completely, linearize the system behavior. The theory is experimentally verified on a dc–dc buck converter and a dc–ac single-phase inverter. This article is accompanied by videos of experimental validations.**

***Index Terms*—Digital pulsewidth modulators (DPWMs), limit cycle oscillations (LCOs), multi-sampled pulsewidth modulators (MS-PWMs), total harmonic distortion (THD).**

I. Introduction

THE advancement of technology related to microcontrollers, digital signal processors, and field-programmable gate arrays (FPGAs) enables increasingly more information to be processed within the same time interval, using standard programming techniques. In regard to processing power, novel wide-bandgap power devices, such as silicon carbide and gallium nitride, enable very high switching frequencies [1]. However, in many high-power and high-voltage applications, the switching frequencies are expected to remain quite low compared to information processing capabilities [2]. Standard digital control solutions still rely on acquiring the feedback and updating the controller output once or twice per switching period [3]. The single-sampled single-update (SS-SU) and double-sampled double-update (DS-DU) methods can be quite susceptible to noise-related issues [4]–[6]. Furthermore, they result in a significant impact on the achievable dynamic response due to the calculation time and the digital pulsewidth modulator (DPWM) delay [7], [8]. To fully exploit the emerging capabilities of control platforms, one of the possible directions is going toward analog-like controllers in digital systems. This is achieved with multi-sampled pulsewidth modulator (MS-PWM) control, where the feedback is processed multiple times per switching period. Due to digital delay reduction, MS-PWM control improves both small-signal and large-signal responses of a power converter [5], [7], [9]–[19]. Furthermore, it is found that the MS-PWM can be a very effective solution for feedback noise suppression [6]. Due to a set of nonlinearities being introduced, mainly because of the discontinuity of the modulating waveform [7], [10], [11], [17], most of the MS-PWM control solutions still rely on completely filtering out the switching ripple from the feedback [5], [9], [13], [18]. The added phase lag due to ripple filtering compromises the dynamic benefits obtained by MS-PWM control. Hence, to better exploit the capabilities of the MS-PWM, it is necessary to more thoroughly analyze the nonlinearities that occur when the switching ripple is not removed, and to find control loop settings that allow its unperturbed operation.

This article provides an investigation on the modulator nonlinearities encountered in MS-PWM control. It is found that different nonlinearity zones appear in the modulator transcharacteristic when the total time delay of the control loop is changed. Provisions for minimizing these nonlinearities are then presented, and application examples of converters operating in each of the nonlinear zones are given. For converters with a dc operating point, the nonlinearities can lead to an undesirable response to transients and to increased jitter of the duty cycle. For converters with an ac operating point, the nonlinearities lead to the output waveform distortion.

The rest of this article is organized as follows. Section II presents the structure of a multi-sampled control system of a power converter. Section III explains the possible relations between the carrier and the modulating waveform, and their impact on MS-PWM transcharacteristics. Section IV provides

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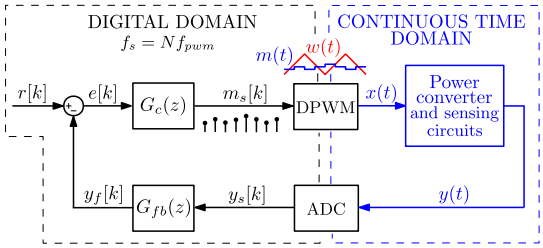

Fig. 1. Block diagram of a power electronic converter's multirate control system.

the analytical procedure for calculating MS-PWM transcharacteristics. Furthermore, definitions of critical operating points are given. The discontinuity graphs are presented to explain the impact of time delay on the MS-PWM behavior. In Section V, the nonlinearity measures are introduced to quantify the transcharacteristics nonlinearities. The related nonlinearity graphs are used to determine which nonlinearity is present, to what extent, and to predict its impact on a converter's operation. The nonlinearity graphs can be used to determine the value of time delay that minimizes the impact of nonlinearities. Section VI provides the verification of the study on a dc–dc buck converter and a dc–ac single-phase inverter. Finally, Section VII concludes this article.

II. Multi-sampled Power Converters

The multirate control system of a power electronic converter is illustrated in Fig. 1. This article focuses on single-stage control loops of converters with only one switching signal $x(t)$ and one output $y(t)$; however, the MS-PWM can be implemented for any control loop and hardware topology, including multilevel and multiphase systems. The transition from the continuous time domain to the digital domain is performed by an analog-to-digital converter (ADC). The digital domain comprises a feedback filter $G_{fb}(z)$, a reference set point $r[k]$, and a controller $G_c(z)$. The operating frequency of the digital part is $f_s = Nf_{\text{pwm}}$, where N is the oversampling (multi-sampling) factor and f_{pwm} is the switching frequency of the converter. The controller output $m_s[k]$, in the form of an impulse train, is used as the input of the DPWM. The update period of m_s, $T_s = \frac{1}{f_s}$, is referred to as the control period. The DPWM block serves as an interface between digital and continuous time domains. Its inherent zero-order-hold action transforms $m_s[k]$ into the piecewise constant modulating waveform $m(t)$, which is compared with the DPWM carrier $w(t)$. In [7], it is shown that the triangular carrier is preferable for MS-PWM applications, which is why it is chosen in this article. The DPWM output is used as the switching signal. The continuous time domain comprises the power electronic converter and sensing circuits.

A. MS-PWM Impact on Dynamic Improvements

Digital control systems that rely on multiple feedback samples per switching period are natural for multilevel and interleaved converters that feature multiple phase-shifted carriers [15], [20], [21]. Due to their effective increase of the switching frequency, more than two instants per switching cycle appear, where sampling the feedback signal yields the average value of the sensed variable.

The MS-PWM can also be implemented for widely used converters with a single carrier. For those, acquiring multiple samples per switching period unavoidably results in the switching ripple being present in the sampled signal. However, updating the controller output multiple times per switching period enhances both small-signal and large-signal properties of the modulator [7]. The triangular DPWM can be closely approximated as a pure time delay equal to $\frac{T_{\text{pwm}}}{2N}$, independently of the operating point [7]. Often, due to the algorithm execution time, the modulating waveform update is delayed by one control period, which brings an additional delay of $\frac{T_{\text{pwm}}}{N}$ [3]. The fact that these digital control loop delays are inversely proportional to the oversampling factor is the main motivation behind the implementation of the MS-PWM control.

As the switching ripple is introduced in the feedback loop, the MS-PWM starts to resemble the analog pulsewidth modulator (PWM), especially for high values of N. However, in many reported applications of MS-PWM, the switching ripple is removed using digital filters [5], [9], [13], [18]. The reason for this is that properties of MS-PWM operated converters, without ripple filtering, are still not completely clarified. First, problems may arise due to aliasing effects as the switching ripple is sampled [9], [18]. Intuitively, aliasing problems are decreased with higher oversampling factors, as the average value of the sampled feedback comes closer to the true average value. The analysis of aliasing-related problems is out of the scope of this article; however, it should be mentioned that aliasing may also occur for DS-DU control [3]. Other problems, specific to the MS-PWM, arise due to discontinuity of the modulating waveform. The switching ripple is most often removed using moving average filters (MAFs) [5], repetitive filters [9], or variations of those [13], [18]. One thing in common is that all of these filters introduce a certain phase lag that impairs the phase margin at any given crossover frequency. For example, if an MAF that averages N latest samples is used to remove the switching ripple, the introduced time delay is equal to $\frac{T_{\text{pwm}}}{2}$, which is equivalent to the modulator delay for SS-SU control [22]. For ripple filters that reduce the added phase lag, their delay compensation is expected to bring higher sensitivity to the presence of feedback noise. Hence, this article focuses on the investigation of nonlinearities introduced by modulating waveform discontinuities for converters with MS-PWM control systems that do not remove the switching ripple from the feedback.

III. Relations Between the Carrier and the Modulating Waveform

An example of MS-PWM operation is shown in Fig. 2. In this article, the time is normalized by T_{pwm} and the magnitude of the carrier is normalized by its maximum value; hence, $m(t)$ is unitless and limited in the range [0,1]. Without loss of generality, it is assumed that the carrier's counter starts from its maximum value with negative slope at $t = 0$. The synchronization between the carrier and the modulating waveform update instants is such

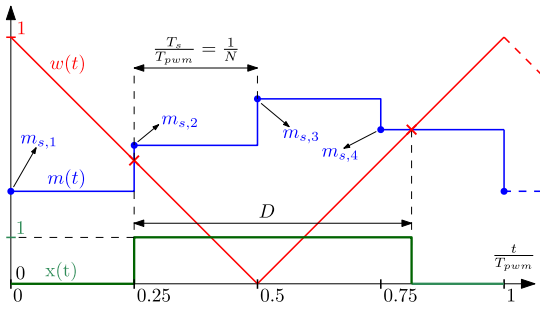

Fig. 2. Example of the modulating waveform $m(t)$, the carrier $w(t)$, and the switching signal $x(t)$ for one switching period of the converter with oversampling factor $N = 4$. One vertical crossing occurs during negative slope of w, which prevents the modulation of the corresponding edge of x.

that the latter occur at $t = \frac{n}{N} T_{\text{pwm}}$, where n belongs to the set of natural numbers. The switching signal $x(t)$ is a square waveform with duty cycle D.

A way to describe the PWM as an actuator is the modulator transcharacteristic, which provides the value of D as a function of the average value of the modulating waveform over one switching period, $< \mathrm{m} >$. In case of digital PWM, the value $< \mathrm{m} >$ is obtained as an average of N controller outputs m_s starting from when $w = 1$, e.g., $\frac{t}{T_{\text{pwm}}} \in [0, 1)$. In Fig. 2, this corresponds to $\frac{m_{s,1}+m_{s,2}+m_{s,3}+m_{s,4}}{4}$. The transcharacteristic is a piecewise linear function, with variable gains corresponding to each linear segment, $k = \frac{dD}{d<\mathrm{m}>}$ [7]. Throughout this article, k will be referred to as the modulator gain. The modulator gain is determined by different types of intersections between m and w.

For single- and double-update methods, with previously noted proper synchronization, the update of m occurs when w is equal to 0 or 1. This always yields horizontal crossings between m and w. The horizontal crossings determine the linear behavior of the DPWM, as the duty cycle is determined by a unique modulating waveform. In those cases, the modulator features unity gain $k = 1$ [7].

For the MS-PWM method, the modulating waveform is updated multiple times per switching period; hence, the intersection between m and w can be either horizontal or vertical [7]. It is clear from Fig. 2 that vertical intersections between m and w may only occur at instants when the modulating waveform is updated and the carrier is not equal to 0 or 1. For further classification of these intersections, it is important to differentiate *in-phase* and *counter-phase* operating regimes [17]. Simply put, in-phase operating regimes occur when, at the update instant of m closest to the intersection with w, the slope of m has the same sign as the slope of w. Counter-phase operating regimes occur when, at the update instant of m closest to the intersection with w, the slope of m has the opposite sign compared to the slope of w.

In Fig. 3(a), horizontal crossings for both in-phase and counter-phase regimes are shown. For cases when horizontal crossings occur during both slopes of w, the modulator gain is $k \approx 1$. As for the analog modulators, the gain is not exactly equal to 1, due to the ripple modulation effect [7]. Regarding vertical crossings, different behavior is obtained for counter-phase and

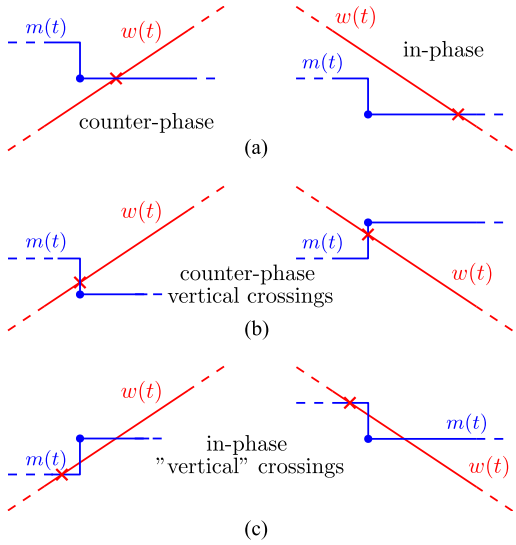

Fig. 3. Types of intersections between the modulating waveform m and the carrier w. (a) Horizontal crossings. (b) Counter-phase vertical crossings. (c) In-phase "vertical" crossings. The closest update of m to the intersection with w is labeled with a blue dot. The intersection that defines the switching signal x is labeled with a red cross.

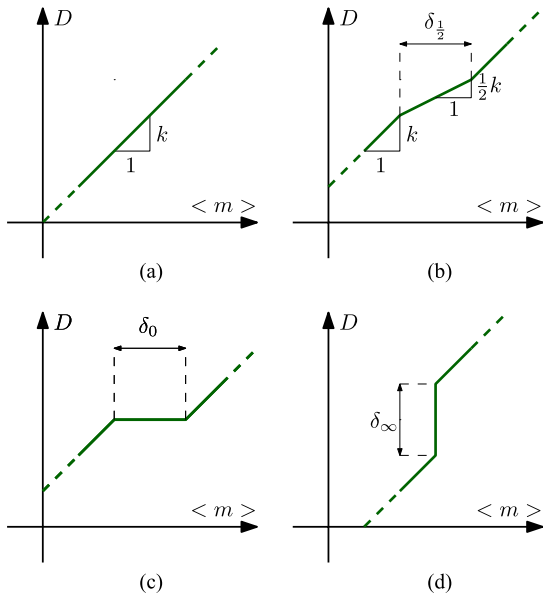

Fig. 4. Types of zones that appear in MS-PWM transcharacteristics. (a) Linear part corresponding to double horizontal crossings. (b) Reduced-gain part corresponding to a single counter-phase vertical crossing. (c) Zero-gain (dead-band) part corresponding to double counter-phase vertical crossings. (d) Infinite-gain part (jitter zone) corresponding to in-phase "vertical" crossings.

in-phase regimes. In Fig. 3(b), counter-phase vertical crossings are shown. The analysis of this type of intersections and their impact on converter dynamics is given in [7]. A counter-phase vertical crossing prevents the modulation of the corresponding edge of $x(t)$, which reduces the modulator gain. In cases where a counter-phase vertical crossing appears for only one slope of w, the modulator gain is halved, $k \approx \frac{1}{2}$ [22]. Example of this operation is seen in Fig. 2, and the corresponding transcharacteristic nonlinearity is shown in Fig. 4(b). If, for some values of $< \mathrm{m} >$,

counter-phase vertical crossings occur during both slopes of w, dead-bands, where $k = 0$, appear in the transcharacteristic and x is not modulated at all [7]. The corresponding nonlinearity is shown in Fig. 4(c). The in-phase "vertical" crossings are shown in Fig. 3(c) for both slopes of the carrier w. To prevent multiple commutations, the switching action of the MS-PWM is always based just on the first intersection between m and w, thus yielding a single turn-ON during the negative slope of w and a single turn-OFF during the positive slope of w. With this logic, in-phase "vertical" crossings are actually turned into horizontal crossings. However, due to the discontinuity of the modulating waveform, this type of intersection yields zones in the transcharacteristic, where steady-state operation cannot be achieved [17]. These zones are labeled "jitter zones" in [17] as they cause limit cycle oscillations (LCOs). In jitter zones, the transcharacteristic is not defined; however, for the sake of illustration of the LCO mechanism, in this article, jitter zones are represented as vertical lines, where $k \to \infty$. An example of the corresponding nonlinearity is shown in Fig. 4(d). In-phase "vertical" crossings can appear for both slopes of w, or in combination with a counter-phase vertical crossing or a horizontal crossing.

It is intuitive that for analog control, even if the switching ripple is introduced in the feedback, vertical crossings do not exist, thanks to the continuity of the modulating waveform. The nonlinear effects introduced by vertical crossings are amplified with higher discontinuities of $m(t)$. These nonlinearities impact steady-state operation [17], system dynamics [7], and may also be a source of harmonic distortion in ac applications.

IV. Modulating Waveform and Discontinuity Calculations

This section provides a procedure to calculate MS-PWM transcharacteristics. Additionally, it analyzes the impact of N, control loop bandwidth, and time delay on the modulating waveform discontinuity. It is shown that time delay determines whether the MS-PWM operates in the counter-phase or in-phase regime.

A. Calculation of the Modulating Waveform

To calculate the MS-PWM transcharacteristic, it is necessary to find $m(t)$. To this purpose, the analog equivalent of the modulating waveform ripple $m_r(t)$ must be obtained [7]. This can be achieved analytically, solving a set of differential equations related to the analog equivalents of the blocks in Fig. 1 from y_s to m_s. For a supposed steady-state duty cycle D, the converter's circuit is solved for all topological states, and the ripple of the output waveform $y_r(t)$ is found. If the control loop features any feedback filtering, a corresponding set of differential equations is used to find the filtered ripple component. The filtered output ripple is then used to solve a set of controller-related equations taking into account the negative feedback sign, which results in $m_{r,1}$. Finally, an arbitrary amount of time delay $\Delta t = \tau_D T_{\text{pwm}}$ is added to obtain m_r. This time delay can be due to the algorithm execution time, delays in the sensing and driver circuits, etc. The procedure above is illustrated in Fig. 5 for an inductor current

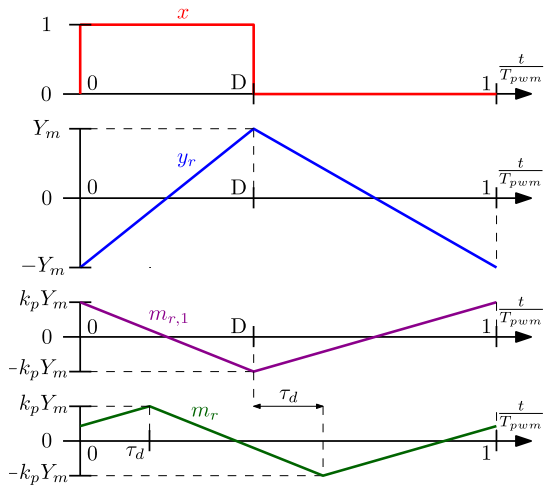

Fig. 5. Example of modulating waveform ripple, $m_r(t)$, for purely proportional inductor current control with gain k_p and a relative delay equal to τ_D.

loop of a two-level converter with negligible output voltage dynamics, without feedback filters, and with a proportional controller with gain k_p.

Based on m_r and D, the complete naturally sampled modulating waveform m_{n-s} can be calculated relative to the carrier, using the procedure described in [7]. Note that this waveform can be calculated analytically, without any iteration. To obtain the actually present uniformly sampled piecewise constant, $m(t)$, an iterative procedure described in [7] can be used. From the assumed steady-state value of D and the average value of the calculated m, one point of the transcharacteristic is obtained. The entire MS-PWM transcharacteristic is derived using the procedure above for $D \in [0, 1]$.

B. Modulating Waveform in Two-Level Current-Controlled Converters

The results in this article are focused on the inductor current control. This is due to the fact that the direct duty-cycle control of the output voltage is rarely implemented in converters with LC output filters. Furthermore, this article provides numerical results for a class of converters with equivalent modulating waveform, such as half-bridge or full-bridge buck converters or single-phase inverters. Note, however, that subsequent results can be found likewise for any converter topology or feedback variable.

In order to provide results that are of general use, the following reasoning is made. First of all, for current control loops with triangular switching ripple, the steady-state peak-to-peak magnitude of the modulating waveform Δm_{p-p} can be very closely approximated as proportional to the designed relative crossover frequency $f_{c,r}$, independently from hardware parameters [7]

$$\Delta m_{p-p} \approx k_p \Delta Y \sim f_c L \Delta Y \sim \frac{f_c}{f_{\text{pwm}}} = f_{c,r} \qquad (1)$$

where ΔY is the peak-to-peak magnitude of the inductor current and f_c is the designed crossover frequency. Approximation (1) allows the investigation of the MS-PWM nonlinearities in a

scalable way, by varying only the relative crossover frequency. Note that, for LC output filters where the resonant frequency is near the crossover frequency, the actual crossover frequency may slightly differ from the designed value used to calculate k_p [3]. In those cases, the subsequent analysis is actually dependent on the designed value f_c and not the actually obtained one.

Besides this, the most important parameter that impacts discontinuity-related effects is the time delay present in the control system. This dependence comes from the fact that intersections between m and w are determined by the shape of the sampled modulating waveform, which changes as the switching ripple component is shifted with respect to the carrier. The structural delays can vary significantly from one converter to another, depending on the hardware circuitry, algorithm execution time, present filtering, and similar. Furthermore, by showing the results as a function of the time delay, the impact of feedback filters and other parts of the controller structure may also be examined by representing those as an equivalent gain and time delay, while the transcharacteristics are derived for a purely proportional controller without any feedback filter. For better generality, the analysis is normalized with respect to the switching period.

C. Critical Duty Cycles and Critical Modulating Segments

For the triangular carrier, due to the imposed synchronization between m and w, vertical intersections may occur only when the normalized value of w is equal to $\frac{2i}{N}$, where $1 \leq i < \frac{N}{2}$ and i is an integer. Assuming that switching instants for both slopes of w occur for a similar value of w, the duty cycle in the presence of vertical crossings is close to the value of $\frac{2i}{N}$. This operating point is defined as the *critical duty cycle*. Nonlinearity zones in transcharacteristics are located around these points. For a given N, *critical duty cycles* can be found using

$$D_c = \frac{2i}{N} \quad , \quad 1 \leq i < \frac{N}{2}. \tag{2}$$

Note that exact operating points for which the vertical intersections occur span a certain range around D_c.

The *critical modulating segments* can be defined as in [17]. Intuitively, these are the two adjacent segments of m before and after the update instant closest to the intersection between w and m, as shown in Fig. 3. Around each D_c, there are two pairs of critical modulating segments: one for the positive and the other for the negative slope of the carrier. Given that the MS-PWM nonlinearities are introduced due to vertical crossings, with an extent determined by the discontinuity of m [7], [17], it is of interest to calculate the discontinuities of critical modulating segments for both positive ($\Delta m_{c,u}$) and negative ($\Delta m_{c,d}$) slopes of w

$$\begin{aligned} \Delta m_{c,u} &= m(T_{c,u} + \epsilon) - m(T_{c,u} - \epsilon) \\ \Delta m_{c,d} &= m(T_{c,d} - \epsilon) - m(T_{c,d} + \epsilon) \end{aligned} \tag{3}$$

where ϵ is an infinitely small positive number and $T_{c,u}$ and $T_{c,d}$ are the modulating waveform update instants closest to the intersection with the carrier. The signs in (3) are chosen so that a positive value of $\Delta m_{c,u,d}$ always corresponds to in-phase condition.

As pointed out in [17], around each D_c, the in-phase discontinuity of critical modulating segments determines the height of the jitter zone in an MS-PWM transcharacteristic. As each slope of the carrier contributes to the total duty cycle with factor $\frac{1}{2}$, each in-phase Δm_c will contribute to its respective jitter zone height as $\delta_\infty = \frac{\Delta m_c}{2}$ [17]. For the case when the in-phase regime is enabled for both slopes of the carrier, the joined height of the jitter zones around the observed D_c can be estimated as

$$\Delta D_\infty = \frac{\Delta m_{c,u}}{2} + \frac{\Delta m_{c,d}}{2}. \tag{4}$$

Also, for the counter-phase vertical crossings, the size of the discontinuity of critical modulating segments is correlated with the extension of reduced- and zero-gain zones. Therefore, it is of interest to find a way to easily determine whether the control system design enables in-phase or counter-phase operation and to predict the size of related discontinuities.

D. Discontinuity Graphs

In this section, the discontinuity graphs are provided to illustrate the change of $\Delta m_{c,u,d}$, for various control loop bandwidths, as a function of time delay. Due to the periodicity of the switching ripple, it is sufficient to show results in the range $\tau_D \in [0, 1]$. The results are given for $N \in \{4, 6, 8\}$ as modulating waveform discontinuities are reduced with the increase of the oversampling factor [7], [17]. The maximum achievable N depends on the available processing power relative to the switching frequency. Some application scenarios are more likely to allow high values of N (e.g., high-power converters) than others (e.g., high-switching-frequency converters). For very high values of N, the discontinuities are strongly reduced as sampled feedback closely resembles the continuous analog signal.

The discontinuity graphs are obtained for each pair of (N, D_c), by calculating m only for $D = D_c$. As previously noted, the vertical crossings appear also in the vicinity of these duty cycles, but it is of interest to see how this simple analytical procedure can be used to predict the properties of MS-PWM transcharacteristics. As stated in Section IV-A, for the exact calculation of m, an iterative procedure is needed. However, an approximated method is proposed here, which reveals discontinuities by solving a set of equations, i.e., without any iteration. This is performed by calculating the naturally sampled equivalent, m_{n-s}, as described in Section IV-A. After this, N sampling instants are assumed, starting from when $w = 1$ and separated by T_s. This approximation slightly shifts the switching instants with respect to the exact calculation. The obtained resampled version of m_{n-s} is then used to calculate the discontinuities $\Delta m_{c,u,d}$ as in (3).

Note that, due to symmetry of the triangular switching ripple, the discontinuity graphs for $D = D_c$ for the positive slope of w are the same as the discontinuity graphs for $D = 1 - D_c$ for the negative slope of w. That is why, for $D_c = \frac{1}{2}$, the discontinuity graphs for positive and negative slopes are always equal.

The results for $N = 4$ and $D_c = \frac{1}{2}$ are shown in Fig. 6. In this figure, a comparison is given for different values of $f_{c,r}$. It

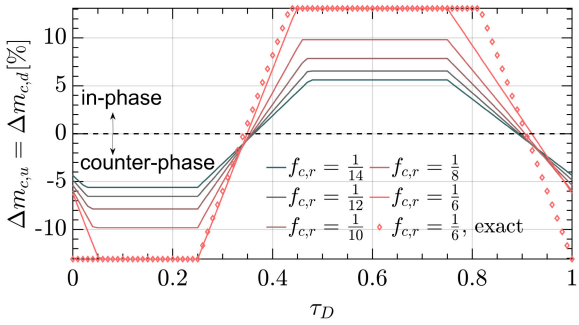

Fig. 6. Discontinuity graphs for $N = 4$ and $D_c = \frac{1}{2}$. The graphs are obtained using the approximated procedure for several values of $f_{c,r}$. The result for $f_{c,r} = \frac{1}{6}$ is compared with the result obtained using the exact procedure.

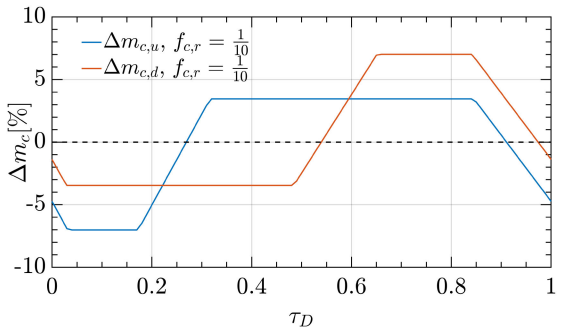

Fig. 7. Discontinuity graphs for $N = 6$ and $D_c = \frac{1}{3}$. The graphs are obtained using the approximated procedure for $f_{c,r} = \frac{1}{10}$.

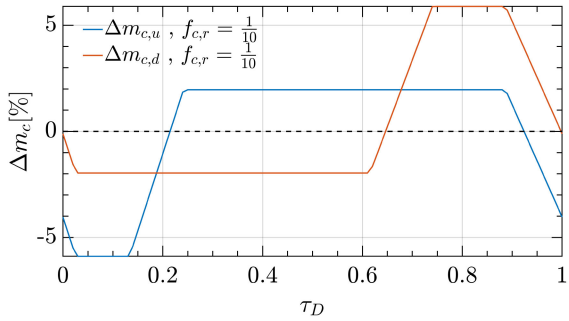

Fig. 8. Discontinuity graphs for $N = 8$ and $D_c = \frac{1}{4}$. The graphs are obtained using the approximated procedure for $f_{c,r} = \frac{1}{10}$.

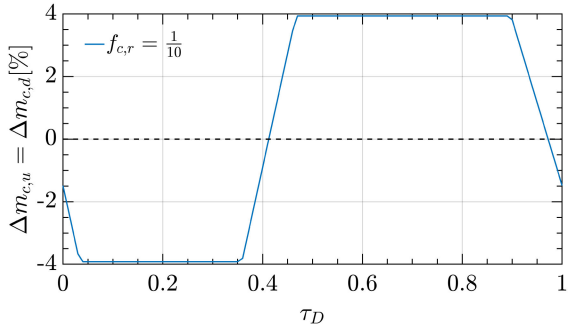

Fig. 9. Discontinuity graphs for $N = 8$ and $D_c = \frac{1}{2}$. The graphs are obtained using the approximated procedure for $f_{c,r} = \frac{1}{10}$.

can be seen that Δm_c is indeed proportional to this parameter. The graphs show that there is a range of time delays, for which the size of discontinuities varies linearly, and a range for which it is constant. For the case of $f_{c,r} = \frac{1}{6}$, a comparison is made with the exact iterative calculation of m. The resulting values in the flat region are perfectly matched, while a small mismatch is seen elsewhere. For the article conciseness, other discontinuity graphs do not feature comparison with the exact procedure; however, it is verified that the mismatch remains practically of the same entity. An important thing to note is the existence of two values of τ_D, almost independent on the relative crossover frequency, for which the operation turns from counter-phase to in-phase. For $N = 4$ and $D_c = \frac{1}{2}$, these values of τ_D are unique for both slopes of w, which is important as it indicates that the existence of such τ_D flattens out both pairs of critical modulating segments, thus preventing any vertical crossings from occurring.

For clarity of presentation, results for other values of (N, D_c) are given only for $f_{c,r} = \frac{1}{10}$. It is verified that with the change of $f_{c,r}$, conclusions remain the same as for $N = 4$; the values of discontinuities are scaled, while the borders between in-phase and counter-phase remain located at nearly constant values of τ_D.

In Fig. 7, discontinuity graphs are given for $N = 6$ and $D_c = \frac{1}{3}$. The results are not shown for $N = 6$ and $D_c = \frac{2}{3}$ as the two discontinuity graphs are symmetrical. It can be seen that the sum of maximum discontinuities for the positive and negative slopes of w is scaled by a factor $\frac{4}{6}$ compared to $N = 4$, which indicates that the increase in N suppresses the problems related to discontinuities.

In Fig. 8, discontinuity graphs are given for $N = 8$ and $D_c = \frac{1}{4}$, yielding similar conclusions as for $N = 6$ and $D_c = \frac{1}{3}$. In Fig. 9, the discontinuity graph, valid for both slopes of the carrier, is given for $N = 8$ and $D_c = \frac{1}{2}$. As for $N = 4$ and $D_c = \frac{1}{2}$, there are two values of time delay τ_D, which result in a borderline operation between in-phase and counter-phase regimes.

An important thing to notice is that for critical duty cycles other than $D_c = \frac{1}{2}$, there is no unique time delay that results in borderline operation between in-phase and counter-phase for both slopes of the carrier. This means that, unlike for $D_c = \frac{1}{2}$, there is no value of τ_D that can flatten out both pairs of critical modulating segments.

To verify predictions of discontinuity graphs, which are calculated only for $D = D_c$, on the MS-PWM operation around the analyzed operating point, three examples of modulator transcharacteristics are given in Fig. 10, for the case of $N = 4$, $D_c = \frac{1}{2}$, and $f_{c,r} = \frac{1}{10}$. The time delay is chosen to emphasize the counter-phase regime ($\tau_D = 0.1$), the in-phase regime ($\tau_D = 0.5$), as well as the border line between these two regimes ($\tau_D = 0.347$). As predicted by the discontinuity graph, the MS-PWM transcharacteristics for $N = 4$ can be completely linearized by imposing an appropriate time delay. Regarding the in-phase regime, as seen in Fig. 10 for $\tau_d = 0.5$, the vertical part of the transcharacteristic matches with the value obtained using (4) and the discontinuity graph shown in Fig. 6. For the case reported in Fig. 10, two jitter zones corresponding to the positive and negative slopes of w are merged. Note that the

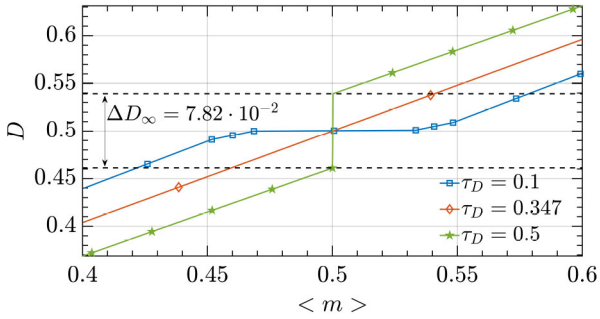

Fig. 10. Demonstration of the impact of τ_D on the MS-PWM nonlinearities for $N = 4$, $D_c = \frac{1}{2}$, and $f_{c,r} = \frac{1}{10}$. The transcharacteristics are given for the counter-phase regime (squares), which features reduced and zero-gain zones, the in-phase regime (stars), which features a jitter zone, and the border-line case (diamonds), which results in a linear transcharacteristic.

match between jitter zone heights and the values predicted by the discontinuity graphs is confirmed for other values of (N, D_c) as well.

To conclude, the discontinuity graphs represent valuable means of predicting the MS-PWM behavior due to the following facts.

1) They are easily calculated by solving a set of differential equations, without any iteration, for a single operating point.
2) They can be used to find a border line between counter-phase and in-phase operation, which remains nearly constant while changing the relative crossover frequency $f_{c,r}$.
3) They can be used to quantify the height of the jitter zone in case of the in-phase operation.

V. Analysis of MS-PWM Transcharacteristics Using Nonlinearity Measures

Complete MS-PWM transcharacteristics can be obtained using the iterative procedure described in Section IV-A. This section examines and quantifies nonlinearities of transcharacteristics, depending on the time delay introduced in the system. Besides a standard measure of nonlinearity, the appearance and extension of each of the nonlinear zones are also provided. The provisions remain the same as explained in Section IV-B.

A. Measures of MS-PWM Nonlinearity

As for the discontinuity graphs, the following results are given as functions of the time delay. In this way, it is possible to find the value of time delay that minimizes a certain measure of nonlinearity. The nonlinearities of MS-PWM transcharacteristics are examined using two measures.

Let the MS-PWM transcharacteristics be labeled as $G = D(< \mathrm{m} >)$. The nonlinearity measures of G used in this article are the following.

1) Root-mean-square (RMS) measure calculated as RMS $(G - L(G))$, where $L(G)$ represents the linear regression of G, obtained using the least-squares error criterion. This standard measure of nonlinearity tells how close is G to the nearest possible straight line. However, it does not discriminate different types of nonlinearities, which may be important for specific applications.
2) Modified differential nonlinearity (M-DNL). This measure discriminates different nonlinearity zones in a transcharacteristic and offers their relative extensions. Standard differential nonlinearity measure, obtained as $\mathrm{DNL} = \max\{|\frac{dG}{d<\mathrm{m}>} - 1|\}$ is not useful as crucial information on the relative extension of each zone is not provided. As explained before, and seen in Fig. 4, there are only three possible types of nonlinearity zones. M-DNL shows which one is present and to what extent. For each piecewise linear G, different zones are detected, and their total relative extensions are plotted: $\Delta< \mathrm{m} >_{\frac{1}{2}}$ is the total span of $< \mathrm{m} >$ for which G features a slope close to $\frac{1}{2}$ (reduced-gain zone); $\Delta< \mathrm{m} >_0$ is the total span of $< \mathrm{m} >$ for which G features a slope equal to 0 (zero-gain zone); $\Delta \mathrm{D}_\infty$ is the total span of D for which G is vertical (infinite-gain zone).

In order to separately analyze each D_c, the RMS measure and M-DNL are calculated for ΔD around each D_c, such that the related nonlinearities are fully covered.

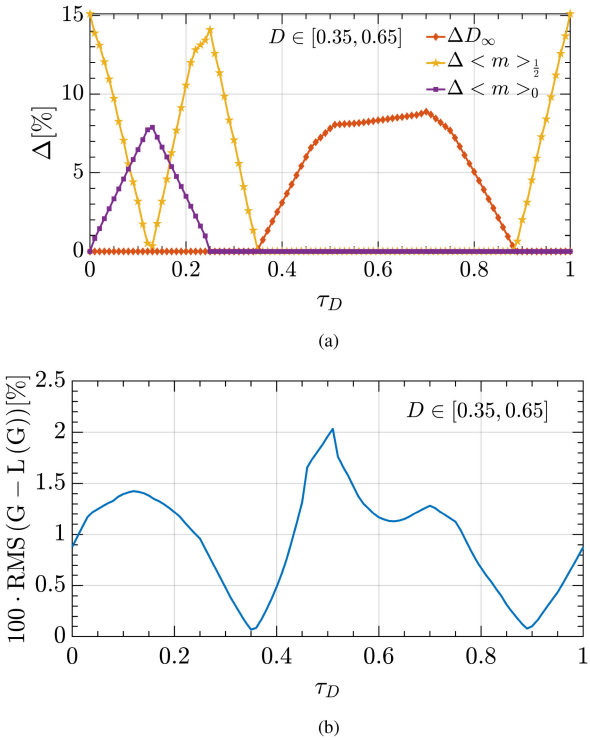

Fig. 11. Nonlinearity measures for $N = 4$, $D \in [0.35, 0.65]$, and $f_{c,r} = \frac{1}{10}$. (a) M-DNL. (b) RMS measure.

B. Nonlinearity Graphs

For each analyzed N, transcharacteristics are calculated for $\tau_D \in [0, 1]$ with 1% resolution and the duty-cycle resolution of 0.1%. The results are given for $f_{c,r} = \frac{1}{10}$.

In Fig. 11, M-DNL and RMS measures are given for $N = 4$ around $D_c = \frac{1}{2}$. From Fig. 11(a), it can be seen that the infinite-gain zones occur approximately for $\tau_D \in (0.35, 0.89)$. There,

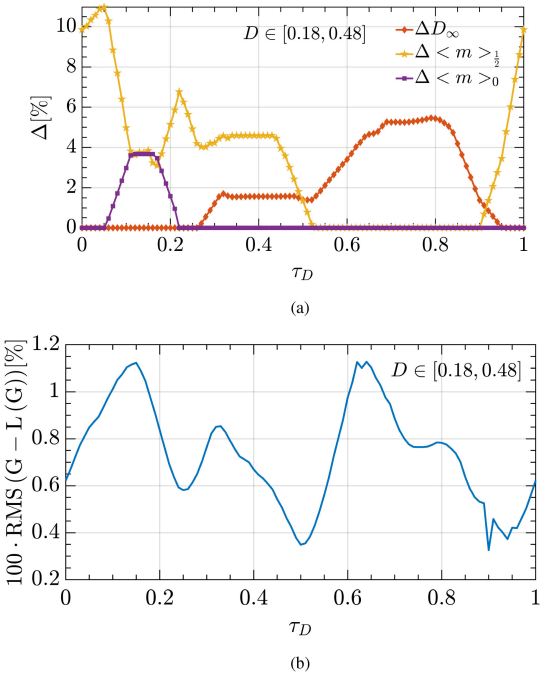

Fig. 12. Nonlinearity measures for $N = 6$, $D \in [0.18, 0.48]$, and $f_{c,r} = \frac{1}{10}$. (a) M-DNL. (b) RMS measure.

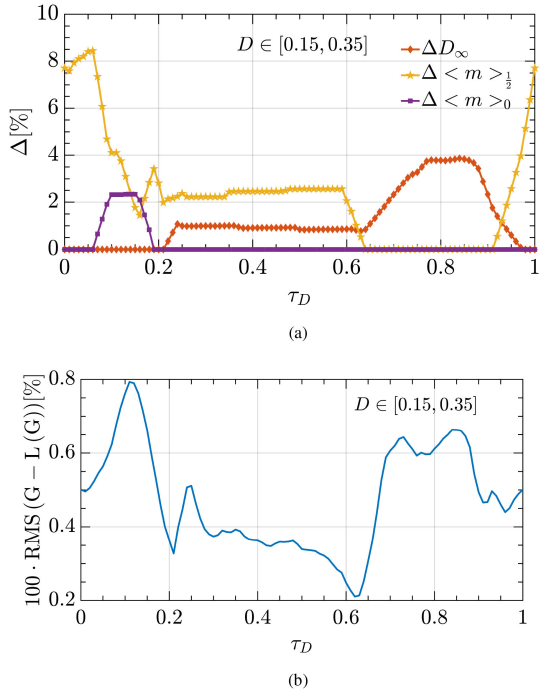

Fig. 13. Nonlinearity measures for $N = 8$, $D \in [0.15, 0.35]$, and $f_{c,r} = \frac{1}{10}$. (a) M-DNL. (b) RMS measure.

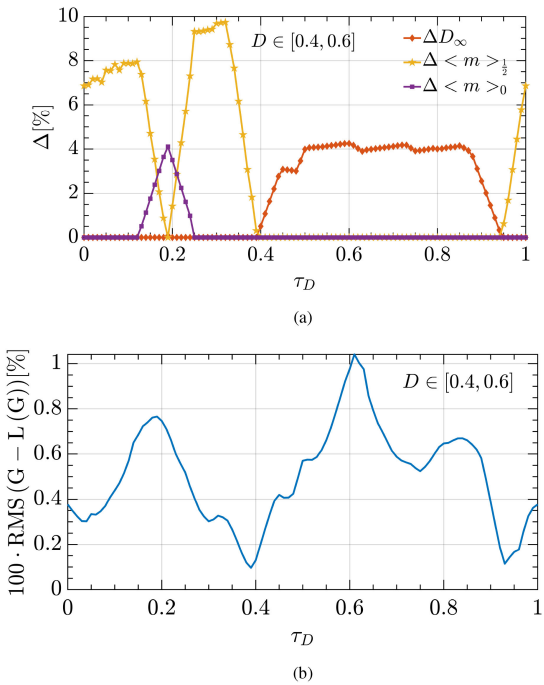

Fig. 14. Nonlinearity measures for $N = 8$, $D \in [0.4, 0.6]$, and $f_{c,r} = \frac{1}{10}$. (a) M-DNL. (b) RMS measure.

the values of ΔD_∞ are in excellent match with the values obtained using (4) and the discontinuity graph seen in Fig. 6. Note that M-DNL does not discriminate whether the jitter zones for positive and negative slopes of w are merged into a single jitter zone, but only shows their joined height. It is also visible that zero-gain zone has the highest extent for $\tau_D \approx 0.13$. There are regions around $\tau_D = 0.3$ and $\tau_D = 0.95$, where reduced-gain is the only nonlinearity. For dc–dc converters, these regions are favorable as there are no uncontrollable operating points due to zero-gain zones and no LCOs due to infinite-gain zones of the transcharacteristics. From Fig. 11(b), it is clear that the border between counter-phase and in-phase operation ($\tau_D \approx 0.35$ and $\tau_D \approx 0.89$) results in the lowest RMS measure. Due to the finite resolution of τ_D, the plot only gets to show RMS values close, but not exactly equal to 0.

In Fig. 12, M-DNL and RMS measures are given for $N = 6$ around $D_c = \frac{1}{3}$. Note that, due to the symmetry mentioned in Section IV-D, these results are also valid around $D_c = \frac{2}{3}$. From Fig. 12(b), it can be seen that the local minimums are found near the values of τ_D, where, for one slope of the carrier, there is a transition between counter-phase and in-phase regimes. The minimization of the modulator nonlinearity near these border lines is intuitive, as it corresponds to the flattening of one critical modulating segment pair. These border-line values of τ_D can also be read from the discontinuity graph in Fig. 7. In Fig. 13, M-DNL and RMS measures are given for $N = 8$ around $D_c = \frac{1}{4}$ that are, thanks to symmetry, also valid for $D_c = \frac{3}{4}$. The conclusions are the same as for $N = 6$ and $D_c = \frac{1}{3}$. In Fig. 14, M-DNL and RMS measures are given for $N = 8$ around $D_c = \frac{1}{2}$. The conclusions are the same as for $N = 4$ and $D_c = \frac{1}{2}$. There are two values of time delay, $\tau_D \approx 0.39$ and $\tau_D \approx 0.95$, for which the transcharacteristic can be completely linearized locally. Again, these are not precisely obtained here due to the resolution of τ_D.

From the presented results, it is clear that the increase in N results in lower nonlinearity measures. It should be noted that the nonlinearity measures are also calculated for several other values of $f_{c,r}$, and the results follow the same trends as

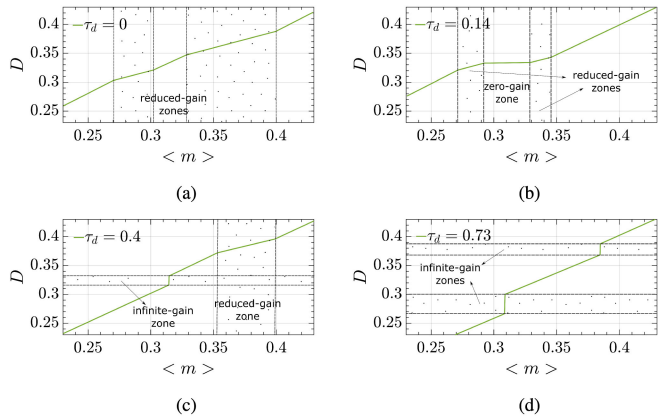

Fig. 15. Examples of transcharacteristics for $N = 6$ around $D = \frac{1}{3}$ for four values of τ_D. Each subfigure corresponds to a different combination of nonlinearity zones, as seen in Fig. 12(a).

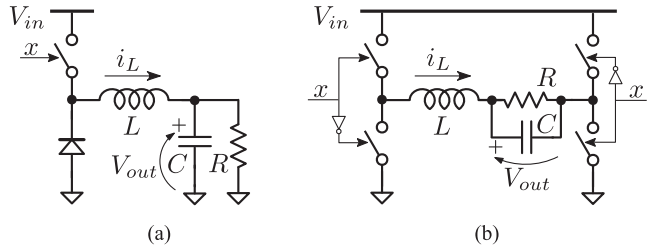

Fig. 16. Converters used for verification of nonlinearities. (a) Buck-type converter. (b) Single-phase inverter.

TABLE I
HARDWARE PARAMETERS

Description	label	value	unit
Input voltage	V_{in}	400	V
Nominal power	P_n	3	kW
Switching frequency	f_{pwm}	20	kHz
Filter inductance	L	1.53	mH
Output capacitance	C	20	μF
Output resistor	R	47	Ω

those reported above. Reduced-gain, zero-gain, and infinite-gain zones are present in nearly the same range of τ_D, while their extensions are scaled proportionally to $f_{c,r}$.

The dependence of nonlinearity measures on time delay allows for an easy prediction of MS-PWM behavior for existing delays in the system, e.g., for verification if dead-bands or jitter zones will appear. Furthermore, the results can be used to minimize the nonlinearities by imposing an additional time delay. This is legitimate if structural delays of the system are below the desired value, also considering the resulting impact on the dynamic response. Note that it might not be optimal to add a pure time delay as a compensation measure. Instead, low-pass filters may be used, such that the same effect on the shape of m is achieved, but with a more favorable impact on the dynamic performance. This is a topic of future research.

To illustrate each of the distinct regions seen in the M-DNL graph in Fig. 12(a), transcharacteristics corresponding to different values of τ_D are plotted in Fig. 15.

VI. Experimental Verification

The impact of MS-PWM nonlinearities on a power converter's operation is strongly dependent on the entire closed-loop control system. As noted in Section V, higher controller gains result in higher nonlinearity measures, but also in a higher disturbance rejection, which should mitigate the final impact on the converter's output. Therefore, this section offers an experimental examination of MS-PWM nonlinearities in typical application scenarios. For dc–dc converters, it is important to investigate the impact on the transient response and occurrence of LCOs. For ac-type converters, it is important to examine the impact on the output waveform distortion.

For experimental verification, an industrial full-bridge converter with a resistive load is used for both dc–dc and dc–ac tests. For dc–dc operation, a nonsynchronous half-bridge buck converter is formed. The passive component sizing is a compromise between these two applications. The switching frequency is chosen based on the used insulated-gate bipolar transistors and the inductor core. The two tested converter configurations are shown in Fig. 16. The hardware parameters are shown in Table I.

The control system is implemented on an NI sbRIO-9606, which is based on a Xilinix Zynq 7020 all programmable system on chip. The inductor current is sensed by a custom interfacing board, based on a shunt resistor. The analog RC antialiasing filter features a time constant of 300 ns. The board uses conditioning circuits, a 12-bit ADC module AD9226 by Analog Devices, and digital isolators. The ADC quantization corresponds to $\text{LSB}_i = 17$ mA. The DPWM clock runs at 160 MHz. For postprocessing, data are acquired with a 25 MS/s rate, using the Tektronix MS056 oscilloscope. The inductor current is sensed using Tektronix TCP202 current probe. For total harmonic distortion (THD) calculations, 100 ms of data is acquired.

The FPGA platform reads the ADC output with a rate of 40 MHz. This allows the addition of τ_D with a resolution of 0.05%, using a delay line. Structural delays in the setup include 700 ns due to the algorithm computation and 1.5 μs due to hardware delays from current sensing to transistor gate voltage. The modulating waveform is updated as soon as the control action is calculated. The current sampling instants are rescheduled to compensate the algorithm computation time. In this way, the modulating waveform update instants are synchronized with the carrier, as explained in Section III. The transcharacteristics are experimentally obtained by imposing a current reference sweep while saving the values of the modulating waveform and the detected duty cycle from the FPGA. The experimentally obtained transcharacteristics are filtered by averaging results from ten consecutive switching periods.

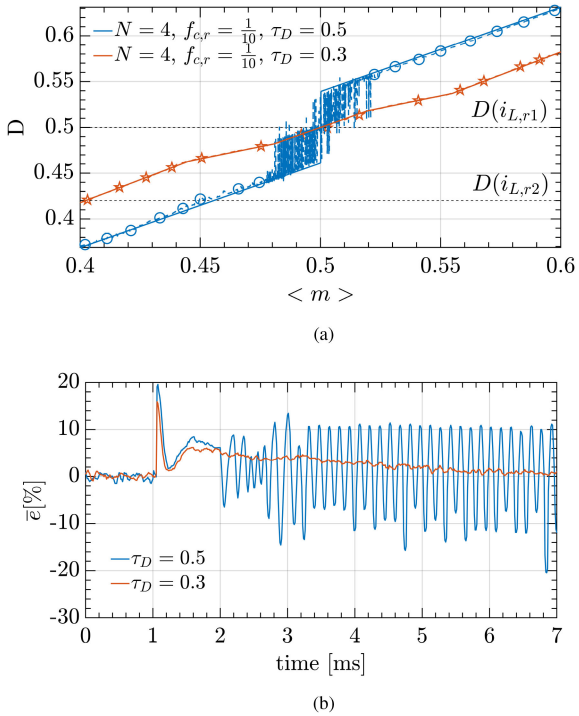

Fig. 17. Operation of a buck converter described in Table I, for $N = 4$, and two values of τ_D. (a) Experimental verification (dashed line with markers) of calculated transcharacteristics corresponding to $\tau_D = 0.5$ (circles) and to $\tau_D = 0.3$ (stars). (b) Corresponding relative current errors of step responses from $D(i_{L,r1}) = 0.42$ to $D(i_{L,r2}) = 0.5$. The switching ripple is filtered out for a better visualization.

A. Impact of Nonlinearities in DC–DC Converters

To verify the impact of nonlinearities on a dc–dc power converter's operation, the converter described in Table I is configured as shown in Fig. 16(a). The implemented controller is a proportional–integral controller and the crossover frequency of the current loop is chosen as $f_c = \frac{1}{10} f_{\text{pwm}}$. The proportional gain is calculated based on the desired crossover frequency as $k_p = 2\pi f_c \frac{L}{V_{\text{in}}} = 0.048\ \text{A}^{-1}$. The integral gain k_i is set equal to 151 $\text{A}^{-1} \cdot \text{s}^{-1}$, to avoid additional crossover before the LC resonance. Note that this kind of control loop is directly compared with the previously shown nonlinearity graphs, which are calculated for a proportional controller. The impact of the integral part at frequencies of switching harmonics is not large; hence, a good match is expected.

For dc–dc converters, it is instructive to verify the jittering operation, which appears when the operating point enters the infinite-gain zone of the MS-PWM transcharacteristics. This operation is problematic because it results in LCOs, which cannot be suppressed by feedback. For this test, the control loop is organized so that $N = 4$ and $\tau_D = 0.5$. From Fig. 11(a), it can be seen that this time delay results in $\Delta D_\infty = 7.82\%$. As a benchmark, results are also shown for $\tau_D = 0.3$, which brings the presence of reduced-gain zones. The transcharacteristics belonging to these settings are shown in Fig. 17(a). The experimentally obtained points of the infinite-gain zone of the transcharacteristic are presented without averaging. The jittering operation is tested by imposing a step reference change, such that the steady-state duty cycle goes from unity-gain part, $D(i_{L,r1}) = 0.42$, to the infinite-gain part, $D(i_{L,r2}) = 0.5$. The tracking errors, relative to the dc value of current, are shown in Fig. 17(b). For visualization, the switching ripple is removed using an MAF over the switching period. Starting from $t = 2$ ms, the LCO occurrence is clearly seen for the case of $\tau_D = 0.5$.

It is of interest to see whether the nonlinearity graphs can be used to predict the impact of LCOs. For this, it is possible to correlate the variance of the duty cycle σ_D^2 with the height of the jitter zone ΔD_∞ [17]:

$$\sigma_D^2 = \frac{1}{2}\left[(D_1 - \mu(D))^2 + (D_2 - \mu(D))^2\right] \approx \frac{\Delta D_\infty^2}{4} \quad (5)$$

where D_1 and D_2 are the jitter zone borders. The approximated value is obtained by assuming that the expected value of the duty cycle, $\mu(D)$, is controlled by the current loop so that $\mu(D) \approx D_c$, and that $D_1 = D_c + \frac{\Delta D_\infty}{2}$ and $D_2 = D_c - \frac{\Delta D_\infty}{2}$. Using (5) and jitter zone height from the nonlinearity graph in Fig. 11(a), the predicted value of the duty-cycle variance is 1.53×10^{-3}. The experimentally obtained variance is equal to 1.7×10^{-3}, which is in a good match with the prediction.

A steady-state operation with and without the LCOs can be seen in the active contents submitted with this article, under the name *dc_dc_jittering.mp4*.

Regarding the impact of the nonlinearities on dc–dc converters in zones where the modulator gain is reduced, several examples are given in [7] and [10]. The impact of reduced- and, especially, zero-gain zones on response to small- and large-signal perturbations is very difficult to analyze in a general form. The response will be certainly affected and deteriorated, but a quantitative analysis is only possible case by case. Nonlinearity graphs can be used to find a suitable value of the time delay that minimizes the extension of reduced- and zero-gain zones, which would, consequently, result in a smaller impact on the converter's operation.

B. Impact of Nonlinearities in AC-Type Converters

For the verification of the nonlinearities' impact on an ac-type power converter, the hardware setup described in Table I is reconfigured as in Fig. 16(b). The operating parameters are summarized in Table II. The inverter operates using the bipolar modulation with dead times set to 1%. Due to the RLC load, the output voltage lags the inductor current by 16° at the fundamental frequency. It should be noted that simulations were performed also for the case of an inductive filter directly connected to an ac voltage source, and the conclusions remain the same as reported below. For the ac-type tests, the controller features a proportional–resonant (PR) structure, discretized using the impulse-invariant method [23]

$$G_{c,\text{PR}}(z) = k_p + k_r T_s \frac{1 - \cos(2\pi f_1 T_s) z^{-1}}{1 - 2\cos(2\pi f_1 T_s) z^{-1} + z^{-2}} \quad (6)$$

where f_1 is the fundamental frequency. The proportional gain is calculated based on the desired crossover frequency as $k_p = 2\pi f_c \frac{L}{2V_{in}}$, while the resonant gain k_r is calculated as $\frac{k_r}{k_p} = \frac{1}{10} 2\pi f_c$ [3].

TABLE II
SUMMARY OF THE DC–AC CONVERTER RESULTS

Description	label	value	unit
Output frequency	f_1	50	Hz
Output voltage - RMS	V_{out}	230	V
Output current - RMS	I_L	4.9	A
Dead time	/	500	ns
Proportional gains	k_p	$\{0.017, 0.024, 0.04\}$	$\frac{1}{A}$
Resonant gains	k_r	$\{15.4, 30.2, 83.9\}$	$\frac{1}{As}$
Relative crossover frequencies	$f_{c,r}$	$\{\frac{1}{14}, \frac{1}{10}, \frac{1}{6}\}$	/
$N = 2$ - benchmark case	label	value	unit
Added delays	τ_D	0	/
Total harmonic distortion	THD	$-\{38.1, 39.8, 42.6\}$	dB
$N = 4$ - nonlinear transch.	label	value	unit
Added delays	τ_D	$\{0.1, 0.1, 0.1\}$	/
Total harmonic distortion	THD	$-\{24.9, 24, 24.1\}$	dB
$N = 4$ - linearized transch.	label	value	unit
Added delays	τ_D	$\{0.354, 0.347, 0.332\}$	/
Total harmonic distortion	THD	$-\{38.5, 39.5, 41.2\}$	dB

For ac-type converters, it is important to investigate the impact on the output waveform distortion. As noted in Section V, the extension of the nonlinearity zones is proportional to the crossover frequency; however, the disturbance rejection also depends on it. Therefore, it is not possible to conclude that the increase of the presented nonlinearity measures, by increasing the bandwidth, would result in a worse quality of the output waveform. Nonetheless, for a defined crossover frequency, nonlinearity graphs can be used to find an optimal τ_D regarding distortion.

As the dead time is a significant source of distortion in ac-type converters [3], the impact of MS-PWM nonlinearities cannot be observed on its own, except in simulations with the dead time set to zero. Therefore, the double-update case ($N = 2$) is used as a benchmark. The designed control loops for $N = 2$ and $N = 4$ feature similar disturbance rejection properties; hence, the differences between these two values of N can be ascribed to the MS-PWM sources of distortion.

The first goal of this subsection is to show that the analyzed nonlinearities in the transcharacteristics are the dominant sources of distortion in MS-PWM-controlled converters. This is tested by providing results for $f_{c,r} \in \{\frac{1}{14}, \frac{1}{10}, \frac{1}{6}\}$ and two sets of transcharacteristics related to $N = 4$. The first set is obtained by imposing a time delay $\tau_D = 0.1$, which results in reduced- and zero-gain zones being present. The experimental verification of these transcharacteristics is shown in Fig. 18. The second set is obtained by adding time delays $\tau_D = \{0.354, 0.347, 0.332\}$, respectively, to the above noted values of $f_{c,r}$. These delays result in linear transcharacteristics, such as the one in Fig. 10. The experimental verification of the linearized transcharacteristics

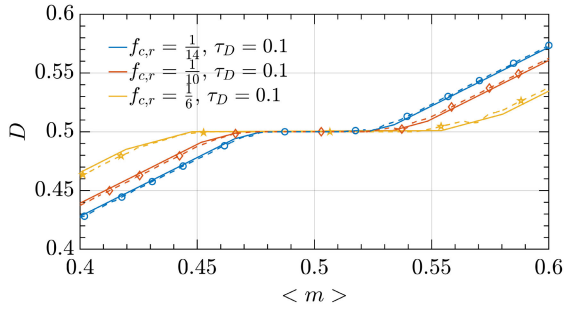

Fig. 18. Experimental verification (dashed line with markers) of calculated transcharacteristics for $\tau_D = 0.1$ and $f_{c,r} = \{\frac{1}{14}, \frac{1}{10}, \frac{1}{6}\}$. The increase of the relative crossover frequency increases the extension of the nonlinearity zones.

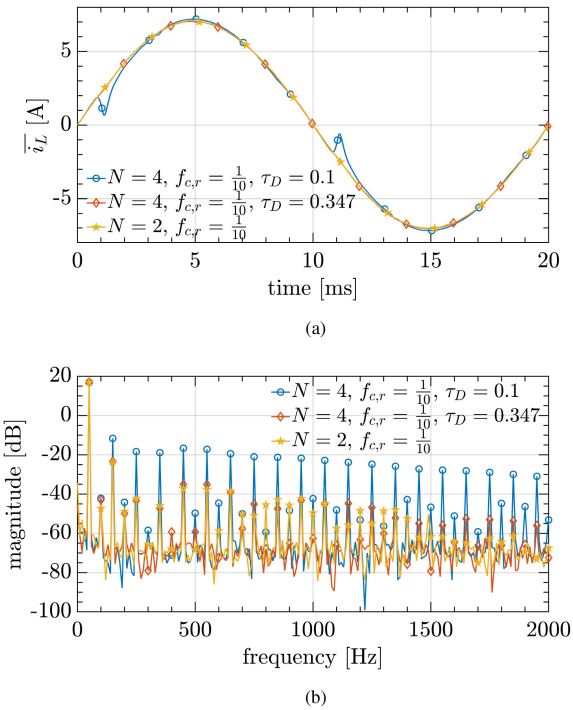

Fig. 19. Example of the inductor current distortion for the single-phase inverter described in Tables I and II. The comparison is made for $f_{c,r} = \frac{1}{10}$ between the double-update case and the cases with $N = 4$ for $\tau_D = 0.1$ and $\tau_D = 0.347$. (a) Time-domain inductor current waveforms. (b) Spectral content in the frequency window used for THD calculations.

is not shown due to article length limitations. The time-domain inductor currents and their spectra can be seen in Fig. 19, for $f_{c,r} = \frac{1}{10}$. For time-domain visualization, the inductor current is averaged over T_{pwm} using an MAF. These results are compared to the benchmark case of the double-update control, which does not feature any of the MS-PWM nonlinearities. It can be seen that for $N = 4$ and $\tau_D = 0.1$, the current is strongly distorted around zero-crossings, and the presence of strong odd harmonics is seen in the spectrum. When the time delay $\tau_D = 0.347$ is applied, the current distortion is significantly improved, and the difference compared to double-update case is practically not visible. This is confirmed by the THD calculations, performed up to the 40th harmonic, which are shown in Table II. These values confirm that the only remaining noticeable distortion is caused by the dead time. The THD is suppressed by 15 dB

by adding the appropriate time delay. The impact of properly added time delay for $N = 4$ and comparison with $N = 2$ is shown in the active contents submitted with this article, under the name $dc\_ac\_distortion.mp4$. Differently from what was concluded in [18], our analysis and experiments suggest that the aliasing effect is not originating the measured distortion. Quite on the contrary, this appears to be a second-order effect, negligible in size with respect to effects of dead times and the nonlinear transcharacteristic. The aliasing-based distortion was noticed only in simulations with linearized transcharacteristic and without any dead times.

The second goal of this subsection is to show that higher nonlinearity measures do not necessarily result in a higher distortion, if the control bandwidth is increased as well. This is tested by comparing the THD results for $N = 4$, $\tau_D = 0.1$, and $f_{c,r} \in \{\frac{1}{14}, \frac{1}{10}, \frac{1}{6}\}$. The relative extensions of reduced- and zero-gain zones can be seen in Fig. 11(a) for $f_{c,r} = \frac{1}{10}$. For different values of $f_{c,r}$, the relative extensions are proportionally scaled. These are calculated and their values are equal to $\Delta< \mathrm{m} >_{\frac{1}{2}} \in \{2.13, 3.18, 5.42\}\%$ and $\Delta< \mathrm{m} >_0 \in \{4.68, 6.47, 10.66\}\%$, respectively, to the tested $f_{c,r}$. The obtained values of THD are equal to $\{-24.9, -24, -24.1\}$ dB, respectively, to the tested $f_{c,r}$. The resulting values of THD are similar, which confirms that the feedback is capable of suppressing the distortion related to nonlinearities in transcharacteristics.

For values of N other than 4, the transcharacteristic cannot be completely linearized by modifying the time delay; however, the resulting distortion can be minimized. As the nonlinearity graphs are given locally, around each D_c, they do not provide means for a global optimization, i.e., if the operating point perturbs across all values of D_c. In case when full-range optimization is required, the nonlinearity measures can be calculated for $D \in [0, 1]$. The other option is to use the presented nonlinearity graphs to find a value of time delay that avoids a specific nonlinearity, e.g., dead-band, in the entire operating range. Due to conciseness, results are not presented for in-phase operating regimes. However, it is found that the in-phase operation is highly unsuitable for ac-type converters as well. This is because, besides low-frequency distortion, it also brings a high-frequency distortion, due to the LCOs being manifested. Hence, the in-phase operation should always be avoided or suppressed, e.g., using some algorithm such as the one in [17].

As a final illustration, the impact of an increase of the oversampling factor on the THD is shown in Fig. 20. The operating point perturbation spans the duty cycle in the range from 0.1 to 0.9. The results are shown for the standard application scenario, where the modulating waveform update is delayed by one control period, resulting in $\tau_D = \frac{1}{N}$. The crossover frequency is set to $f_{c,r} = \frac{1}{10}$, and no other actions for reducing the nonlinearities were taken. It can be seen that distortion level is high for $N = 4$ and $N = 8$. An effective mitigation of the additional distortion caused by the nonlinearities starts to appear at $N > 8$.

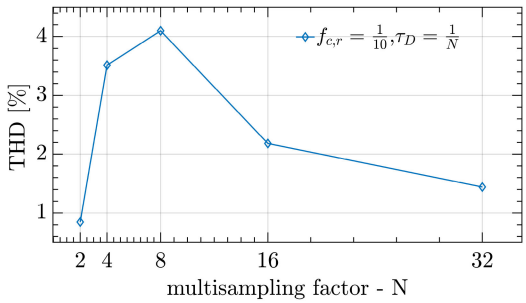

Fig. 20. Inductor current distortion for $f_{c,r} = \frac{1}{10}$ and control systems that feature one-step calculation delay. The RMS value of the inductor current is equal to 4.9 A, and the RMS value of the output voltage is equal to 230 V. The fundamental frequency is equal to 50 Hz.

VII. Conclusion

This article presents an investigation of the nonlinearities introduced by the MS-PWM control of power converters. The motivation is to provide a guideline for the optimal implementation of the MS-PWM without the need to remove the switching ripple. Different nonlinearities are identified and the conditions for their appearance are provided using discontinuity and nonlinearity graphs. The time delay of the control system is chosen as an independent variable, which allows the subsequent use of these graphs for various design purposes. Experimental verifications, performed on a dc–dc buck converter and a dc–ac inverter, have demonstrated that the presented nonlinearity graphs have a general value for predicting and improving time-domain behavior of power converters. It is shown that, for dc–dc-type converters, certain values of time delay can cause unacceptable LCOs. For ac-type converters, instead, it is shown that the transcharacteristic nonlinearities are sources of current distortion. By imposing a specific time delay, the impact of nonlinearities can be minimized.

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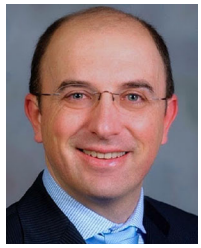

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