Discontinuous Modulation of a Cascaded H-Bridge Low-Capacitance StatCom

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***Abstract*—This article presents a discontinuous modulation (DM) strategy for static compensators (StatComs) based on a cascaded H-bridge (CHB) converter with a star configuration. The proposed DM strategy considers the capacitor voltage oscillations at twice the fundamental frequency and the effect of zero-sequence voltage injection on the capacitor voltages. Considering these effects is especially important in CHB-StatComs with large capacitor voltage ripples (low-capacitance StatComs), where the assumption of a constant dc-link voltage, which is the basis of conventional DM strategies, does not apply. This article also describes a coherent set of steady-state waveforms for CHB-StatComs under DM. In addition to the well-known benefit of reducing the switching losses, the proposed DM also reduces the dc-link capacitors size and extends the operating range. The viability of the proposed DM strategy is verified experimentally on a small-scale prototype. In addition, simulation results are obtained using a real-scale system to study feasibility of the DM under unbalanced conditions.**

***Index Terms*—Capacitance reduction, capacitor voltage ripples (CVRs), cascaded H-bridge (CHB), discontinuous modulation (DM), static compensator (StatCom), zero-sequence voltage.**

I. Introduction

DISCONTINUOUS modulation (DM) is achieved by injecting a suitable voltage offset to clamp the ac-side converter voltage to the dc rail [1]–[9]. In a three-phase system, zero-sequence voltage injection provides the degree of freedom to clamp the phase arms without affecting the fundamental component of the output currents [3]–[9]. As no switching losses in the clamped submodules (SMs) are produced during the clamping periods, DM normally reduces the overall switching losses [1]–[9]. The authors of [1] and [2] propose DM strategies for single-phase cascaded H-bridge (CHB) converters to clamp a given number of SMs. Obviously, in single-phase systems, zero-sequence voltage does not exist, but this partial clamping strategy shows improved performance. Particularly, Alcaide *et al.* [1] focus on improving the converter output voltage quality, while Ko *et al.* [2] aim at reducing the converter thermal stress. Zero-sequence voltage injection is implemented in [3] to improve the ride-through capability of SM failures in CHB static compensators (StatComs) with a star configuration. The authors of [4] and [5] applied the DM for switching loss reduction in a modular multilevel converter and a neutral-point-clamped inverter, respectively. In [6]–[8], different DM methods for voltage-source inverters are introduced. The effects of different DM methods on the current quality and switching losses of a StatCom are studied in [9], where the so-called DPWM3 offers the best results. However, the above studies assume a constant dc-link voltage, which is unaffected by the zero-sequence voltage (a negligible interaction between the zero-sequence voltage for DM and the dc-side converter voltages). In CHB-StatComs, where the dc sources are floating capacitors, this simplifying assumption only holds for large enough capacitance values. Neglecting the capacitor voltage dynamics and the capacitor voltage ripple (CVR) in CHB-StatComs leads to an inaccurate representation of the converter steady-state trajectory, which, in turn, deteriorates the steady-state converter performance. This problem is exacerbates by reducing the capacitance values, as in low-capacitance StatComs (LC-StatComs) [10]–[15].

In [12] and [13], the concepts of the LC-StatCom and peak capacitor voltage control are introduced. A lower average capacitor voltage operation allows the LC-StatCom to achieve improved output voltage/current quality and less switching losses [16], [17]. However, a reduced inductive operation range is the main drawback [12], [13]. Solutions to eliminate this drawback are reported in [10], [18] and [19]. Thyristor-bypassed-reactors are used in [10] and [18], whereas Rodriguez *et al.* [19] present a solution based on the third-harmonic zero-sequence compensation method for a delta configuration. However, extra hardware and large arm current magnitudes are the drawbacks of these approaches, respectively.

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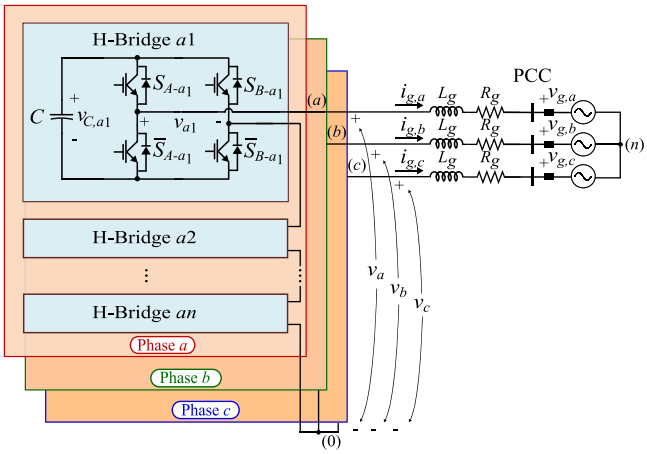

Fig. 1. Circuit diagram of a three-phase CHB power converter with the star configuration.

Given the above context, this article proposes a DM strategy for CHB-StatCom applications that takes into account the CVR and the effect of zero-sequence voltage injection on the capacitor voltages. Thus, its application is not just restricted to the conventional CHB-StatComs with negligible CVR, but it is also valid for the LC-StatComs with nonnegligible CVR [20]. Furthermore, this article formulates the zero-sequence voltage and capacitor voltage references. This explicit characterization of the steady-state waveforms in terms of the dc-link capacitor size is needed for the design and control of the CHB-StatComs operated in DM.

The rest of this article is organized as follows. In Section II, the CHB-StatComs with the star configuration is revisited. Section III describes the proposed DM strategy and introduces analytical expressions for the piecewise zero-sequence voltage and the capacitor voltages under balanced condition. By using these analytical expressions, benefits of the proposed DM strategy are studied in Section IV. Section V verifies the effectiveness of the proposed DM strategy experimentally. Section VI provides simulation results illustrating the practicability of the proposed DM strategy in a real-scale LC-StatCom system. Finally, Section VII concludes this article.

II. CHB-StatComs With a Star Configuration

In this section, the circuit topology of the CHB-StatCom with a star configuration, its main electrical variables, and their relationships are reviewed.

A. Topology and Main Variables

The topology of a CHB-StatCom with star configuration is shown in Fig. 1. The positive ac-side terminals of the converter, i.e., (a), (b), and (c), are connected to the point of common coupling (PCC) grid voltages $v_{g,a}$, $v_{g,b}$, and $v_{g,c}$ through filtering inductors L_g. The negative ac-side terminals of the converter arms are connected forming a star configuration. Each phase arm of the CHB converter consists of n H-bridge SMs (with $j \in \{1, 2, \ldots, n\}$ as the SM index), each of them with a dc-side capacitor with capacitance C.

The total ac-side converter voltages to be generated v_a, v_b, and v_c consist of: 1) fundamental-frequency voltages v'_a, v'_b, and v'_c and 2) zero-sequence voltage for discontinuous operation $v_{Z,d}$, i.e.,

$$v_x = v'_x + v_{Z,d}, \quad x \in \{a,\ b,\ c\}\,. \tag{1}$$

The cluster dc-side converter voltages of each phase arm, $v_{\text{clus},x}$, are defined as

$$v_{\text{clus},x} = \sum_{j=1}^{n} v_{C,xj}. \tag{2}$$

In the averaged model, v_x and $v_{\text{clus},x}$ are related by the modulating signals $\delta_x \in [-1,\ 1]$ as [20]

$$\delta_x = \frac{v_x}{v_{\text{clus},x}}. \tag{3}$$

The dynamics of the cluster voltages $v_{\text{clus},x}$ are given by the following power relationship between the converter ac-side and dc-side quantities:

$$\frac{1}{2}\frac{C}{n}\frac{dv^2_{\text{clus},x}}{dt} = -\left(v'_x + v_{Z,d}\right) i_{g,x} \tag{4}$$

with $i_{g,x}$ denoting the StatCom currents. As can be seen from (4), the cluster voltages depend on the zero-sequence voltage $v_{Z,d}$.

B. Steady-State Relationships Under Continuous Modulation

In order to calculate the steady-state trajectory of the CHB-StatCom's variables, the following definitions for the fundamental-frequency ac-side converter voltages v'_x and the StatCom currents $i_{g,x}$ are considered (neglecting losses and harmonics):

$$v'_x = V'_x \cos\left(\omega t + \phi_x\right) \tag{5}$$

$$i_{g,x} = I_{g,x} \sin\left(\omega t + \phi_x\right) \tag{6}$$

where ω is the angular frequency of the grid voltage and ϕ_x is the phase-shift angle of phase x. V'_x and $I_{g,x}$ represent the amplitude of v'_x and $i_{g,x}$. Note that $I_{g,x}$ has the same/opposite sign as V'_x under capacitive/inductive operation, according to $i_{g,x}$ direction shown in Fig. 1. It is important to note that even during unbalanced grid conditions (or negative-sequence current injection), v'_x and $i_{g,x}$ are orthogonal in steady state, thanks to the fundamental-frequency zero-sequence voltage injection, as described in [21].

From (5) and (6), and considering $v_{Z,d} = 0$ under continuous modulation (CM), (4) can be solved analytically, yielding the following expression for the cluster voltages [12]:

$$v_{\text{clus},x} = \sqrt{A + \frac{I_{g,x}V'_x}{2\omega C/n}\cos\left(2\left(\omega t + \phi_x\right)\right)} \tag{7}$$

TABLE I
COMBINATIONAL ALGORITHM FOR THE ZERO-SEQUENCE VOLTAGE CALCULATION

Clamped Phase	Condition	Zero-Sequence Voltage, $v_{Z,d}$	Capacitor Voltage Dynamics
a	$\lvert v'_a\rvert \geq \lvert v'_b\rvert$ & $\lvert v'_a\rvert \geq \lvert v'_c\rvert$	$v_{Z,d} = \text{sign}\ (v'_a)\, v_{clus,a} - v'_a$	$\frac{C}{n}\frac{dv_{clus,a}}{dt} = -\text{sign}\ (v'_a)\, i_{g,a}$
c	$\lvert v'_c\rvert \geq \lvert v'_a\rvert$ & $\lvert v'_c\rvert \geq \lvert v'_b\rvert$	$v_{Z,d} = \text{sign}\ (v'_c)\, v_{clus,c} - v'_c$	$\frac{C}{n}\frac{dv_{clus,c}}{dt} = -\text{sign}\ (v'_c)\, i_{g,c}$
b	$\lvert v'_b\rvert \geq \lvert v'_a\rvert$ & $\lvert v'_b\rvert \geq \lvert v'_c\rvert$	$v_{Z,d} = \text{sign}\ (v'_b)\, v_{clus,b} - v'_b$	$\frac{C}{n}\frac{dv_{clus,b}}{dt} = -\text{sign}\ (v'_b)\, i_{g,b}$

where

$$A = V_{\text{clus,max}}^2 - \left|\frac{I_{g,x}V'_x}{2\omega C/n}\right|. \tag{8}$$

Note that, with this definition of term A, $v_{\text{clus},x}$ maintains a prescribed maximum cluster voltage value equal to $V_{\text{clus,max}}$ regardless the current amplitude $I_{g,x}$. Imposing a prescribed maximum cluster voltage values is important in LC-StatComs to provide a safe converter hardware operation [12].

III. PROPOSED DM STRATEGY

This section analyzes the proposed zero-sequence voltage injection strategy for DM purposes and for achieving capacitance reduction. An analytical piecewise equation for the proposed zero-sequence voltage is derived, which is then used to derive an explicit characterization of piecewise continuous capacitor voltage waveforms. The proposed DM strategy considers the time-varying nature of the capacitor voltages in the CHB-StatCom, and the interaction between the capacitor voltages and the injected zero-sequence voltage.

A. Zero-Sequence Voltage Expression

According to which phase is being clamped, one can define three sectors and analyze the steady-state relationships in each sector. The voltage conditions in each sector and their corresponding dynamics are shown in Table I. When phase x is clamped, its modulating signal δ_x is saturated to 1 or -1, and consequently, its ac-side converter voltage corresponds to $v_{\text{clus},x}$ or $-v_{\text{clus},x}$, while its dc-side current corresponds to $-i_{g,x}$ or $i_{g,x}$, respectively. Note that conditions in Table I are independent on whether the converter operates in balanced or unbalanced situations.

Therefore, in the steady state, the capacitor voltage waveforms during their clamping periods can be analytically solved by integrating (6) [according to (4)], which yields

$$v_{\text{clus},x,} = V_{\text{cons}} + \frac{I_{g,x}}{\omega C/n}\left|\cos\left(\theta_x\right)\right| \tag{9}$$

where $\theta_x = \omega t + \phi_x$, and V_{cons} is a constant that provides a degree of freedom to regulate the peak (or the average) capacitor voltage.

Taking into account that the cluster voltages in clamped operation correspond to $v_{\text{clus},x} = \text{sign}(v'_x)(v'_x + v_{Z,d})$, the steady-state zero-sequence voltage $v_{Z,d}$ can be derived from (5) and (9) as follows:

$$v_{Z,d} = V_{Z,x}\cos\left(\theta_x\right) + \text{sign}\left(v'_x\right)V_{\text{cons}} \tag{10}$$

where V_Z corresponds to

$$V_{Z,x} = \frac{I_{g,x}}{\omega C/n} - V'_x. \tag{11}$$

During balanced grid conditions, the resulting zero-sequence voltage for DM, $v_{Z,d}$, only contains triplen harmonics, and as a result, the product $v_{Z,d}i_{g,x}$ does not generate any active power component. However, during unbalanced conditions, $v_{Z,d}i_{g,x}$ can generate active power, which must be compensated by the integral action of the interphase voltage balancing loop [3]. This interaction between DM and interphase balancing represents a limitation of the proposed DM to be analyzed in more depth in the future.

B. Capacitor Voltage Steady-State Expression

In this subsection, using (4) and (10), the analytic expression of the cluster voltages $v_{\text{clus},x}$ is derived. For the sake of brevity, balanced grid conditions are considered henceforth (i.e., $I_{g,x} = I_g$, $V'_x = V'$, and $V_{Z,x} = V_Z$).

The sector where phase x is clamped is denoted as Sector I, and it corresponds to $\theta_x \in (-\frac{\pi}{6}, \frac{\pi}{6}] + k\pi$. The cluster voltage expression corresponds to (9), i.e.,

$$v_{\text{clus},x,I}\left(\theta_x\right) = V_{\text{cons}} + \text{sign}\left(v'_x\right)\frac{I_g}{\omega C/n}\cos\left(\theta_x\right). \tag{12}$$

In the next sector, denoted as Sector II, the phase leading phase x by $2\pi/3$, represented as x^+, is clamped. In this case, the zero-sequence voltage in (10) is calculated according to phase x^+, i.e., $v_{Z,d} = V_Z\cos(\theta_{x^+}) + \text{sign}(v'_{x^+})V_{\text{cons}}$, with $\theta_{x^+} = \theta_x + 2\pi/3$. According to (4)–(6) and (10), the square cluster voltage of phase x when phase x^+ is clamped corresponds to

$$\begin{aligned} v_{\text{clus},x,II}^2\left(\theta_x\right) = &+ \frac{I_g V'}{2\omega C/n}\left[\cos\left(2\theta_x\right) - \cos\left(2\theta_I\right)\right] \\ &- \frac{I_g V_Z}{2\omega C/n}\left[\sin(2\theta_x + \pi/6) - \sin(2\theta_I + \pi/6)\right] \\ &+ \text{sign}\left(v'_{x^+}\right)\frac{2I_g V_{\text{cons}}}{\omega C/n}\left[\cos\left(\theta_x\right) - \cos\left(\theta_I\right)\right] \\ &+ \frac{\sqrt{3}}{2}\frac{I_g V_Z}{\omega C/n}\cdot(\theta_x - \theta_I) + v_{\text{clus},x,I}^2(\theta_I) \end{aligned} \tag{13}$$

where $\theta_I = \frac{\pi}{6} + k\pi$ is the value of θ_x at the end of Sector I.

Similarly, x^- represents the phase that is lagging phase x by $2\pi/3$ and Sector III is where this phase is clamped. Similar to Sector II, $v_{Z,d}$ is calculated according to phase x^- ($v_{Z,d} = V_Z\cos(\theta_{x^-}) + \text{sign}(v'_{x^-})V_{\text{cons}}$, with $\theta_{x^-} = \theta_x - 2\pi/3$), and the square cluster voltage of phase x when phase x^- is clamped

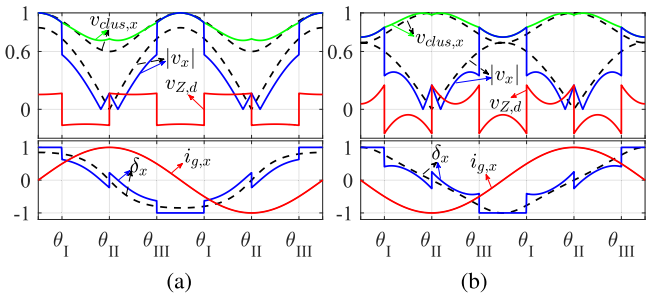

Fig. 2. Main converter waveforms of phase x when applying the proposed DM strategy to a CHB-StatCom. The black dashed lines correspond to CM, while the solid lines correspond to the proposed DM strategy. (a) Capacitive operation. (b) Inductive operation.

corresponds to

$$v^2_{\text{clus},x,III}(\theta_x) = +\frac{I_g V'}{2\omega C/n}\left[\cos(2\theta_x) - \cos(2\theta_{II})\right] - \frac{I_g V_Z}{2\omega C/n}\left[\sin(2\theta_x + 5\pi/6) - \sin(2\theta_{II} + 5\pi/6)\right] + \text{sign}\left(v'_{x^-}\right)\frac{2I_g V_{\text{cons}}}{\omega C/n}\left[\cos(\theta_x) - \cos(\theta_{II})\right] - \frac{\sqrt{3}}{2}\frac{I_g V_Z}{\omega C/n}\cdot(\theta_x - \theta_{II}) + v^2_{\text{clus},x,II}(\theta_{II}) \quad (14)$$

where $\theta_{II} = \frac{\pi}{2} + k\pi$ is the value of θ_x at the end of Sector II.

The piecewise continuous capacitor voltage waveforms (12)–(14) under DM stand in contrast with the continuous waveform (7) under CM. For a better illustration, Fig. 2 shows the main StatCom waveforms of phase x under DM (in solid lines) and under CM (in dashed lines). Note that $[\theta_{III},\ \theta_I)$ corresponds to Sector I, $[\theta_I,\ \theta_{II})$ corresponds to Sector II, and $[\theta_{II},\ \theta_{III})$ corresponds to Sector III. As can be observed, under the same reactive power, the CVR reduces when the proposed DM strategy is applied, thus allowing to reduce the capacitance value.

In order to illustrate the importance of considering the piecewise continuous nature of the capacitor voltages, i.e., the result of interaction between the zero-sequence voltage and the capacitor voltages, Fig. 3 depicts a simulation result. Before the transition at $t = 0.025$ s, (7) is used as reference capacitor voltage, whereas (12)–(14) are used after the transition. The controller used for the simulation is based on incremental passivity theory, as in [20], adapted to the three-phase case with star configuration and DM. System parameters are the same as those used in the experimental tests, as presented in Table II. Fig. 3(a) shows the phase a converter voltages, while Fig. 3(b) depicts the grid currents. It can be observed that when the effect of $v_{Z,d}$ on cluster voltages is not considered, i.e., before $t = 0.025$ s, the variables cannot follow their references, and consequently, the grid current presents low-frequency distortion. After the transition, correct references are generated based on the proposed DM strategy, and proper reference tracking is achieved.

IV. Benefits of the Proposed DM Strategy

In this section, the effects of the proposed DM strategy on capacitance requirement (see Section IV-A), inductive operation range (see Section IV-B), converter voltage total harmonic distortion (THD) (see Section IV-C), and switching losses (see Section IV-D) are analyzed.

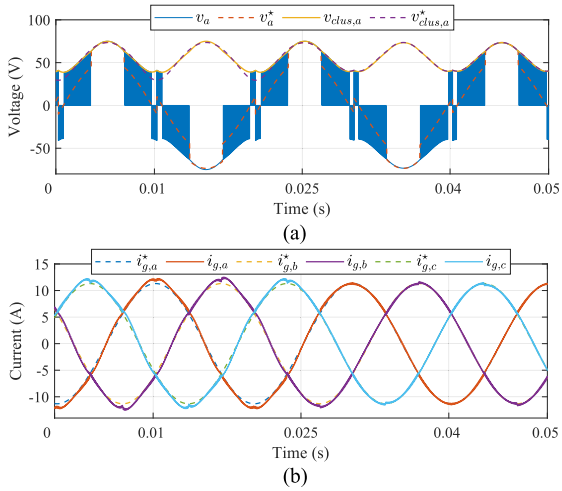

Fig. 3. Simulation waveforms during a transition from neglecting the effect of $v_{Z,d}$ on cluster voltages to the proposed DM at $t = 0.025$ s under full capacitive power. (a) Phase a ac-side PWM voltage v_a and the cluster voltage $v_{\text{clus},a}$ with their references (dashed line) and (b) grid currents.

TABLE II
Experimental System Parameters

Parameters	Value
PCC Phase Voltage Nominal Amplitude, $\hat{V}_{gn}$	$40\sqrt{2}$ V (1 p.u.)
Nominal Reactive Power, S_n	0.96 kVA (1 p.u.)
Grid Angular Frequency, ω	100π rad/s
Individual Switch Switching Frequency, f_s	5 kHz
Number of SMs on each phase-arm, n	1
Maximum Cluster Voltage, $V_{clus,max}$	$1.3\hat{V}_{gn}$
Capacitance per H-Bridge, C	480 μF
Filter Inductance, L_g	2 mH (0.13 p.u.)

A. Capacitor Size

The capacitor size is mainly determined by the desired CVR under rated capacitive power and the prescribed maximum cluster voltage $V_{\text{clus,max}}$. To evaluate the capacitance requirement when the proposed DM strategy is applied, the maximum and minimum cluster voltages under capacitive operation are calculated as follows.

As shown in Fig. 2(a), under capacitive operation, the cluster voltage of phase x reaches its maximum in Sector I, and according to (12), the maximum cluster voltage can be fixed at a prescribed value $V_{\text{clus,max}}$ by setting

$$V_{\text{cons}} = V_{\text{clus,max}} - \frac{I_g}{\omega C/n}. \quad (15)$$

In Sector II, the cluster voltage of phase x presents a minimal value at θ_m, where its time derivative is equal to zero. According to (4), and since the grid current $i_{g,x}$ is not zero in Sector II, θ_m can be easily calculated by solving $v_x = 0$. According to (5),

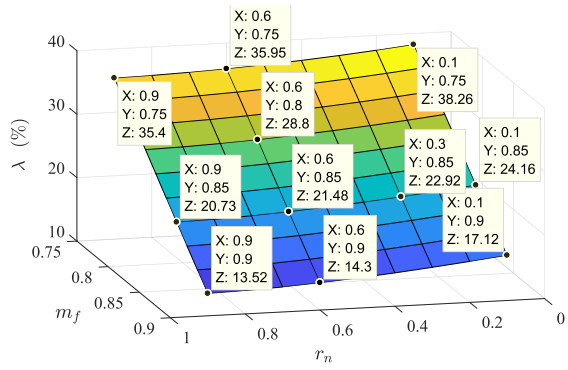

Fig. 4. Capacitance reduction effect.

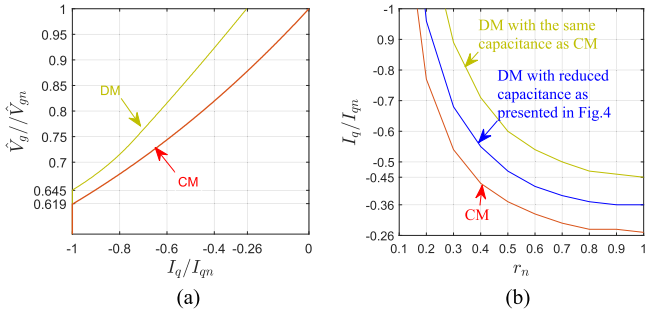

Fig. 5. Inductive operating range comparison between CM and the proposed DM strategy. (a) V–I character of the LC-StatCom under nominal condition. (b) Inductive operation range varying with r_n when $m_f = 0.85$.

and $v_{Z,d}$ in Sector II, θ_m corresponds to

$$\theta_m = \arccos\left(\frac{V_{\text{cons}}}{\sqrt{(V')^2 + (V_Z)^2 - V'V_Z}}\right) - \varphi \tag{16}$$

where $\varphi = \arctan 2(\frac{\sqrt{3}}{2}V_Z, V' - \frac{1}{2}V_Z)$.

Substituting the value of θ_m into (13), the instantaneous minimum cluster voltage $v_{\text{clus,min}}$ under capacitive operation can be analytically obtained. Once the maximum and minimum capacitor voltages are characterized, the capacitance needed to achieve a desired CVR can be calculated.

Note that a similar procedure can be carried out to fix a desired $V_{\text{clus,max}}$ for inductive operation.

The CVR, denoted as r henceforth, is defined as [22]

$$r = 1 - \frac{v_{\text{clus,min}}}{V_{\text{clus,max}}}. \tag{17}$$

Therefore, for a desired CVR under nominal conditions, denoted as r_n, the minimum cluster voltage can be written as

$$V_{\text{clus,min}} = V_{\text{clus,max}}\,(1 - r_n)\,. \tag{18}$$

For example, when CM is implemented, the minimum cluster voltage corresponds to [according to (7) and (8)]

$$V_{\text{clus,min}} = \sqrt{V_{\text{clus,max}}^2 - \left|\frac{I_g V'}{\omega C'/n}\right|}. \tag{19}$$

Replacing $V_{\text{clus,min}}$ from (19) in (18), and solving for the equivalent arm capacitance C'/n, yields

$$\frac{C'}{n} = \frac{I_g V'}{V_{\text{clus,max}}^2 \omega r_n\,(2 - r_n)}. \tag{20}$$

For the sake of clarity, C' represents the individual H-bridge capacitance when using CM, while C refers to the DM case. Note that for the DM case, the procedure is exactly the same, i.e., the minimum cluster voltage is analytically calculated using (13) and (16); then, it is replaced in (18), and the resulting equation is solved for the equivalent arm capacitance C/n.

Fig. 4 illustrates the capacitance reduction effect, which is defined as

$$\lambda = 1 - \frac{C}{C'} \tag{21}$$

for different values of r_n and modulation index

$$m_f = \frac{V'}{V_{\text{clus,max}}}. \tag{22}$$

As can be observed, for a given m_f, λ gradually increases when r_n reduces. This means that the capacitance reduction effect is slightly larger if CVR is lower. Particularly, with $m_f = 0.85$, $[20.5\%,\ 23.5\%]$ capacitance reduction can be achieved in an LC-StatCom ($r_n \geq 0.2$) by using the proposed DM strategy, whereas $[23.5\%,\ 24\%]$ capacitance reduction can be achieved in a conventional CHB-StatCom ($r_n < 0.2$). For the LC-StatCom, when the desired $r_n = 0.6$, with m_f varying from 0.75 to 0.9, the capacitance reduction is in the range of $[36\%,\ 14\%]$, or equivalently, $C \in [0.64C', 0.86C']$.

B. Inductive Operation Range

As mentioned in the Introduction, the limited inductive operation of the LC-StatCom is a major drawback. In this subsection, the inductive operation range of an LC-StatCom when using the proposed DM strategy is evaluated. The inductive operation range is obtained according to [10] and [12], where the filtering impedances are neglected and the constraint $|v_x| \leq v_{\text{clus},x}$ is imposed.

In Fig. 5, $\hat{V}_g/\hat{V}_{gn}$ and I_q/I_{qn} denote the per-unit values of PCC grid voltage and inductive current, respectively. Fig. 5(a), obtained with $m_f = 1$ and $r_n = 1$ at rated capacitive power, shows the operating limits with the proposed DM strategy (shown in the figure in yellow). The figure also shows the operating limits with CM (shown in the figure in red) for comparison. As can be observed, at rated voltage condition ($\hat{V}_g = \hat{V}_{gn}$), the LC-StatCom with CM cannot provide reactive inductive power, whereas with the proposed DM strategy, the LC-StatCom can provide a maximum of 26% reactive inductive power.

A more realistic case, with $m_f = 0.85$ and $\hat{V}_g = 1$ p.u., is illustrated in Fig. 5(b). This operation condition allows more than 20% capacitance reduction, if the proposed DM strategy is applied, according to Fig. 4. As depicted in Fig. 5(b), even though the capacitance is significantly reduced (shown in the figure in blue), the inductive operation range is enlarged.

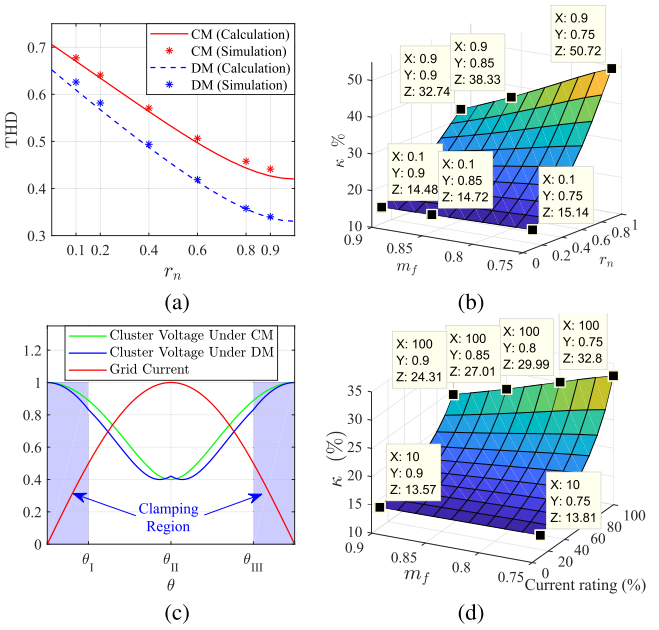

Fig. 6. THD and switching loss comparison between CM and the proposed DM strategy. (a) THD comparison under different r_n when $m_f = 0.85$. (b) Switching loss reduction under nominal operation with different r_n and m_f. (c) Cluster voltage waveforms for the two modulations when $r_n = 0.6$ and $m_f = 0.85$. (d) Switching loss reduction under different current ratings and m_f when $r_n = 0.6$.

C. Voltage THD Assessment

Reduced current quality is a known drawback of applying the DM at low modulation indexes [6], [23], [24]. However, for CHB-StatComs, the drawback is avoidable because the modulation index can be maintained high by controlling the capacitor voltages. The injected zero-sequence voltage and resultant cluster voltage waveforms shape the pulsewidth modulation (PWM) ac-side converter voltages, and hence, the proposed DM strategy will affect the converter voltage THD [25]. According to [22], the THD of the PWM ac-side converter voltage under unipolar modulation corresponds to

$$\text{THD}_v = \frac{\sqrt{2\overline{v_{\text{clus},x}\,|v_x|} - (V')^2}}{V'} \tag{23}$$

where the overline notation shows the average (over a fundamental period) value of a quantity.

In this subsection, for the sake of comparison, equal $V_{\text{clus,max}}$ and r_n values are imposed for both modulation techniques. Moreover, $m_f = 0.85$ and capacitive operation have been considered. According to Section IV-A, this yields to two different capacitances, C' (for CM) and C (for DM), where $C < C'$. This is illustrated in Fig. 6(c).

Fig. 6(a) depicts the converter ac-side voltage THD of the CHB-StatCom according to (23), which is in agreement with the numerical values obtained from simulation with MATLAB Simulink. As can be observed, the THD decreases at higher CVR values. The results show that the voltage THD decreases by the use of DM as compared to the CM.

D. Switching Losses

In this subsection, the switching loss reduction by applying the proposed DM strategy is quantified for different operating conditions. Again, two different capacitances C and C' are defined for comparison purposes.

The instantaneous switching energy loss is assumed to be proportional to the magnitude of the capacitor voltage and the grid current at the switching instant [22], and it is defined as follows:

$$e_s = \mu e_{sn} \left|\frac{i_{g,x}}{I_g}\right| \left(\frac{v_{\text{clus},x}}{V_{\text{clus,max}}}\right) \tag{24}$$

where μ is a discrete variable that is equal to 1 at the switching instants, while 0 otherwise, and e_{sn} represents e_s when $v_{\text{clus},x} = V_{\text{clus,max}}$ and $i_{g,x} = I_g$.

The average switching loss (over a fundamental period $1/f_g$) can be written as

$$p_s = f_g \sum_{m=1}^{f_s/f_g} e_s(m) \tag{25}$$

where f_s is the switching frequency and f_g is the frequency of the power system.

Fig. 6(b)–(d) illustrates the switching loss reduction effect with $f_g = 50$ Hz and $f_s = 5$ kHz, which is defined as

$$\kappa = 1 - \frac{p_s}{p'_s} \tag{26}$$

where p'_s and p_s are the switching losses corresponding to CM and DM, respectively. Fig. 6(b) presents the switching loss reduction effect under rated voltage and current, for different r_n and m_f values. As shown, the switching loss reduction effect can be larger than 30% if r_n is large enough. It is worth noting that the switching loss reduction effect is not only due to the discontinuous operation of the converter, but also due to a lower instantaneous cluster voltage outside the clamping region, as illustrated in Fig. 6(c). Especially, for $r_n = 0.6$, Fig. 6(d) presents the switching loss reduction for different current ratings and m_f values, and as can be observed, the switching loss reduction is larger than 20% at the rated reactive current.

V. Experimental Results

The CHB-StatCom prototype used for experimental validation consists of three IMPERIX PEH2015 H-bridge converters. The PCC grid voltage is provided by a GL&EL 15-kVA CINERGIA grid emulator. The experimental setup is shown in Fig. 7, and system parameters are given in Table II. The control algorithm is implemented on a B-Box RCP 3.0 Board from IMPERIX. The controller used for experimental tests is based on the incremental passivity theory, as in [20], adapted to the three-phase case with a star configuration and DM. In order to provide a more clear illustration of the different waveforms, the data from the oscilloscope and the controller platform (B-Box RCP 3.0) have been used to plot Figs. 8– 11. Note that the transition between modulations in the following parts is just presented for illustration purposes, i.e., to show how the different waveforms vary depending on the modulation used.

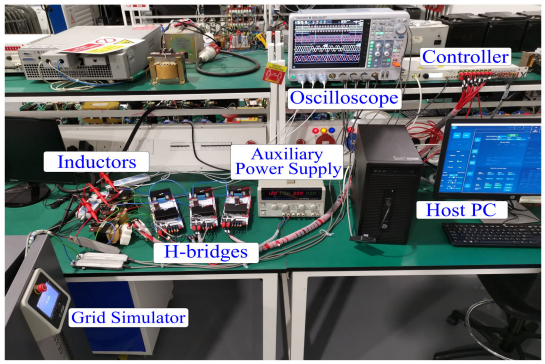

Fig. 7. Experimental setup.

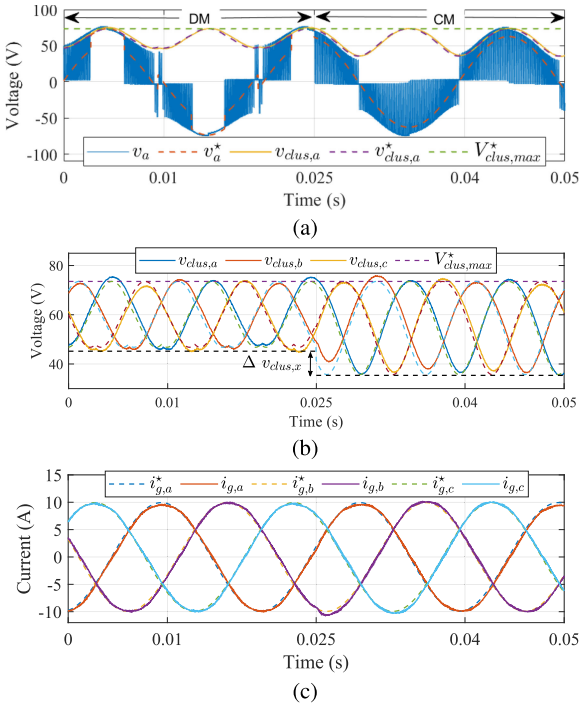

Fig. 8. Experimental waveforms during a transition from DM to CM at $t = 0.025$ s under approximately 90% rated capacitive power. (a) Cluster voltages and converter ac-side PWM voltages of phase a with their reference (dashed line). (b) Capacitor voltages. (c) Grid currents.

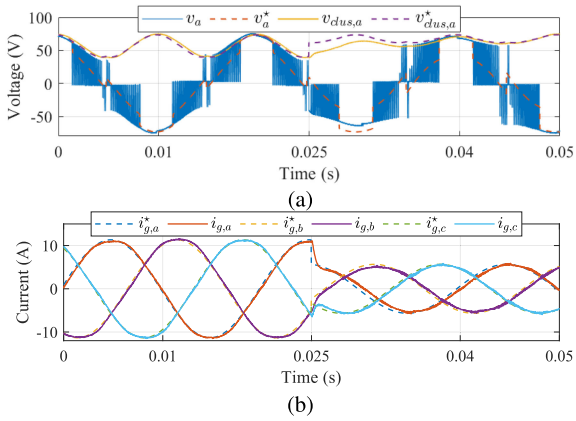

Fig. 9. Experimental waveforms of a transition from 100% rated capacitive power to 50% rated capacitive power at $t = 0.025$ s under DM. (a) Phase a voltages. (b) StatCom currents.

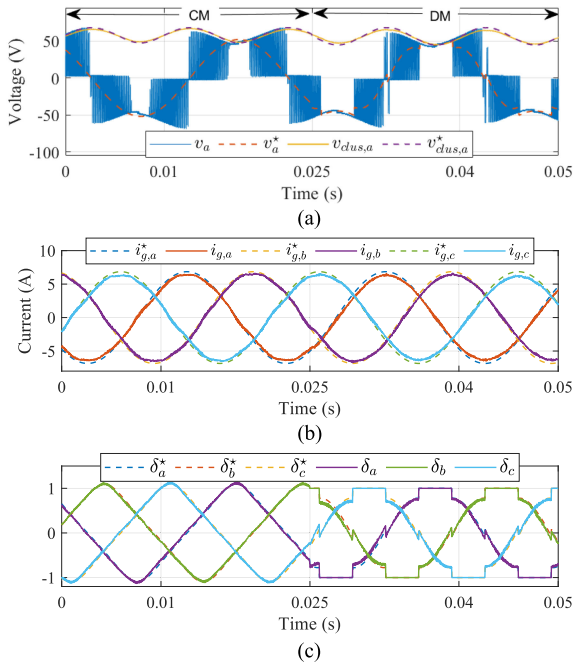

Fig. 10. Experimental waveforms of a transition from CM to DM at $t = 0.025$ s under 60% inductive power. (a) Cluster voltage and converter voltage of phase a. (b) StatCom currents. (c) Modulating signals.

Fig. 8 presents a transition from DM to CM at approximately 90% rated capacitive power. The transition occurs at time instant $t = 0.025$ s. The discontinuous behavior of the converter before $t = 0.025$ s is evident from Fig. 8(a), where the ac-side converter voltages v_x are clamped to their corresponding cluster capacitor voltages $v_{\text{clus},x}$. During these clamping periods, no switching is produced.

A detailed illustration of the cluster voltages and corresponding references is given in Fig. 8(b), where it can be observed that the peak capacitor voltage $V_{\text{clus,max}}$ is constant regardless of the modulation approach, and that the cluster voltages are properly balanced. It is important to note that the CVR presents a reduction of approximately 15% when the proposed DM strategy is applied, i.e., $\Delta v_{\text{clus},x}/V_{\text{clus,max}} \approx 15\%$. The CVRs under DM and CM are around 0.36 and 0.51, respectively, and according to (20), to achieve the same CVR as DM under the same conditions, the capacitance needs to be increased by 28% under CM, which corresponds to a 22% capacitance reduction. This result is in agreement with Fig. 4. An excellent current tracking with very little distortion can be observed from Fig. 8(c), where currents are barely affected by the applied modulation due to the rapid response of the capacitor voltages.

Fig. 9 depicts a transition from 100% to 50% rated capacitive power under DM. The abrupt change in power takes place at $t = 0.025$ s. Fig. 9(a) presents the transition in the converter ac-side and dc-side voltages of phase a. It can be seen how the prescribed maximum cluster voltage $V_{\text{clus,max}}$ is maintained.

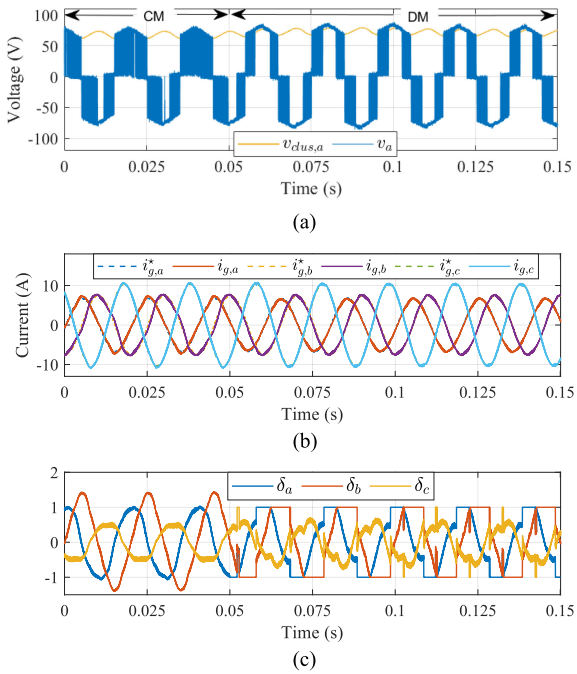

Fig. 11. Experimental waveforms of a transition from CM to DM at $t = 0.05$ s, with negative-sequence current $I_d^- = -0.15$ p.u., $I_q^- = -0.15$ p.u., 70% positive-sequence capacitive current, and balanced PCC grid voltages. (a) Cluster voltage and converter voltage of phase a. (b) StatCom currents. (c) Modulating signals.

This is achieved owing to the reference design explained in Section IV-A. Again, a very fast recovery time after the transient is observed in the capacitor voltages.

Fig. 9(b) shows a fast and damped transient response in the StatCom currents, with a response time lower than 2 ms after an abrupt change of reactive power occurs during DM.

Fig. 10 depicts a transition from CM to the proposed DM at $t = 0.025$ s under 60% inductive power, with peak cluster voltage defined as $V_{\text{clus,max}} = 1.2\hat{V}_{gn}$. It is worth highlighting that the absence of switching events in v_a when using CM, as shown in Fig. 10(a), is a consequence of overmodulation. After the transition, the absence of switching is due to the discontinuous operation imposed by the proposed DM, as the modulating signals in Fig. 10(c) indicate. Consequently, the StatCom currents under CM are distorted, while under the proposed DM, the currents are sinusoidal.

The agreement between the measured waveforms and their references corroborates the correctness of the analytical derivations in Section III. The experimental results verify the feasibility and effectiveness of the proposed DM strategy.

Experimental results under negative-sequence current compensation are presented in Fig. 11, which illustrates a transition at $t = 0.05$ s from CM to the proposed DM (the capacitor size is double for this unbalanced experiment due to the large CVRs). The LC-StatCom is providing 70% rated positive-sequence capacitive current and 21% rated negative-sequence current ($I_d^- = -0.15$ p.u., $I_q^- = -0.15$ p.u., where the abc–$dq0$ transformation follows the amplitudes invariant transformation [26]). As depicted in Fig. 11, when CM is used, the absence of switching events in v_a in Fig. 11(a) is due to overmodulation,

TABLE III
SIMULATION SYSTEM PARAMETERS

Parameters	Value
PCC Phase Voltage Nominal Amplitude, $\hat{V}_{gn}$	$6000\sqrt{2}$ V (1 p.u.)
Nominal Reactive Power, S_n	36MVA (1 p.u.)
Grid Angular Frequency, ω	100π rad/s
Individual Switch Switching Frequency, f_s	5 kHz
Number of SMs on each phase-arm, n	5
Maximum Cluster Voltage, $V_{clus,max}$	$1.3\hat{V}_{gn}$
Capacitance per H-Bridge, C	6.2 mF
Filter Inductance, L_g	1.1 mH (0.115 p.u.)

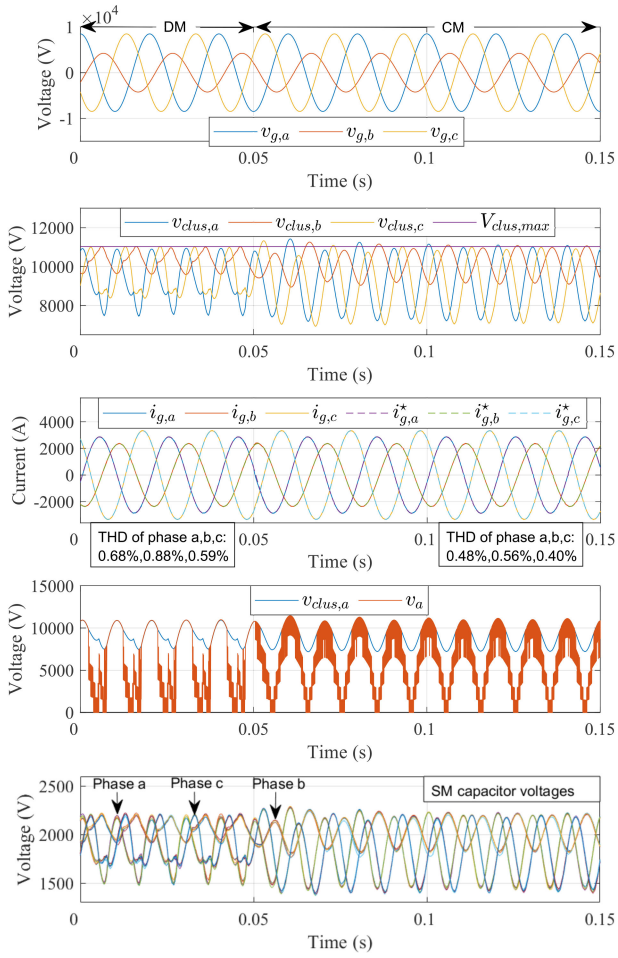

Fig. 12. Unbalanced Condition I: $I_d^- = -0.2$ p.u., $I_q^- = 0$ p.u., and $\hat{V}_{g,b} = 0.5$ p.u., under positive-sequence full capacitive current with a transition from the proposed DM to CM at $t = 0.05$ s.

as the modulating signals in Fig. 11(c) clearly show (they are outside the $[-1, 1]$ range). This causes low-frequency distortion in the injected StatCom currents, as shown in Fig. 11(b). Once the proposed DM is applied at $t = 0.05$ s, the low-frequency distortion in the injected StatCom currents vanishes, as shown in Fig. 11(b), and the modulating signals are within the range $[-1, 1]$, as shown in Fig. 11(c).

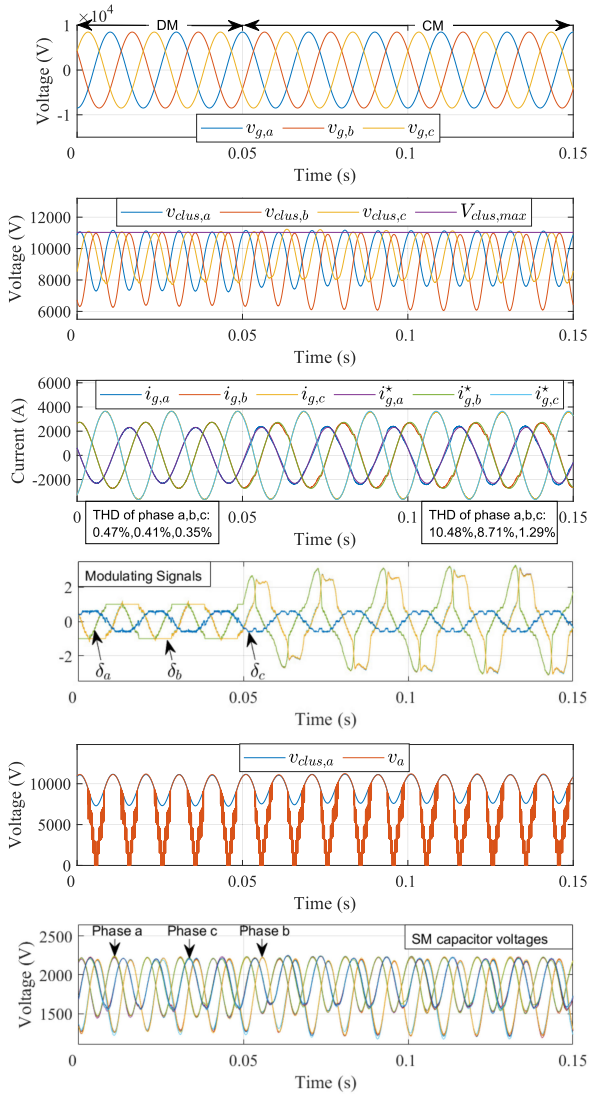

Fig. 13. Unbalanced Condition II: $I_d^- = -0.21$ p.u. and $I_q^- = -0.21$ p.u. under positive-sequence full capacitive power and balanced PCC grid voltages with a transition from the proposed DM to CM at $t = 0.05$ s.

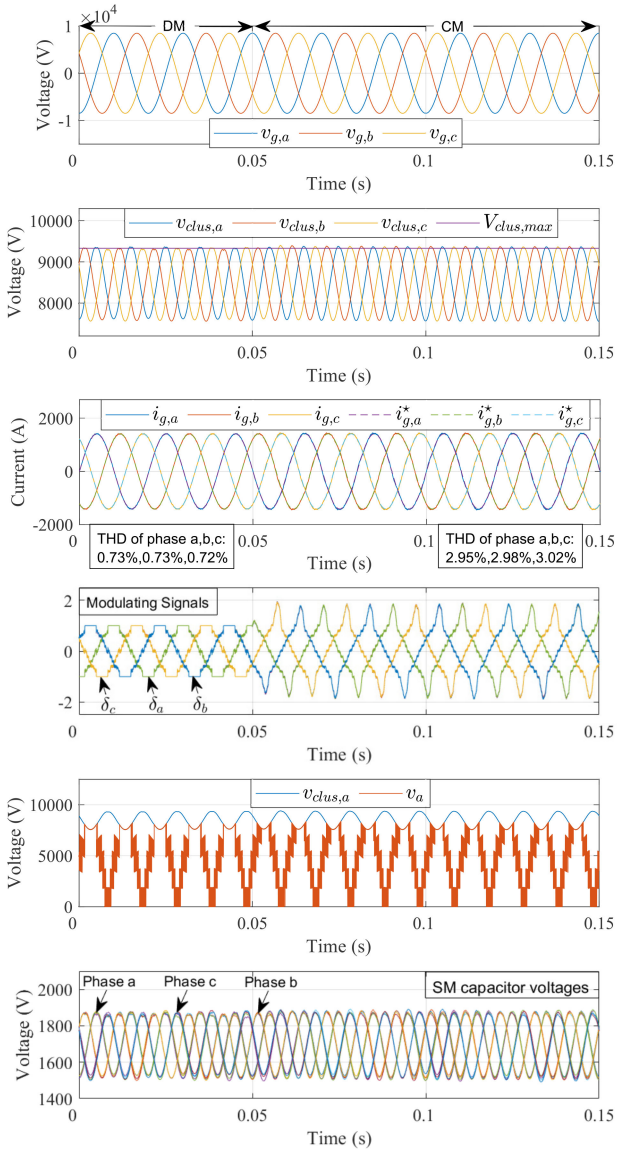

Fig. 14. Inductive operation: A transition from DM to CM under 50% positive-sequence inductive power and balanced grid voltage.

The experimental results in Fig. 11 show the capability of the proposed DM in enhancing the negative-sequence current compensation capability compared to CM. This happens because the phase with the highest voltage magnitude, which is the most unfavorable, is always clamped by the proposed DM algorithm.

VI. Simulation Verification of a Practical LC-StatCom System

Simulation results obtained using a 36-MVA LC-StatCom with five SMs per phase connected to a 6-kV grid are discussed in this section. Table III provides the parameters used in the simulation. Simulation results present a transition from DM to CM at $t = 0.05$ s. Two typical unbalanced conditions under positive-sequence full capacitive current are presented, namely, *Unbalanced Condition I* and *Unbalanced Condition II*. *Unbalanced Condition I* corresponds to Fig. 12, and it shows the negative-sequence current compensation ability of the LC-StatCom under steady-state asymmetrical grid voltage operation, whereas *Unbalanced Condition II* corresponds to Fig. 13, and it presents the behavior of the LC-StatCom under balanced grid voltages when the negative-sequence current reference is beyond its manageable limits, i.e., the converter will be in its overmodulation region if CM is applied [21].

Fig. 12 shows that the voltage in phase b is about half that of the voltage in the other phases, and the dq components of the negative-sequence current correspond to $I_d^- = -0.2$ p.u. and $I_q^- = 0$ p.u. Note that the active power introduced by the negative sequence is compensated by means of a controller that generates a positive-sequence d component current reference. It can be observed that the current quality is excellent under both modulation techniques and that the magnitude of the CVR is lower under the proposed DM strategy. Capacitor voltages

are tightly balanced, and their peaks correctly regulated to the predefined value $V_{\text{clus,max}}$.

Fig. 13 presents an operating condition with $I_d^- = -0.21$ p.u., $I_q^- = -0.21$ p.u., and rated PCC grid voltages. As depicted in Fig. 13, the LC-StatCom currents present low-frequency distortion under CM due to overmodulation. Nevertheless, by using the proposed DM strategy, the LC-StatCom currents are sinusoidal. The simulation results in Fig. 13 are in agreement with those in Fig. 11.

Furthermore, the inductive operation enhancement previously discussed in Section IV-B is corroborated via simulation. Fig. 14 presents a transition from DM to CM under 50% inductive power. For the sake of comparison with Fig. 5(b), $V_{\text{clus,max}} = 1.1\hat{V}_{gn}$ has been adjusted in order to guarantee that m_f is approximately 0.85 and r_n is approximately 0.55. The result shows that the LC-StatCom can provide 50% inductive reactive power by using the proposed DM strategy, while by using a conventional CM, the converter is overmodulated, and the currents present low-frequency distortion. This result is in agreement with Fig. 5(b), where 50% inductive reactive power at $r_n = 0.55$ can only be attained by using the proposed DM strategy. This result effectively demonstrates the capability of the proposed DM strategy to enhance the inductive range in LC-StatCom applications. Unlike methods in [10], [18], and [19], the proposed DM strategy represents a hardware-free solution with no associated losses.

VII. Conclusion

A DM technique for CVR reduction in the CHB-StatCom with a star configuration has been proposed in this article. The proposed DM strategy takes into account the CVR and the capacitor voltage dynamics, and as a result, it produces a better converter steady-state performance, particularly when small capacitance values are used. In addition to preserving the known DM benefit of lower switching losses, the proposed DM strategy yields reduced capacitance requirements and an enhanced inductive operation for the LC-StatCom. Experimental results verified the validity of the proposed DM strategy for CHB-StatComs, while showing its potential for capacitance reduction, inductive operation, and negative-sequence current compensation range enhancement in comparison with CM. Simulation results show the feasibility of the proposed DM strategy in a practical LC-StatCom system and illustrate the effectiveness of the proposed DM strategy in dealing with severe unbalanced grid conditions and its ability to outperform CM.

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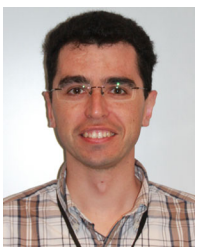

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