# Dead Time Optimization in a GaN-Based Buck Converter

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***Abstract*—A gallium nitride (GaN) field effect transistor can provide superior performance over a Si-MOSFET due to its low ON-state resistance and low junction capacitances. However, a GaN-based converter exhibits higher dead time loss during reverse conduction. Thus, to improve the efficiency, dead time optimization is required. This article proposes simple models for dead time optimization in a GaN-based buck converter under different load conditions. The proposed models are analytical in nature compared to the conventional models available for Si-based converters. A buck converter prototype is designed using a 100 V GaN device (GS61008P from GaN Systems) and the proposed analytical model-based dead time optimization techniques are validated experimentally. The proposed modeling techniques can be extended for other GaN-based dc–dc converters.**

***Index Terms*—Buck converter, dead time, efficiency, gallium nitride (GaN) field effect transistor (FET), reverse conduction.**

## I. Introduction

THE Si-MOSFET started its journey in the power management industry in 1976 [1]. Over the past four decades, power management circuits have improved their efficiency, power density, and cost. These improvements are largely contributed by continuous optimization and improvements in the production process of Si-MOSFETS. With the continuous optimization and improvements over the years, the Si-MOSFET has almost reached its theoretical limits [2]. Thus, power electronics practitioners are looking for new devices for further improvements of efficiency and power density of power management circuits.

Recently, gallium nitride (GaN) high electron mobility transistor (HEMT) has emerged as a potential replacement of the MOSFET for the next generation power management circuits [3]. Compared to a Si-MOSFET, a GaN HEMT has higher electron mobility, higher electric breakdown voltage, low intrinsic carrier concentration, smaller junction capacitance, and zero reverse recovery, etc. [4]. These properties are responsible to achieve high-efficiency operation of power electronic circuits at high-frequency. Furthermore, GaN devices are cost-effective as these are produced using the standard silicon device manufacturing procedures [5].

GaN HEMTs of different ratings are now available in the market. Recently, switching characteristics of GaN HEMTs were evaluated using the double pulse test (DPT) board [6], [7]. A number of GaN HEMT based power electronic converters were reported in the literature [8]–[10]. A GaN HEMT-based boost converter was tested at 1 MHz in [8], which achieved a peak efficiency of 97.8%. Efficiency of 99% at 100 kHz under hard-switching condition was demonstrated in [9]. Besides single-stage converters, two-stage converter modules using GaN HEMT can also achieve 95.1% efficiency [10].

Unlike MOSFETs, GaN HEMTs have no body diode for reverse conduction [11]. Lateral structure of a GaN HEMT is shown in Fig. 1. It can be seen that source and drain are connected by a 2-D electron gas (2-DEG) channel. This channel is used during reverse conduction. However, to enable this channel for conduction, source to drain voltage must be higher than the gate threshold voltage required for forward conduction [1]. The enhancement-mode GaN HEMT has no minority carrier. Thus, it produces no reverse recovery loss like a silicon diode. However, during reverse conduction, the source-to-drain voltage drop is much higher compared to a Si-MOSFET body diode.

Schematic of a GaN-based synchronous buck converter is shown in Fig. 2. Here, $v_{\rm in}$ is the input voltage, $v_{\rm o}$ is the output voltage, and $R$ is the load resistance of the buck converter. $L$ is the inductor, $C_{\rm in}$ and $C_{\rm o}$ are the input capacitor and output capacitor, respectively. The gate drive voltages $V_{\rm g1}$ and $V_{\rm g2}$ are applied to the high-side and low-side FETs, respectively. Gate resistance $R_{\rm g}$ is used to control the ON/OFF slew rate. Capacitor $C_{\rm gs}$ refers to the gate to source parasitic capacitance. The gate to drain parasitic capacitance is shown as $C_{\rm gd}$ and $C_{\rm ds}$ refers to the drain to source capacitance. To model the reverse conduction of the GaN HEMT at gate voltage $V_{\rm g1} = V_{\rm g2} = 0$, antiparalleled body diodes are shown in both the GaN FETs $S_{\rm H}$ and $S_{\rm L}$. Two switches $S_{\rm H}$ and $S_{\rm L}$ of a half-bridge switch cell (shown in Fig. 2) operate in a complementary fashion. To avoid shoot-through, dead times are introduced between the state transition of two gate signals. During dead time, any switch may operate in reverse conduction mode depending on the direction of the inductor current. Thus, to optimize the converter's efficiency, dead time duration needs to be optimized.

Several dead time optimization techniques are available in the literature [12]–[15]. However, these techniques were proposed

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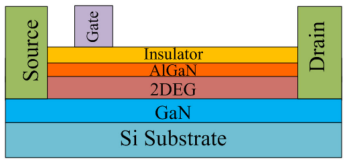


Fig. 1. Lateral structure of GaN FETs.

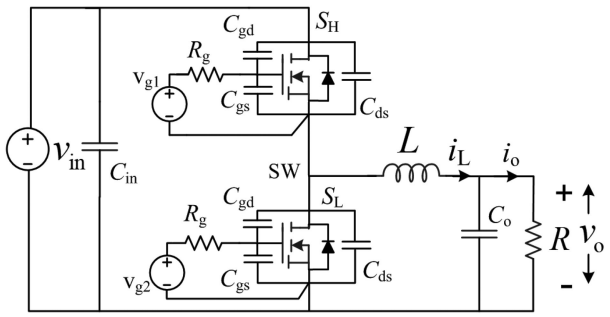


Fig. 2. GaN-based synchronous buck converter.

for Si-MOSFET-based converters. dead time optimization techniques for GaN-based converters were presented in [16]–[21]. In [16], a predictive dead time control for the GaN-based boost converter was proposed. A digital dead time correction controller was presented in [17] which can adjust the dead time during the converter operation by sensing the switch-node voltage and low-side gate voltage. An adaptive dead time control method was presented in [18] based on sensing the switch-node voltage and an up/down counter. A comparator-based dead time controller was proposed in [19]. A dual-edge dead time modulation technique for the buck converter was proposed based on a zero-crossing sensor circuit [20]. An adaptive dead time controller for the active clamp flyback (ACF) was realized by sampling the switch-node voltage and magnetizing peak/valley current in [21]. All these techniques take a few switching cycles to obtain the optimal dead time. Furthermore, sensing of switch-node voltage is necessary for all the above mentioned dead time controllers. In switching converters, switching transition causes high-frequency oscillations in the switch-node voltage. Thus, capturing exact switch-node voltage during switching transition is difficult. This may degrade the performance of the dead time controller. Furthermore, external circuitry requires for sensing the switch-node voltage may degrade the power density and increase the cost. A dynamic dead time optimization technique for the ACF converter was proposed in [22]. This technique needs an additional circuit connected in parallel with the low-side GaN FET. The circuit, consisting of a MOSFET, diode, and capacitor, may affect the performance of the GaN FET. Furthermore, input voltage sensing is also required to effectively implement this technique. A self-excited dead time minimizer circuit was proposed in [23]. The circuit takes a few cycles to adjust the optimal dead time for the buck converter. Dynamic dead time control for the full-bridge class-D ZVS inverter was presented in [24]. This technique needs input voltage sensing and digital POTs to adjust rising-edge delay. A dynamic dead time controller based on a current sense FET was used in a silicon carbide (SiC)-based converter [25] to reduce the diode conduction time. Optimized dead time can be obtained experimentally [26], [27]. However, these techniques are not scalable as they depend on converter topology and operating point.

Analytical models for dead time optimization technique were proposed in [28]. Here, the proposed models consider fixed input parasitic capacitance for analytical solutions. Thus, the effects of nonlinearity in parasitic capacitances are not incorporated which degrades the accuracy of the optimized dead time. To improve the accuracy, nonlinearity of junction capacitances needs to be considered. In [29], an adaptive dead time controller was proposed which considers the nonlinearity of the parasitic capacitances. However, this controller was designed for triangular current modulation; thus, application of this controller for fixed-frequency dc–dc converters is not straightforward. Furthermore, input and output voltages sensing, average current computation, and zero crossing current detection are needed for the controller. Computational burden of the controller is huge as the nonlinearity was incorporated in the models. Two central processing units were exploited to compute the optimal dead time. Thus, this controller will increase the cost of implementation and degrades the power density of the converter. In [30], voltages across switches were modeled considering parasitic inductances and capacitances. Using these models, different losses were decomposed. Based on the losses, dead time can be optimized numerically. However, no analytical expression of optimized dead time was presented. To optimize dead time for the buck converter, an adaptive dual-edge modulator was employed in [31]. The modulator senses the switch-node voltage, input voltage, and output current to compute the optimal dead time. The dead time computation was based on a simplified equation which considers only the parasitic capacitance across the low-side switch. Effects of other parasitic capacitances were ignored. Furthermore, the nonlinear behavior of the parasitic capacitance was not incorporated in the equation. Thus, the proposed modulator-based technique is not very effective under varying load and input voltage conditions.

A buck converter model is created in LTSpice (as shown in Fig. 2) using the Spice model of GS61008P GaN device provided by GaN Systems. Simulation waveforms of gate driver voltage $V_{g2}$ and gate to source voltage of low side FET $S_L$ are shown in Fig. 3. It is evident that the gate to source voltage does not cease to zero immediately. This indicates that the low side FET $S_L$ remains on for some time even with zero gate driver voltage. Turning ON the high side FET $S_H$ during this time may lead to shoot through. Shoot through can be avoided if the high side FET $S_H$ is turned ON when the gate to source voltage of low side FET $S_L$ reaches below the gate threshold voltage. Thus, the time taken by the gate to source voltage to reach below the gate threshold voltage is the lowest dead time requires to avoid shoot through. Typically, Gan FETs have low gate threshold voltage and parasitic inductance in practical gate drive circuit slows down the discharge process of the gate to source capacitance. Therefore, the high side FET should be turned ON once the low side gate-to-source voltage reaches to a very small value. This article is focused to derive this time duration $t_{d,cs}$ (see Fig. 3).

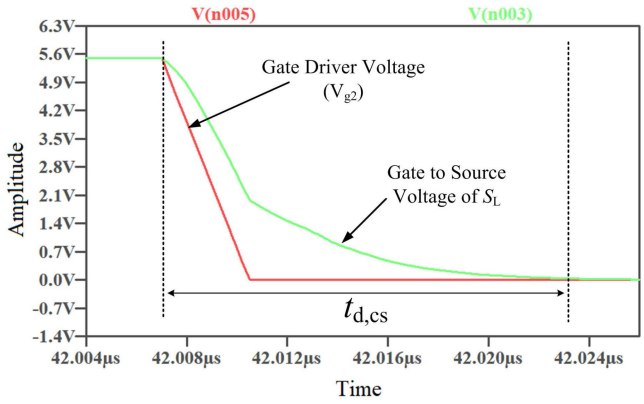


Fig. 3. Simulation waveforms of gate driver voltage $V_{g2}$ and gate-to-source voltage of the GaN device GS61008P.

Unlike MOSFET, the gate to source voltage of the GaN device has no Miller plateau. Thus, the existing modeling approaches available for MOSFETs are not readily applicable.

This article proposes analytical models for heavy and light load conditions. Unlike [28], the proposed work considers gate charge to introduce the effects of nonlinear behavior of the junction capacitances in the analytical models. This makes the model simple and easy to implement in digital controllers compared to the model presented in [29]. Effects of all the parasitic capacitances are considered in the proposed analytical approaches which improve the accuracy of the proposed models compared to the model proposed in [31]. Dead time optimization in real-time can be easily implemented using the proposed models without sensing the switch-node voltage. Furthermore, the proposed analytical approaches can be easily extended to other dc–dc converters.

The rest of this article is organized as follows. Need for dead time optimization in a synchronous buck converter is discussed in Section II. Analytical models for dead time optimization under high and light loads are proposed in Section III. Simulation and experimental validations of the analytical results are presented in Section IV. Finally, Section V concludes this article.

## II. Proposed Analytical Model for Dead Time Optimization

### A. Need for Dead Time Optimization

A synchronous buck converter is more efficient compared to an asynchronous buck converter when operated at high-load and low duty ratio condition [32]. However, to avoid shoot-through in a synchronous buck converter, dead time intervals are introduced into the complementary gate signals. Fig. 4 shows waveforms of the gate drive voltages $V_{g1}$ and $V_{g2}$ in one switching cycle $f_s = 1/T$. Dead time $t_{don}$ is introduced before the turn-ON of the high-side switch $S_H$ and dead time $t_{doff}$ is introduced between the turn-OFF of the high-side switch $S_H$ and turn-ON of the low-side switch $S_L$. Rise and fall time of the gate drive voltages are very small, thus, not shown in Fig. 4.

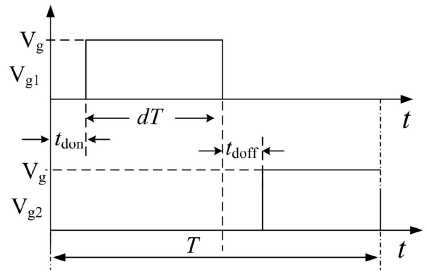


Fig. 4. Gate drive voltages of the high-side and low-side switches. Dead time is applied between two complementary gate signals.

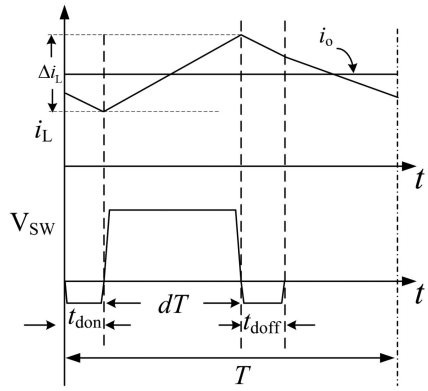


Fig. 5. Impact of dead time on the switch node voltage $V_{SW}$ when the inductor current is positive. The output current $i_o$ is equal to the average inductor current.

Waveform of the switch node voltage under high load condition is shown in Fig. 5. During dead time durations $t_{don}$ and $t_{doff}$, equivalent body diode of the low-side FET $S_L$ conducts. Thus, switch node voltage $V_{SW}$ goes negative during $t_{don}$ and $t_{doff}$. The amplitude of this negative voltage depends on the gate-to-source threshold voltage $V_{th}$, reverse current $i_r$, and ON-resistance of the channel $R_{ds,on}$. Here, the applied gate-to-source voltage $V_g$ is zero, thus, an approximate numerical value of $V_{SW}$ can be calculated from

$$V_{SW} \approx -\left(V_{th} + i_r R_{ds,on}\right). \tag{1}$$

During $t_{don}$ duration, the reverse current $i_r = i_{L,v}$ and during $t_{doff}$ duration the reverse current $i_r = i_{L,p}$; where $i_{L,v}$ and $i_{L,p}$ are the valley and peak inductor currents, respectively.

The power loss $P_{dt}$ during $t_{don}$ and $t_{doff}$ can be calculated using the following:

$$P_{dt} = V_{SW} i_{L,v} t_{don} f_s + V_{SW} i_{L,p} t_{doff} f_s. \tag{2}$$

From (1) it is evident that the forward voltage drop is roughly proportional to the reverse current $i_r$. Thus, efficiency degrades as the load current increases. Power loss in (2) can be minimized by reducing the dead time durations $t_{don}$ and $t_{doff}$. However, too small dead time may lead to shoot-through when both the switches remain in the ON-state. This condition degrades the efficiency and may damage the switches due to excessive current. However, sufficient amount of dead time durations $t_{doff}$ and $t_{don}$ help to achieve a near zero voltage turn-ON and turn-OFF for the

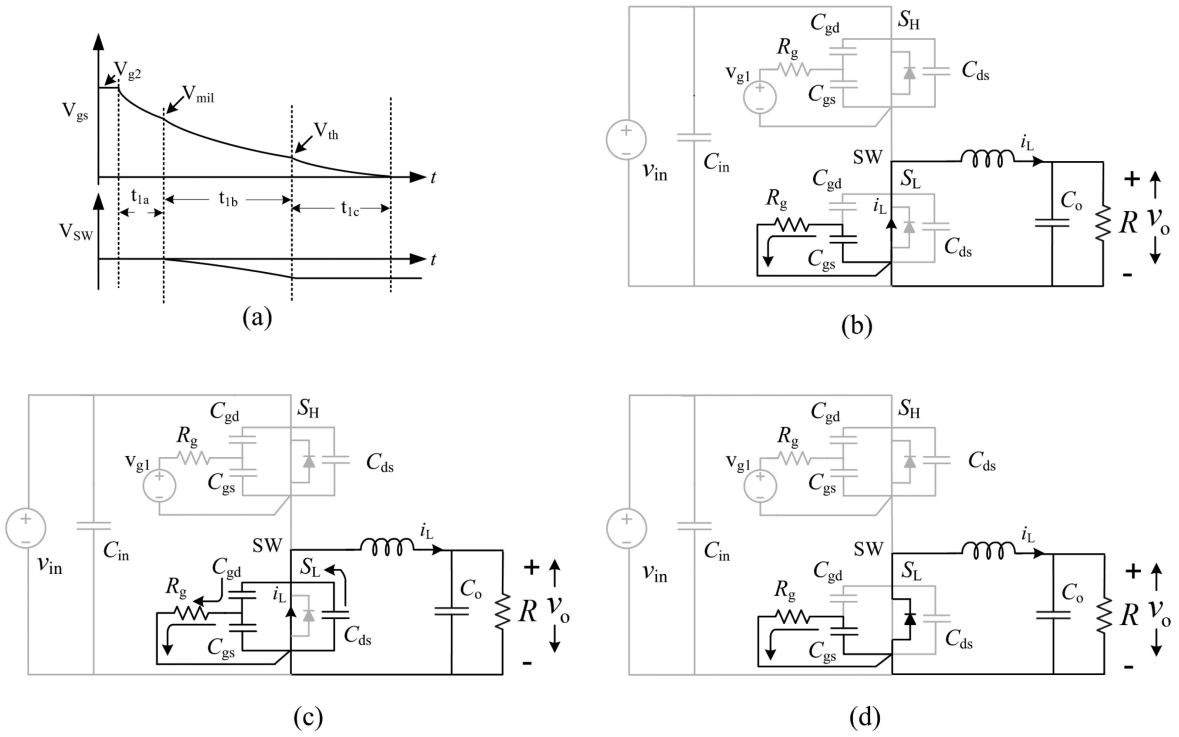


Fig. 6. Turn-OFF stages of the low-side FET $S_{\rm L}$. (a) Waveforms of the gate-to-source voltage and switch-node voltage $V_{\rm SW}$. (b) Equivalent circuit during $t_{1\rm a}$ time duration; $C_{\rm gs}$ discharges through the gate resistance $R_{\rm g}$ and the inductor current $i_{\rm L}$ flows through the channel. (c) Equivalent circuit during $t_{1\rm b}$ time duration; $C_{\rm gd}$ starts discharging and $C_{\rm ds}$ start charging in the reverse direction. (d) Equivalent circuit during $t_{1\rm c}$ time duration; equivalent body diode carries the inductor current $i_{\rm L}$.

low-side FET $S_{\rm L}$, thus, reduce the switching loss. Therefore, optimization of the dead time duration is required to 1) eliminate shoot-through situation; 2) enable near zero voltage switching (ZVS) for the low-side FET $S_{\rm L}$; 3) reduce the loss in (2) due to reverse conduction.

### *B. Dead Time Optimization Under High Load Condition*

*1) Turn-ON Dead Time $t_{\rm don}$ Optimization:* Turn-ON dead time starts when $V_{\rm g2} = 0$. The gate-to-source voltage starts falling from $V_{g2}$ to the Miller voltage $V_{\rm mil}$ as shown in Fig. 6(a). The Miller voltage of the gate at a particular operating point can be calculated from [33]

$$V_{\rm mil} = \frac{i_{\rm ch}}{g_{\rm m}} + V_{\rm th} \tag{3}$$

where $i_{\rm ch}$ is the channel current, $g_{\rm m}$ is the transconductance, and $V_{\rm th}$ is the gate-to-source threshold voltage.

The transconductance $g_{\rm m}$ depends on the channel current $i_{\rm ch}$ and the relationship between the channel current $i_{\rm ch}$ and transconductance $g_{\rm m}$ is nonlinear [34]. Thus, it is difficult to find the exact value of the Miller voltage $V_{\rm mil}$ using (3). A good approximation is to find the average transconductance $g_{\rm m}$ from the following [35] using the drain current $i_{\rm DS}$ versus gate-to-source voltage $V_{\rm gs}$ characteristic curve of the device datasheet

$$g_{\rm m} = \frac{\Delta i_{\rm DS}}{\Delta V_{\rm gs}}. \tag{4}$$

The channel current $i_{\rm ch} = i_{\rm L,v}$ during turn-ON dead time. In a buck converter, the output current $i_{\rm o} = v_{\rm o}/R$ is equal to the average inductor current and the inductor current ripple can be obtained from the following:

$$\frac{\Delta i_{\rm L}}{dT} = \frac{v_{\rm in} - v_{\rm o}}{L}. \tag{5}$$

An expression of the valley inductor current $i_{\rm L,v}$ can be written as follows:

$$i_{\rm L,v} = i_{\rm o} - (\Delta i_{\rm L}/2)\,. \tag{6}$$

By using (5) and (6), the valley current $i_{\rm L,v}$ can be expressed as follows:

$$i_{\rm L,v} = \frac{v_{\rm o}}{R} - \frac{T v_{\rm o}}{2L}\left(1 - \frac{v_{\rm o}}{v_{\rm in}}\right) \tag{7}$$

where $d = v_{\rm o}/v_{\rm in}$.

The Miller voltage $V_{\rm mil}$ can be computed using (3), (4), and (7) as given as follows:

$$V_{\rm mil} = \frac{v_{\rm o}\left(2Lv_{\rm in} - TRv_{\rm in} + TRv_{\rm o}\right)}{2RLv_{\rm in}g_{\rm m}} + V_{\rm th}. \tag{8}$$

The gate-to-source capacitance $C_{\rm gs}$ discharges through the gate resistor $R_{\rm g}$ from $V_{\rm g2}$ to $V_{\rm mil}$ [see Fig. 6(b)] and can be written as follows:

$$V_{\rm mil} = V_{\rm g2} e^{-t_{1\rm a}/(R_{\rm g}C_{\rm gs})}. \tag{9}$$

From (9), time duration $t_{1\rm a}$ can be obtained. During this time, the gate-to-drain capacitance also loses a small amount

of charge. However, to maintain the simplicity of the analytical model, the gate-to-drain capacitance is not considered in (9).

Unlike MOSFETs, the Miller voltage is not constant in GaN FETs during the time duration $t_{1b}$ in Fig. 6(a). This indicates that all the parasitic capacitances discharge during this time [see Fig. 6(c)]. Furthermore, $C_{gd}$ and $C_{ds}$ are not fixed capacitances; thus, time duration $t_{1b}$ cannot be obtained using (9). However, the gate charge $Q_g$ data can be obtained from the device datasheet, which can be exploited to calculate an equivalent capacitance $C_{eq}$ using (10) and (11). This approach does not need to calculate the exact value of the nonlinear capacitances $C_{gd}$ and $C_{ds}$ using differential equations. Thus, the proposed analytical model becomes simpler

$$Q_{1b} = Q_g - Q_{g(th)} - Q_{1a} \tag{10}$$

$$Q_{1b} = C_{eq}\left(V_{mil} - V_{th}\right) \tag{11}$$

where $Q_{1b}$ is the gate charge for the time duration $t_{1b}$ and $Q_{g(th)}$ is the gate threshold charge. $Q_{1a}$ is the gate charge for the time duration $t_{1a}$ and can be computed using the following:

$$Q_{1a} = C_{gs}\left(V_{g2} - V_{mil}\right). \tag{12}$$

The time duration $t_{1b}$ can be calculated using the standard capacitor discharge equation as follows:

$$t_{1b} = -R_g C_{eq} \ln \frac{V_{th}}{V_{mil}}. \tag{13}$$

During time duration $t_{1c}$ in Fig. 6(a), the gate-to-source voltage $V_{gs}$ reaches to zero from the gate-to-source threshold voltage $V_{th}$ and this duration can be obtained using the following:

$$V_{\varepsilon} = V_{th} e^{-t_{1c}/(R_g C_{gs})}. \tag{14}$$

$V_{\varepsilon}$ can be taken as $0.1$ V for numerical calculation. During the time duration $t_{1c}$, the equivalent body diode of the low side FET $S_L$ conducts [see Fig. 6(d)]. At the end of the time duration $t_{1c}$ the high-side FET $S_H$ can be turned ON. So far the model is derived without considering the driver circuit's fall-time. A practical driver has a nonzero fall-time. This will introduce addition delay in the turn-OFF process of the low-side FET. Thus, the optimized turn-ON dead time $t_{don} = t_{1a} + t_{1b} + t_{1c} + t_{f,L}$; where, $t_{f,L}$ is the fall-time of the low-side driver. The final expression of the optimized turn-ON dead time $t_{don}$ is obtained in the following using (9), (13), and (14):

$$t_{don} = t_{f,L} - \left(R_g C_{gs} \ln \frac{V_{mil}}{V_{g2}} + R_g C_{eq} \ln \frac{V_{th}}{V_{mil}} + R_g C_{gs} \ln \frac{V_{\varepsilon}}{V_{th}}\right). \tag{15}$$

Time duration $t_{1c}$ is considered for dead time calculation to avoid shoot-through condition. However, this duration can be eliminated if the high-side driver circuit has a significant amount of rise time.

Impacts of variations in switching frequency $f_s$ and duty ratio on the turn-ON dead time $t_{don}$ can be assessed from (8). The $t_{don}$ expression in (15) does not contain frequency or duty ratio terms. However, the Miller voltage $V_{mil}$ in (15) depends on duty ratio and switching frequency of the converter. Simplification of (8) provides the following expression:

$$V_{mil} = V_{th} + \frac{v_o}{R g_m} - \frac{v_o}{2 f_s L g_m}\left(1 - \frac{v_o}{v_{in}}\right). \tag{16}$$

An increase in switching frequency will decrease the magnitude of the term $\frac{v_o}{2 f_s L g_m}(1 - \frac{v_o}{v_{in}})$. This will increase the Miller voltage. An increase in the Miller voltage will decrease time durations $t_{1a}$ and $t_{1b}$. Thus, the turn-ON dead time $t_{don}$ decreases as switching frequency increases. The $LC$ filter of the buck converter is designed based on switching frequency and allowable ripples in the inductor current and output voltage. Thus, a large variation in switching frequency is not desirable. In Section IV, the effect of frequency variation on the turn-ON dead time is demonstrated graphically using numerical values of the system parameters.

If the input voltage of the converter increases and other parameters remain constant, the magnitude of the term $\frac{v_o}{2 f_s L g_m}(1 - \frac{v_o}{v_{in}})$ will increase. This will decrease the Miller voltage and increase the turn-ON dead time $t_{don}$. In Section IV, the effect of input voltage variation on the turn-ON dead time is shown graphically using numerical values of the system parameters.

*2) Turn-OFF Dead Time $t_{doff}$ Optimization:* Turn-OFF dead time starts when $V_{g1}$ goes to zero. The gate-to-source voltage of the high-side FET $S_H$ starts falling from $V_{g1}$ to the Miller voltage $V_{mil}$ as shown in Fig. 7(a) as the gate-to-source capacitance $C_{gs}$ discharges through the gate resistor $R_g$ [see Fig. 7(b)]. The channel current $i_{ch}$ is equal to the peak inductor current $i_{L,p}$ as given in the following:

$$i_{L,p} = i_o + \left(\Delta i_L / 2\right). \tag{17}$$

Using (5) and (17), the peak inductor current $i_{L,p}$ can be expressed as given in the following:

$$i_{L,p} = \frac{v_o}{R} + \frac{T v_o}{2L}\left(1 - \frac{v_o}{v_{in}}\right). \tag{18}$$

The Miller voltage at the end of the time duration $t_{2a}$ can be obtained using the methodology discussed in Section II-B1 and replacing $i_{ch}$ with $i_{L,p}$ in (3). Duration of this interval $t_{2a}$ can be obtained as

$$t_{2a} = -R_g C_{gs} \ln \frac{V_{mil}}{V_{g1}}. \tag{19}$$

During the time duration $t_{2b}$ in Fig. 7(a), the input and output capacitances of the high-side FET $S_H$ discharge [see Fig. 7(c)]. Using the similar procedure as discussed for the $t_{don}$ time for the positive current, an equivalent capacitance $C_{eq}$ can be found using (10) and (11). Thus, the time duration $t_{2b}$ can be obtained as

$$t_{2b} = -R_g C_{eq} \ln \frac{V_{th}}{V_{mil}}. \tag{20}$$

During the time duration $t_{2c}$ in Fig. 7(a), the gate-to-source voltage $V_{gs}$ of the high-side FET $S_H$ reaches to zero from the gate-to-source threshold voltage $V_{th}$ and this duration can be computed using the methodology discussed for $t_{1c}$ duration. During this interval, the equivalent body diode of the low side FET $S_L$ conducts [see Fig. 7(d)]. At the end of this interval $t_{2c}$, the low-side FET $S_L$ can be turned ON. Thus, the optimized

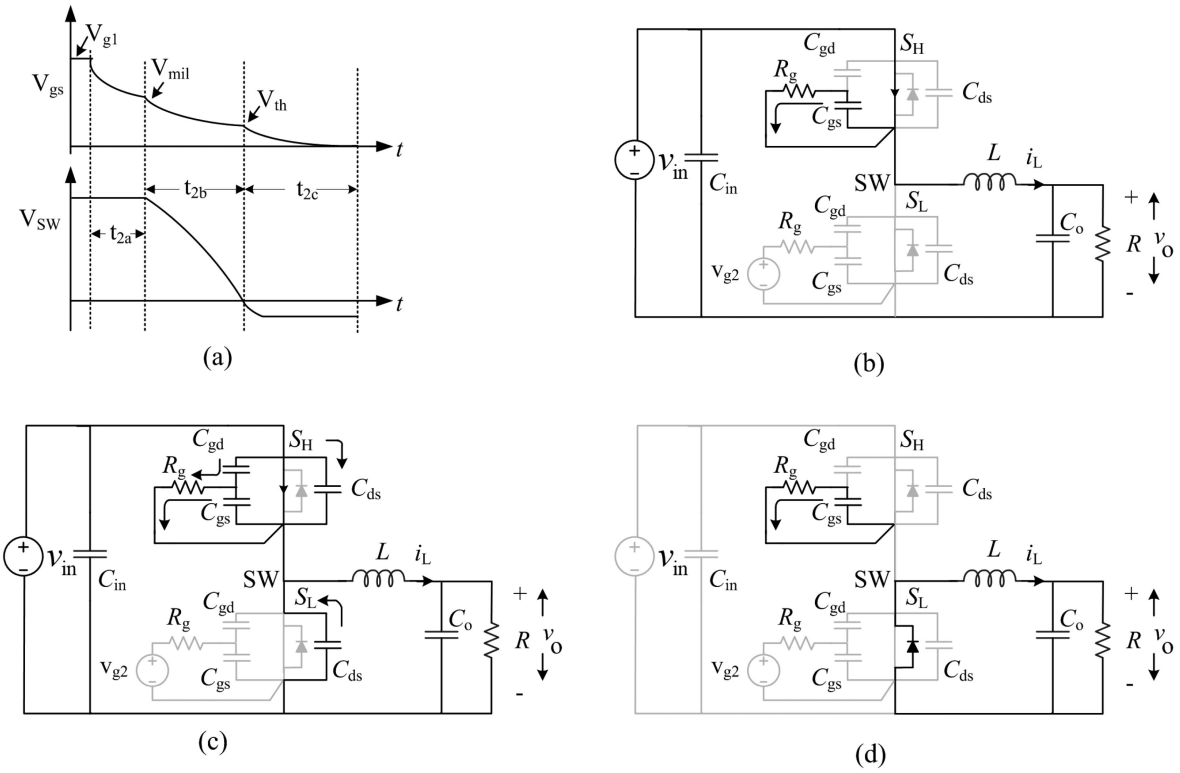


Fig. 7. Turn-OFF stages of the high-side FET $S_{\rm H}$. (a) Waveforms of the gate-to-source voltage and switch-node voltage $V_{\rm SW}$. (b) Equivalent circuit during $t_{2\rm a}$ time duration; $C_{\rm gs}$ discharges through the gate resistance $R_{\rm g}$ and the inductor current $i_{\rm L}$ flows through the channel. (c) Equivalent circuit during $t_{2\rm b}$ time duration; $C_{\rm gd}$ starts discharging and $C_{\rm ds}$ start charging. (d) Equivalent circuit during $t_{2\rm c}$ time duration; equivalent body diode of the low-side FET $S_{\rm L}$ carries the inductor current $i_{\rm L}$.

turn-OFF dead time is obtained in the following:

$$t_{\rm doff} = t_{2\rm a} + t_{2\rm b} + t_{2\rm c} + t_{\rm f,H} \tag{21}$$

where $t_{\rm f,H}$ is the fall-time of the high-side driver. The effects of switching frequency and duty ratio variations on turn-OFF dead time can be demonstrated in a similar manner as discussed in the previous section.

Unlike the controller in [29], the derived analytical expressions of optimized dead-time in (15) and (21) do not need any complex calculation. Thus, the proposed analytical models significantly reduce the controller's burden. Furthermore, detection of zero crossing current and computation of average current are not required.

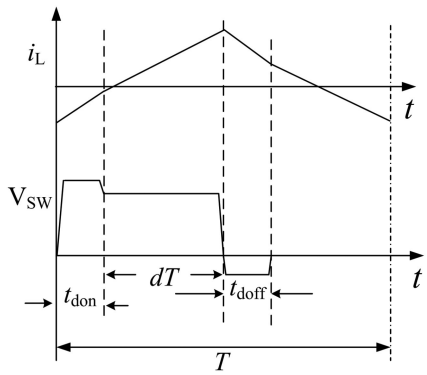


Fig. 8. Impact of dead time on the switch node voltage $V_{\rm SW}$ when the inductor current goes negative.

### *C. Dead-Time Optimization Under Light Load Condition*

Waveform of the switch node voltage under light load condition is shown in Fig. 8. During dead-time $t_{\rm don}$, the equivalent body diode of the high-side FET $S_{\rm H}$ conducts. Due to the negative inductor current, the drain-to-source capacitance $C_{\rm ds}$ dumps the stored energy to the supply. Thus, an optimized turn-ON dead-time $t_{\rm don}$ enables ZVS for the high-side FET $S_{\rm H}$ and reduces the power loss in (2). Similarly, during turn-OFF dead-time $t_{\rm doff}$, the equivalent body diode of the low-side FET $S_{\rm L}$ conducts. This achieves ZVS for the low-side FET $S_{\rm L}$.

*1) Turn-ON Dead-Time $t_{\rm don}$ Optimization:* The turn-ON dead-time starts when $V_{\rm g2} = 0$. The gate-to-source voltage $V_{\rm gs}$ starts falling from $V_{\rm g2}$ to the Miller voltage $V_{\rm mil}$ as shown in Fig. 9(b). Under light load condition $V_{\rm mil} = V_{\rm th}$ as $i_{\rm ch}/g_{\rm m}$ term in (3) is negligible. Thus, turn-OFF process of the low-side FET can be divided into two stages. The first stage ends when $V_{\rm gs}$ reaches to $V_{\rm th}$ as shown in Fig. 9(a) and the duration of this stage $t_{3\rm a}$ can be obtained from the following:

$$V_{\rm th} = V_{\rm g2} e^{-t_{3\rm a}/(R_{\rm g} C_{\rm gs})}. \tag{22}$$

At the beginning of the second stage, the channel current $i_{\rm ch}$ ceases to zero as the gate-to-source voltage $V_{\rm gs}$ goes below the gate threshold voltage $V_{\rm th}$. Thus, the inductor current $i_{\rm L}$ flows

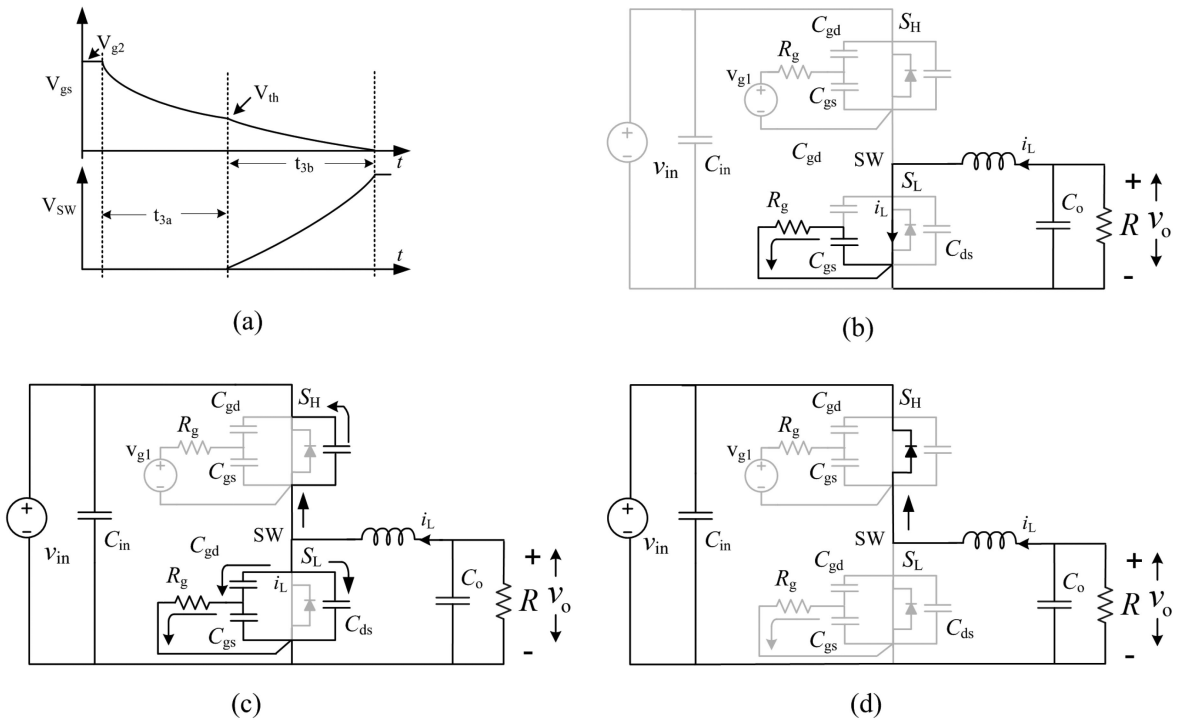


Fig. 9. Turn-OFF stages of the low-side FET $S_{\rm L}$. (a) Waveforms of the gate-to-source voltage and switch-node voltage $V_{\rm SW}$. (b) Equivalent circuit during $t_{3\rm a}$ time duration; $C_{\rm gs}$ discharges through the gate resistance $R_{\rm g}$ and the inductor current $i_{\rm L}$ flows through the channel. (c) Equivalent circuit during $t_{3\rm b}$ time duration; $C_{\rm gd}$ is discharging and $C_{\rm ds}$ of the high-side FET $S_{\rm H}$ is discharging and $C_{\rm ds}$ of the low-side FET is charging. (d) Equivalent body diode of the high-side FET carries the inductor current $i_{\rm L}$.

through the drain-to-source capacitance of the high-side FET $S_{\rm H}$ and output capacitance $C_{\rm oss} = C_{\rm gd} + C_{\rm ds}$ of the low-side FET $S_{\rm L}$ as shown in Fig. 9(c). This process will discharge the drain-to-source capacitance $C_{\rm ds}$ of the high-side FET $S_{\rm H}$ and charges the drain-to-source capacitance $C_{\rm ds}$ of the low side FET $S_{\rm L}$ to $V_{\rm in} + V_{\rm d}$; where $V_{\rm d}$ is the forward voltage drop of the equivalent body diode of the high-side FET $S_{\rm H}$. The duration of the second stage $t_{3\rm b}$ [see Fig. 9(a) and (c)] can be obtained from (23), where $Q_{\rm oss}$ is the output charge of the GaN FET. The output capacitance $C_{\rm oss}$ varies as the voltage across the drain to source changes [34]. Thus, the output charge $Q_{\rm oss}$ is considered in the following:

$$t_{3\rm b} = \frac{2Q_{\rm oss}}{i_{\rm L,v}}. \tag{23}$$

At the end of the second stage, the equivalent body diode of the high-side FET $S_{\rm H}$ conducts the inductor current $i_{\rm L}$ as shown in Fig. 9(d). Therefore, to eliminate the reverse conduction loss, the high-side FET $S_{\rm H}$ needs to be turned ON immediately after the end of the second stage. Thus, the optimized turn-ON dead time $t_{\rm don}$ can be obtained using (22) and (23) as given in the following:

$$t_{\rm don} = -R_{\rm g}C_{\rm gs}\ln\frac{V_{\rm th}}{V_{\rm g2}} + \frac{2Q_{\rm oss}}{i_{\rm L,v}} + t_{\rm f,L}. \tag{24}$$

*2) Turn-OFF Dead Time $t_{\rm doff}$ Optimization:* Turn-OFF dead time starts when $V_{\rm g1} = 0$. Similar to the turn-ON dead time under the negative inductor current condition, the turn-OFF dead time can be divided into two stages as shown in Fig. 10(a). The first stage ends when $V_{\rm gs}$ reaches to $V_{\rm th}$ as shown in Fig. 10(a) and (b) and the duration of this stage $t_{4\rm a}$ can be obtained using (22) by replacing $t_{3\rm a}$ by $t_{4\rm a}$ and $V_{\rm g2}$ by $V_{\rm g1}$.

In the second stage, the channel current $i_{\rm ch}$ ceases to zero. The inductor current $i_{\rm L}$ flows through the drain-to-source capacitance of the low-side FET $S_{\rm L}$ and output capacitance of the high-side FET $S_{\rm H}$ as shown in Fig. 10(c). This process will discharge the drain-to-source capacitance $C_{\rm ds}$ of the low-side FET $S_{\rm L}$ and charges the drain-to-source capacitance $C_{\rm ds}$ of the high-side FET $S_{\rm H}$ to $V_{\rm in}$. The duration of the second stage $t_{4\rm b}$ [see Fig. 10(a)] can be obtained from (23). At the end of the second stage, the equivalent body diode of the low-side FET $S_{\rm L}$ conducts the inductor current $i_{\rm L}$ as shown in Fig. 10(d). Therefore, to eliminate the reverse conduction loss, the low-side FET $S_{\rm L}$ needs to be turned ON immediately after the end of the second stage. Thus, the optimized turn-OFF dead time is derived as

$$t_{\rm doff} = t_{4\rm a} + t_{4\rm b} + t_{\rm f,H}. \tag{25}$$

Variations in switching frequency and duty ratio affect the turn-ON and turn-OFF dead time durations under light load conditions. The rate of displacement of the output charge $Q_{\rm oss}$ depends on the value of the inductor current at the dead time durations. At turn-ON dead time, the inductor current is equal to the valley of the inductor current $i_{\rm L,v}$ and at turn-OFF, it is peak of the inductor current $i_{\rm L,p}$. The peak-to-peak ripple of the inductor current is inversely proportional to the switching frequency and

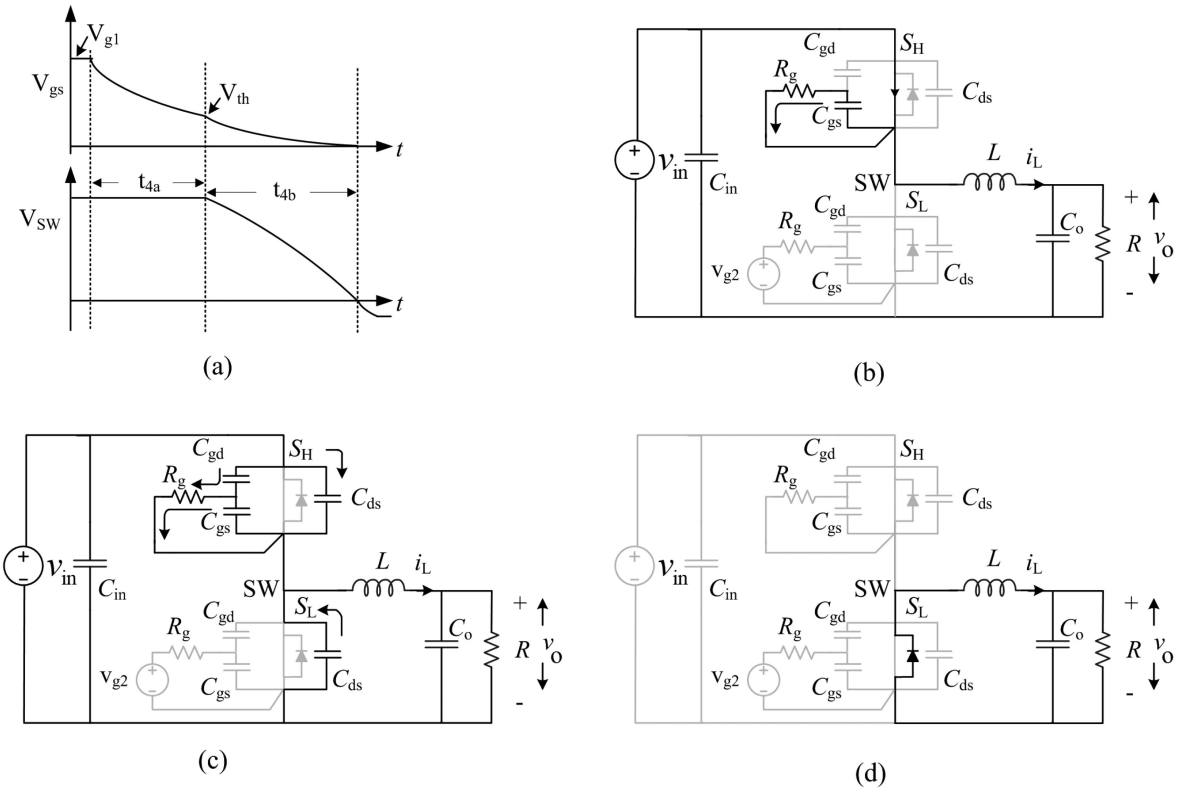


Fig. 10. Turn-OFF stages of the high-side FET $S_{\rm H}$. (a) Waveforms of the gate-to-source voltage and switch-node voltage $V_{\rm SW}$. (b) Equivalent circuit during $t_{4a}$ time duration; $C_{\rm gs}$ discharges through the gate resistance $R_{\rm g}$ and the inductor current $i_{\rm L}$ flows through the channel. (c) Equivalent circuit during $t_{4b}$ time duration; $C_{\rm gd}$ is discharging and $C_{\rm ds}$ of the high-side FET $S_{\rm H}$ is charging and $C_{\rm ds}$ of the low-side FET is discharging. (d) Equivalent body diode of the low-side FET $S_{\rm L}$ carries the inductor current $i_{\rm L}$.

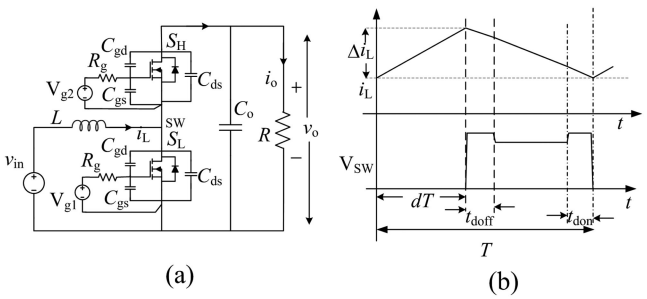


Fig. 11. (a) GaN-based synchronous boost converter. (b) Impact of dead time on the switch node voltage $V_{\rm SW}$ when the inductor current is always positive.

duty ratio. Thus, an increase in switching frequency or duty ratio will decrease the peak-to-peak inductor current ripple. Decrease in ripple will decrease $i_{\rm L,v}$ and $i_{\rm L,p}$. Thus, the magnitude of $\frac{2Q_{\rm oss}}{i_{\rm L,v}}$ in (24) will increase. As a result, optimized dead time duration will increase. In Section IV, the effect of frequency and duty ratio variations on turn-ON dead time under light load conditions is demonstrated graphically using numerical values of the system parameters.

## III. Extension to a Boost Converter

Schematic of a GaN-based synchronous boost converter is shown in Fig. 11(a). Here, $v_{\rm in}$ is the input voltage, $v_{\rm o}$ is the output voltage, and $R$ is the load resistance of the boost converter. $L$ is the inductor and $C_{\rm o}$ is the output capacitor. The gate drive voltages $V_{\rm g1}$ and $V_{\rm g2}$ are applied to the low-side and high-side FETs, respectively. Gate resistance $R_{\rm g}$ is used to control the ON/OFF slew rate. Capacitor $C_{\rm gs}$ refers to the gate to source parasitic capacitance. The gate-to-drain parasitic capacitance is shown as $C_{\rm gd}$ and $C_{\rm ds}$ refers to the drain-to-source capacitance. To model the reverse conduction of the GaN HEMT at gate voltage $V_{\rm g1} = V_{\rm g2} = 0$, antiparalleled body diodes are shown in both the GaN FETs $S_{\rm H}$ and $S_{\rm L}$. The two switches $S_{\rm H}$ and $S_{\rm L}$ [shown in Fig. 11(a)] operate in a complementary fashion. To avoid shoot-through, dead times are introduced between the state transition of two gate signals. Waveform of the switch node voltage under high load condition is shown in Fig. 11(b). During dead time durations $t_{\rm don}$ and $t_{\rm doff}$, equivalent body diode of the high-side FET $S_H$ conducts. Thus, the switch node voltage $V_{\rm SW}$ goes to $v_{\rm d} + v_{\rm o}$ during $t_{\rm don}$ and $t_{\rm doff}$ durations. Amplitude of $v_{\rm d}$ depends on the gate-to-source threshold voltage $V_{\rm th}$, reverse current $i_{\rm r}$, and ON-resistance of the channel $R_{\rm ds,on}$ and can be written as

$$v_d \approx (V_{th} + i_{\rm r} R_{\rm ds,on})\,. \tag{26}$$

During $t_{\rm don}$ duration, the reverse current $i_{\rm r} = i_{\rm L,v}$ and during $t_{\rm doff}$ duration the reverse current $i_{\rm r} = i_{\rm L,p}$, where $i_{\rm L,v}$ and $i_{\rm L,p}$ are the valley and peak inductor currents, respectively.

Turn-ON dead time starts when $V_{\rm g2} = 0$. The gate-to-source voltage starts falling from $V_{g2}$ to the Miller voltage $V_{\rm mil}$ as shown

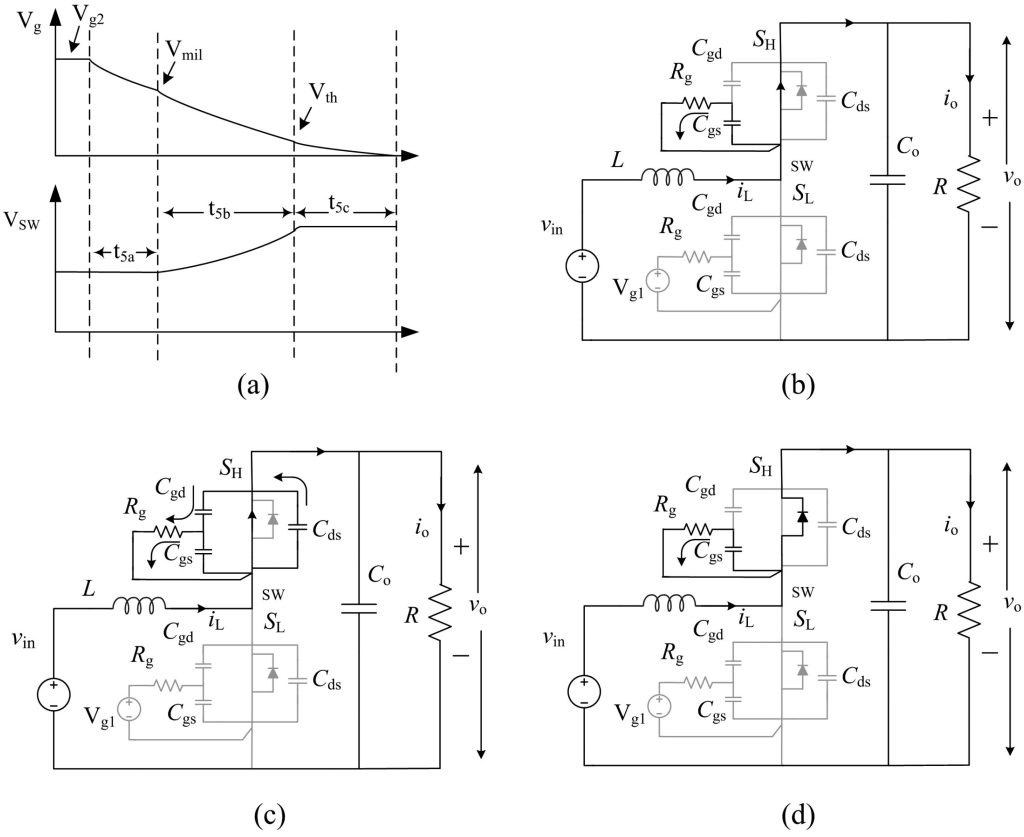


Fig. 12. Turn-OFF stages of the high-side FET $S_{\rm H}$. (a) Waveforms of the gate-to-source voltage and switch-node voltage $V_{\rm SW}$. (b) Equivalent circuit during $t_{5\rm a}$ time duration; $C_{\rm gs}$ discharges through the gate resistance $R_{\rm g}$ and the inductor current $i_{\rm L}$ flows through the channel. (c) Equivalent circuit during $t_{5\rm b}$ time duration; $C_{\rm gd}$ is discharging and $C_{\rm ds}$ of the high-side FET $S_{\rm H}$ is charging. (d) Equivalent body diode of the high-side FET $S_{\rm H}$ carries the inductor current $i_{\rm L}$ during $t_{5\rm c}$.

in Fig. 12(a). The Miller voltage of the gate at a particular operating point can be calculated using (3). The transconductance $g_{\rm m}$ can be computed using the drain current $i_{\rm DS}$ vs gate-to-source voltage $V_{\rm gs}$ characteristic curve of the device datasheet. The channel current $i_{\rm ch} = i_{\rm L,v}$ during turn-ON dead time. An expression of the valley inductor current $i_{\rm L,v}$ of the boost converter can be written as

$$i_{\rm L,v} = \frac{i_{\rm o} v_{\rm o}}{v_{\rm in}} - \frac{v_{\rm in} T \left(1 - \frac{v_{\rm in}}{v_{\rm o}}\right)}{2L}. \tag{27}$$

The Miller voltage $V_{\rm mil}$ can be computed using (3), (4), and (27) as given as follows:

$$V_{\rm mil} = \frac{2L\Delta V_{\rm gs} v_o^3 - TRv_{\rm in}^2(v_{\rm o} - v_{\rm in})\Delta V_{\rm gs}}{2Rv_{\rm in} L v_{\rm o} \Delta i_{\rm DS}} + V_{\rm th}. \tag{28}$$

The gate-to-source capacitance $C_{\rm gs}$ discharges through the gate resistor $R_{\rm g}$ from $V_{\rm g2}$ to $V_{\rm mil}$ [see Fig. 12(b)]. Time duration $t_{5\rm a}$ can be obtained by replacing $t_{1\rm a}$ with $t_{5\rm a}$ in (9). The time duration $t_{5\rm b}$ can be calculated by computing the equivalent capacitance as discussed in Section II-B1 and using (12) and (13). Time duration $t_{5\rm c}$ can be computed using the equation in (14) by replacing $t_{1\rm c}$ by $t_{5\rm c}$. During the time duration $t_{5\rm c}$, the equivalent body diode of the high-side FET $S_{\rm H}$ conducts as shown in Fig. 12(c). At the end of the time duration $t_{5\rm c}$, the low-side FET $S_{\rm L}$ can be turned ON. Thus, the optimized turn-ON dead time $t_{\rm don} = t_{5\rm a} + t_{5\rm b} + t_{5\rm c} + t_{\rm f,H}$, where $t_{\rm f,H}$ is the fall-time of the high-side driver. Following a similar procedure, the optimized dead time duration $t_{\rm doff}$ under heavy load can be computed.

TABLE I
PARAMETER SET

| $v_{\rm in}$ (V) | $v_{\rm o}$ (V) | $C_{\rm o}$ ($\mu$F) | $L$ ($\mu$H) | $R$ ($\Omega$) | $f_{\rm s}$ (kHz) |
|---|---|---|---|---|---|
| 24-40 | 12 | 288 | 3.3 | 1.35-50 | 500 |

## IV. Simulation and Experimental Verification of the Proposed Model

### A. Simulation Verification

To validate the proposed model, circuit simulations are carried out using LTSpice. Parameters for the simulations are taken from Table I. A SPICE model of GS61008P from GaN Systems is used as both high-side and low-side switches. The gate drive circuit is designed using two programmable independent voltage sources. To make it more realistic, rise time of 7 ns and fall time of 3.5 ns are incorporated in the voltage source. Furthermore, pull-up resistance $R_{\rm g,on} = 4.1\,\Omega$ and pull-down resistance $R_{\rm g,off} = 1.6\,\Omega$ are also added. Parasitic resistances of other components are also added to the simulation model. For numerical computation

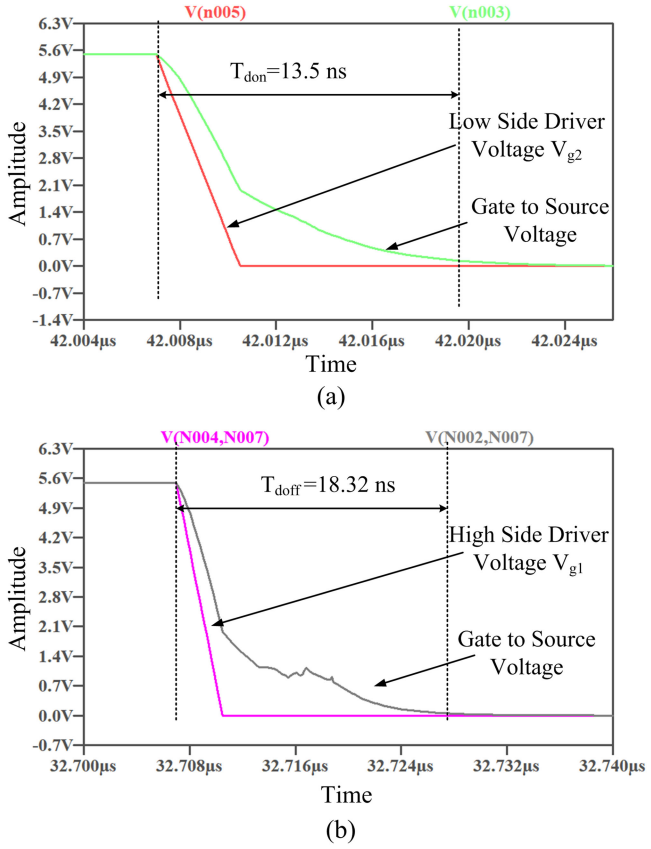


Fig. 13. Gate to source voltage waveforms at $R = 1.35\,\Omega$. (a) Gate to source voltage waveform of the low-side FET during turn-ON dead time ($t_{\rm don}$). (b) Gate-to-source voltage waveform of the high-side FET during turn-OFF dead time ($t_{\rm doff.}$).

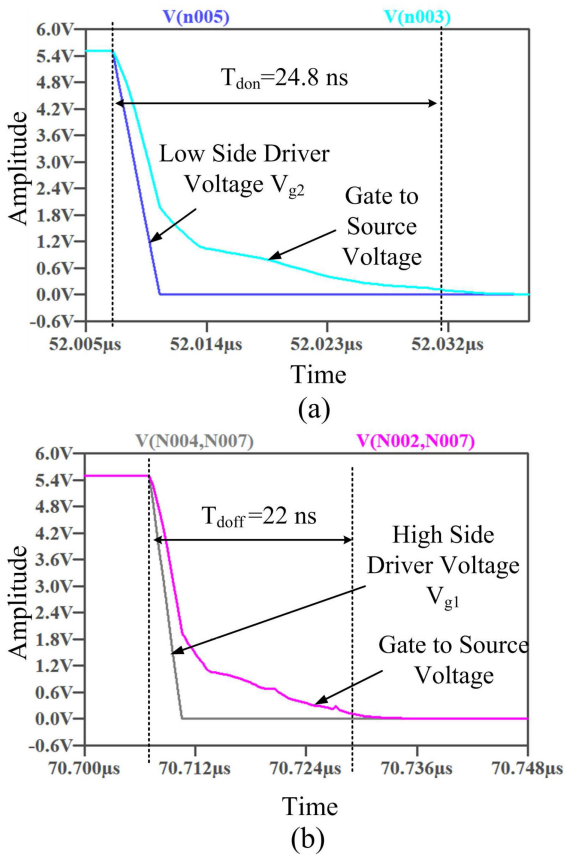


Fig. 14. Gate-to-source voltage waveforms at $R = 50\,\Omega$. (a) Gate-to-source voltage waveform of the low-side FET during turn-ON dead time ($t_{\rm don}$). (b) Gate-to-source voltage waveform of the high-side FET during turn-OFF dead time ($t_{\rm doff.}$).

TABLE II
COMPARATIVE STUDY AT $R = 1.35\,\Omega$

| Dead Time | LTSpice Simulation (ns) | Obtained From Proposed Model (ns) |
|---|---|---|
| $t_{\rm don}$ | 13.5 | 15.97 |
| $t_{\rm doff}$ | 18.32 | 15.54 |

TABLE III
COMPARATIVE STUDY AT $R = 50\,\Omega$

| Dead Time | LTSpice Simulation (ns) | Obtained From Proposed Model (ns) |
|---|---|---|
| $t_{\rm don}$ | 24.8 | 22.3 |
| $t_{\rm doff}$ | 22 | 18.93 |

using the proposed models, $V_{\rm th} = 1.1$ V and $g_{\rm m} = 28$ S are taken. Fig. 13(a) shows the gate-to-source voltage pattern of the low-side FET when the low-side driver voltage becomes zero. The time taken by the gate to source voltage to reach from 5.5 to 0.1 V is 13.5 ns. Under a similar operating condition, the derived model in (15) provides 15.97 ns (see Table II). The gate to source voltage pattern of the high-side FET when high side driver voltage becomes zero is shown in Fig. 13(b). The high-side gate to source voltage reaches 0.1 from 5.5 V within 18.32 ns. The derived model in (21) provides 15.54 ns.

The gate-to-source voltages of the high-side and low-side FETs under light load conditions are also investigated using LTSpice simulation. Fig. 14 shows that the low-side gate to source voltage takes 24.8 ns to reach to 0.1 V and the high-side gate to source voltage takes 22 ns to reach to 0.1 V. These values are compared with the numerical values obtained from the proposed analytical models in (24) and (25) and shown in Table III. The comparison shows a close correlation between the numerical and simulation values. Furthermore, the numerical values of $t_{\rm don}$ and $t_{\rm doff}$ obtained from the analytical models are validated experimentally in a GaN-based buck converter and discussed in the next section.

To quantify the impact of dead time, simulations are carried with different $t_{\rm doff}$ dead time values. Fig. 15 shows as the turn-OFF dead time decreases, reverse conduction loss also decreases. Similar study can be carried out with turn-ON dead time also.

To see the effect of variation in switching frequency on turn-ON dead time under heavy load conditions, a graph is plotted using (15) and (16). The input voltage $v_{\rm in} = 40$ V, and $R = 1.35\,\Omega$ are chosen and other parameters remain the same. Switching frequency varies from 400 to 500 kHz. The graph

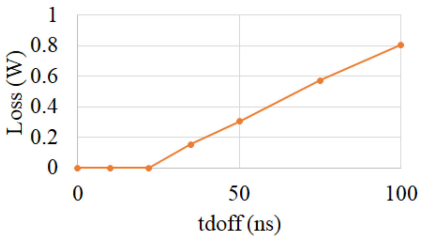


Fig. 15. Turn-OFF dead time ($t_{\mathrm{doff}}$) versus reverse recovery loss.

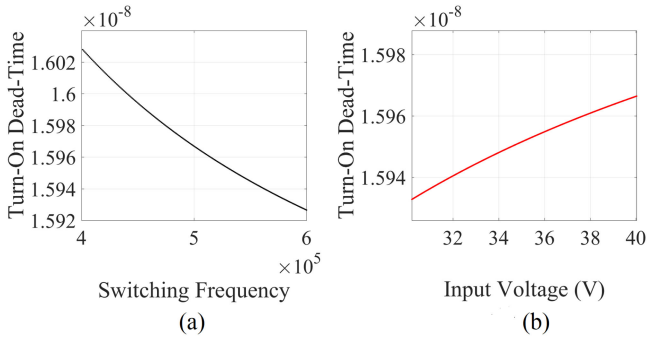


Fig. 16. Effects of variations in switching frequency and input voltage on turn-ON dead-time at $R = 1.35\,\Omega$. (a) Switching frequency varies from 400 to 500 kHz. (b) Input voltage varies from 30 to 40 V.

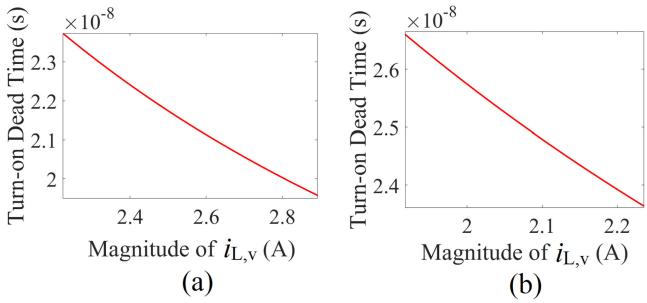


Fig. 17. Effects of variations in switching frequency and duty ratio on turn-ON dead-time at $R = 50\,\Omega$. (a) $i_{\mathrm{L,v}}$ varies from 2.225 to 2.892A due to variation in switching frequency from 500 to 400 kHz. (b) $i_{\mathrm{L,v}}$ varies from 1.918 to 2.235 A due to variation in duty from 0.4 to 0.3 (input voltage varies from 30 to 40 V).

TABLE IV
EFFICIENCY COMPARISON IN SIMULATION AT $f_{\mathrm{s}} = 500$ KHZ AND $v_{\mathrm{in}} = 40$ V

| $R$ ($\Omega$) | Efficiency achieved using technique in [28] | Efficiency achieved using proposed technique |
|---|---|---|
| 1.35 | 95.861 | 96.034 |
| 50 | 74.525 | 83.093 |

in Fig. 16(a) shows that as the switching frequency increases the turn-ON dead-time decreases. This is consistent with the analysis presented in Section II-B1. From the graph it is clear that variation in switching frequency does not significantly affect the turn-ON dead time.

Similarly, under heavy load, the effect of variation in the input voltage on turn-ON dead-time can be demonstrated by plotting a graph using (15) and (16). Switching frequency $f_{\mathrm{s}} = 500$ kHz and $R = 1.35\,\Omega$ and other parameters remain the same. The input voltage $v_{\mathrm{in}}$ varies from 30 to 40 V. The graph in Fig. 16(b) shows that as the input voltage increases the turn-ON dead-time increases. This pattern is consistent with the analysis presented in Section II-B1. A similar study can also be carried out using (18) and (21) for turn-OFF dead time ($t_{\mathrm{doff}}$). It can be seen from the graph that a variation in the input voltage has an insignificant effect on turn ON dead-time. Thus, adjustment of dead time for different duty ratios is not required.

Under light load conditions ($R = 50\,\Omega$), variation in switching frequency from 500 to 400kHz at $v_{\mathrm{in}} = 40$ V causes a variation in magnitude of $i_{\mathrm{L,v}}$ from 2.225 to 2.892A. This variation in $i_{\mathrm{L,v}}$ is used in (24) to show the effect of switching frequency variation on turn-ON dead time graphically in Fig. 17(a). During $t_{\mathrm{don}}$, $i_{\mathrm{L,v}}$ is negative. This indicates that the direction of the inductor current is opposite; thus, negative sign is ignored while plotting the graph. Similarly, when duty ratio varies from 0.4 to 0.3, magnitude of $i_{\mathrm{L,v}}$ varies from 1.918 to 2.235A. This variation in $i_{\mathrm{L,v}}$ is used in (24) to produce the graph in Fig. 17(b). The graphs in Fig. 17 manifest that as the $i_{\mathrm{L,v}}$ increases (switching frequency decreases or input voltage increases), the optimized turn-ON dead time decreases. Furthermore, it is evident from the graphs that under light load conditions, the effects of switching frequency and input voltage variations on turn-ON dead time are significant compared to heavy load conditions. A similar discussion can be also carried out for turn-OFF dead time duration.

To show the effectiveness of the proposed dead time optimization technique in improving efficiency, the same LT Spice model of the buck converter is considered and compared with efficiency achieved using the method proposed in [28]. Efficiency obtained using both these methods are tabulated in Table IV. Comparison shows that the proposed method is more efficient in improving the efficiency.

The dead time optimization models in [28] provide aggressive dead time to improve efficiency. Simulation waveforms of the gate voltages using the method in [28] at $R = 1.35\,\Omega$ and $R = 50\,\Omega$ are shown in Fig. 18. It can be seen that at $R = 1.35\,\Omega$ the gate-to-source voltage of low-side and high-side FETs are crossing each other at 1 V [see Fig. 18(a)]. However, as the load decreases to 0.24A ($R = 50\,\Omega$), these two voltages cross each other at 1.12 V as shown in Fig. 18(b). This causes shoot-through as the gate-to-source threshold voltage of the selected GaN device is 1.1 V. This leads to efficiency degradation as shown in Table IV.

### B. Experimental Verification

To validate the analytical model, a 120 W GaN-based buck converter prototype is built (see Fig. 19) using the parameter set in Table I. GS61008P from GaN Systems is used as both high-side and low-side switches. To drive these switches, a half-bridge GaN driver (LM5113QDPRRQ1 from Texas Instruments) is chosen. The PWM signals for the switches are generated using

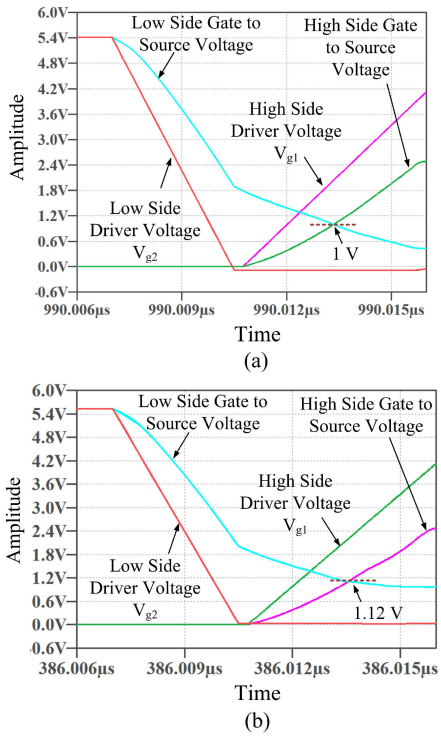


Fig. 18. Low-side and high-side gate driver and gate-to-source voltages when turn-ON dead time ($t_{\rm don}$) is selected based on [28]. (a) Load resistance $R = 1.35\,\Omega$. (b) Load resistance $R = 50\,\Omega$.

Fig. 19. Prototype of the GaN-based buck converter. Parameter set of this prototype is given in Table I. It is a prototype of the circuits shown in Figs. 6, 7, 9, and 10.

a TI DSC. The dead time obtained from the model refers to the dead time present at the PWM inputs of the gate driver. Thus, to validate the model, the dead time is generated in such a way that the effective dead time in the PWM inputs of the driver circuit matches with the dead time used in simulations and obtained from the analytical models. Fig. 20(a) shows the switch node voltage waveform when $t_{\rm don} = t_{\rm doff} = 100$ ns. The switch node voltage goes negative during both the dead time durations as the inductor current is always positive. Reverse conduction exists in the 2DEG channel between source and drain of the low-side GaN FET $S_{\rm L}$ during both the dead time durations. Fig. 20(b) shows that the reverse conduction ceases to zero during $t_{\rm don}$ duration when $t_{\rm don} = 16$ns is applied. A similar phenomenon of zero

TABLE V
EXPERIMENTAL EFFICIENCY COMPARISON AT $R = 1.35\,\Omega$

| $v_{\rm in}$ (V) | $f_{\rm s}$ (kHz) | Efficiency obtained using fixed dead time $t_{\rm don} = 50$ ns $t_{\rm doff} = 50$ns | Efficiency Obtained using Proposed technique |
|---|---|---|---|
| 40 | 500 | 93.283 | 95.188 |
| 30 | 500 | 91.979 | 95.815 |
| 40 | 400 | 92.685 | 95.841 |
| 30 | 400 | 91.614 | 96.156 |

reverse conduction during $t_{\rm doff}$ is also seen when $t_{\rm doff} = 16$ns is applied [see Fig. 20(c)]. Fig. 21 shows the effect of variation in $t_{\rm don}$ on efficiency. Turn ON dead time varies from 100 to 7 ns and turn OFF dead time $t_{\rm doff}$ is kept constant. It can be seen that the efficiency is maximum when the dead time reaches its optimum value of 16 ns obtained from the analytical model. A further reduction of $t_{\rm don}$ to 7 ns degrades the efficiency. Similarly, when $t_{\rm don}$ is fixed at 100 ns and $t_{\rm doff}$ is varied from 100 to 7 ns, the efficiency improves till the optimal dead time of 16 ns (see Fig. 22). A further reduction to 7 ns reduces the efficiency. Fig. 20(d) shows the switch node voltage waveform under light load condition when $t_{\rm don} = t_{\rm doff} = 100$ ns. Reverse conduction exists during both the dead time durations. Due to negative inductor current, high-side switch $S_{\rm H}$ shows reverse conduction during $t_{\rm don}$ through its 2DEG channel between source and drain. However, during $t_{\rm doff}$, the reverse conduction is enabled by the low-side switch $S_{\rm L}$. Fig. 20(e) shows the switch node voltage during turn ON dead time of 22 ns and turn-OFF dead time of 100 ns. No reverse conduction is seen during turn-ON dead time as the optimized turn ON dead time obtained from the model is applied. Similarly, when the optimized dead time $t_{\rm doff} = 19$ ns obtained from the model is applied, no reverse conduction can be seen during $t_{\rm doff}$ [see Fig. 20(f)]. Fig. 23 shows the effect of variation in $t_{\rm don}$ at $R = 50\,\Omega$ and $t_{\rm doff} = 100$ ns. $t_{\rm don}$ varies from 100 to 10 ns. The efficiency is maximum at the optimal turn ON dead time of 22 ns obtained from the model. Similarly, in Fig. 24, $t_{\rm don}$ is fixed at 100 ns and $t_{\rm doff}$ is varied from 100 to 10 ns. The efficiency is maximum at the optimal $t_{\rm doff} = 19$ ns obtained from the proposed analytical model.

Effectiveness of the optimal dead time obtained from the proposed analytical models is further validated under different input voltages and frequencies. Table V compares the efficiency achieved using fixed dead time and the optimal dead time obtained from the proposed technique under different frequencies and input voltages. The fixed dead time duration is chosen as $t_{\rm don} = t_{\rm doff} = 50$ns as the similar state-of-the-art 80 V MOSFETs (comparable with 100 V GaN FETs) typically use $44 \pm 16$ ns dead time for all load current conditions [36]. Thus, it would be interesting to see the effect of applying a similar dead time for GaN FETs. At $v_{\rm in} = 40$ V and $f_{\rm s} = 500$ kHz, the buck converter under fixed dead time can achieve an efficiency of 93.283%. Under the same operating condition, the optimal dead time improves the efficiency to 95.188%. Thus, the percentage of

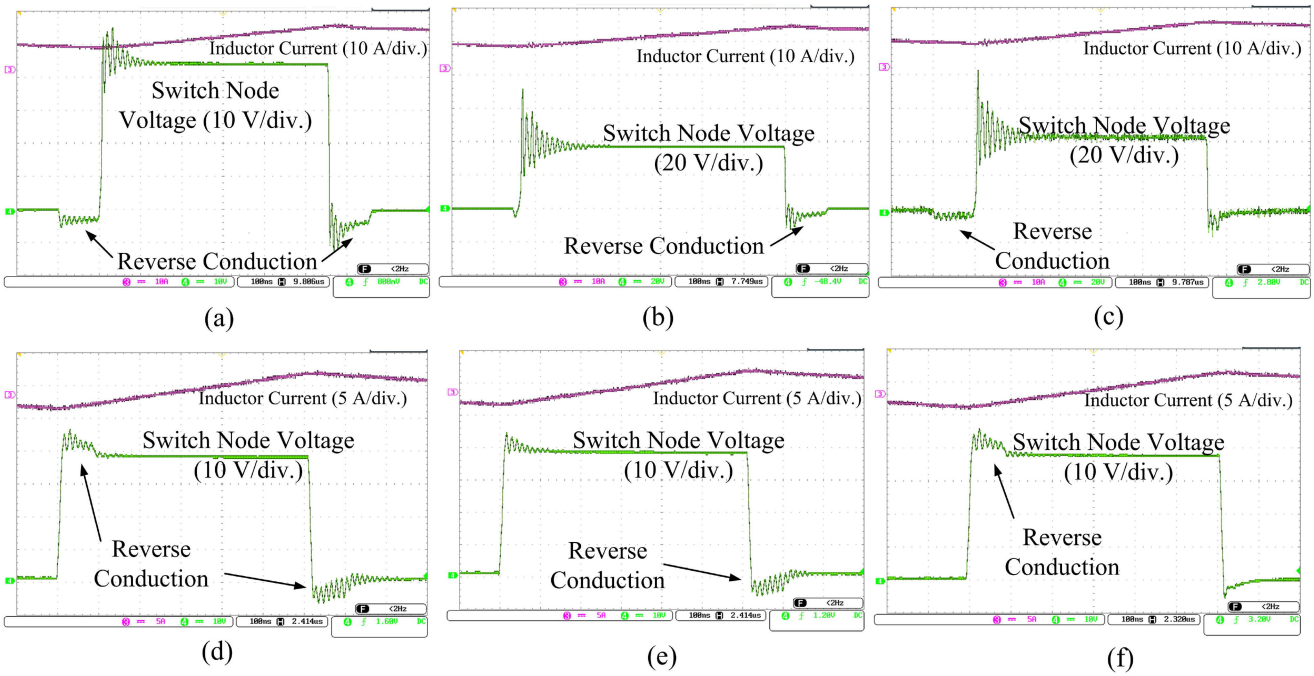


Fig. 20. (a) Switch node voltage at $R = 1.35\,\Omega$; $t_{\rm don} = 100$ ns, $t_{\rm doff} = 100$ ns; reverse conduction can be seen during $t_{\rm don}$ and $t_{\rm doff}$. (b) Switch node voltage at $R = 1.35\,\Omega$; $t_{\rm don} = 16$ ns, $t_{\rm doff} = 100$ ns; reverse conduction can be seen during $t_{\rm doff}$. (c) Switch node voltage at $R = 1.35\,\Omega$; $t_{\rm don} = 100$ ns, $t_{\rm doff} = 16$ ns; reverse conduction can be seen during $t_{\rm don}$. (d) Switch node voltage at $R = 50\,\Omega$; $t_{\rm don} = 100$ ns, $t_{\rm doff} = 100$ ns; reverse conduction can be seen during $t_{\rm don}$ and $t_{\rm doff}$. (e) Switch node voltage at $R = 50\,\Omega$; $t_{\rm don} = 22$ ns, $t_{\rm doff} = 100$ ns; reverse conduction can be seen during $t_{\rm doff}$. (f) Switch node voltage at $R = 50\,\Omega$; $t_{\rm don} = 100$ ns, $t_{\rm doff} = 19$ ns; reverse conduction can be seen during $t_{\rm don}$.

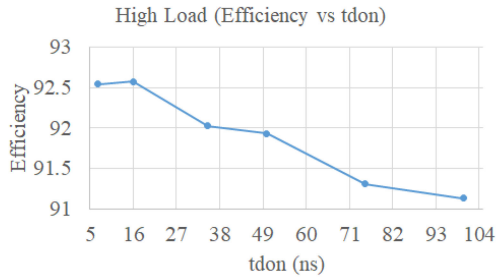


Fig. 21. Efficiency at $v_{\rm in} = 24V$, $f_{\rm s} = 500$ kHz, and $R = 1.35\,\Omega$ when $t_{\rm don}$ varies. $t_{\rm doff} = 100$ ns. Efficiency improves till the optimal $t_{\rm don} = 16$ ns. Efficiency degrades when $t_{\rm don}$ reduces to 7 ns.

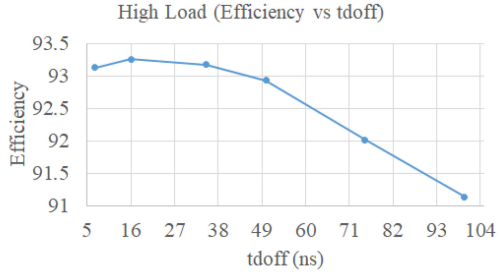


Fig. 22. Efficiency at $v_{\rm in} = 24\,{\rm V}$, $f_{\rm s} = 500$ kHz, and $R = 1.35\,\Omega$ when $t_{\rm doff}$ varies. $t_{\rm don} = 100$ ns. Efficiency improves till the optimal $t_{\rm doff} = 16$ ns. Efficiency degrades when $t_{\rm doff}$ reduces to 7 ns.

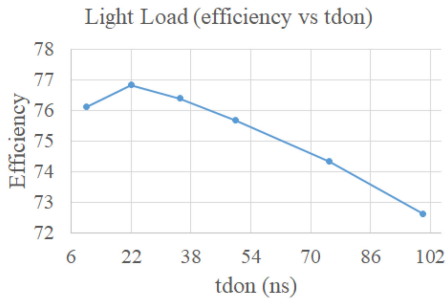


Fig. 23. Efficiency at $v_{\rm in} = 24V$, $f_{\rm s} = 500$ kHz, and $R = 50\,\Omega$ when $t_{\rm don}$ varies. $t_{\rm doff} = 100$ ns. Efficiency improves till the optimal $t_{\rm don} = 22$ ns. Efficiency degrades when $t_{\rm don}$ reduces to 10 ns.

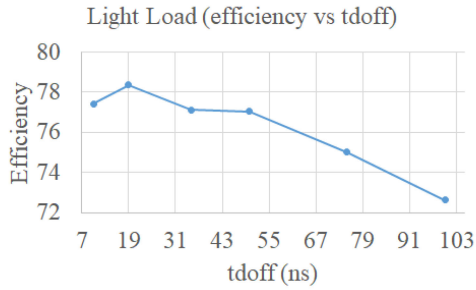


Fig. 24. Efficiency at $v_{\rm in} = 24V$, $f_{\rm s} = 500$ kHz, and $R = 50\,\Omega$ when $t_{\rm doff}$ varies. $t_{\rm don} = 100$ ns. Efficiency improves till the optimal $t_{\rm doff} = 19$ ns. Efficiency degrades when $t_{\rm doff}$ reduces to 10 ns.

improvement is 1.905. A similar improvement is also observed when the input voltage is kept at $v_{\rm in} = 30$ V. At $v_{\rm in} = 40$ V and $f_{\rm s} = 400$ kHz, the buck converter under fixed dead time can achieve an efficiency of 92.685%. Under the same operating condition, the optimal dead time improves the efficiency by 3.156%. At $v_{\rm in} = 30$ V and $f_{\rm s} = 400$ kHz, the optimal dead time improves the efficiency by 4.542%. In a similar manner,

TABLE VI
EXPERIMENTAL EFFICIENCY COMPARISON ($f_{\rm s} = 500$ kHz AND $v_{\rm in} = 40$ V)

| $R$ ($\Omega$) | Efficiency achieved using technique in [28] | Efficiency achieved using proposed technique |
|---|---|---|
| 1.35 | 94.557 | 95.188 |
| 50 | 74.152 | 80.884 |

the effectiveness of the proposed technique can also be demonstrated under light load conditions.

Performance of the proposed dead time optimization technique is further examined experimentally by comparing it with the method proposed in [28]. Efficiencies obtained using both these methods are given in Table VI. Comparison shows that the proposed method is more efficient in improving the efficiency under both heavy and light load conditions.

## V. CONCLUSION

This article proposes analytical models for dead time optimization in a GaN-based buck converter under different load conditions. The reverse capacitance and drain-to-source capacitance are nonlinear. To eliminate the nonlinearity effect, the proposed models have considered the gate charge. This makes the models simple and accurate compared with the conventional models available for Si-based converters. Accuracy of the models was checked using LTSpice simulation. An in-house buck converter prototype was built using GaN System's 100 V GaN device (GS61008P) for experimental validation. Experimental results showed close correlations with the results obtained from the proposed model. The proposed modeling techniques can be extended for other GaN-based dc–dc converters.

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