Comprehensive Optimization Modulation Scheme of Low Current Level and Wide ZVS Range for Dual Active Bridge Converter With Dead-Zone Control

Jia Li, Quanming Luo, *Member, IEEE*, Di Mou, *Student Member, IEEE*, Yuqi Wei, *Graduate Student Member, IEEE*, and Xinyue Zhang

***Abstract*—Due to the contradiction between low circuit current and wide zero-voltage switching (ZVS) range, for dual active bridge (DAB) converters, optimization schemes only aiming at minimum current will inherently induce a large switching loss. To extend the ZVS range while ensuring a low current level over the whole power range, this article proposes a comprehensive efficiency optimization scheme with triple-phase-shift in buck and boost modes of converters. Distinct from the previous modulation schemes, the proposed scheme is a multiobjective optimization based on the accurate ZVS constraints, and it is implemented in combined with the dead-zone control. To explore the accurate ZVS constraints, this article quantitatively analyzes the commutation process of switching devices in dead-band and comprehensively considers the influence of secondary-side voltage and parasitic capacitances. Based on this, a comprehensive optimization of current level and ZVS range is presented. And through the Lagrange multiplier method, a close-form global optimal solutions are obtained to realize the real-time control across a wide load and voltage ranges. Meanwhile, to further ensure a complete ZVS process and avoid the additional loss caused by reverse diode, the dead-zone control is also proposed to realize the dynamic adjustment of the dead time at different working conditions. Finally, a 1.5 kW laboratory prototype is built and the maximum measurement efficiency can reach 97.3% when $M = 0.8$ and 97.6% when $M = 1.2$, which verifies the feasibility and effectiveness of the proposed modulation scheme.**

***Index Terms*—Comprehensive efficiency optimization, dead-zone control, dual active bridge (DAB), peak current, triple-phase-shift (TPS), zero-voltage switching (ZVS) range.**

I. Introduction

THE dual active bridge (DAB) converter was first proposed in [1], and it is one of the commonly used topologies in bidirectional applications due to the advantages of bidirectional power flow capability, ease of zero-voltage switching (ZVS) without any additional elements, electrical isolation, and high power-density [2]. In recent years, the DAB converters are widely applied in various applications, such as electric vehicles, dc microgrids, solid-state transformers, and power electronic traction transformers, etc.

To improve the efficiency of the DAB converters, various advanced phase-shift modulation schemes have been introduced. As the most straightforward phase-shift modulation scheme, the single-phase shift (SPS) [1] has merely one degree of freedom to regulate the power flow. The average transmission power and the direction of power are controlled by the outer phase shift between the square waves generated by the H-bridges (HBs). Although the one-dimensional modulation is easy to be realized, converters modulated by SPS have poor steady-state characteristics. Based on this, the extended phase shift (EPS) was discussed in [3]–[5]. In addition to the outer phase shift, the inner phase shift of one of the HBs is introduced to improve the converter's performance. Different from EPS, the dual-phase shift (DPS) regulates the inner phase shifts of the two HBs with the same value [6]–[8]. Both EPS and DPS have merely two degrees of freedom, and the optimization effect is limited because of the unsatisfactory circulating current level and ZVS range. While for the triple-phase-shift (TPS) modulation scheme [9], the inner phase shifts of the two HBs and the outer phase shift are adjusted simultaneously to achieve the optimized operation of the converter. Since TPS has three degrees of freedom and it is more flexible, many optimal modulation schemes based on TPS have been extensively researched.

In [8], the loss-model based optimization scheme under TPS is proposed, which is the most straightforward way to achieve optimal efficiency for the DAB converter. However, it is complex and burdensome to establish an accurate loss-model [10]. And the scheme can only be carried out through offline look-up table. Based on this, most researchers prefer indirectly improving the system efficiency by minimizing the circulating current level. In [11], the fundamental duty modulation (FDM) scheme is proposed, which avoids the heavy computation burden of the time-domain analysis (TDA) and builds a unified mathematical model using frequency-domain analysis (FDA). However, the FDM lacks accuracy since only the fundamental component

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is considered in the optimization process. The efficiency at light load is not satisfactory since the current level is relatively high. To overcome the inaccurate performance analysis of FDA, a minimum-reactive-power strategy is developed in [12]. The scheme takes the sum of some series as an objective and obtains optimal operation points through the intelligent algorithm. Because of the difficulty in dealing with infinite series, the offline manner is still inevitable. As for the time-domain based optimization, a square wave superposition method in time-domain is introduced in [13], which decomposes the ac three-level voltages of HBs into a superposition of two two-level square waves. And a minimal rms current modulation scheme is addressed in [14]. Since it is the nonconvex optimization to select rms current as objective, a complicated global-optimal-condition equation is developed to solve the optimization problem in the nonconvex feasible region. In order to simplify calculation and optimization process, peak current is selected as the target in most TPS-based optimization schemes [9], [15]–[17] to achieve low conduction loss. For instance, in [15], a current-stress-optimized TPS modulation strategy (CSO-TPS) is discussed, and Lagrange multiplier method (LLM) is used to obtain optimal phase shift angles.

For these TPS-based optimization schemes, either the peak current or rms current is selected as the optimal objective, the circulating current level of the DAB converter can be reduced significantly, thus achieving minimum conduction loss and high system efficiency. Unfortunately, a major problem with these kinds of optimization scheme is that all of them are single-objective. That is to say, the optimal objective is simply to minimize the circulating current (such as rms current, peak current, or backflow power) without considering the ZVS operation of the converter. Specifically, in [9], [13], [15]–[17], in order to minimize the current level as low as possible, the instantaneous inductor current flowing through switches $S_3 - S_8$ at turn-ON instance is equal to zero, which will cause the six switches suffering from hard switching at light-load condition. According to the loss analysis result in [15] and [16], in addition to the conduction loss, the switching loss also accounts for a large proportion of the total loss, especially in the low power range. Therefore, under these optimization schemes, the system efficiency may not be the highest at light load.

To achieve a larger ZVS range, the ZVS control strategies under the buck and boost modes of the DAB converter are, respectively, proposed in [18] and [19]. Combined with the ZVS constraints, these strategies are derived by modifying the rms optimization results in [13]. However, it is only based on the direction of the current to determine whether the switching device can achieve soft switching. The minimum commutation current and the required dead time are not considered. In [20], a multiobjective optimization strategy of circuit current and ZVS range is presented. Although the scheme considers the commutation energy on the basis of [18] and [19], the influence of secondary-side voltage is neglected when calculating the commutation current to achieve ZVS. More importantly, in addition to the minimum current constraint, the setting of dead time also plays a vital role in ZVS operation. Excessive dead time will lead to lose of ZVS operation or even additional loss caused by the reverse recovery diode. While insufficient dead time will result in incomplete ZVS operation, even if the minimum communication current is met. Hence, in practical applications, it is always desirable to shorten the dead time under the premise of ensuring ZVS operation and avoiding the shoot-through phenomenon. However, in the control implement of [18]–[20], all of them do not consider the effect of the dead time.

To sum up, for these single-objective optimization strategies of DAB converters, it is difficult to make a tradeoff between the wide ZVS range and the minimum current level. Modulation schemes only simply aiming at minimum current are usually achieved at the expense of the ZVS range, thus resulting in a large switching loss. And for the multiobjective optimization without considering accurate current constraints, it is not an efficient multiobjective optimization because the realization of soft switching cannot be guaranteed.

In order to overcomes the above limitations and further improve the efficiency of the DAB converter, a comprehensive optimization method combining accurate ZVS constraints and dead-zone control is proposed in this article. And the major contributions of this article are listed as follows.

1) The commutation process of switching devices in deadband is analyzed quantitatively. And the accurate ZVS constraints are deduced through comprehensively considering the following factors: the direction of the current, the minimum communication current, the required dead time, and the influence of secondary-side voltage and parasitic capacitances.
2) This article proposes a comprehensive TPS-based efficiency optimization scheme for the DAB converter. A multiobjective optimization is presented to simultaneously achieve minimum current level and wide ZVS range. And a closed-form global optimal solutions in buck and boost modes of the DAB converter are obtained to realize the real-time control across a wide load and voltage ranges.
3) To further ensure a complete ZVS operation and avoid additional loss caused by antiparallel diode, the dead-zone control is proposed to achieve the dynamic adjustment of dead time under different working conditions. And this article combines optimization modulation and dead-zone control to jointly improve system efficiency.

This article is organized as follows. In Section II, the modulation principle and performance analysis of TPS are presented in detail. Section III analyzes the commutation process of switching devices at the same leg and obtains the accurate constraints for ZVS operation. In Section IV, a minimum-peak-current optimization scheme with all-ZVS operation is proposed and a set of the optimal modulation signals are obtained using LLM. Considering the highest efficiency over the whole operating range, Section V further discusses another improved optimization modulation strategy with near-all-ZVS operation. Based on this, in Section VI, the steady-state characteristics of proposed schemes are presented and compared with other related works

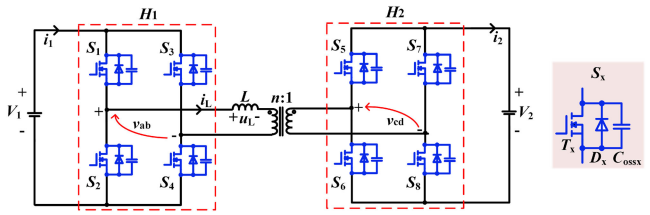


Fig. 1. Diagram of DAB dc–dc converter.

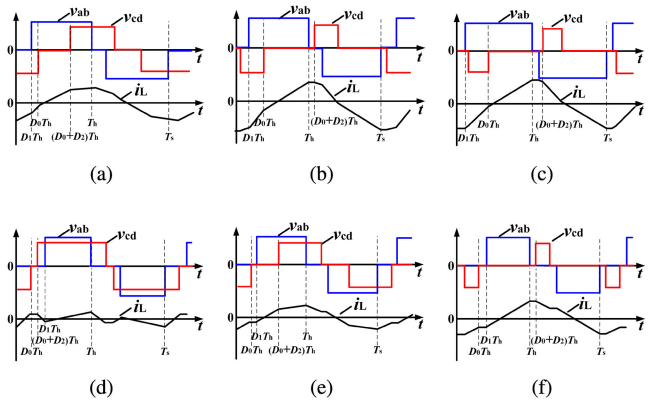


Fig. 2. Waveforms of DAB converter with TPS. (a) Mode 1. (b) Mode 2. (c) Mode 3 (d) Mode 4. (e) Mode 5. (f) Mode 6.

graphically. At last, in Section VII, a 1.5 kW laboratory prototype is built and a dead-zone control is introduced to achieve the dynamic adjustment of dead time under different working conditions. Based on this, the typical working waveforms, ZVS waveforms and dynamical dead-zone waveforms are measured to verifies the feasibility and effectiveness of the proposed modulation scheme.

II. Derivation and Analysis of the DAB Converter With TPS

The diagram of the DAB converter is shown in Fig. 1, where H_1 and H_2 are the primary and the secondary HBs; S_x is the semiconductor switching device composed of an active switch T_x, an antiparallel diode D_x and a parasitic capacitance C_{ossx}; L is the sum of the transformer leakage inductor and auxiliary inductor; n is the primary-to-secondary turns ratio of transformer. v_{ab} and v_{cd} are the high-frequency ac output voltages of bridges H_1 and H_2. u_L and i_L are the voltage and current of inductor L, respectively. The reference directions of the voltages and currents are also shown in Fig. 1.

The main waveforms of the DAB converter with TPS are shown in Fig. 2. D_1 denotes the inner phase-shift ratio between S_1 and S_4; D_2 denotes the inner phase-shift ratio between S_5 and S_8, and D_0 denotes the outer phase-shift ratio between S_1 and S_5. According to the values of the modulation variables D_0, D_1, and D_2, it can be divided into the following six working modes: Mode 1 ($0 < D_1 < D_0 < 1 \wedge D_1 < D_0 + D_2 < 1$); Mode 2 ($0 < D_1 < D_0 < 1 \wedge 1 < D_0 + D_2 < 1 + D_1$); Mode 3 ($0 < D_1 < D_0 < 1 \wedge 1 + D_1 < D_0 + D_2 < 2$); Mode 4 ($0 < D_0 < D_1 < 1 \wedge 0 < D_0 + D_2 < D_1$); Mode 5 ($0 < D_0 < D_1 < 1 \wedge D_1 < D_0 + D_2 < 1$); Mode 6 ($0 < D_0 < D_1 < 1 \wedge 1 < D_0 + D_2 < 1 + D_1$). As shown in Fig. 2, for Mode 2, 3, and 6, since there are no time intervals that satisfy the expression $v_{ab}v_{cd} > 0$, the power is stored in the inductor L and cannot be transferred directly from bridge H_1 to bridge H_2, which will cause additional losses and increase the circulating current level. Also, for the Mode 5, there are at least two switches losing ZVS operation. Because the instantaneous currents of S_5 and S_4 at turned-ON instant are equal. However, for the switches S_5 and S_4 to achieve ZVS, the directional conditions of the current should be $i_L > 0$ and $i_L < 0$, respectively. Therefore, only Mode 1 and Mode 4 are further discussed for the DAB converters in this article.

TABLE I
Instantaneous Value of Inductance Current i_L

Mode 1	$I_L(0) = I_{L\_S_1} = \frac{V_1}{4Lf_s}[(D_1-1) - M(2D_0+D_2-1)]$ $I_L(D_1T_h) = I_{L\_S_4} = \frac{V_1}{4Lf_s}[(D_1-1) - M(-2D_1+2D_0+D_2-1)]$ $I_L(D_0T_h) = I_{L\_S_5} = \frac{V_1}{4Lf_s}[(2D_0-D_1-1) - M(D_2-1)]$ $I_L(D_0T_h+D_2T_h) = I_{L\_S_8} = \frac{V_1}{4Lf_s}[(-D_1+2D_0+2D_2-1) - M(D_2-1)]$
Mode 4	$I_L(0) = I_{L\_S_1} = \frac{V_1}{4Lf_s}[(D_1-1) - M(2D_0+D_2-1)]$ $I_L(D_0T_h) = I_{L\_S_5} = \frac{V_1}{4Lf_s}[(D_1-1) - M(D_2-1)]$ $I_L(D_0T_h+D_2T_h) = I_{L\_S_8} = \frac{V_1}{4Lf_s}[(D_1-1) - M(D_2-1)]$ $I_L(D_1T_h) = I_{L\_S_4} = \frac{V_1}{4Lf_s}[(D_1-1) - M(2D_1-2D_0-D_2-1)]$

In order to explore the steady-state characteristics of the DAB converter and prepare for the efficiency optimization, it is necessary to conduct the performance analysis for Mode 1 and Mode 4. According to the square wave superposition method in time-domain [13], the instantaneous value of inductance current i_L can be obtained in Table I, where $I_{L\_S_x}$ denotes the instantaneous inductor current flowing through S_x at turn-ON instance; f_s denotes switching frequency; M denotes the voltage conversion ratio which is defined as $M = nV_2/V_1$. According to Table I, the average transferred power in Mode 1 is calculated as

$$P = \frac{\int_0^{T_s} V_1 i_1(t)dt}{T_s P_N} = 2D_2(1-D_2) - 2D_1(D_1-D_2) - 4D_0(D_0-D_1+D_2-1) \quad (1)$$

where T_s is the switching period, and P_N is the maximum transmission power, i.e.,

$$P_N = \frac{NV_2V_1}{8Lf_s}. \quad (2)$$

The average transferred power in Mode 4 can also be described as

$$P = -2[-2D_0 + D_1 + 2D_0D_1 - D_1^2 - D_2 + D_2D_1]. \quad (3)$$

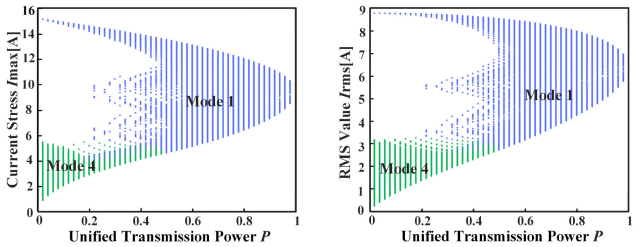


Fig. 3. All the $I_{\rm rms}$ and $I_{\rm max}$ values at $M = 0.6$. (a) $I_{\rm max}$-P. (b) $I_{\rm rms}$-P.

The rms current and peak current of the inductor current in Mode 1 and Mode 4 are the same, which are derived as

$$I_{\rm max} = \frac{V_1}{4Lf_{\rm s}}[(1-D_1) - M(1-D_2-2D_0)] \tag{4}$$

$$I_{\rm rms} = \sqrt{\frac{1}{T_{\rm s}}\int_0^{T_{\rm s}} i_{\rm L}(t)^2 {\rm d}t}$$

$$= \sqrt{\frac{V_1^2}{64f_{\rm s}^2L^2}\left[\begin{array}{l}(2-6D_1^2+4D_1^3)(1+M^2) - M\cdot \\ \left[\begin{array}{l}(1-6D_0^2+4D_0^3) \\ +(1-6(D_0+D_2)^2 \\ +4(D_0+D_2)^3) \\ +(1-6(D_0-D_1)^2 \\ +4|D_0-D_1|^3) \\ +(1-6(D_1-D_0-D_2)^2 \\ +4|D_1-D_0-D_2|^3)\end{array}\right]\end{array}\right]}. \tag{5}$$

For the triple-variable modulation scheme, to transport a required power P, there are infinite combinations of (D_1, D_2, D_3) with different system performances (such as current level and ZVS range). Here, according to (1)–(5), Fig. 3 illustrates all the $I_{\rm rms}$ and $I_{\rm max}$ values for a given transferred power P at M =0.6, where the green and blue dotted-region, respectively, represent Mode 4 and Mode 1. As shown in Fig. 3, the normalized transferred power range in Mode 1 can reach the maximum transmission power, but Mode 1 has a higher current level at light load. Although Mode 4 has a narrow power range, it tends to achieve a lower current level. Therefore, both Mode 4 and Mode 1 should be analyzed in the subsequent analysis and efficiency optimization.

III. Accurate Conditions for ZVS Operation

As the switching frequency increases, the ZVS range becomes one of the most important factors to affect the efficiency of the DAB converter. Most of the papers only make an approximate judgment based on the current direction when judging whether switches can operate in ZVS. Whereas for a proper ZVS operation, the resonance between the parasitic capacitance of switching devices and the inductance need to be considered, and the energy stored in the parasitic capacitance cannot be ignored as well. In this section, the accurate quantitative conditions for ZVS operation have been derived by analyzing the commutation process of two switches at the same bridge arm. To simplify

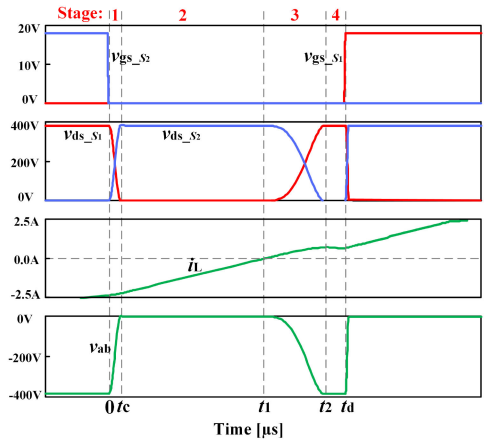


Fig. 4. Commutation process of switches S_1 and S_2 in dead-band.

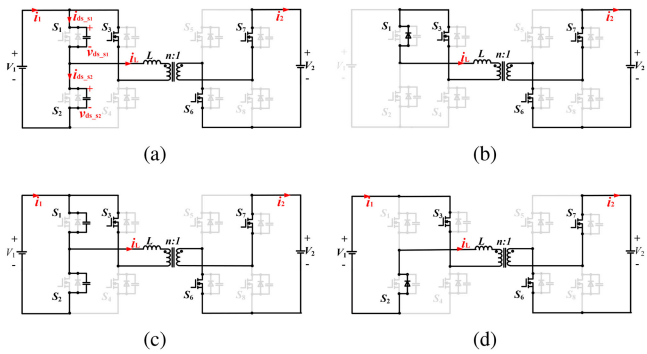


Fig. 5. Equivalent circuits. (a) Satge 1. (c) Satge 2. (d) Satge 3. (e) Satge 4.

the analysis, some assumptions are made as follows: 1) The parasitic capacitance of each switching device equals to $C_{\rm oss}$; 2) In the dead time interval, the turn-OFFand turn-ON delay time of switches are ignored.

A. Analysis of the Commutation Process in Dead-Band

Here, taking the commutation process from S_1 to S_2 in Mode 4 for example. And the process of switching devices S_1 and S_2 in dead-band is simulated by LTSPICE in Fig. 4, where $v_{\rm gs\_}S_1$ and $v_{\rm gs\_}S_2$ are the gate-source voltages of S_1 and S_2, $v_{\rm ds\_}S_1$ and $v_{\rm ds\_}S_2$ are the drain–source voltages of S_1 and S_2, $i_{\rm L}$ is the inductor current, and $v_{\rm ab}$ is the primary output voltage. Notice in Fig. 4 that a long dead time is set to fully display the commutation process. As observed, it is divided into four stages and the corresponding equivalent circuits are shown in Fig. 5.

Before $t = 0$, switches S_2, S_3, S_6, and S_7 are conducting and $i_{\rm L} < 0$. At $t = 0$, S_2 is turned OFF, and $v_{\rm ds\_}S_2 = 0$, $v_{\rm ds\_}S_1 = V_1$, $i_L < 0$. Then, S_1 and S_2 enter the following commutation process:

1) Stage 1 [see Fig. 5(a)]: S_3, S_6, and S_7 are ON, S_1, S_2, S_4, S_5, and S_8 are OFF. Inductor L resonates with $C_{\rm oss\_}S_1$ and $C_{\rm oss\_}S_2$ to complete the process of discharging $C_{\rm oss\_}S_1$ and charging $C_{\rm oss\_}S_2$. The stage ends up when the voltage $v_{\rm ds\_}S_1$ decreases to 0 and $v_{\rm ds\_}S_2$ increases to V_1 at $t = t_{\rm c}$.

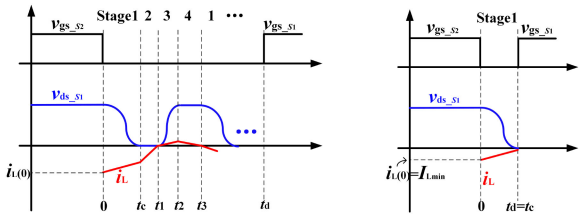


Fig. 6. (a) Waveforms of $v_{\mathrm{ds\_}S_1}$ and i_{L}. (b) ideal working case.

2) Stage 2 [see Fig. 5(b)]: S_3, S_6, and S_7 and the antiparallel diode of S_1 are ON, S_2, S_4, S_5, and S_8 are OFF. The inductor voltage v_{L} is clamped at nV_2, and i_{L} increases gradually. The stage ends up with i_{L} increasing to 0 at $t = t_1$. If S_1 is not gated on during this stage, the following stages will occur.
3) Stage 3 [see Fig. 5(c)]: S_3, S_6, and S_7 are ON, S_1, S_2, S_4, S_5, and S_8 are OFF. The resonance occurs between L, $C_{\mathrm{oss\_}S_1}$, and $C_{\mathrm{oss\_}S_2}$ to complete the process of charging $C_{\mathrm{oss\_}S_1}$ and discharging $C_{\mathrm{oss\_}S_2}$. The stage ends up with $v_{\mathrm{ds\_}S_2}$ decreasing to 0 and $v_{\mathrm{ds\_}S_1}$ increasing to V_1 at $t = t_2$.
4) Stage 4 [see Fig. 5(d)]: S_3, S_6, and S_7 and the antiparallel diode of S_2 are ON, S_1, S_4, S_5, and S_8 are OFF. The inductor voltage v_{L} is clamped at $nV_2 - V_1$ and i_{L} starts to decrease. The stage ends up when i_{L} decreases to 0.

If the dead time is long enough and the circuit loss is not considered, the commutation process will repeat as stage 1-2-3-4-1-2-3-4 during the dead time interval, as shown in Fig. 6(a). Apparently, an inappropriate dead time will result in voltage polarity reversal or voltage sag phenomena, further changing the switching characteristics and transmission power characteristics [21]. Meanwhile, additional loss and even the loss of ZVS operation will be caused due to excessive dead time. Hence, in practical applications, it is always desirable to shorten the dead time under the premise of ensuring ZVS operation and avoiding the shoot-through phenomenon.

B. Solution of the Accurate Conditions for ZVS Operation

According to the previous analysis, the following three qualitative conditions should be satisfied to realize a proper ZVS operation at the turn-ON instant of S_1 (at $t = 0$):

1) The direction of i_{L}: at $t = 0$, $i_L(0) < 0$. Only when the direction of i_L is correct, the charging process will begin and the voltage $v_{\mathrm{ds\_}S_1}$ will start to drop.
2) The critical current I_{Lmin}: at $t = 0$, $|i_L(0)| > |I_{\mathrm{Lmin}}|$, where I_{Lmin} is the minimum commutation current for ZVS. In the commutation process, I_{Lmin} is required to provide enough charge to complete the charge–discharge process in Stage 1. It ensures the charge in the parasitic capacitor $C_{\mathrm{oss\_}S_1}$ is completely carried away, thus the voltage $v_{\mathrm{ds\_}S_1}$ can decrease to 0.
3) The dead time t_{d}: $t_{\mathrm{c}} < t_{\mathrm{d}} < t_1$, where t_{c} denotes the duration of the charge–discharge process of Stage 1. The reasonable dead time t_{d} should be slightly larger than t_{c}, which ensures the switch S_1 could be turned ON at Stage 2.

As observed, to solve the quantitative conditions for ZVS operation, the critical current I_{Lmin} and the commutation time t_{c} of Stage 1 is required. To obtain the critical value I_{Lmin}, a limiting case shown in Fig. 6(b) is analyzed, that is, the inductor current is required to be $i_{\mathrm{L}}(t_{\mathrm{c}}) = 0$ when Stage 1 is completed. According to Fig. 5(a), the circuit equations can be written as

$$\begin{cases} i_{\mathrm{L}}(t) = C_{\mathrm{oss}}\dfrac{\mathrm{d}v_{\mathrm{ds\_}S_1}(t)}{\mathrm{d}t} - C_{\mathrm{oss}}\dfrac{\mathrm{d}v_{\mathrm{ds\_}S_2}(t)}{\mathrm{d}t} \\ v_{\mathrm{ds\_}S_1}(t) = V_1 - v_{\mathrm{ds\_}S_2}(t) \\ V_1 + L\dfrac{\mathrm{d}i_{\mathrm{L}}(t)}{\mathrm{d}t} - v_{\mathrm{ds\_}S_2}(t) - nV_2 = 0. \end{cases} \tag{6}$$

The initial conditions are $i_{\mathrm{L}}(0) = I_{\mathrm{L\_}S_1}$ and $v_{\mathrm{ds\_}S_1}(0) = V_1$. And the expression of the current i_{L} and the voltage $v_{\mathrm{ds\_}S_1}$ in Stage 1 can be derived as

$$\begin{cases} i_{\mathrm{L}}(t) = I_{\mathrm{L\_}S_1} \cdot \cos\omega t - \dfrac{nV_2 - V_1}{L\omega} \cdot \sin\omega t \\ v_{\mathrm{ds\_}S_1}(t) = L\omega \cdot I_{\mathrm{L\_}S_1} \cdot \sin\omega t - (nV_2 - V_1) \cdot \cos\omega t + nV_2 \\ \quad = \sqrt{(L\omega \cdot I_{\mathrm{L\_}S_1})^2 + (nV_2 - V_1)^2}\sin(\omega t + \alpha) + nV_2 \end{cases} \tag{7}$$

where

$$\omega = \frac{1}{\sqrt{2C_{\mathrm{oss}}L}}; \qquad \tan\alpha = -\frac{nV_2 - V_1}{L\omega \cdot I_{\mathrm{L\_}S_1}}. \tag{8}$$

In order to ensure that the voltage $v_{\mathrm{ds\_}S_1}$ can resonant to 0 in Stage 1, the condition in (9) must be satisfied

$$\sqrt{(L\omega \cdot I_{\mathrm{L\_}S_1})^2 + (nV_2 - V_1)^2} \geq nV_2. \tag{9}$$

According to (9) and the direction condition of i_{L}, the critical current $I_{\mathrm{Lmin\_}S_1}$ of S_1 can be deduced as

$$I_{\mathrm{Lmin\_}S_1} = \begin{cases} -\sqrt{\dfrac{2C_{\mathrm{oss}}V_1^2(2M-1)}{L}} & (1/2 < M < 1) \\ 0 & (0 < M < 1/2). \end{cases} \tag{10}$$

Moreover, under the condition of $v_{\mathrm{ds\_}S_1} = 0$, the duration $t_{\mathrm{c\_}S_1}$ of Stage 1 can be written as

$$t_{\mathrm{c\_}S_1} = \frac{1}{\omega}\left[\arctan\left(\frac{nV_2 - V_1}{L\omega I_{\mathrm{L\_}S_1}}\right) + \arcsin\left(\frac{nV_2}{\sqrt{(L\omega I_{\mathrm{L\_}S_1})^2 + (nV_2 - V_1)^2}}\right)\right]. \tag{11}$$

Similarly, the duration t_{c} and current conditions of all the switches in Mode 4 and Mode 1 could be derived in Table II, where C_{p} and C_{s} denote the patristic capacitances C_{oss} of primary and secondary switches, respectively. Since the conduction of the upper and lower switches at the same bridge arm is complementary, only S_1, S_4, S_5, and S_8 are presented here.

C. Explication of the Minimum Current Conditions

As shown in Fig. 7, it draws the curves of current i_{L} and voltage $v_{\mathrm{ds\_}S_1}$ during the commutation process of S_1 and S_2 in Stage 1, according to (7). The red and blue lines represent the current and voltage curves, respectively. Theoretically, in Stage 1, the sum of energy stored in the parasitic capacitances does not change, although there is a process of discharging $C_{\mathrm{oss\_}S_1}$

TABLE II
DURATION T_c OF STAGE 1 AND CURRENT CONDITIONS

Mode 4	
Current condition	$I_{\text{L\_}S_1} < I_{\text{Lmin\_}S_1} = \begin{cases} 0 & (0 < M < 1/2) \\ -\sqrt{\frac{2C_pV_1^2(2M-1)}{L}} & (1/2 < M < 1) \end{cases}$ $I_{\text{L\_}S_4} < I_{\text{Lmin\_}S_4} = \begin{cases} -\sqrt{\frac{2C_pV_1^2(1-2M)}{L}} & (0 < M < 1/2) \\ 0 & (1/2 < M < 1) \end{cases}$ $I_{\text{L\_}S_5} > I_{\text{Lmin\_}S_5} = 0$ $I_{\text{L\_}S_8} > I_{\text{Lmin\_}S_8} = \sqrt{\frac{2C_sV_2^2}{L}}$
Duration of Stage 1 t_c	$t_{c\_S_1} = \frac{1}{\omega}\left[\arctan\left(\frac{nV_2 - V_1}{L\omega \cdot I_{\text{L\_}S_1}}\right) + \arcsin\left(\frac{nV_2}{\sqrt{(L\omega \cdot I_{\text{L\_}S_1})^2 + (nV_2 - V_1)^2}}\right)\right]$ $t_{c\_S_4} = -\frac{1}{\omega}\left[\arctan\left(\frac{nV_2}{L\omega \cdot I_{\text{L\_}S_4}}\right) + \arcsin\left(\frac{nV_2 - V_1}{\sqrt{(L\omega \cdot I_{\text{L\_}S_4})^2 + nV_2^2}}\right)\right]$ $t_{c\_S_5} = \frac{1}{n\omega}\arctan\left(\frac{V_2}{L\omega \cdot I_{\text{L\_}S_5}}\right)$ $t_{c\_S_8} = \frac{1}{n\omega}\arcsin\left(\frac{V_2}{L\omega \cdot I_{\text{L\_}S_8}}\right)$
Mode 1	
Current condition	$I_{\text{L\_}S_1} < I_{\text{Lmin\_}S_1} = \begin{cases} 0 & (0 < M < 1/2) \\ -\sqrt{\frac{2C_pV_1^2(2M-1)}{L}} & (1/2 < M < 1) \end{cases}$ $I_{\text{L\_}S_4} < I_{\text{Lmin\_}S_4} = -\sqrt{\frac{2C_pV_1^2(1+2M)}{L}}$ $I_{\text{L\_}S_5} > I_{\text{Lmin\_}S_5} = 0$ $I_{\text{L\_}S_8} > I_{\text{Lmin\_}S_8} = 0$
Duration of Stage 1 t_c	$t_{c\_S_1} = \frac{1}{\omega}\left[\arctan\left(\frac{nV_2 - V_1}{L\omega \cdot I_{\text{L\_}S_1}}\right) + \arcsin\left(\frac{nV_2}{\sqrt{(L\omega \cdot I_{\text{L\_}S_1})^2 + (nV_2 - V_1)^2}}\right)\right]$ $t_{c\_S_4} = \frac{1}{\omega}\left[\arctan\left(\frac{nV_2}{L\omega \cdot I_{\text{L\_}S_4}}\right) + \arcsin\left(\frac{V_1 + nV_2}{\sqrt{(L\omega \cdot I_{\text{L\_}S_4})^2 + (nV_2)^2}}\right)\right]$ $t_{c\_S_5} = \frac{1}{n\omega}\left[\arcsin\left(\frac{-V_1}{n\sqrt{(L\omega \cdot I_{\text{L\_}S_5})^2 + (V_2 + V_1/n)^2}}\right) + \arctan\left(\frac{V_2 + V_1/n}{L\omega \cdot I_{\text{L\_}S_5}}\right)\right]$ $t_{c\_S_8} = \frac{1}{n\omega}\left[\arcsin\left(\frac{V_2 - V_1/n}{n\sqrt{(L\omega \cdot I_{\text{L\_}S_8})^2 + (V_1/n)^2}}\right) + \arctan\left(\frac{V_1/n}{L\omega \cdot I_{\text{L\_}S_8}}\right)\right]$

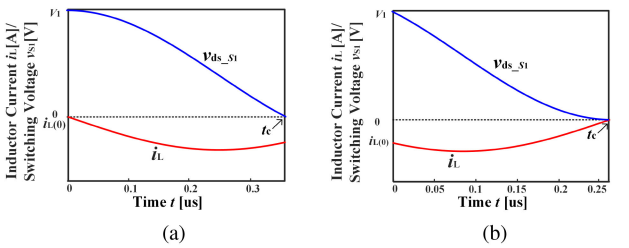


Fig. 7. Curves of inductance current i_{L} and voltage $v_{\text{ds\_}S_1}$. (a) $0 < M < 1/2$. (b) $1/2 < M < 1$.

and charging $C_{\text{oss\_}S_2}$. Hence, the energy E_{d} transferred from the input side to the output side during Stage 1 is expressed as

$$E_{\text{d}} = \int_0^{t_{\text{c}}} V_1 i_1(t)dt - \int_0^{t_{\text{c}}} V_2 i_2(t)dt = C_{\text{oss}} V_1^2 (1 - 2M). \tag{12}$$

According to (12), when $M < 1/2$, the energy $E_{\text{d}} > 0$. It means the energy provided by the input side is more than the energy required by the output side, the energy difference is stored in the inductance, and the absolute value of i_{L} increases, which is consistent with Fig. 7(a). Consequently, as demonstrated in (10), there is no minimum current limitation. As long as the direction of i_{L} at the turned-ON instant is satisfied, S_1 can be switched ON with ZVS. In addition, when $M > 1/2$, the energy $E_{\text{d}} < 0$. That is, the energy provided by the input side is less than the energy required at the output side, the energy difference is provided by the inductance in the commutation process, and the absolute value of i_{L} decreases, which is consistent with the curve of i_{L} in Fig. 7(b). Therefore, as demonstrated in (10), a minimum commutation current I_{Lmin} is required to complete the Stage 1. In addition, it is worth noting that to obtain the critical value I_{Lmin}, Fig. 7(b) illustrates a limiting case, where the current i_{L} decreases to 0 when $v_{\text{ds\_}S_1}$ drops to 0. But in practice, some margin is needed to ensure a complete ZVS operation.

IV. MINIMUM-PEAK-CURRENT MODULATION SCHEME WITH ALL-ZVS OPERATION

A. Optimization Modulation Scheme

In order to improve the system efficiency by reducing switching loss and conduction loss simultaneously, this article proposes an ALL-ZVS optimization modulation scheme based on TPS. Under the primes that all the switching devices achieve ZVS operation over the whole power range, the converter modulated by the proposed ALL-ZVS can obtain a low peak current level. Specifically, the optimization problem of the ALL-ZVS is formulated into the standard form as

$$\begin{aligned} &min\ I_{\max} = \frac{V_1}{4Lf_{\text{s}}}[(1 - D_1) - M(1 - D_2 - 2D_0)] \\ &st.\quad Power\ \ constraint \\ &\qquad Critical\ \ current\ \ constraint \\ &\qquad Mode\ \ constraint. \end{aligned}$$

It is described as finding the extremum of the peak-current function limited by some equality or inequality constraints to obtain an optimal operating point (D_1, D_2, D_3). The constraints include power constraints, mode constraints, and critical current constraints for ZVS operation, listed in Table III. As observed, the optimization problem is divided into the three cases ($1/2 < M < 1$ in Mode 4, $0 < M < 1/2$ in Mode 4, and $0 < M < 1$ in Mode 1). Here, taking $1/2 < M < 1$ in Mode 4 as an example to solve the optimal solution. According to Table III, the optimization problem is formulated into the standard form as

$$\begin{aligned} &min\quad I_{\max} = \frac{V_1}{4Lf_{\text{s}}}[(1 - D_1) - M(1 - D_2 - 2D_0)] \\ &st. \\ &P + 2[-2D_0 + D_1 + 2D_0D_1 - D_1^2 - D_2 + D_2D_1] = 0 \\ &\frac{V_1}{4Lf_{\text{s}}}[(D_1 - 1) - M(2D_1 - 2D_0 - D_2 - 1)] + I_{\text{m}} \le 0 \\ &\frac{V_1}{4Lf_{\text{s}}}[(D_1 - 1) - M(D_2 + 2D_0 - 1)] + \sqrt{\frac{2C_pV_1^2(2M-1)}{L}} \le 0 \\ &-D_0 \le 0 \\ &D_0 - D_1 \le 0 \\ &D_1 - 1 \le 0 \\ &-D_0 - D_2 \le 0 \\ &D_0 + D_2 - D_1 \le 0. \end{aligned} \tag{13}$$

Noted that, according to the current constraint in Table II, when $1/2 < M < 1$ in Mode4, as long as the current $I_{\text{L\_}S_4}$ is less than 0, S_4 can realize ZVS operation. But in order to ensure some

TABLE III
CONSTRAINTS OF THE ALL-ZVS OPTIMIZATION SCHEME

Mode 4	
Power constraint	$P+2[-2D_0+D_1+2D_0D_1-D_1^2-D_2+D_2D_1]=0$
Mode constraint	$-D_0\le 0; D_0-D_1\le 0; D_1-1\le 0$ $-D_0-D_2\le 0; D_0+D_2-D_1\le 0$
Critical current constraint	when $0<M<1/2$: $\begin{cases}\frac{V_1}{4Lf_s}[(D_1-1)-M(2D_0+D_2-1)]\le 0\\ \sqrt{\frac{2C_sV_2^2}{L}}-\frac{V_1}{4Lf_s}[(D_1-1)-M(D_2-1)]\le 0\\ \frac{V_1}{4Lf_s}[(D_1-1)-M(2D_1-2D_0-D_2-1)]+\sqrt{\frac{2C_pV_1^2(1-2M)}{L}}\le 0\end{cases}$ when $1/2<M<1$: $\begin{cases}\frac{V_1}{4Lf_s}[(D_1-1)-M(2D_0+D_2-1)]+\sqrt{\frac{2C_pV_1^2(2M-1)}{L}}\le 0\\ \sqrt{\frac{2C_sV_2^2}{L}}-\frac{V_1}{4Lf_s}[(D_1-1)-M(D_2-1)]\le 0\\ \frac{V_1}{4Lf_s}[(D_1-1)-M(2D_1-2D_0-D_2-1)]+I_m\le 0\end{cases}$
Mode 1	
Power constraint	$P+[2D_0(D_0-1-D_1+D_2)+D_1(D_1-D_2)+D_2(D_2-1)]=0$
Mode constraint	$-D_1\le 0; D_1-D_0\le 0; D_0-1\le 0$ $D_1-D_0-D_2\le 0; D_0+D_2-1\le 0$
Critical current constraint	$\begin{cases}\frac{V_1}{4Lf_s}[(D_1-1)-M(-2D_1+2D_0+D_2-1)]+\sqrt{\frac{2C_pV_1^2(1+2M)}{L}}\le 0\\ -\frac{V_1}{4Lf_s}[(2D_0-D_1-1)-M(D_2-1)]\le 0\end{cases}$

margin, the current I_m ($I_m>0$) is introduced in the critical current constraint, shown in (13).

Using the LLM and Karush–Kuhn–Tucker (KKT) conditions [17], the optimized analytical expression of modulation variables D_1, D_2, and D_0 can be calculated as

$$\begin{cases} D_1=1-\dfrac{2\sqrt{2}f_sI_mL-\sqrt{8f_s^2I_m^2L^2-PV_1nV_2(M-1)}}{\sqrt{2}V_1(1-M)} \\ D_0=\dfrac{\sqrt{8f_s^2I_s^2L^2-PV_1nV_2(M-1)}+\sqrt{16f_s^2LC_s^2}}{\sqrt{2}nV_2} \\ D_2=D_1-\dfrac{\left[\begin{matrix}2\sqrt{8f_s^2Imm^2L^2-PV_1nV_2(M-1)}\\ +(1-M)\sqrt{64f_s^2LC_s^2}\end{matrix}\right]}{\sqrt{2}nV_2(1-M)} \end{cases}. \tag{14}$$

And this optimization solution only applies to the power range $0<P<P_{x1}$, where P_{x1} is

$$P_{x1}=-\frac{\left[\begin{matrix}\sqrt{2}V_2(M-1)+2\sqrt{2}f_sI_mL\\ -8(M-1)\sqrt{C_sf_s^2LV_2^2}\end{matrix}\right]^2-8f_s^2I_m^2L^2}{nV_1V_2(M-1)}. \tag{15}$$

In the same way, the optimization solutions of the other two conditions can also be derived. The results are shown in Table A.I in Appendix A.

B. Verification of Correctness of the Optimization Solution

Similar to Fig. 3, under the premise that the critical current constraints in Table III are satisfied (that is, when DAB is in all-ZVS operation), all the I_{max} and I_{rms} values for a given transmission power P are illustrated in Fig. 8. The green and blue dotted-region, respectively, represent Mode 4 and Mode 1. The red dotted lines are the optimal curves of I_{max} and I_{rms} drawn by the optimized solution in Table A.I. From Fig. 8(a), the peak-current optimal curve is at the bottom of the dotted-region, which intuitively proves the proposed ALL-ZVS scheme can effectively find the optimal working point (D_1, D_2, D_0).

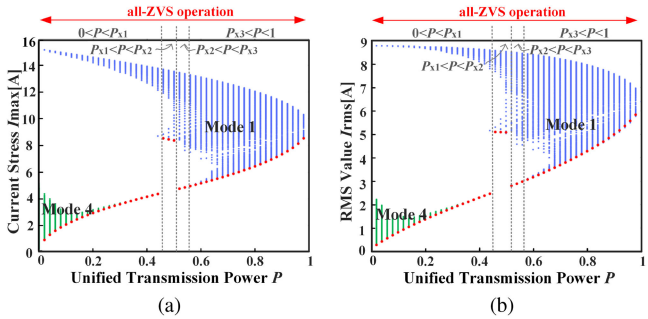


Fig. 8. Optimal curves with the proposed ALL-ZVS and all the possible values of I_{rms} and I_{max} at $M=0.6$. (a) I_{max}-P. (b) I_{rms}-P.

In addition, it can be observed in Fig. 8(b) that the I_{rms} curve drawn by the proposed ALL-ZVS almost overlaps the smallest rms current level, even though the optimal objective is I_{max} rather than I_{rms}. It is demonstrated that the minimum I_{max} and the minimum I_{rms} varied with the operating condition (M, P) are basically consistent with each other, except for some subtle differences at heavy load. Therefore, either the peak current or rms current can be selected as the optimization objective, they have a similar effect on reducing the current level. Moreover, compared with the I_{rms}, the expression of I_{max} is simpler, the corresponding optimization process and optimized expression will be greatly simplified, making it easier to implement. However, with I_{rms} as optimal objective, since the rms minimal optimization problem is nonconvex, the LMM is no longer effective to obtain the analytical optimal solutions. Hence, although the influence of the rms current on conduction loss is more direct than that of the peak current, it is reasonable to take I_{max} as the optimization objective.

V. MINIMUM-PEAK-CURRENT MODULATION SCHEME WITH NEAR-ALL-ZVS OPERATION

A. Optimization Modulation Scheme

As can be seen from Fig. 8, the proposed ALL-ZVS modulation scheme can achieve ZVS operation down to no-load and obtain a low peak current level simultaneously. However, in the power range $P_{x1}<P<P_{x2}$, to achieve all-ZVS operation, the proposed scheme will cause unexpected high circulating currents, increase conduction loss, and reduce the system efficiency. To tackle this problem and balance the two optimization objectives, this article tries to reduce the intensity of the ZVS constraints, and proposes an improved near-all-ZVS scheme. Specifically, in the power range $P_{x1}<P<P_{x2}$ of Fig. 8, we attempt to make one of the four bridge arms of the DAB converter suffer from hard switching, while the other three are

TABLE IV
CURRENT CONSTRAINTS OF THE NEAR-ALL-ZVS OPTIMIZATION PROBLEM

Mode 4	
Critical current constraint	when $0 < M < 1/2$: $\begin{cases} \frac{V_1}{4Lf_s}[(D_1-1)-M(2D_1-2D_0-D_2-1)] \le 0 \\ \sqrt{\frac{2C_sV_2^2}{L}} - \frac{V_1}{4Lf_s}[(D_1-1)-M(D_2-1)] \le 0 \end{cases}$ when $1/2 < M < 1$: $\begin{cases} \sqrt{\frac{2C_sV_2^2}{L}} - \frac{V_1}{4Lf_s}[(D_1-1)-M(D_2-1)] \le 0 \\ \frac{V_1}{4Lf_s}[(D_1-1)-M(2D_1-2D_0-D_2-1)] + I_m \le 0 \end{cases}$
Mode 1	
Critical current constraint	when $0 < M < 1/2$: $\begin{cases} \frac{V_1}{4Lf_s}[(D_1-1)-M(2D_0+D_2-1)] \le 0 \\ -\frac{V_1}{4Lf_s}[(2D_0-D_1-1)-M(D_2-1)] \le 0 \end{cases}$ when $1/2 < M < 1$: $\begin{cases} \frac{V_1}{4Lf_s}[(D_1-1)-M(2D_0+D_2-1)] + \sqrt{\frac{2C_sV_2^2(2M-1)}{L}} \le 0 \\ -\frac{V_1}{4Lf_s}[(2D_0-D_1-1)-M(D_2-1)] \le 0 \end{cases}$

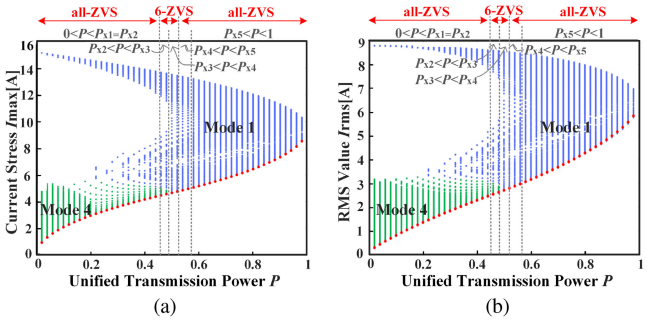


Fig. 9. Optimal curves with the proposed near-ALL-ZVS and all the possible values of $I_{\rm rms}$ and $I_{\rm max}$ at $M = 0.6$. (a) $I_{\rm max}$-P. (b) $I_{\rm rms}$-P.

still turned-ON with ZVS. That is, in this power range, only six switches operate in ZVS instead of all.

By comparing the circulating current levels in the four cases, the improved near-all-ZVS scheme eventually selects the lagging bridge arm in the primary side (S_3 and S_4) suffer from hard switching in power rang $P_{\rm x1} < P < P_{\rm x2}$ of Fig. 8. Based on this, for the improved optimal problem, the power constraint and mode constraint remain the same while the current conditions for ZVS operation have changed, which is shown in Table IV. Similarly, using the LLM method and KKT conditions, the optimal solutions of the near-ALL-ZVS modulation scheme based on TPS can also be derived, as shown in Table A.II in Appendix A.

B. Verification of Correctness of the Optimization Solution

Similarly, under the critical current constraints in Table IV, all the $I_{\rm max}$ and $I_{\rm rms}$ values for a given transmission power P are illustrated in Fig. 9. The green and blue dotted-region, respectively, represent Mode 4 and Mode 1. The red dotted lines are the optimal curves of $I_{\rm max}$ and $I_{\rm rms}$ drawn by the optimized solution in Table A.II. It is demonstrated that the improved

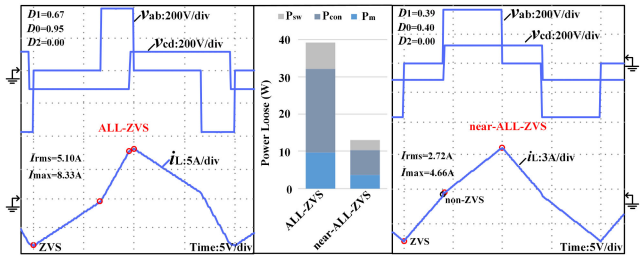


Fig. 10. Simulating waveforms and loss breakdown of the two proposed schemes ALL-ZVS and near-ALL-ZVS at optimal operating point ($M = 0.6$, $P = 0.5$).

TABLE V
MAIN PARAMETERS OF THE DAB CONVERTER

Item	Parameter
Input Voltage V_1	380 V
Output Voltage V_2	0-380V
Maximum power $P_{\rm max}$	1.5 kW
Transformer Turns Ratio N	2:1
Switching Frequency f_s	50 kHz
Additional Inductance L	200 uH
Switching device	SCT3060AR

near-ALL-ZVS modulation strategy can effectively reduce the current level in this power range.

In addition, to verify the superiority of the improved near-ALL-ZVS scheme in this power range, the operating point ($M = 0.6$, $P = 0.5$) is selected for comparison. The simulating waveforms and loss breakdown of the two optimization schemes are illustrated in Fig. 10. It can be seen that the peak current $I_{\rm max}$ decrease from 8.33 A under ALL-ZVS to 4.66 A under near-ALL-ZVS, respectively. And the rms current $I_{\rm rms}$ decrease from 5.1 A under ALL-ZVS to 2.72 A under near-ALL-ZVS. Hence, with the improved near-ALL-ZVS, the conduction loss and the loss in the magnetic components can be reduced to a large extend. Moreover, although there are two switches S_3 and S_4 cannot achieve ZVS operation with near-ALL-ZVS scheme, the total switching loss is still lower than that with the ALL-ZVS scheme due to a lower current level at switching instance. Accordingly, to realize a higher system efficiency in this power range, the improved near-ALL-ZVS optimization scheme is a better choice.

VI. SIMULATION ANALYSIS AND VERIFICATION

In this section, a linear charge-equivalent capacitance $C_{\rm eq}$ is introduced, and a comprehensive comparative analysis is carried out in terms of the current level, ZVS range, and loss breakdown. The proposed near-ALL-ZVS scheme is compared with the three typical optimization schemes, where SPS is a basic modulation scheme of the DAB converter, CSO-TPS discussed in [15] is a minimal peak current modulation scheme based on TDA, and FDM proposed in [11] is a minimal rms current scheme based on FDA. The main simulation parameters of the DAB converter is shown in Table V.

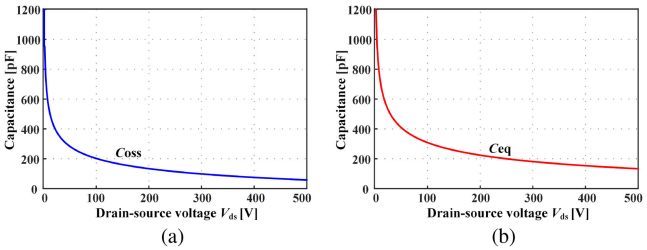


Fig. 11. Curves of $C_{\rm oss}$ and $C_{\rm eq}$ varying with $V_{\rm DS}$.

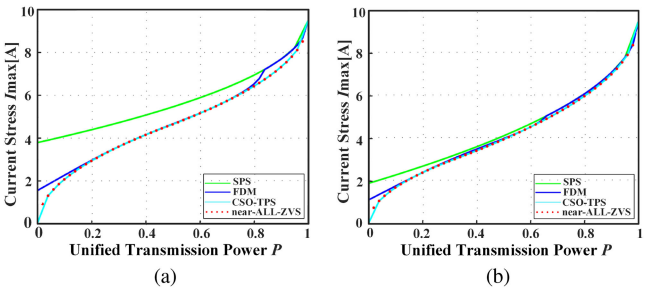


Fig. 12. $I_{\rm max}$ of various modulation schemes. (a) $M = 0.6$. (b) $M = 0.8$.

A. Linear Charge-Equivalent Capacitance $C_{\rm eq}$

According to the datasheet of SCT3060AR, the curve of the parasitic capacitance $C_{\rm oss}$ varying with the drain–source voltage drop $V_{\rm ds}$ can be described in Fig. 11(a), where the relationship between $C_{\rm oss}$ and $V_{\rm ds}$ is nonlinear. Note that, $V_{\rm ds}$ of the switching device gradually changes from the operating voltage V_1 to 0 during the dead-zone. Accordingly, $C_{\rm oss}$ will increase nonlinearly to 1200 pF. For more precise analysis, a linear charge-equivalent capacitance $C_{\rm eq}$ is introduced in [22], where the amount of the charge stored in nonlinear parasitic capacitance is the same as that stored in $C_{\rm eq}$ at a given $V_{\rm ds}$

$$C_{\rm eq} = 1685 V_{\rm ds}^{(-0.2558)} - 210.6. \tag{16}$$

According to the datasheet of SCT3060AR and reference [22], the relationship between $C_{\rm eq}$ and $V_{\rm ds}$ can be derived as (16). And the curves of charge-equivalent capacitance $C_{\rm eq}$ varying with $V_{\rm ds}$ is shown in Fig. 11(b). According to (16), the $C_{\rm p}$ of switching devices on the primary side is 158 pF when $V_{\rm in} =$ 380 V, the $C_{\rm s}$ of switching devices on the secondary side are, respectively, 291 pF when $M = 0.6$ and 255 pF when $M = 0.8$.

B. Steady-State Performance Analysis

According to the optimized strategies in Table A.II, the $I_{\rm max}$ and $I_{\rm rms}$ curves of the four modulation strategies varying with transmission power P at $M = 0.6$ and 0.8 are shown in Figs. 12 and 13, respectively. Besides, based on the accurate conditions of ZVS analyzed in Section III, the ZVS ranges of the four modulation schemes varying with the transmission power P and voltage conversion ratio M are, respectively, depicted in Fig. 14. The gray lines indicate the conditions, where all the switching devices S_1–S_8 can turn ON with ZVS. And the blank area represents that only part of the switching devices turned-ON in ZVS. Obviously, the SPS has the highest-circulating current level and

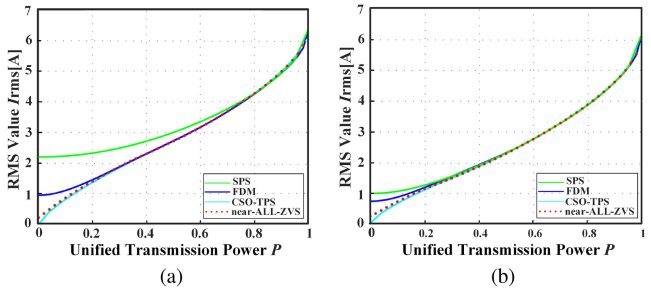


Fig. 13. $I_{\rm rms}$ of various modulation schemes. (a) $M = 0.6$. (b) $M = 0.8$.

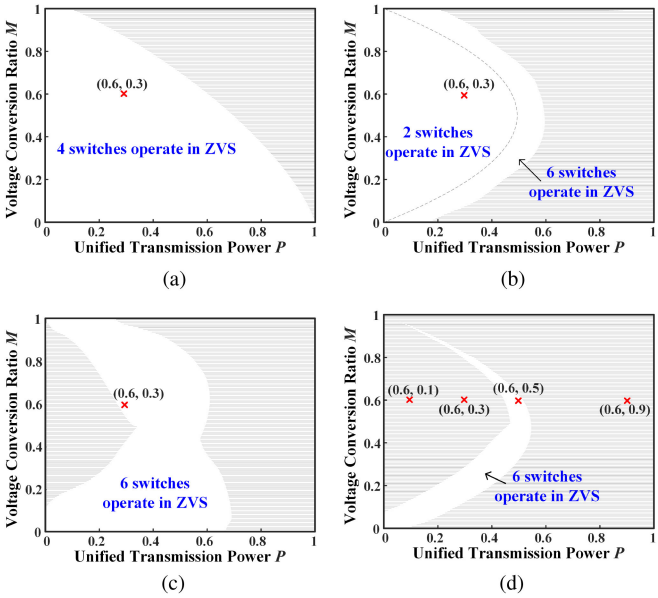


Fig. 14. Ranges of ZVS of the four modulation schemes. (a) SPS. (b) CSO-TPS. (c) FDM. (d) near-ALL-ZVS.

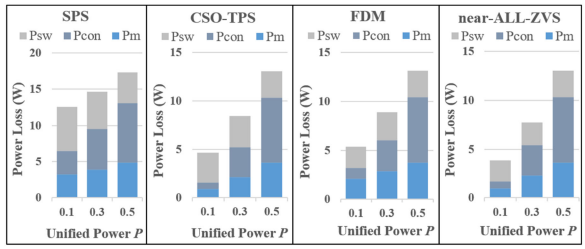
suffers from hard switching in light-load and low-M condition, causing a low system efficiency. Since the CSO-TPS scheme is a global optimization scheme aimed at peak current, it achieves the lowest peak current and rms current level in the whole operating conditions. But there are only two switches (S_1 and S_2) of the primary-side leading leg that are turned-ON with ZVS at light load. The FDM modulation slightly increase the current level to achieve ZVS operation at light-load conditions, resulting in the increased circulating current compared to CSO-TPS. Although the ZVS range can be significantly extended at light load, it still has a large non-ZVS region at medium power operation. And for the proposed near-ALL-ZVS, under the guarantee of near-all-ZVS operation, the curves of peak current and rms current of the scheme are almost overlapped with the CSO-TPS and has a reduced current level compared to FDM. Therefore, the proposed near-ALL-ZVS can efficiently expand the ZVS range while remaining a low current level.

C. Loss Breakdown Analysis

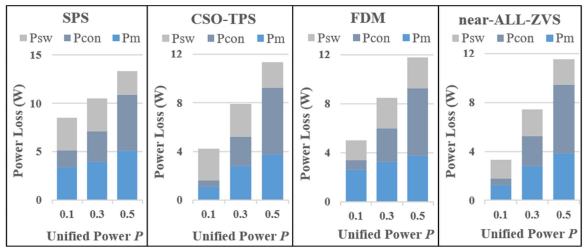
In this section, a loss model for the DAB converter has been derived. The power loss mechanism consists of three main loss factors: switching losses $P_{\rm sw}$, core losses $P_{\rm m}$, and

TABLE VI
COMPARISON OF COMMUTATION TIME

		Duration of Stage 1 t_c/ns		
		Theory	LTSPICE	Experiment
M=0.6 P=0.3	S_1	37	36	40
	S_4	370	385	390
	S_5	57	60	60
	S_8	60	61	60
M=0.6 P=0.7	S_1	24	23	25
	S_4	63	57	60
	S_5	26	24	28
	S_8	26	24	28
M=0.8 P=0.3	S_1	45.3	44.19	50
	S_4	in non-ZVS		
	S_5	128	132	135
	S_8	128	132	138
M=0.8 P=0.7	S_1	26	25	28
	S_4	44	41	45
	S_5	15	15	17
	S_8	15	15	17



(a)



(b)

Fig. 15. Loss breakdown of the four modulation schemes at unified transmission power $P = 0.1$, 0.3, and 0.5. (a) $M = 0.6$. (b) $M = 0.8$.

conduction losses $P_{\rm con}$. As for switching losses $P_{\rm sw}$, referring to the literature [23], this article adopts a simple and effective switching loss model. It is based on the LTSPICE simulation platform to predict the turn-OFFand turn-ON switching loss at different switching currents. For the core loss $P_{\rm m}$ of the magnetic elements, the previous model uses the conventional Steinmetz equation to estimate the core loss, but the formula is only suitable for sinusoidal waveforms. To have a more accurate model, the modified Steinmetz equation is used, referring to the literature [24]. Moreover, the conduction loss $P_{\rm con}$ includes the conduction loss of the switching device and the copper loss of the magnetic element, where copper loss is mainly caused by skin effect and proximity effect of windings. In this article, the influence of skin effect is only considered, and the ac copper loss at each harmonic is calculated by adding up the losses from 1st to 32nd harmonics.

Based on the derived loss model and circuit parameters given in Table VI, the loss breakdown of the four modulation schemes at $M = 0.6$ and $M = 0.8$ is shown in Fig. 15. According to the current level and ZVS range shown in Figs. 12–14, these modulation strategies differ significantly over light to medium power range, while in the heavy power range, they all operate in a similar steady-state performance. Hence, only the loss breakdown at $P = 0.1$, 0.3, and 0.5 is illustrated here. As observed, the conduction loss and core loss increase with the increase of transmission power. The switching loss accounts for a large proportion of the total loss, especially in the low power range. And the proposed near-ALL-ZVS scheme significantly reduces the switching loss while ensuring the low conduction loss in an extensive power range.

VII. EXPERIMENTS

An experimental platform is built to verify the theoretical analysis above. And the experimental parameters are the same as those shown in Table VI. In this section, the theoretically calculated time t_c is verified by experiment, the implementation of the control is given in detail, and the comparative analysis of the steady-state characteristics among the four modulation schemes is carried out.

A. Dead-Zone

To verify the correctness of t_c computed in Table II, Table VI compares theoretically calculated values, LTSPICE simulation values, and experimental values. It is demonstrated that the theoretical calculation can approximately predict t_c. Therefore, the dead time can be determined through the theoretically calculated t_c in the experimental implementation. In addition, as observed from Table VI, the commutation time t_c corresponding to the four bridge arms is different even under the same voltage conversion ratio M and power transmission P. For instance, at $M = 0.6$, $P = 0.3$, the commutation time t_c of S_1 is 40 ns while that of S_4 is 390 ns, which is nearly ten times longer than S_1. This is because the instantaneous inductor current flowing through S_1 and S_4 at turn-ON instance are -3.52 and -0.3 A, respectively. And the larger the switching current at the turned-ON instance is, the faster the parasitic capacitor will charge and discharge at stage 1. Therefore, to set the dead time accurately, the dead time of the four bridge arms should also be set separately and should be recalculated once the working condition changes.

B. Control Block Diagram

The control block diagram of DAB dc–dc converters with the proposed modulation scheme is shown in Fig. 16, which is implemented in a digital signal processor TMS320F28335 to generate the gate driving signals. The input voltage V_1 is fixed to 380 V. V_2^* represents the desired output voltage, which is compared with the actual output voltage V_2 to generate the voltage error v_e. As the input of automatic power regulator PI, v_e generates the reference transmission power P. Then, according

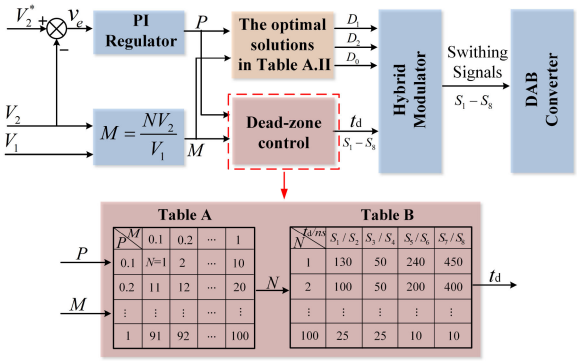


Fig. 16. Control block diagram with near-ALL-ZVS control.

to (P, M) and the optimal solutions in Table A.II, the optimized operating points (D_1, D_2, D_3) are computed.

Besides, to achieve the dynamic adjustment of dead time under different working conditions (P, M), the look-up table method is introduced in this article. As shown in Fig. 16, the basic idea is to calculate the dead times required by different working conditions in advance, and load them into the DSP controller. During the control implementation, according to (P, M), the dead time of bridge arms can be obtained by looking up tables. Table A is used to determine the serial number N of different working conditions (P, M). According to N, Table B is used to find the dead time corresponding to different working conditions. Since this article only focuses on whether the MOSFET can be turned-ON with ZVS, and ignores the influence of the length of dead time on efficiency. Therefore, this article does not strictly require the MOSFET to be turned-ON at the end of Stage 1 (that is, $t_{\rm d} = t_{\rm c}$). Conversely, to leave some margin, the relatively loose dead time is given in the experiment.

C. Steady-State Waveforms

The steady-state waveforms corresponding to the operating point marked in Fig. 14 are measured in this section. Fig. 17 illustrates the typical working waveforms of the proposed near-all-ZVS at $M = 0.6$. The rms current and ZVS range are given in the waveforms, where the red (blue) circle represents ZVS (non-ZVS) operating point. As observed in Fig. 17(a) and (b), the DAB converter not only realizes full-ZVS operation, it also leads to the quasi-minimum rms current under light load conditions with $P = 0.1$ and 0.3. And in Fig. 17(c), at medium power range with $P = 0.5$, the proposed optimization strategy backs to EPS modulation. And there are two switches suffering from hard switching, which is predicated by the previous analysis. Furthermore, at heavy load condition with $P = 0.9$ shown in Fig. 17(d), it is also in EPS modulation and all switches are operating in the soft-switching condition.

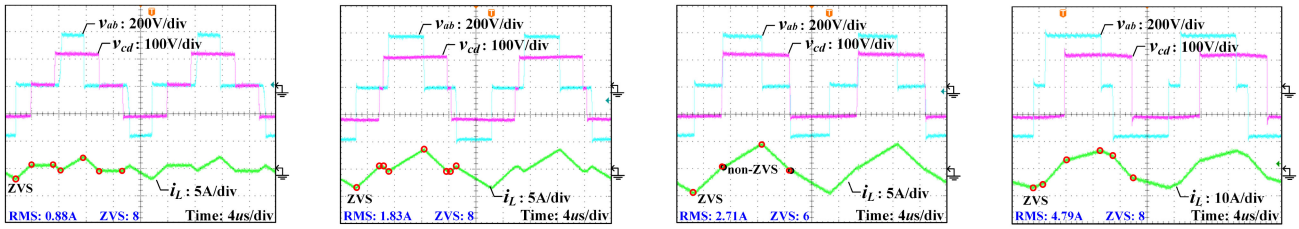
In addition, to highlight the improvement of the proposed scheme, Fig. 18 shows the typical working waveforms of the four optimization schemes when $M = 0.6$ and $P = 0.3$. For the proposed near-all-ZVS scheme in Fig. 18(a), it can efficiently expand the ZVS range while remaining a low current level. However, as seen in Fig. 18(b), the DAB converter under SPS has the highest-circulating current level over the whole power range. And there are four switching devices can not be turned-ON in ZVS. In Fig. 18(c), as the typical TPS optimization schemes based on the TDA method, the CSO-TPS has a minimal circulating current level. But it comes at the expense of the ZVS operation. specifically, there are six switches suffer form hard switching, which is consistent with the theoretical analysis. In Fig. 18(d), as the typical optimization schemes based on FDA, the FDM has a better effect on ZVS operation, but it leads to a higher current level.

Moreover, Table A.III in Appendix A gives the optimal solutions of $M > 1$. And to verify the effectiveness of the proposed scheme in boost mode, the typical working waveforms of SPS, CSO-TPS, and the proposed scheme at $M = 1.2$ are also measured in Fig. 19. Noted that, since the optimal solutions at $M > 1$ are not discussed in FDM scheme, its experimental waveform is not given here. In Fig. 19(a), at low power range with $P = 0.1$, the converter operates in Mode 5. As seen from the waveforms, although the proposed scheme can greatly reduce the current level, due to the inherent characteristics of Mode 5, there are only six switches could achieve ZVS operation at light load. This is slightly different from the optimization result when $M < 1$. However, compared with the working waveforms under SPS and FDM, shown in Fig. 19(b) and (c), the proposed scheme still has a remarkable improvement in current level and ZVS range. And in Fig. 19(d), at medium power range with $P = 0.5$, the converter is working in Mode 1, and all the eight switches are turned-ON with ZVS, which is consistent with the condition of $M < 1$.

Besides, in order to verify the validity of the theoretical analysis across a wide voltage range, the working waveforms at $M = 0.2$, 0.4, 0.8, and 1.2 when $P = 0.2$ are tested in Fig. 20. As observed, even if the output voltage is changed in a wide voltage range from 38 to 228 V, the proposed optimization scheme can still ensure the full-ZVS operation and low current level.

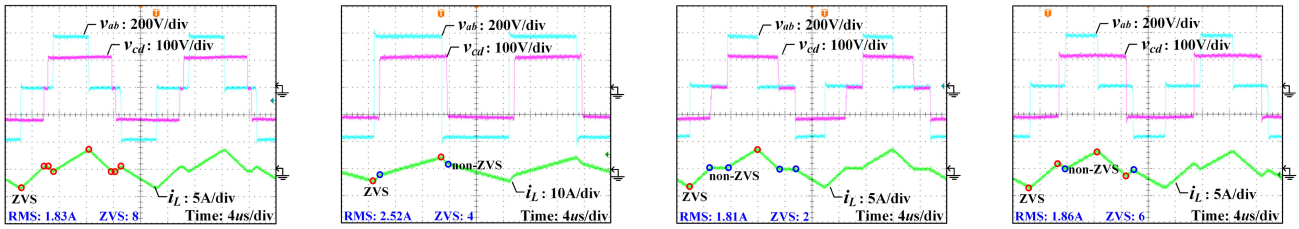
D. ZVS Characteristics

To verify the importance of the accurate ZVS constraints, Fig. 21 shows the four hard-switching cases due to inaccurate ZVS constraints. The waveforms of the inductor current $i_{\rm L}$, the gate-source voltage $v_{\rm gs}$ and drain-source voltage $v_{\rm ds}$ at turn-ON instance are separately measured. In Fig. 21(a), since the direction of instance current flowing through the MOSFET is wrong, the MOSFET is in non-ZVS operation. In Fig. 21(b), the reason for hard switching is that the value of instance current is less than the required minimum commutation current. So there is no enough energy to get the voltage $v_{\rm ds}$ down to zero and complete the commutation process. In Fig. 21(c), due to the insufficient dead time, the driving signal arrives before the drain–source voltage $v_{\rm ds}$ drops to zero. Therefore, even if the minimum communication current is met, the MOSFET will also fail to achieve soft switching. On the contrary, Fig. 21(d) shows a commutation process with an excessive dead time, which is consistent with the theory analysis in Section III. When the drain–source voltage $v_{\rm ds}$ drops to zero, antiparallel diode of the MOSFET is conducted in Stage 2, which leads to an additional system loss. Then, when the inductor current $i_{\rm L}$ drops to zero,



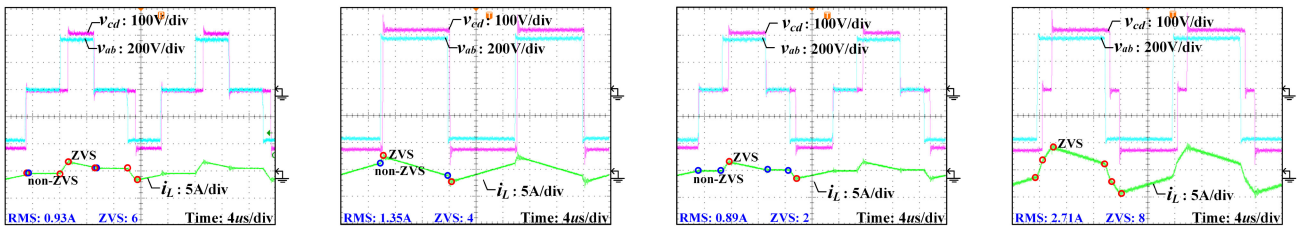
(a) (b) (c) (d)

Fig. 17. Typical working waveforms of DAB with the proposed near-ALL-ZVS at $M = 0.6$. (a) $P = 0.1$. (b) $P = 0.3$. (c) $P = 0.5$. (e) $P = 0.9$.



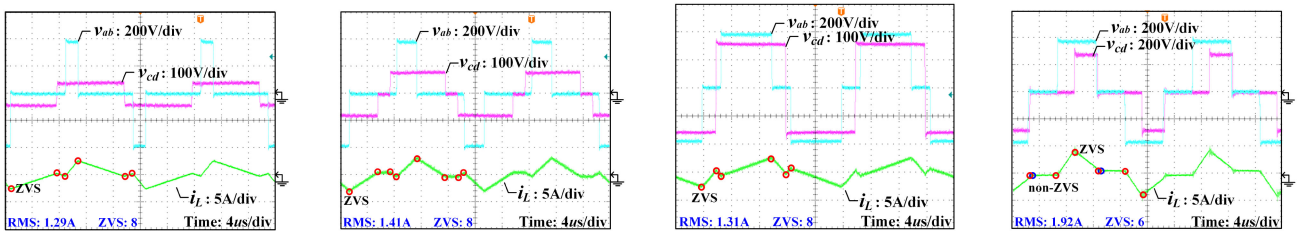
(a) (b) (c) (d)

Fig. 18. Typical working waveforms under the four schemes when $M = 0.6$ and $P = 0.3$. (a) near-ALL-ZVS. (b) SPS. (c) CSO-TPS. (d) FDM.



(a) (b) (c) (d)

Fig. 19. Typical working waveforms under the three schemes when $M = 1.2$. (a) near-ALL-ZVS at $P = 0.1$. (b) SPS at $P = 0.1$. (c) CSO-TPS at $P = 0.1$. (d) near-ALL-ZVS at $P = 0.5$.



(a) (b) (c) (d)

Fig. 20. Typical working waveforms of DAB under the proposed near-ALL-ZVS strategy at $P = 0.2$. (a) $M = 0.2$. (b) $M = 0.4$. (c) $M = 0.8$. (e) $M = 1.2$.

the drain–source voltage v_{ds} rises. If the MOSFET is turned-ON at this time, the ZVS operation will be lost.

Moreover, to show the soft-switching superiority of the proposed scheme, when $M = 0.6$ and $P = 0.3$, the ZVS characteristics under the four optimization strategies are demonstrated in Fig. 22. In Fig. 22(a), under SPS modulation, all the four switching devices on secondary HBs are suffering hard switching due to the wrong inductor current direction. And under FDM scheme in Fig. 22(b), the lagging primary bridge arm corresponding to S_3 and S_4 is in non-ZVS operation. Because the instantaneous current flowing through S_3 and S_4 at turn-ON instance is 0, which does not meet the critical current condition. And in Fig. 22(c), under CSO-TPS scheme, there are six switching devices can not achieve ZVS operation for the same reason. While when the DAB converter is modulate by the proposed near-ALL-ZVS in Fig. 22(d), all the eight switches can achieve soft switching,

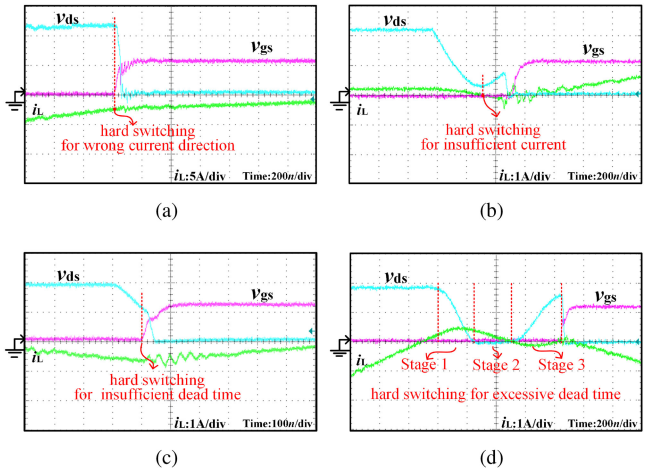


Fig. 21. Four conditions of hard switching. (a) Wrong current direction. (b) Insufficient current. (c) Insufficient dead time. (d) Excessive dead time.

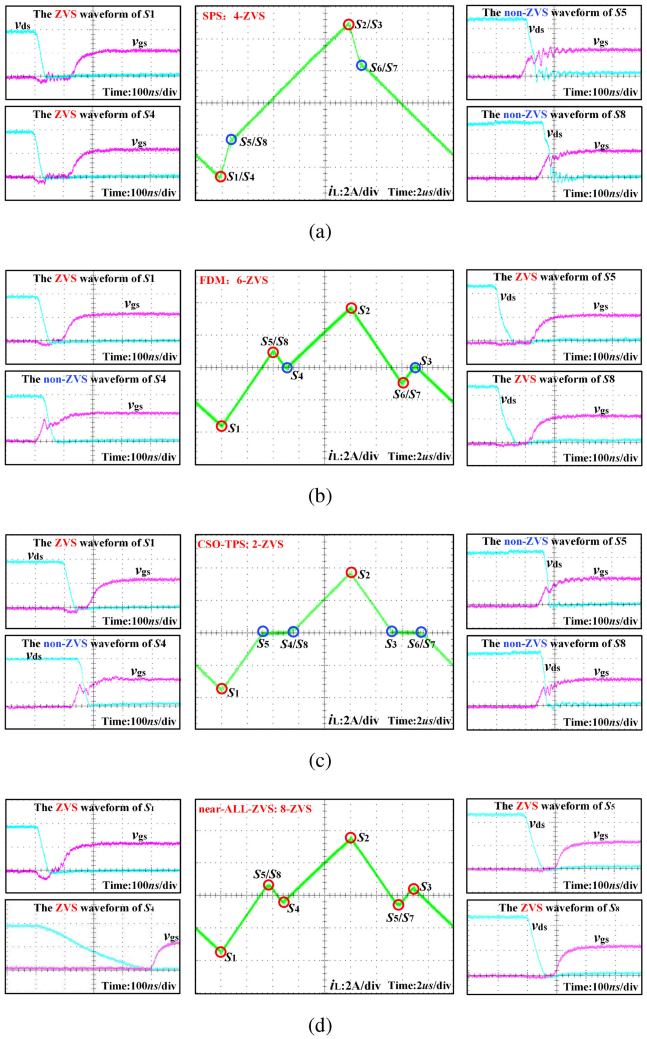


Fig. 22. ZVS waveforms at $M = 0.6$ and $P = 0.3$. (a) SPS. (b) FDM. (c) TPS. (d) near-ALL-ZVS.

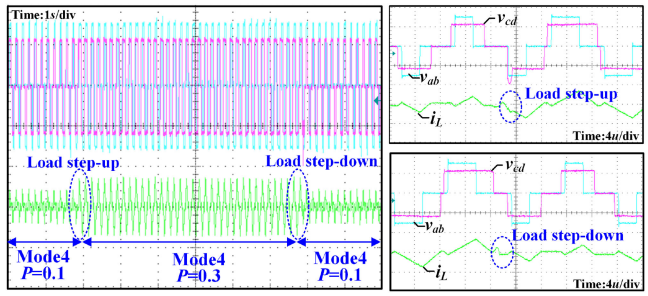


Fig. 23. Dynamic working waveforms under closed-loop control at $M = 0.6$ when P switches from 0.1 to 0.3 and back to 0.1.

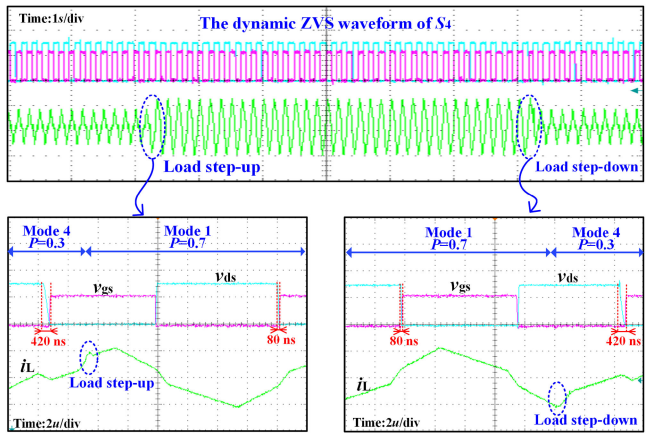


Fig. 24. Dynamic ZVS waveforms of S_4 under closed-loop control at $M = 0.6$.

which is consistent with the theory analysis. It is demonstrated that the proposed comprehensive efficiency optimization based on the accurate ZVS constraints and dead-zone control can availably expand the ZVS range.

E. Dynamic Response of the System

Dynamic characteristics of DAB under closed-loop control strategy were also tested in Fig. 23. It shows the dynamic working waveforms when transmission power P steps between 0.1 and 0.3. The blue dotted box represents the transient instance. As observed, the proposed closed-loop control strategy can adjust the output power to the required value. And the proposed optimization strategy does not have obvious negative impact on dynamic performance, although this article is not focused on the transient problems.

Besides, to verify the effectiveness of the proposed dead-zone control, the experiments have been carried out to test the dynamic ZVS performance when load switches between 0.3 and 0.7. In Fig. 24, the waveforms of the inductor current i_{L}, the gate-source voltage v_{gs} and drain–source voltage v_{ds} of S_4 are measured. According to Table VI, the commutation time t_{c} of S_4 is, respectively, 390 ns at $P = 0.3$ and 60 ns at $P = 0.7$. And under the adjustment of the dead-zone control, when the power is switched between 0.3 and 0.7, the dead time of S_4 also changes between 420 and 80 ns to ensure a complete ZVS operation. It is demonstrated that the look-up table control

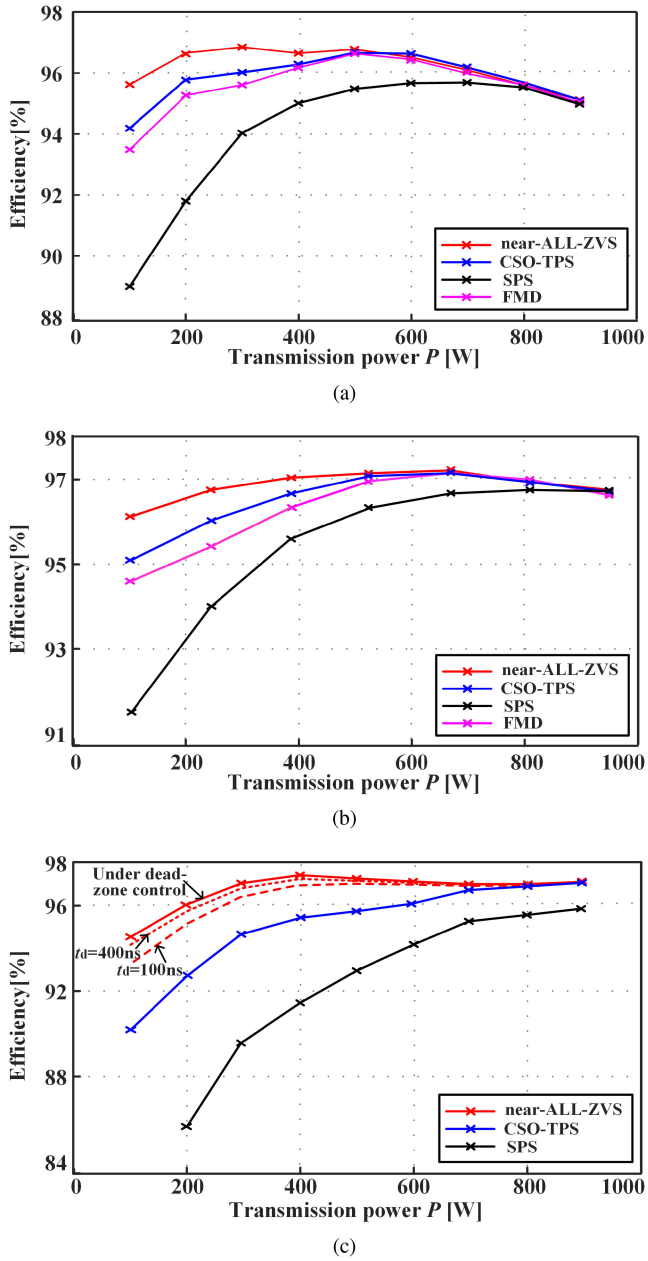


Fig. 25. Experiment efficiency curves of the DAB converter with the four optimization strategies at (a) $M = 0.6$. (b) $M = 0.8$. (c) $M = 1.2$.

can effectively achieve dynamic adjustment of dead time under different working conditions.

F. Efficiency Curves

The experimental efficiency curves of SPS, FDM, CSO-TPS and near-ALL-ZVS at $M = 0.6$, $M = 0.8$, and $M = 1.2$ are depicted in Fig. 25. As observed, some conclusions can be drawn from the figures.

1) The DAB converter modulated by SPS can natively achieve high efficiency at heavy load. However, as load decrease and voltage gain drive away from unity, the large rms current and limited ZVS range will be inherently induced, resulting in poor system efficiency.
2) Over light to medium power range, FDM, CSO-TPS, and near-ALL-ZVS can significantly improve the system efficiency due to more degrees of freedom compared with SPS. While as the power increases further, at heavy-load conditions, the optimal results of the four modulation schemes approach SPS modulation because they have almost the similar system performance.
3) Since CSO-TPS scheme achieves a low peak current and rms current level in the whole operating conditions, compared with SPS, the system efficiency modulated by CSO-TPS has been greatly improved. However, under CSO-TPS modulation, none of the six switching devices can achieve ZVS conduction at light load. Therefore, the efficiency at light load is not high due to the large switching losses.
4) The FDM modulation slightly sacrifices the current level to expand ZVS operation range at light-load conditions, resulting in larger conduction losses and smaller switching losses than CSO-TPS. It is noted that the experimental platform is based on SiC MOSFETs, which have a smaller switching loss than Si MOSFETs. Therefore, even though FDM has a better ZVS performance at light load, its efficiency is still lower than CSO-TPS due to the large circuit current. Whereas under the experimental platform based on Si MOSFET, FDM may have a more remarkable performance improvement than CSO-TPS [15].
5) On the whole, since the proposed near-ALL-ZVS optimization scheme can achieve a low peak current level and near-all-ZVS operation, it realizes a remarkable improvement on system efficiency. Under the proposed scheme, the maximum efficiency of the converter can reach 96.8% when $M = 0.6$ and 97.3% when $M = 0.8$. When $M = 1.2$, the maximum efficiency increase can reach 10% compared with SPS and 4.5% compared with CSO-TPS.

Moreover, in order to highlight the contribution of the dead-zone control, Fig. 25(c) also gives the efficiency curves of the near-ALL-ZVS without the dead-zone control. Theoretically, to achieve ZVS operation, the dead time required by the switching devices S_1–S_4 ON the primary side is about 400 ns, while the switching devices S_7–S_8 ON the secondary side only need about 100 ns. Based on this, the two red dotted lines, respectively, measure the efficiency curves when the dead time is fixed at 100 and 400 ns. As observed, under the fixed dead time $t_{\rm d} =$ 100 ns, the switching devices S_7–S_8 can realize a complete ZVS operation. However, the switching devices S_1–S_4 will suffer from an incomplete ZVS turned-ON process due to insufficient dead time, as illustrated in Fig. 21(c). The incomplete ZVS operation will cause some switching loss and slightly lower efficiency, but this loss is less than the loss caused by hard switching. Correspondingly, with a fixed dead time $t_{\rm d} = 400$ ns, all six switching devices is in soft switching. However, due to the long dead time for S_7–S_8, the antiparallel diodes of the two switching devices will conduct and cause additional system losses, as illustrated in Fig. 21(d). Because the longer dead

TABLE VII
COMPREHENSIVE COMPARISON BETWEEN THE PROPOSED SCHEME AND SOME TYPICAL STRATEGIES

Optimization schemes	Modulation method	Analysis method	ZVS constraints	Optimization objective	Dead-zone control	Steady state performance		
						Current level	ZVS range	Efficiency
[1]	SPS	TDA	\	\	no	high	narrow	low
[4]	DPS	TDA	\	$I_{\max}$	no	high	narrow	low
[6]	EPS	TDA	\	$I_{\max}$	no	medium	medium	medium
[11]	TPS	FDA	\	$I_{\rm rms}$	no	medium	medium	medium
[15]-[17]	TPS	TDA, FDA	\	$I_{\max}$	no	low	narrow	medium
[18]-[19]	TPS	TDA	approximate	$I_{\rm rms}$ + ZVS	no	low	medium	medium
[20]	TPS	TDA	approximate	$I_{\rm rms}$ + $I_{\max}$ + ZVS	no	low	medium	medium
The proposed	TPS	TDA	accurate	$I_{\max}$ + ZVS	yes	low	wide	high

TABLE A.I
OPTIMIZATION SOLUTIONS OF ALL-ZVS SCHEME AND CORRESPONDING POWER RANGES

$0 < P < P_{\rm x1}$ (Mode 4)	$0 < M < 1/2$	$D_1 = 1 - \frac{\sqrt{2PM(1-M) + 32C_{\rm p}f_{\rm s}^2L(1-2M)} + \sqrt{32C_{\rm p}f_{\rm s}^2L(1-2M)}}{2(1-M)}$; $D_0 = \frac{D_1 - D_2}{2} + \frac{P}{4(1-D_1)}$ $D_2 = 1 - \frac{\sqrt{2PM(1-M) + 32C_{\rm p}f_{\rm s}^2L(1-2M)} + \sqrt{32C_{\rm p}f_{\rm s}^2L(1-2M)}}{2M(1-M)} + \frac{\sqrt{32C_{\rm p}f_{\rm s}^2L}}{n}$
	$1/2 < M < 1$	$D_1 = 1 - \frac{2\sqrt{2}f_{\rm s}I_{\rm m}L - \sqrt{8f_{\rm s}^2I_{\rm m}^2L^2 - PV_1nV_2(M-1)}}{\sqrt{2}V_1(1-M)}$ $D_0 = \frac{\sqrt{8f_{\rm s}^2I_{\rm m}^2L^2 - PV_1nV_2(M-1)} + \sqrt{16f_{\rm s}^2LC_{\rm s}V_2^2}}{\sqrt{2}nV_2}$ $D_2 = 1 - \frac{2\sqrt{2}f_{\rm s}I_{\rm m}L + (1-M)\sqrt{64f_{\rm s}^2LC_{\rm s}V_2^2} + \sqrt{8f_{\rm s}^2I_{\rm m}^2L^2 - PV_1nV_2(M-1)}}{\sqrt{2}nV_2(1-M)}$
$P_{\rm x1} < P < P_{\rm x2}$ (Mode 1)		$D_1 = -U\sqrt{-\frac{H}{16R}} - O$; $D_0 = A - Q\sqrt{-\frac{H}{16R}}$; $D_2 = 0$; if $D_0 > 1$: $D_1 = \left(P - \frac{1}{2}\right)\sqrt{\frac{1}{1-2P}} + \frac{1}{2}$; $D_0 = 1$; $D_2 = 0$;
$P_{\rm x2} < P < P_{\rm x3}$ (Mode 1)		$D_1 = U\sqrt{-\frac{H}{16R}} - O$; $D_0 = A + Q\sqrt{-\frac{H}{16R}}$; $D_2 = 0$;
$P_{\rm x3} < P < 1$ (Mode 1)		$D_1 = (1-M)\sqrt{\frac{1-P}{2M^2-2M+1}}$; $D_2 = 0$; $D_0 = \frac{(1 + D_1 - D_2) - \sqrt{1 - D_1^2 - D_2^2 - P}}{2}$

$$P_{\rm x1} = \begin{cases} \dfrac{2\left[M\left((1-M) + \dfrac{1}{n}\sqrt{32C_{\rm s}f_{\rm s}^2L}\right) + \sqrt{8C_{\rm p}f_{\rm s}^2L(1-2M)}\right]^2 - 16C_{\rm p}f_{\rm s}^2L(1-2M)}{M(1-M)} & (0 < M < 1/2) \\ -\dfrac{(\sqrt{2}nV_2(M-1) - 8(M-1)\sqrt{C_{\rm p}f_{\rm s}^2LV_2^2} + 2\sqrt{2}f_{\rm s}I_{\rm m}L)^2 - 8f_{\rm s}^2I_{\rm m}^2L^2}{nV_1V_2(M-1)} & (1/2 < M < 1) \end{cases}$$

$$P_{\rm x2} = 1 - M^2 - \frac{(1 - M^2 - \sqrt{32f_{\rm s}^2C_{\rm p}L(2M+1)})^2}{(1+M)^2}$$

$$P_{\rm x3} = 2M(1-M) - 32C_{\rm p}Lf_{\rm s}^2(1 - 2M^2 + 4M^3) + 8\sqrt{2C_{\rm p}Lf_{\rm s}^2(1+2M)}(1 - 2M + 2M^2)$$

time can ensure ZVS operation of the switching devices, the efficiency curve with the fixed dead time 400 ns is relatively high. Besides, it is worth noting that since the switching loss accounts for a greater proportion of the total loss at light-load condition, the impact in low power range is more obvious.

G. Comprehensive Comparison

To further highlight the advantages of the proposed near-ALL-ZVS scheme, a comprehensive comparison between the proposed scheme and some typical optimization methods has been listed in Table VII. As observed, this article adopts the unified TPS modulation method and TDA method, which could provide greater optimization freedom and more accurate analysis model. Besides, to achieve wide ZVS operation, the accurate ZVS constraints (including minimum commutation current and required dead time) are deduced in this article. Then, on the basis of the accurate current constraints, a comprehensive multi-objective efficiency optimization method is proposed to achieve minimum current level and wide ZVS range, thus improving

TABLE A.II
OPTIMIZATION SOLUTIONS OF NEAR-ALL-ZVS SCHEME AND CORRESPONDING POWER RANGES

$0 < P < P_{x1}$ (Mode 4)	$0 < M < 1/2$	$D_1 = 1 - \frac{\sqrt{2PM(1-M) + 32C_p f_s^2 L(1-2M)} + \sqrt{32C_p f_s^2 L(1-2M)}}{2(1-M)}$; $D_0 = \frac{D_1 - D_2}{2} + \frac{P}{4(1-D_1)}$ $D_2 = 1 - \frac{\sqrt{2PM(1-M) + 32C_p f_s^2 L(1-2M)} + \sqrt{32C_p f_s^2 L(1-2M)}}{2M(1-M)} + \frac{\sqrt{32C_p f_s^2 L}}{n}$
	$1/2 < M < 1$	$D_1 = 1 - \frac{2\sqrt{2} f_s I_m L - \sqrt{8 f_s^2 I_m^2 L^2 - PV_1 n V_2 (M-1)}}{\sqrt{2} V_1 (1-M)}$; $D_0 = \frac{\sqrt{8 f_s^2 I_m^2 L^2 - PV_1 n V_2 (M-1)} + \sqrt{16 f_s^2 L C_s V_2^2}}{\sqrt{2} n V_2}$ $D_2 = 1 - \frac{2\sqrt{2} f_s I_m L + (1-M)\sqrt{64 f_s^2 L C_s V_2^2} + \sqrt{8 f_s^2 I_m^2 L^2 - PV_1 n V_2 (M-1)}}{\sqrt{2} n V_2 (1-M)}$
$P_{x1} < P < P_{x2}$ (Mode 4)		$D_1 = 1 - \sqrt{\frac{MP}{1-M}}$; $D_2 = 1 - \sqrt{\frac{32 f_s^2 L C_s}{n}} - \sqrt{\frac{P}{2M(1-M)}}$; $D_0 = \frac{D_1 - D_2}{2} + \frac{P}{4(1-D_1)}$;
$P_{x2} < P < P_{x3}$ (Mode 1/4)	$0 < M < 1/2$ (Mode 1)	$D_1 = \frac{1 + \sqrt{1-2P}}{2}$; $D_2 = 0$; $D_0 = \frac{(1 + D_1 - D_2) - \sqrt{1 - D_1^2 - D_2^2 - P}}{2}$
	$1/2 < M < 1$ (Mode 4)	$D_1 = 1 - M + \frac{M\sqrt{32 f_s L C_s}}{n}$; $D_2 = 0$; $D_0 = \frac{D_1 - D_2}{2} + \frac{P}{4(1-D_1)}$
$P_{x3} < P < P_{x4}$ (Mode 1)		$D_1 = (1-M)\sqrt{\frac{1-P}{2M^2 - 2M + 1}}$; $D_2 = 0$; $D_0 = \frac{(1 + D_1 - D_2) - \sqrt{1 - D_1^2 - D_2^2 - P}}{2}$
$P_{x4} < P < P_{x5}$ (Mode 1)		$D_1 = U\sqrt{-\frac{H}{16R}} - O$; $D_2 = 0$; $D_0 = A + Q\sqrt{\frac{H}{16R}}$;
$P_{x5} < P < 1$ (Mode 1)		$D_1 = (1-M)\sqrt{\frac{1-P}{2M^2 - 2M + 1}}$; $D_2 = 0$; $D_0 = \frac{(1 + D_1 - D_2) - \sqrt{1 - D_1^2 - D_2^2 - P}}{2}$

$$P_{x1} = \begin{cases} \dfrac{2\left[M\left((1-M) + \frac{1}{n}\sqrt{32 C_s f_s^2 L}\right) + \sqrt{8 C_p f_s^2 L(1-2M)}\right]^2 - 16 C_p f_s^2 L(1-2M)}{M(1-M)} & (0 < M < 1/2) \\ -\dfrac{(\sqrt{2} n V_2 (M-1) - 8(M-1)\sqrt{C_p f_s^2 L V_2^2} + 2\sqrt{2} f_s I_m L)^2 - 8 f_s^2 I_m^2 L^2}{n V_1 V_2 (M-1)} & (1/2 < M < 1) \end{cases}$$

$$P_{x2} = \begin{cases} -\dfrac{2V_2(M-1)\left[N^2 V_2 + 32 C_p f_s^2 L V_2 - 8\sqrt{2} f_s L n \sqrt{\frac{C_s V_2^2}{L}}\right]}{M V_1 1^2} & (0 < M < 1/2) \\ -\dfrac{(\sqrt{2} n V_2 (M-1) - 8(M-1)\sqrt{C_p f_s^2 L V_2^2} + 2\sqrt{2} f_s I_m L)^2 - 8 f_s^2 I_m^2 L^2}{n V_1 V_2 (M-1)} & (1/2 < M < 1) \end{cases}$$

$$P_{x3} = 2M(1-M); \quad P_{x4} = 1 - M^2 - \frac{(1 - M^2 - \sqrt{32 f_s^2 C_p L(2M+1)})^2}{(1+M)^2}$$

$$P_{x5} = 2M(1-M) - 32 C_p L f_s^2 (1 - 2M^2 + 4M^3) + 8\sqrt{2 C_p L f_s^2 (1+2M)}(1 - 2M + 2M^2)$$

the system efficiency significantly. Meanwhile, on the basis of the required dead time, the dead-zone control is introduced to achieve the dynamic adjustment of dead time under different working conditions, thereby further ensuring a complete ZVS operation and avoiding the additional loss caused by antiparallel diode. To sum up, distinct from theses modulation schemes, the proposed scheme is a multiobjective optimization based on the accurate ZVS constraints and is implemented in combined with the dead-zone control.

VIII. CONCLUSION

In order to reduce switching loss and conduction loss simultaneously, this article first proposes a comprehensive multiobjective optimization method (that is, ALL-ZVS scheme). It aims at minimizing peak current level while achieving all-ZVS operation down to no-load. Unfortunately, at a certain power range, the proposed ALL-ZVS will cause unexpected high circulating currents and increased conduction loss, which in turn reduces the system efficiency. To tackle this problem, this article tries to reduce the intensity of the ZVS constraints, and proposes an improved comprehensive optimization method (that is, near-ALL-ZVS scheme). And a closed-form global optimal solutions in buck and boost modes of the DAB converter are obtained to realize the real-time control across a wide load and voltage ranges. By comparing the steady-state characteristics of SPS, FDM, CSO-TPS and the proposed near-ALL-ZVS in terms of current level, ZVS range and loss breakdown, it demonstrated that the proposed scheme can simultaneously achieve near-all-ZVS operation and low peak current level over the whole power range.

In addition, since the accurate ZVS constraints are required for the proposed optimization schemes, the commutation process in the dead-band is analyzed in detail. And the accurate conditions,

TABLE A.III
OPTIMIZATION SOLUTIONS OF NEAR-ALL-ZVS SCHEME WHEN $P > 0$ AND $M > 1$

$P_{x1} < P < P_{x2}$ (Mode 5)	$D_1 = \frac{(2\sqrt{2}Lf_s\sqrt{C_p/L}-1)(1-M)+2\sqrt{2}Lf_s\sqrt{C_p(2M-1)/L}}{M-1} + \frac{\sqrt{-M(PM(M+1)+16C_pf_s^2(2-3M))}}{\sqrt{2}(M-1)}$; $D_2 = \frac{(2\sqrt{2}Lf_s\sqrt{C_p/L}+M)(M-1)+2\sqrt{2}Lf_s\sqrt{C_p(2M-1)/L}}{M(M-1)} + \frac{\sqrt{-M(PM(M+1)+16C_pf_s^2(2-3M))}}{\sqrt{2}(M-1)}$; $D_2 = 1 - \frac{\sqrt{2}\sqrt{2D_1D_2-2D_2-P-2D_1+2}}{2} - D_2$;
$P_{x1} < P < P_{x2}$ (Mode 5)	$D_1 = \frac{M\sqrt{-(3M^2-3M+3)(3P-2)/2}+1}{3(3M^2-3M+3)}$; $D_2 = \frac{1-(2M-3)\sqrt{-(M^2-3M+3)(3P-2)/2}}{3(M^2-3M+3)}$; $D_0 = 1 - \frac{\sqrt{2D_1D_2-2D_2-P-2D_1+2}}{\sqrt{2}} - D_2$;
$P_{x2} < P < 1$ (Mode 1)	$D_1 = 0$; $D_2 = -\frac{(M-1)(P-1)\sqrt{-(M^2-2M+2)/(P-1)}}{M^2-2M+2}$; $D_0 = \frac{D_1-D_2-\sqrt{-D_1^2-D_2^2-P+1}+1}{2}$;
$P_{x1} = \frac{8\sqrt{2}Lf_s\sqrt{C_p/L}(M-1)-2(M-1)+32C_pLf_s^2\sqrt{2M-1}-8\sqrt{2}Lf_s\sqrt{C_p(2M-1)/L}+32C_pLMf_s^2}{M^2}$;	
$P_{x2} = -(M-1)^2 - \frac{(M^2-2M+2)(1-M^2+32C_pLMf_s^2(2M+1)-8\sqrt{2}Lf_s\sqrt{C_p(2M+1)/L})}{M^2}$;	

including minimum commutation current and required dead time, are deduced step by step. Meanwhile, to ensure the ZVS operation, a look-up table method is introduced to implement the dynamic dead-zone control in this paper. At last, a 1.5 kW laboratory prototype is built. The proposed modulation scheme and theoretical analysis are verified on the built platform, yielding a significant improvement of the system efficiency.

APPENDIX

The optimal solutions of the proposed ALL-ZVS and near-ALL-ZVS schemes in buck mode are, respectively, presented in Tables A.I and A.II, where *A*, *H*, *U*, *G*, and *Q* in Tables A.I and A.II are also expressed in (A.1)–(A.6), as shown at the bottom of the this page. And the optimal solutions of the proposed near-ALL-ZVS schemes in boost mode are presented in Table A.III.

$$A = \frac{M^2+1+M-2\sqrt{2}f_s\sqrt{LC_p\,(1+2M)}}{2M^2+2M+1} \tag{A.1}$$

$$H = P-2M^2+2PM^2-2M+32C_pLf_s{}^2+2PM+64C_pLMf_s{}^2-8\sqrt{2}f_s\sqrt{LC_p(1+2M)} \tag{A.2}$$

$$U = \frac{4M\left[P-2M^2+2PM^2-2M+32C_pLf_s{}^2+2PM+64C_pLMf_s{}^2-8\sqrt{2}f_s\sqrt{LC_p(1+2M)}\right]}{(2M^2+2M+1)} \tag{A.3}$$

$$G = \frac{8\sqrt{2}M^2f_s\sqrt{LC_p\,(1+2M)}+12\sqrt{2}Mf_s\sqrt{LC_p\,(1+2M)}+4\sqrt{2}f_s\sqrt{LC_p\,(1+2M)}-2M^2-3M-1}{(1+2M)\;(2M^2+2M+1)} \tag{A.4}$$

$$Q = \frac{2\left[\begin{array}{l}-4M^3-6M^2-2M+4PM^3+P+4PM+32C_pLf_s{}^2+6PM^2-8\sqrt{2}f_s\sqrt{LC_p(1+2M)}+64C_pLMf_s^2\\+64C_pLf_s^2M+128C_pLM^2f_s^2-16\sqrt{2}Mf_s\sqrt{LC_p(1+2M)}\end{array}\right]}{2M^2+2M+1} \tag{A.5}$$

$$\begin{aligned}R = {} & 4M^4+P^2-8PM^4+8M^3+4P^2M^4+4M^2-12PM^2+8P^2M^3-4PM+1024C_p{}^2L^2f_s{}^4+8P^2M^2\\ & +128C_pLf_s{}^2+4P^2M-16PM^3+4096C_p{}^2L^2Mf_s{}^4+256C_pLMf_s{}^2+64C_pLPf_s{}^2+4096C_p{}^2L^2M^2f_s{}^4\\ & -724C_pLf_s{}^3\sqrt{LC_p(1+2M)}-128C_pLM^2f_s{}^2+128C_pLMPf_s{}^2-128C_pLMf_s{}^2-256C_pLM^3f_s{}^2\\ & +32\sqrt{2}Mf_s\sqrt{LC_p(1+2M)}-256C_pLM^2f_s{}^2+128C_pLPM^2f_s{}^2+32\sqrt{2}M^2f_s\sqrt{LC_p(1+2M)}\\ & -1448C_pLMf_s{}^3\sqrt{LC_p(1+2M)}-32\sqrt{2}PMf_s\sqrt{LC_p(1+2M)}+256C_pLPM^3f_s{}^2+256C_pLM^2Pf_s{}^2\\ & -16\sqrt{2}Pf_s\sqrt{LC_p(1+2M)}-32\sqrt{2}LPM^2f_s\sqrt{LC_p(1+2M)}+128C_pLPMf_s{}^2\end{aligned} \tag{A.6}$$

REFERENCES

[1] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[2] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148–3172, Mar. 2020.

[3] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional DC-DC converter for power distribution in microgrid," *IEEE Trans. power Electron.*, vol. 27, no. 11, pp. 4667–4680, Nov. 2012.

[4] F. An, W. Song, K. Yang, S. Luo, and X. Feng, "Optimised power control and balance scheme for the output parallel dual-active-bridge DC-DC converters in power electronic traction transformer," *IET Power Electron.*, vol. 12, no. 9, pp. 2295–2303, Aug. 2019.

[5] H. Shi *et al.*, "Minimum-backflow-power scheme of dab-based solid-state transformer with extended-phase-shift control," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3483–3496, Jul./Aug. 2018.

[6] B. Zhao, Q. Song, W. Liu, and W. Sun, "Current-stress-optimized switching strategy of isolated bidirectional DC-DC converter with dual-phase-shift control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4458–4467, Oct. 2012.

[7] H. Wen and B. Su, "Reactive power and soft-switching capability analysis of dual-active-bridge DC-DC converters with dual-phase-shift control," *J. Power Electron.*, vol. 15, no. 1, pp. 18–30, 2015.

[8] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC-DC converter based on dual-phase-shift control for DC distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.

[9] N. Hou, W. Song, and M. Wu, "Minimum-current-stress scheme of dual active bridge DC-DC converter with unified phase-shift control," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8552–8561, Dec. 2016.

[10] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2009.

[11] W. Choi, K.-M. Rho, and B.-H. Cho, "Fundamental duty modulation of dual-active-bridge converter for wide-range operation," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4048–4064, Jun. 2015.

[12] H. Shi, H. Wen, Y. Hu, and L. Jiang, "Reactive power minimization in bidirectional DC-DC converters using a unified-phasor-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10990–11006, Dec. 2018.

[13] A. Tong *et al.*, "Power flow and inductor current analysis of PWM control for dual active bridge converter," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 1036–1041.

[14] A. Tong, L. Hang, G. Li, X. Jiang, and S. Gao, "Modeling and analysis of a dual-active-bridge-isolated bidirectional DC/DC converter to minimize RMS current with whole operating range," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5302–5316, Jun. 2018.

[15] S. Shao, M. Jiang, W. Ye, Y. Li, J. Zhang, and K. Sheng, "Optimal phase-shift control to minimize reactive power for a dual active bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10193–10205, Oct. 2019.

[16] Q. Gu, L. Yuan, J. Nie, J. Sun, and Z. Zhao, "Current stress minimization of dual-active-bridge DC-DC converter within the whole operating range," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 129–142, Mar. 2018.

[17] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.

[18] K. Shen *et al.*, "ZVS control strategy of dual active bridge DC/DC converter with triple-phase-shift modulation considering RMS current optimization," *J. Eng.*, vol. 2019, no. 18, pp. 4708–4712, 2019.

[19] J. Qiu, K. Shen, A. Tong, L. Hang, and J. Liao, "Unified ZVS strategy for dab with triple-phase-shift modulation in boost mode," *J. Eng.*, vol. 2019, no. 18, pp. 4906–4910, 2019.

[20] L. Zhou, Y. Gao, H. Ma, and P. T. Krein, "Wide-load range multi-objective efficiency optimization produces closed-form control solutions for dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8612–8616, Aug. 2021.

[21] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC-DC converter for high-frequency-link power-conversion system," *IEEE Trans. power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[22] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[23] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W.-K. Ling, and J. Lam, "Computer-aided design and optimization of high-efficiency LLC series resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3243–3256, Jul. 2012.

[24] J. Reinert, A. Brockmeyer, and R. W. De Doncker, "Calculation of losses in ferro-and ferrimagnetic materials based on the modified steinmetz equation," *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1055–1061, Jul./Aug. 2001.

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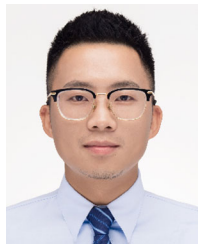

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