# An Improved Full-Bridge Converter With a Five-Diode Rectifier for High Efficiency in Wide Voltage Range

Yunqiu Zhu, Zhiqiang Guo, *Member, IEEE*, and Qingbo Geng

***Abstract*—This article presents an improved full-bridge converter with a five-diode rectifier. The primary side circuit is composed of a full bridge with two transformers and two split capacitors. On the secondary side, five diodes are employed in the rectifier stage. By using the asymmetrical pulse width modulation (PWM) signals, this converter can realize the zero-voltage switching (ZVS) of all switches and reduce the circulating current. The two transformers share the load power equally in whole load range. Compared with the other dual transformer isolated full-bridge converters, the transformers in the proposed converter are easy to optimize because of the load power equal sharing. Furthermore, the output filter inductance is reduced, which reduces the loss and volume. According to the loss analysis, the proposed converter has higher efficiency compared with some other dc-dc converters. The experimental results of a prototype with 300–400 V input voltage and 250 V/4 A output verify the performance of the proposed converter.**

***Index Terms*—Dual transformers, five-diode rectifier, reduced circulating current, reduced output filter inductance, zero voltage switching.**

## I. Introduction

THE CONVENTIONAL phase-shift full-bridge (PSFB) dc-dc converter, as shown in Fig. 1, is currently favored in medium and high power applications. PSFB converters have the characteristics of fixed frequency, simple structure, high power density, wide conversion ratio, and soft switching based on its parasitic parameters. However, the performance of the PSFB converter cannot meet high efficiency in the wide conversion ratio. In the case of light load or small resonant inductance, the lagging switches $Q_3$ and $Q_4$ will lose the ZVS, so the converter will work in hard switching conditions leading to power loss increment. Meanwhile, during the freewheeling period, there is large circulating current flowing through the switches in the primary side, resulting in more conduction loss. The circulating current loss is especially considerable in high current and low duty cycle cases. For small duty cycle situations, the output current ripple is increased. To reduce the output current ripple, a large output filter inductance is necessary.

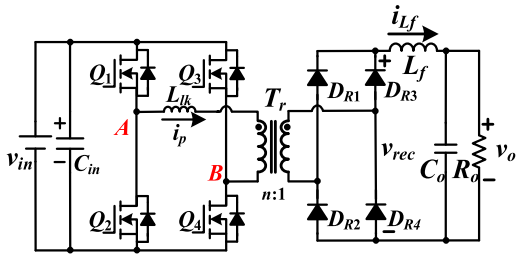


Fig. 1. Conventional PSFB converter.

The reason for losing the ZVS of the lagging switches under light load is the insufficient energy store in the resonant inductance. Therefore, the main idea to solve this issue is to add auxiliary resonant components or circuits. Increasing the leakage inductance of the transformer [1] or adding an external series inductance [2] can provide extra energy for the ZVS of lagging switches. A saturable inductor can be added in the primary side [3] or the secondary side [4]. In [5], a coupled inductor on the primary side is employed. Furthermore, *LC* network [6] and *LLC* circuit [7] can also be integrated into the traditional PSFB converter. With these auxiliary resonant components or circuits, the entire ZVS of lagging switches can be guaranteed. However, the addition of redundant resonant components will lead to more duty cycle loss and increase the voltage stress on the rectifier stage. Some other improved PSFB converters with auxiliary circuits are also proposed to extend the ZVS range [8]–[10]. The current in the auxiliary circuit is decreased with the increase of the load power. The narrow ZVS range of the lagging switches is extended with lower conduction loss in the auxiliary circuit.

To reduce the circulating current, the zero-voltage zero-current switching (ZVZCS) full-bridge converter schemes are proposed [11]–[13]. In the ZVZCS full-bridge converters, MOSFETs for ZVS are applied in the leading switches, and insulated gate bipolar transistors (IGBTs) for ZCS are applied in the lagging switches. Based on the above work, more ZVZCS converters are proposed in [14]–[16]. However, due to the existence of IGBTs, the switching frequency of the ZVZCS converters cannot be very high, causing difficulty in the optimization of

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The authors are with the School of Automation, Beijing Institute of Technology, Beijing 100081, China (e-mail: zyq0514@126.com; guozq32@bit.edu.cn; kingboy@bit.edu.cn).

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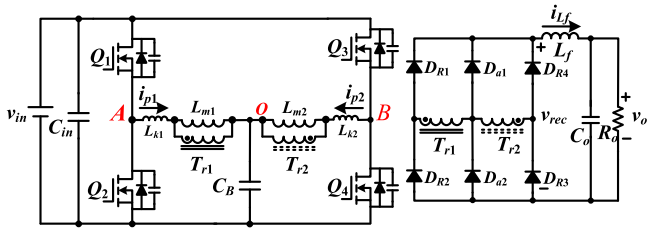


Fig. 2. Topology of the proposed converter in [19].

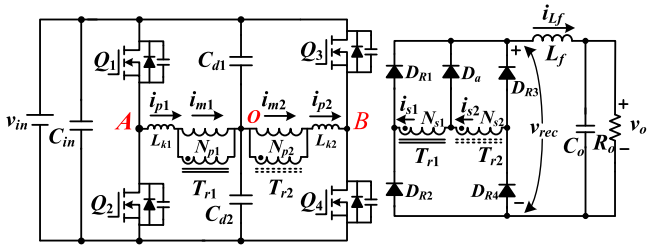


Fig. 3. Proposed IFB-5R stage.

magnetic components. In [17], a full-bridge converter with a new coupled inductor rectifier is proposed to reduce the circulating current, and the magnetizing inductor current is designed large enough to charge and discharge the junction capacitors of the lagging switches for ZVS. However, the magnetizing inductor current will cause more conduction loss, especially in a wide conversion ratio. The isolated series capacitor-based full-bridge converter with a simple auxiliary circuit is proposed [18]. By employing the pulsewidth modulated scheme, the circulating current is reduced. However, some switches still work in hard switching. The dual transformer scheme [19]–[21] can also extend the ZVS range and reduce the circulating current and output current ripple. Fig. 2 shows the converter with two transformers, in which the magnetizing inductor current is used for ZVS of the lagging switches [19]. However, controlled by the phase-shifted method, it cannot achieve equal power-sharing between the two transformers. The conversion ratio of the converter in [19] cannot reach down to zero, leading to poor wide voltage regulation capacity. Meanwhile, the control loop cannot limit the load current during the output short circuit situation. In [22], a new PSFB converter using a center-tapped clamp circuit is presented. The clamp circuit is composed of two diodes and one capacitor. The magnetizing current is necessary for the ZVS of the lagging switches. When the converter works in a wide conversion ratio, especially in the low duty cycle condition, the magnetizing current amplitude is very low. Therefore, the lagging switches may still work in hard switching. A modified PSFB converter with a low freewheeling period for the wide conversion ratio is proposed in [23]. The converter can be regarded as two converters in parallel or series connection. The configurable interconnection structures can handle the wide voltage conversion ratio and wide load range. A full-bridge converter with an auxiliary coupling inductor can achieve ZVS for all the switches [24]. However, the auxiliary inductor still causes more conduction loss.

According to the previous works, the ZVZCS full-bridge converter can reduce the circulating current with the loss of the ZVS performance. The magnetizing inductor current should be designed large enough for the ZVS in lagging switches, but it will cause more conduction loss especially in a wide conversion ratio. Using the two transformers integrated into the full-bridge converter, the circulating current can be reduced, and the ZVS in the lagging switches can be achieved by using the magnetizing inductor current. However, the two transformers cannot share the load power equally. It cannot optimize the volume of the transformers. To improve the demerits of the previous works, this article presents an improved full-bridge converter with two transformers and a five-diode rectifier stage. Using the asymmetric PWM controlled method, the proposed converter has the following merits.

1) The circulating current in the primary circuit is reduced, so the conduction loss in the switches and the copper loss in the transformers are reduced.
2) Although the circulating current is reduced, all the switches still meet the ZVS constraint without the auxiliary circuit.
3) Two transformers can share the load power equally during the whole load range. Therefore, the volume and design of the transformers can be easily optimized.
4) For the same output current ripple, the output filter inductance is reduced. Compared with PSFB converters, a smaller core and a small number of turns are selected to fabricate the inductor. Therefore, the loss of the output filter inductor is reduced.

The article is organized as follows. Section II introduces the topology and working modes of the proposed converter. Section III gives the design guidelines of the key parameters. The performance is analyzed in Section IV. Section V gives the experimental results for the prototype with 300–400 V input voltage and 250 V/4 A output. Finally, Section VI concludes this article.

## II. Operation Modes

Fig. 3 shows the circuit of the proposed isolated full-bridge converter with a five-diode rectifier (IFB-5R). Compared to the conventional PSFB converter, two transformers and two split capacitors are added in the primary side of the circuit. In the secondary side, the rectifier stage consists of five diodes and the secondary windings of the transformers. To facilitate the following analysis of the proposed converter, some components and parameters are assumed as follows.

1) The split capacitors $C_{d1}$ and $C_{d2}$ are large enough to be regarded as constant voltage sources during the steady-state operation.
2) $C_1$–$C_4$ are the parasitic capacitors of the switches. The capacity of all parasitic capacitors is the same and equal to $C$.
3) The turns ratio of the two transformers are the same, and the turns ratio is defined as $n = N_{s1}/N_{p1} = N_{s2}/N_{p2}$.

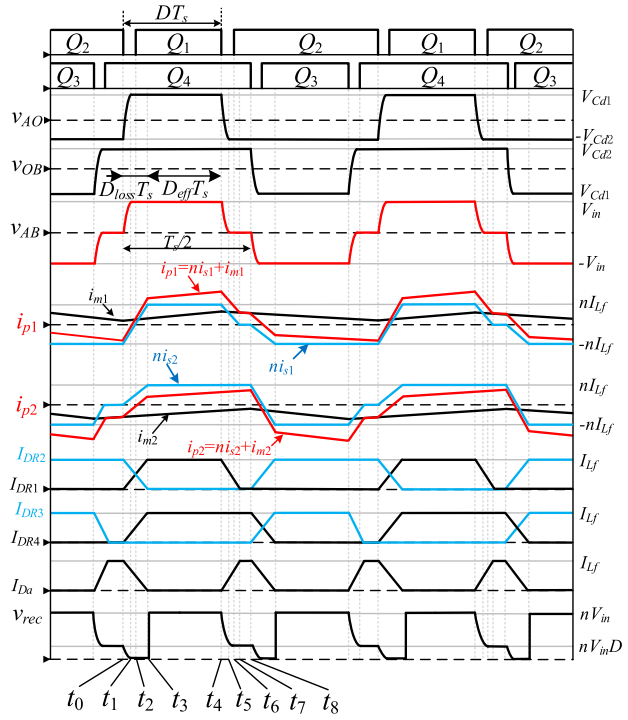


Fig. 4. Key waveforms of the isolated full-bridge converter with five-diode rectifier.

$L_{m1}$ and $L_{m2}$ are the magnetizing inductance of the transformer, where $L_{m1} = L_{m2} = L_m$. $i_{m1}$ and $i_{m2}$ are the magnetizing inductor current in the transformers.

4) The output filter inductance $L_f$ is large enough to be regarded as a constant current source. The average output filter inductor current is $I_{Lf}$.
5) The output capacitor $C_o$ is large enough so that the output voltage keeps constant.

Controlled by the asymmetric PWM signals, the turn-ON time of $Q_1$ and $Q_3$ is equal. For the IFB-5R converter, the output voltage is regulated by the duty cycle $D$. $D$ is defined as the duty cycle of $Q_1$ and $Q_3$, and $D \leq 0.5$. $D_{\text{eff}}$ is the effective duty cycle, and $D_{\text{loss}}$ is the duty cycle loss, where $D = D_{\text{eff}} + D_{loss}$. Fig. 4 shows the key waveforms of the IFB-5R converter when working in a steady state. $v_{\text{rec}}$ is the output voltage of the rectifier stage. Because of the symmetry of the circuit working modes, the working stages of the proposed IFB-5R converter during a switching period can be divided into two half cycles. Fig. 5 shows the detailed working modes in a half cycle from $t_0$ to $t_8$.

*Mode 1([$t_0$, $t_1$]) [Fig. 5(a)]:* Before $t_0$, $i_{p1}$ is the primary winding current of $T_{r1}$, and it is negative. $i_{p2}$ is the primary winding current of $T_{r2}$, and it is equal to the magnetizing current $i_{m2}$. $D_{R2}$ and $D_a$ are conducted for the output filter current $i_{Lf}$. Mode 1 begins when $Q_2$ is turned OFF at $t_0$. On the primary side, the parasitic capacitor of $Q_1$ is discharged and the parasitic capacitor of $Q_2$ is charged by the energy stored in the leakage inductance $L_{k1}$. $v_{AO}$ increases from $-V_{Cd2}$ to $V_{Cd1}$, and $v_{OB}$ keeps constant at $V_{Cd2}$, where $V_{cd1}$ and $V_{cd2}$ are the quiescent voltage across split capacitors $C_{d1}$ and $C_{d2}$, and $V_{\text{in}}$ is the quiescent value of the input voltage. Therefore, $v_{AB}$ is increased from zero to $V_{\text{in}}$. In the rectifier stage, the current flowing through $D_{R2}$ and $D_a$ is decreasing, and the current flowing through $D_{R4}$ and $D_{R1}$ is increasing. Therefore, $i_{p1}$ starts to increase from a negative current, and $i_{p2}$ starts to increase from the magnetic current $i_{m2}$.

*Mode 2([$t_1$, $t_2$]) [Fig. 5(b)]:* Mode 2 begins at $t_1$ when the voltage across the parasitic capacitor of $Q_1$ is discharged to zero. Therefore, $i_{p1}$ flows through the body diode of $Q_1$. Because $i_{DR2}$ and $i_{Da}$ have not dropped to zero, the current of the rectifier stage works the same as Mode 1. $i_{p1}$ and $i_{p2}$ are still increasing. In this stage, $i_{p1}$ and $i_{p2}$ are expressed as

$$\begin{cases} i_{p1}(t) = i_{p1}(t_1) + \frac{V_{cd1}}{L_k}(t - t_1) \\ i_{p2}(t) = i_{p2}(t_1) + \frac{V_{cd2}}{L_k}(t - t_1). \end{cases} \tag{1}$$

*Mode 3([$t_2$, $t_3$]) [Fig. 5(c)]:* Mode 3 begins at $t_2$ when $Q_1$ is turned ON with ZVS. $i_{DR2}$ and $i_{Da}$ are still larger than zero, so the proposed IFB-5R converter works similarly to Mode 2. $i_{p1}$ and $i_{p2}$ are also expressed in (1).

*Mode 4([$t_3$, $t_4$]) [Fig. 5(d)]:* Mode 4 begins at $t_3$ when the secondary winding currents of $T_{r1}$ and $T_{r2}$ are both equal to $i_{Lf}$. In the rectifier stage, only $D_{R1}$ and $D_{R4}$ are conducted for the output filter inductance current $i_{Lf}$. In this stage, the two transformers transmit power to the load simultaneously. In this stage, $i_{p1}$ and $i_{p2}$ are expressed as follows:

$$\begin{cases} i_{p1}(t) = nI_{Lf} + i_{m1} = nI_{Lf} + i_{m1}(t_3) + \frac{V_{cd1}}{L_m}(t - t_3) \\ i_{p2}(t) = nI_{Lf} + i_{m2} = nI_{Lf} + i_{m2}(t_3) + \frac{V_{cd2}}{L_m}(t - t_3). \end{cases} \tag{2}$$

*Mode 5([$t_4$, $t_5$]) [Fig. 5(e)]:* Mode 5 begins at $t_4$ when $Q_1$ is turned OFF. On the primary side, the parasitic capacitor of $Q_1$ is charged and the parasitic capacitor of $Q_2$ is discharged by the energy stored in the output filter inductance $L_f$. $v_{AO}$ decreases from $V_{Cd1}$ to $-V_{Cd2}$, and $v_{OB}$ still keeps at $V_{Cd2}$. Therefore, $v_{AB}$ is reduced from $V_{\text{in}}$ to zero. In the rectifier stage, $D_a$ starts to be conducted. $i_{DR4}$ keeps equal to $i_{Lf}$, so the secondary winding current of $T_{r2}$ keeps constant. The current flowing through $D_{R1}$ decreases and the current flowing through $D_a$ increases. Therefore, $i_{p1}$ starts to decrease and $i_{p2}$ still maintains $i_{p2} = i_{m2} + nI_{Lf}$.

*Mode 6([$t_5$, $t_6$]) [Fig. 5(f)]:* Mode 6 begins at $t_5$ when the voltage across the parasitic capacitor of $Q_2$ is discharged to zero. Therefore, $i_{p1}$ flows through the body diode of $Q_2$. Because $i_{DR1}$ has not dropped to zero, the current of the rectifier stage works the same as Mode 5. $i_{p1}$ is still decreasing and $i_{p2}$ still meets $i_{p2} = i_{m2} + ni_{Lf}$. $i_{p1}$ and $i_{p2}$ are expressed as follows:

$$\begin{cases} i_{p1}(t) = i_{p1}(t_5) - \frac{V_{cd2}}{L_k}(t - t_5) \\ i_{p2}(t) = nI_{Lf} + i_{m2} = nI_{Lf} + i_{m2}(t_3) + \frac{V_{cd2}}{L_m}(t - t_3). \end{cases} \tag{3}$$

*Mode 7([$t_6$, $t_7$]) [Fig. 5(g)]:* Mode 7 begins at $t_6$ when $Q_2$ is turned ON with ZVS. $i_{DR1}$ is still larger than zero, so this working mode works similarly to Mode 6. $i_{p1}$ and $i_{p2}$ are also expressed in (3).

*Mode 8([$t_7$, $t_8$]) [Fig. 5(h)]:* Mode 8 begins at $t_7$ when the secondary winding current of $T_{r1}$ is dropped to zero. Therefore,

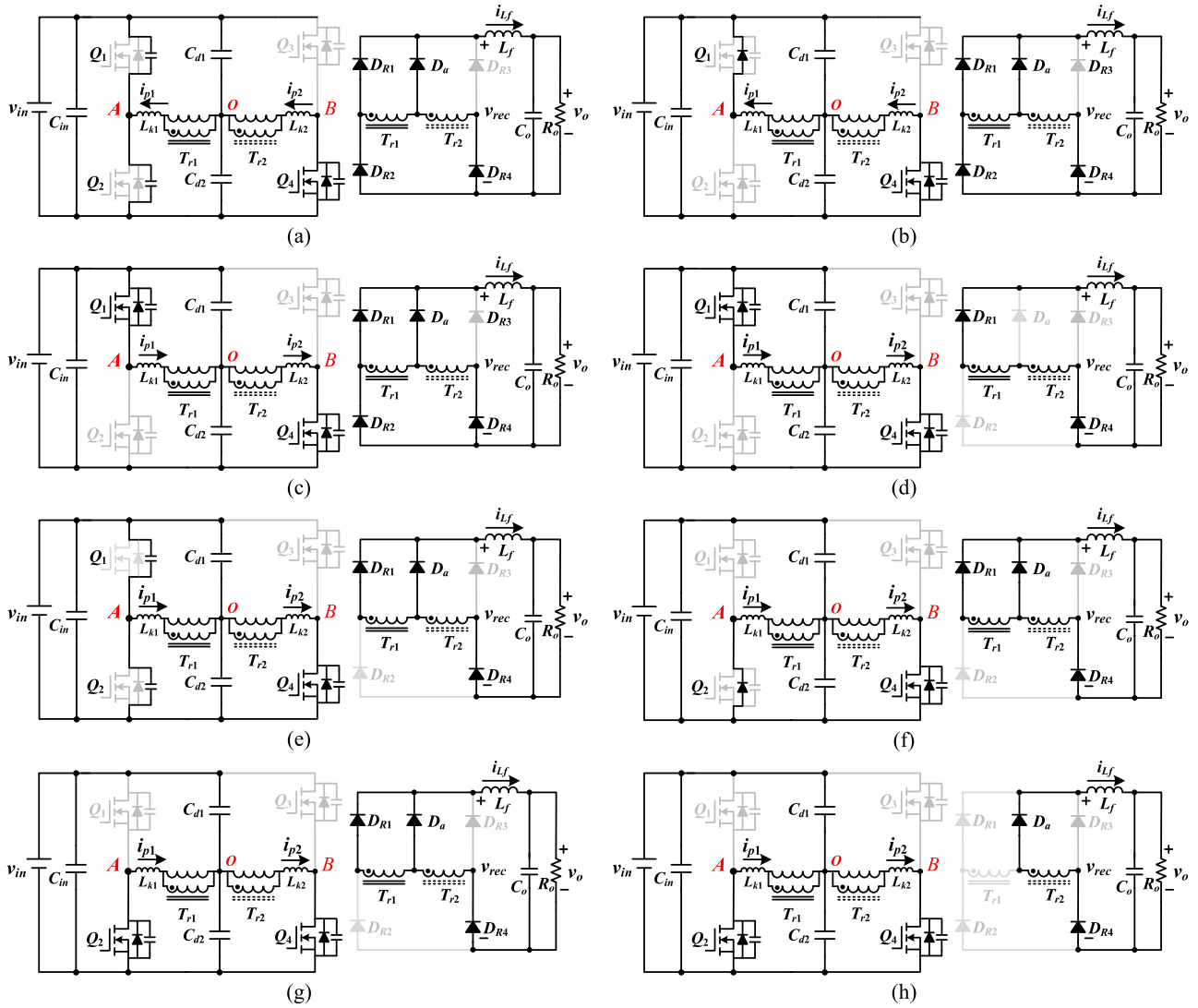


Fig. 5. Working modes of the proposed IFB-5R converter. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$. (c) $[t_2, t_3]$. (d) $[t_3, t_4]$. (e) $[t_4, t_5]$. (f) $[t_5, t_6]$. (g) $[t_6, t_7]$. (h) $[t_7, t_8]$.

there are only $D_a$ and $D_{R4}$ conducted for the output filter inductance current. In this mode, $i_{p1}$ is reduced to the magnetic current $i_{m1}$. $T_{r1}$ does not transmit power, and the power is transmitted from the input to the output only through $T_{r2}$. $i_{p1}$ and $i_{p2}$ are expressed as follows:

$$\begin{cases} i_{p1}(t) = i_{p1}(t_7) - \frac{V_{cd2}}{L_m + L_k}(t - t_7) \\ i_{p2}(t) = nI_{Lf} + i_{m2} = nI_{Lf} + i_{m2}(t_3) + \frac{V_{cd2}}{L_m}(t - t_3). \end{cases} \tag{4}$$

Mode 1 to Mode 8 is half of the switching cycle. Due to the symmetry of the working modes, in the next half of the switching cycle, the circuit working modes are similar to the above working stages.

## III. Design Guidelines

In this article, the design specification is the 300–400 V input voltage and 250 V/4 A output. To demonstrate the performance of the proposed converter, the IFB-5R converter is compared with the conventional PSFB converter and the converter in [19].

### A. Voltage Across the Split Capacitors

The voltage across the split capacitors determines the voltage of the primary windings of the transformers, which shows as the waveforms of $v_{AO}$ and $v_{OB}$ in Fig. 4. In the proposed IFB-5R converter circuit, the voltage across the split capacitors meets the following:

$$V_{Cd1} + V_{Cd2} = V_{\text{in}}. \tag{5}$$

In the steady state, the voltage across the magnetic inductor should meet the voltage-second balance in a switching period. Taking $T_{r1}$ for example, the following equation can be obtained:

$$V_{Cd1} D T_s - V_{Cd2}(1 - D) T_s = 0. \tag{6}$$

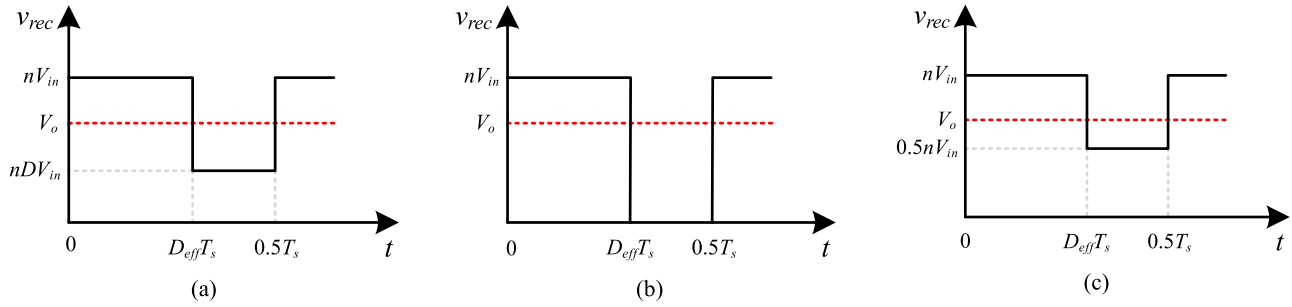


Fig. 6. Ideal rectifier stage output voltage. (a) IFB-5R converter. (b) PSFB converter. (c) Converter in [19].

Derived from (5) and (6), the voltage across the two split capacitors $C_{d1}$ and $C_{d2}$ are expressed as follows:

$$\begin{cases} V_{Cd1} = V_{\text{in}}\,(1-D) \\ V_{Cd2} = V_{\text{in}} D. \end{cases} \tag{7}$$

In the steady state, the voltage across the split capacitors are determined by the input voltage $V_{\text{in}}$ and duty cycle $D$. Because of $D \leq 0.5$, $V_{Cd1}$ is larger than $V_{Cd2}$. The voltage across the two split capacitors is not equal. It illustrates the asymmetrical waveforms of $v_{AO}$ and $v_{OB}$ in Fig. 4. Although $v_{AO}$ and $v_{OB}$ are asymmetric in the proposed IFB-5R converter, the voltage across the midpoints of full-bridge $v_{AB}$ is the same as that in the conventional PSFB converter.

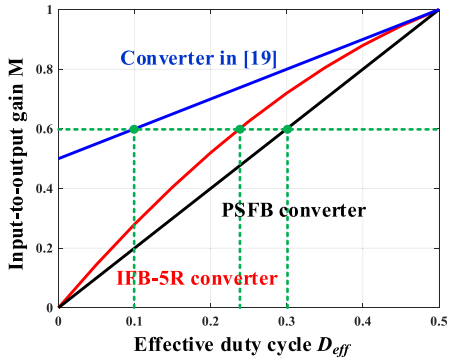


Fig. 7. Input-to-output gain versus the effective duty cycle when $n = 1$.

### B. Input-to-Output Gain

The conversion ratio is associated with the effective duty cycle. Ignoring the duty cycle loss, the ideal output voltage of the rectifier stage $v_{\text{rec}}$ in IFB-5R converter is shown in Fig. 6(a). The average voltage of $v_{\text{rec}}$ is the output voltage $V_o$, where $V_o$ is the quiescent value of the output voltage. Ignoring the duty cycle loss, the constraint is derived as the following equation:

$$0.5T_s V_o = D_{\text{eff}} T_s n V_{\text{in}} + (0.5T_s - D_{\text{eff}} T_s)\, n D_{\text{eff}} V_{\text{in}}. \tag{8}$$

The input-to-output gain can be gotten as follows:

$$M_{\text{IFB}-5R} = \frac{V_o}{V_{\text{in}}} = n\left(3D_{\text{eff}} - 2{D_{\text{eff}}}^2\right). \tag{9}$$

Fig. 6(b) gives the rectifier output voltage of the PSFB converter. Derived in the same way, the input-to-output gain of the PSFB converter is as follows:

$$M_{\text{PSFB}} = \frac{V_o}{V_{\text{in}}} = 2nD_{\text{eff}}. \tag{10}$$

Fig. 6(c) gives the rectifier output voltage of the converter in [19]. The input-to-output gain can be derived as

$$M_{[19]} = \frac{V_o}{V_{\text{in}}} = n\,(D_{\text{eff}} + 0.5). \tag{11}$$

Fig. 7 shows the input-to-output gain of the PSFB, the converter in [19], and the proposed IFB-5R converters versus the effective duty cycle when $n = 1$. When the duty cycle is equal to zero, the input-to-output gain of the converter in [19] is greater than zero. Thus, the converter in [19] cannot achieve wide output voltage regulation, which demonstrates that it cannot meet the short circuit condition. The minimum and maximum input-to-output gain of the proposed IFB-5R converter is the same as the PSFB converter, which indicates that the proposed IFB-5R converter also has a wide voltage conversion capacity.

Equation (12) gives the design guidelines of the turns ratio of the transformers in the proposed IFB-5R converter. For constant output voltage, the turns ratio is designed to meet the minimum input voltage and maximum duty cycle. The maximum effective duty cycle is designed as 0.4. For the specification of $V_{\text{in}} =$ 300–400 V, $V_o = 250$ V, the turns ratio of the transformers is designed as 0.94

$$n = \frac{V_o}{V_{\text{in\_min}}\,(3D_{\max} - 2D_{\max}^2)}. \tag{12}$$

### C. Magnetizing Current

If the magnetizing current is ignored, the primary winding current is shown as $ni_{s1}$ and $ni_{s2}$ in Fig. 4. $ni_{s1}$ and $ni_{s2}$ cannot make the transformers meet charge and discharge balance. Therefore, to keep the charge and discharge balance, the magnetizing current is the key component in the converter.

Considering the primary winding current in $T_{r1}$ and ignoring the duty cycle loss, the charge and discharge balance can be written as

$$DT_s \cdot nI_{Lf} + \frac{1}{2}T_s I_{m1} = \frac{1}{2}T_s \cdot nI_{Lf} - \frac{1}{2}T_s I_{m1} \tag{13}$$

where $I_{m1}$ is the average magnetic current of $T_{r1}$. Simplifying this equation, the average magnetic current of $T_{r1}$ gives as follows:

$$I_{m1}=\left(\frac{1}{2}-D\right)nI_{Lf}. \tag{14}$$

According to the symmetry, the magnetic current of $T_{r2}$ is

$$I_{m2}=\left(D-\frac{1}{2}\right)nI_{Lf}. \tag{15}$$

As analyzed in Mode 8, the circulating current in $T_{r1}$ is reduced to the magnetic current during the freewheeling period. In Fig. 7, the duty cycle $D$ is reduced with the increase of the input voltage. Therefore, for the IFB-5R converter, the maximum circulating current occurs when the input voltage and load power are maximum. For the specification of $V_{\rm in}=400$ V, $V_o=250$ V, $n=0.94$, and $P_{\rm max}=1$ kW, ignoring the magnetic current ripple, the average circulating current in the proposed IFB-5R converter during a switching period is 0.714 A. The circulating current in the PSFB converter during the switching period is at least 4 A. Therefore, the circulating current is greatly reduced. To avoid the saturation of the transformers, there are air gaps in the transformers of the IFB-5R converter.

### D. ZVS Conditions

As described in Mode 5, the parasitic capacitors are charged and discharged to achieve the ZVS for $Q_2$ and $Q_4$. In this stage, the switch parasitic capacitor is fully discharged by the primary current in the primary winding of the transformers. The ZVS condition of $Q_2$ and $Q_4$ is associated with the energy reflected from the output filter inductance and the energy stored in the leakage inductor. It is expressed as

$$\frac{1}{2}\left(L_{k1}+\frac{L_f}{n^2}\right)(ni_{s1}+i_{m1})^2\geq\frac{1}{2}(2C)V_{\rm in}^2. \tag{16}$$

Because the output filter inductance $L_f$ is very large and the parasitic capacitor $C$ is small, it is easy to realize the ZVS of $Q_2$ and $Q_4$.

As described in Mode 1, the parasitic capacitors are charged and discharged to achieve the ZVS for $Q_1$ and $Q_3$. In this stage, the switch parasitic capacitor should be fully discharged by the energy stored in the leakage inductor. In the view of energy, the ZVS constraint is expressed as

$$\frac{1}{2}L_{k1}(ni_{s1}-I_{m1})^2\geq\frac{1}{2}(2C)V_{\rm in}^2. \tag{17}$$

Submitting (14) into (17), the leakage inductance is determined as follows:

$$L_k\geq\frac{2CV_{\rm in}^2}{[(0.5+D)nI_{Lf}]^2}. \tag{18}$$

In the proposed IFB-5R converter, the leakage inductance of the transformers is designed by the maximum input voltage and 30% load power. The value of the leakage inductance is calculated as 15.3 $\mu$H. The leakage inductor is the intrinsic parameter of the transformer. If the transformer has no air gap, the leakage inductor is very low. The air gap is used to adjust the leakage inductance of the transformer. In Section II-C, the dc bias current in the magnetizing inductor current is used to keep the charge balance in the primary winding current in the transformer. To avoid the saturation of the transformer with the dc bias current in the magnetizing inductor current and adjust the leakage inductance, the air gap is necessary.

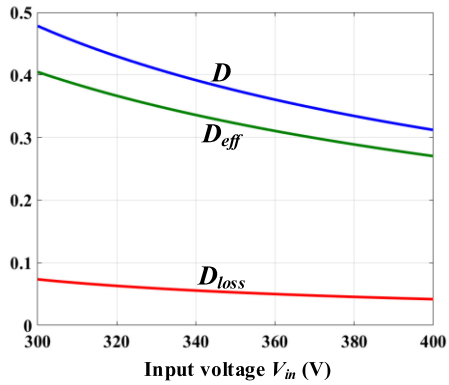


Fig. 8. Duty cycle versus the input voltage.

### E. Duty Cycle Loss Analysis

As seen in Fig. 4, the duty cycle loss $D_{\rm loss}$ is associated with the leakage inductor and the input voltage. Considering the duty cycle loss, $V_{cd1}$ is expressed as follows:

$$V_{cd1}=V_{\rm in}(1-D)=V_{\rm in}(1-D_{\rm eff}-D_{\rm loss}). \tag{19}$$

Equation (20) is satisfied during the duty cycle loss interval. Therefore, the duty cycle loss is expressed in (21). The curves of the duty cycle versus the input voltage are shown in Fig. 8, where $V_o=250$, $I_{Lf}=4$ A, $n=0.94$, and $L_k=15.3$ $\mu$H. The duty cycle loss is decreased with the increase of the input voltage. Considering the duty cycle loss, the duty cycle $D$ is still less than 0.5 for 300–400 V input voltage, which demonstrates the validity of the transformer design

$$L_r\frac{di_{p1}}{dt}=V_{cd1}\Rightarrow L_r\frac{2nI_{Lf}}{D_{\rm loss}T_s}=V_{\rm in}(1-D_{\rm eff}-D_{\rm loss}) \tag{20}$$

$$D_{\rm loss}=\frac{(1-D_{\rm eff})-\sqrt{(1-D_{\rm eff})^2-\frac{8nL_rI_{Lf}}{V_{\rm in}T_s}}}{2}. \tag{21}$$

### F. Output Filter Inductance Condition

The output current ripple is determined by the voltage across the output filter inductance. Fig. 6 in Section II-B has given the ideal output voltage of the rectifier stage in PSFB, IFB-5R, and converter in [19]. The voltage across the output filter inductance is expressed as

$$v_L=L_f\frac{di}{dt}=v_{\rm rec}-V_o. \tag{22}$$

According to (18), the output filter inductance current ripple of the IFB-5R converter, PSFB converter, and converter in [19]

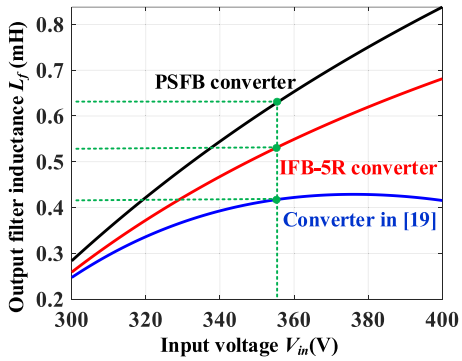


Fig. 9. Output filter inductance versus the input voltage.

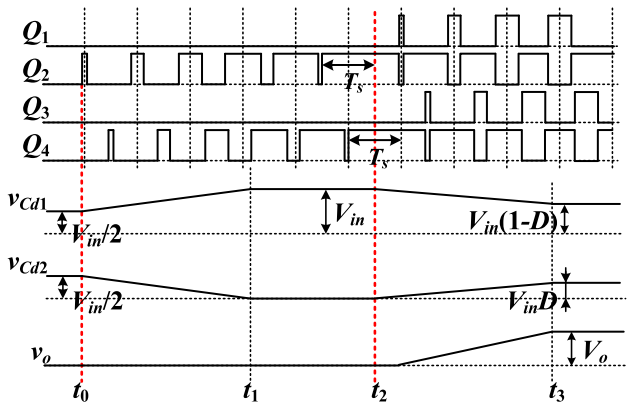


Fig. 10. Waveforms during the soft start-up.

can be uniformly expressed as

$$\Delta i = \frac{nV_{\rm in} - V_o}{L_f} DT_s. \tag{23}$$

For the same required current ripple, the output filter inductance capacity is associated with the duty cycle. In Fig. 7, for the same input and output voltage, the duty cycle relationship of the three converters is

$$D_{[19]} < D_{IFB-5R} < D_{\rm PSFB}. \tag{24}$$

Therefore, for the same current ripple, the output filter inductance meets the following qualitative relationship:

$$L_{f\_[19]} < L_{f\_{\rm IFB-5R}} < L_{f\_{\rm PSFB}}. \tag{25}$$

Introducing the expression of the duty cycle $D$, the output filter inductance of three converters can be obtained as

$$\begin{cases} L_{f\_{\rm IFB-5R}} = \frac{(nV_{\rm in}-V_o)T_s}{\Delta i} \frac{3-\sqrt{9-\frac{8V_o}{nV_{\rm in}}}}{4} \\ L_{f\_{\rm PSFB}} = \frac{(nV_{\rm in}-V_o)T_s}{\Delta i} \frac{V_o}{2nV_{\rm in}} \\ L_{f\_[19]} = \frac{(nV_{\rm in}-V_o)T_s}{\Delta i} \left(\frac{V_o}{nV_{\rm in}} - 0.5\right). \end{cases} \tag{26}$$

Fig. 9 shows the relationship of the output filter inductance versus the input voltage when the filter inductor current ripple is selected as $\Delta i = 0.5$ A. As seen, compared with the PSFB converter, the output filter inductance is reduced in the proposed IFB-5R converter. The output filter inductance in the IFB-5R converter is designed as 0.6 mH in the prototype.

### G. Soft Start-Up Strategy

Fig. 10 shows the key waveforms during the soft start-up. The initial voltages of the input split capacitors are equally shared with the input voltage before the start-up. To achieve soft start-up, the duty cycle of the converter should be gradually increased from zero. To meet the voltage-second balance of the voltage waveforms during the soft start-up procedure, the voltage of $C_{d2}$ should be discharged to zero before the soft start-up. In Fig. 10, the duty cycle of $Q_2$ and $Q_4$ are increased gradually at $t_0$, and $Q_1$ and $Q_3$ are turned OFF during this interval. $C_{d2}$ is discharged, and $C_{d1}$ is charged. At $t_1$, $v_{Cd2}$ reaches zero, and $v_{Cd1}$ reaches $V_{\rm in}$. At this time, the duty cycle of $Q_2$ and $Q_4$ is still not equal to one, so it continues to increase. At $t_2$, the duty cycle of $Q_2$ and $Q_4$ is equal to one. After $t_2$, the duty cycle of $Q_1$ and $Q_3$ starts to increase from zero, and the duty cycle of $Q_2$ and $Q_4$ starts to decrease from one. The voltages of the input split capacitors are varied with the duty cycle of the converter. The output voltage is also increased with the increase of the duty cycle. At $t_3$, the output voltage reaches the voltage reference, and the soft start-up procedure is finished.

## IV. Performance Analysis

### A. Switch Conduction Loss

In the proposed IFB-5R converter, the circulating current in $T_{r1}$ is reduced to the magnetic current $i_{m1}$ in Mode 8. In the other half switching period, the circulating current in $T_{r2}$ is also reduced to $i_{m2}$.

Fig. 11 shows the key voltage and current waveforms in the IFB-5R converter, PSFB converter, and converter in [19].

For the proposed IFB-5R converter, according to the current waveforms in Fig. 11(a), the root mean square (rms) currents of $Q_1$ and $Q_3$ are the same, and the rms currents of $Q_2$ and $Q_4$ are the same. Therefore, the rms current of the switches is calculated as

$$\begin{cases} I_{\rm IFB\text{–}5R\_Q_1\&Q_3} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{Q1}^2 dt} = \sqrt{\frac{1}{T_s}\int_0^{DT_s} i_{p1}^2 dt} \\ I_{\rm IFB\text{–}5R\_Q_2\&Q_4} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{Q2}^2 dt} = \sqrt{\frac{1}{T_s}\int_{DT_s}^{T_s} i_{p1}^2 dt}. \end{cases} \tag{27}$$

For the conventional PSFB converter, according to the current waveforms in Fig. 11(b), the four switches have the same rms current. Therefore, the switch rms current is expressed as

$$I_{\rm PSFB\_Q_1-Q_4} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{Q1}^2 dt} = \sqrt{\frac{1}{T_s}\int_0^{0.5T_s} i_p^2 dt}. \tag{28}$$

For the converter in [19], according to the current waveforms in Fig. 11(c), the rms currents of $Q_1$ and $Q_2$ are the same, and the rms currents of $Q_3$ and $Q_4$ are the same. To achieve the ZVS of $Q_1$ and $Q_2$, the magnetizing current should be designed large enough to charge and discharge the junction capacitors. Therefore, the magnetizing current will cause more conduction

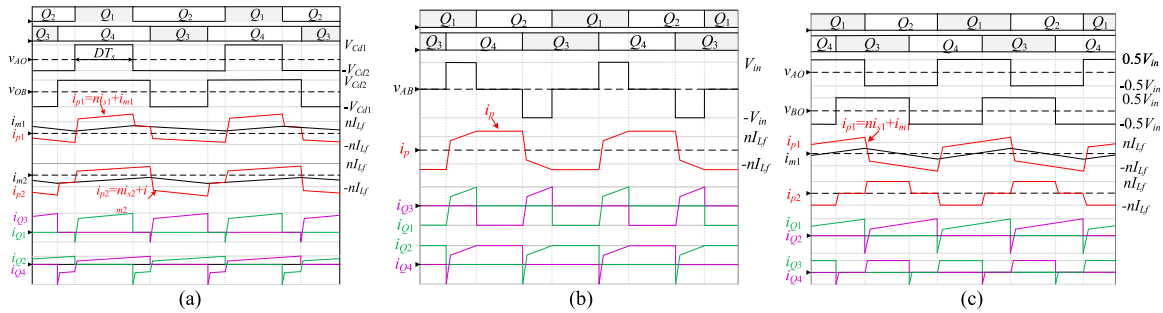


Fig. 11. Key voltage and current in three converters. (a) IFB-5R converter. (b) PSFB converter. (c) Converter in [19].

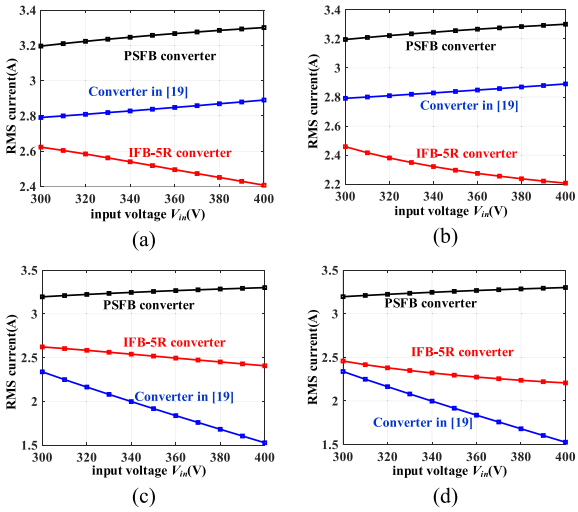


Fig. 12. Switch current versus the input voltage. (a) Q1. (b) Q2. (c) Q3. (d) Q4.

loss. The rms current of the switches is expressed as

$$\begin{cases} I_{[19]\_Q_1\&Q_2} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{Q1}^2 dt} = \sqrt{\frac{1}{T_s}\int_0^{0.5T_s} i_{p1}^2 dt} \\ I_{[19]\_Q_3\&Q_4} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{Q3}^2 dt} = \sqrt{\frac{1}{T_s}\int_0^{DT_s} i_{p2}^2 dt}. \end{cases} \tag{29}$$

Fig. 12 shows the curves of the switch rms currents versus the input voltage for the rated output of 250 V/4 A. As seen, the rms currents of all switches in the IFB-5R converter are less than that of the PSFB converter. Compared with the converter in [19], the rms current of $Q_1$ and $Q_2$ in the IFB-5R converter is smaller, and the rms current of $Q_3$ and $Q_4$ is larger.

The conduction loss of the switches can be calculated according to the following formula:

$$P_{\text{con\_loss}} = \sum_{i=1}^{4} I_{Qi}^2 R_{Qi} \tag{30}$$

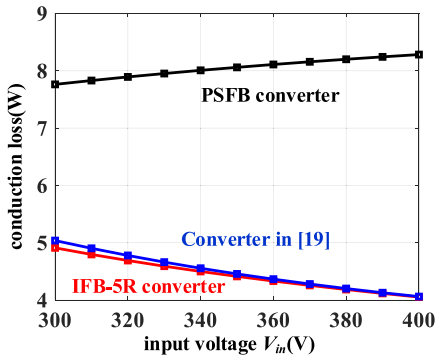


Fig. 13. Switch conduction loss in three converters.

where $R_{Qi}$ is the turn-ON resistance of the switches.

The switch conduction loss versus the input voltage in three converters is plotted in Fig. 13, which is based on the same turns ratio of the transformer. Large duty cycle causes a low freewheeling period. As seen in Fig. 7, the three converters have the same maximum voltage gain. The turns ratio of the transformer in the PSFB and the converter in [19] is also selected the same as that in the proposed converter. In this case, the three converters can nearly reach the maximum duty cycle in the minimum input voltage. In this case, all three converters are designed in the optimized condition. With 300–400 V input voltage, the proposed IFB-5R converter has the lowest switch conduction loss. The circulating current is reduced and the switch conduction loss is also reduced.

### *B. Power-Sharing Between Transformers*

The load power distributed between two transformers in the IFB-5R converter and converter in [19] is considered.

$$\begin{cases} P_{Tr1\_\text{IFB}-5R} = \frac{1}{T_s}\int_0^{T_s} n i_{s1} v_{AO} dt = \frac{1}{T_s}\left[\int_0^{DT_s} nI_{Lf} V_{Cd1} dt + \int_{0.5T_s}^{T_s} (-nI_{Lf})(-V_{Cd2})\, dt\right] \\ \quad = nI_{Lf}\left(DV_{Cd1} + 0.5V_{Cd2}\right) \\ P_{Tr2\_\text{IFB}-5R} = \frac{1}{T_s}\int_0^{T_s} n i_{s2} v_{OB} dt = \frac{1}{T_s}\left[\int_0^{0.5T_s} nI_{Lf} V_{Cd2} dt + \int_{0.5T_s}^{(0.5+D)T_s} (-nI_{Lf})(-V_{Cd1})\, dt\right] \\ \quad = nI_{Lf}\left(DV_{Cd1} + 0.5V_{Cd2}\right) \end{cases} \tag{31}$$

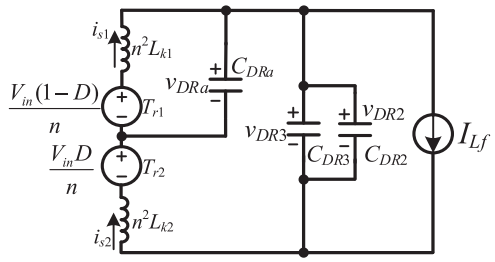


Fig. 14. Equivalent circuit of the secondary side in Fig. 5(d).

On the primary side of the transformers, the power transmitted to the output does not include the magnetic current. By integrating the product of voltage and current, the power transferred by each transformer can be obtained.

From Fig. 11(a), the power transmitted by $T_{r1}$ and $T_{r2}$ in the proposed IFB-5R converter is as follows: (31) shown at the bottom of this page.

Therefore, the equation in the following can be derived in the IFB-5R converter:

$$P_{Tr1\_\mathrm{IFB}-5R} = P_{Tr2\_\mathrm{IFB}-5R}. \tag{32}$$

From Fig. 11(c), the power transmitted by $T_{r1}$ and $T_{r2}$ in the converter in [19] is as follows:

$$\begin{cases} P_{Tr1\_[19]} = \frac{1}{T_s}\int_0^{T_s} n i_{s1} v_{AO} dt \\ = 2\int_0^{0.5T_s} (-nI_{Lf})\,(-0.5V_{\mathrm{in}})\,dt \;\; = 0.5nI_{Lf}V_{\mathrm{in}} \\ P_{Tr2\_[19]} = \frac{1}{T_s}\int_0^{T_s} i_{p2} v_{BO} dt = 2\int_0^{DT_s} (nI_{Lf} \times 0.5V_{\mathrm{in}}) dt \\ \;\; = Dn\, I_{Lf} V_{\mathrm{in}}. \end{cases} \tag{33}$$

In the converter in [19], the following constraint can be gotten:

$$P_{Tr1\_[19]} \neq P_{Tr2\_[19]}. \tag{34}$$

From the above analysis and equations, the two transformers in the IFB-5R converter share the load power equally. Therefore, each transformer can be designed according to half of the rated output load. And smaller transformer cores can be selected compared with the traditional PSFB converter. However, for the converter in [19], the two transformers cannot achieve equal power-sharing. One transformer may handle the whole load power when the duty cycle is minimum. It is difficult to distribute the load power for the two transformers, which leads to difficulty in optimizing the transformer volume.

### C. Rectifier Diode Voltage Stress Analysis

As seen in Fig. 5(d), when $D_{R1}$ and $D_{R4}$ are conducting, the leakage inductor is resonant with the junction capacitors of $D_{R2}$, $D_{R3}$, and $D_{Ra}$. It will cause ringing in the rectifier stage. The equivalent circuit of the secondary side in Fig. 5(d) is shown in Fig. 14, where the output current filter inductance is large enough to be regarded as a current source. $i_{s1}$ and $i_{s2}$ are the currents in the secondary windings of the transformers, and $C_{DRx}$ is the junction capacitor of $D_{Rx}$, where $x = 1, 2, 3, a$.

In terms of Fig. 14, the state equation of the leakage inductor current and the output voltage of the rectifier diodes are shown as follows:

$$\begin{cases} n^2L_{k1}\frac{di_{s1}}{dt} = v_{Tr1} - v_{DRa} \\ n^2L_{k2}\frac{di_{s2}}{dt} = v_{Tr2} + v_{DRa} - v_{DR3} \\ C_{DRa}\frac{dv_{DRa}}{dt} = i_{DRa} = i_{s1} - i_{s2} \\ 2C_{DR3}\frac{dv_{DR3}}{dt} = 2i_{DR3} = i_{s2} - I_{Lf}. \end{cases} \tag{35}$$

Equation (35) indicates that it is a high-order differential equation group, and it is unsolvable. Therefore, the simulation method is used to evaluate the voltage stress of the diodes. Fig. 13 shows the simulation results of the voltage across the rectifier diodes in 400 V input voltage. In the simulation, all the elements are ideal, so there is no intrinsic resistance to damp the resonance. Because of the internal damping effect by the parasitic resistance, the resonance in the prototype is decreasing. According to Fig. 15, the voltage stress in $D_{R1}$ and $D_{R2}$ is 700 V, and the voltage stress in $D_{Ra}$ 450 V. Therefore, the peak reverse voltage of the diodes in the rectifier stage should be larger than 700 V. The diodes with 1200 V reverse voltage are preferable.

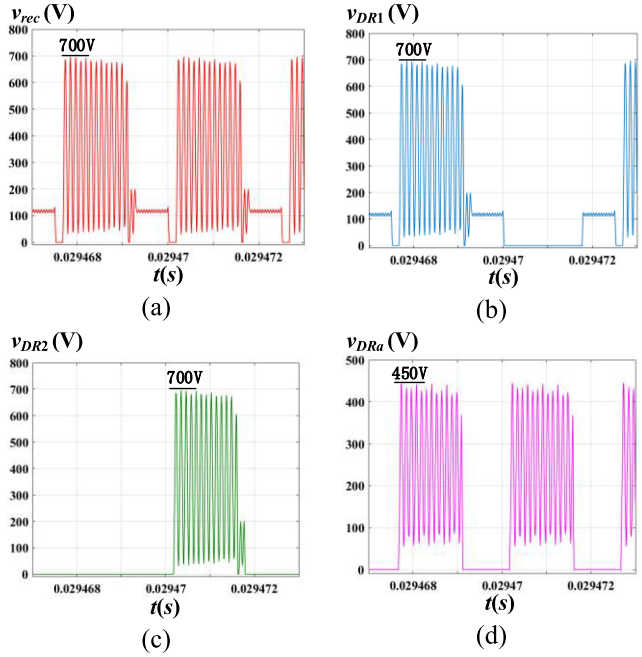


Fig. 15. Simulation results of the voltages in the rectifier stage in 400 V input voltage. (a) $v_{\mathrm{rec.}}$ (b) $v_{DR1.}$ (c) $v_{DR2}$. (d) $v_{DRa}$.

To damp the resonance and improve the electromagnetic interference (EMI) performance, the snubber circuit can be used. An resistor–capacitor–diode (RCD) snubber circuit can be used in the proposed converter, and the rectifier stage with the snubber circuit is shown in Fig. 16. The other snubber circuit also can be used in the converter.

### D. Power Loss Analysis

*1) Switch Loss:* As seen in Fig. 13, the switch conduction loss in the IFB-5R converter is reduced. Because of the ZVS, the turn-ON loss is ignored, and the turn-OFF loss will be taken into account. The waveforms when the switch is turned OFF are shown in Fig. 17.

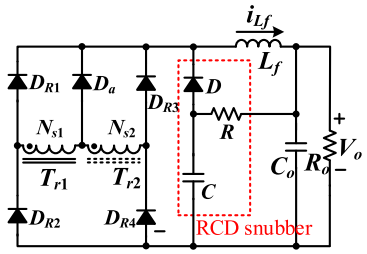


Fig. 16. Rectifier stage with the snubber circuit.

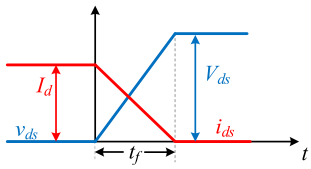


Fig. 17. Switch turn-OFF process.

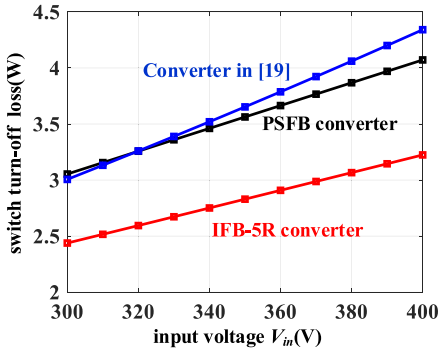


Fig. 18. Switch turn-OFF loss versus the input voltage in the rated load power.

The switch turn-OFF loss expression is approximately evaluated as

$$P_{\text{switch\_off\_loss}} = \int_0^{t_f} v_{ds} i_{ds} dt \approx \frac{V_{ds} I_d t_f}{6T_s} \tag{36}$$

where $t_f$ is the turn-OFF time.

Fig. 18 shows the switch turn-OFF loss versus the input voltage in the rated output power. The IFB-5R converter has a low turn-OFF current, so the IFB-5R converter has the lowest switch turn-OFF loss than the PSFB converter and the converter in [19].

*2) Transformer Loss:* The transformer loss includes the transformer core loss and the transformer copper loss.

The transformer core loss is mostly estimated by the following Steinmetz empirical formula:

$$P_v = k f^{\alpha} B_m^{\beta} V_e \tag{37}$$

where $\alpha$, $\beta$, and $k$ are the material parameters, $B_m$ is the maximum flux density, and $V_e$ is the volume of the magnetic core. However, the Steinmetz empirical formula is only valid for sinusoidal excitation. To calculate the core loss of any flux waveform, an improved generalized Steinmetz equation (iGSE) is proposed

$$P_v = \frac{V_e}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt. \tag{38}$$

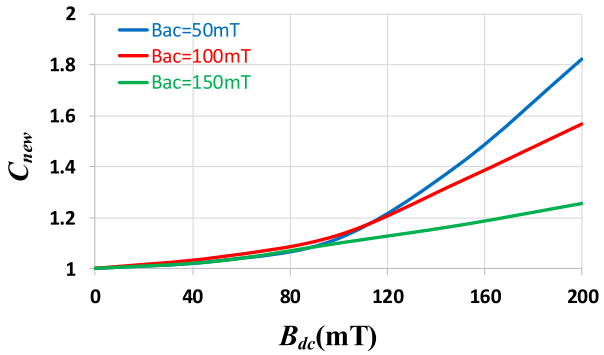


Fig. 19. Factor $C_{\text{new}}$ versus the $B_{\text{dc}}$ and $B_{\text{ac}}$.

$\Delta B$ is the peak to peak flux density, and $k_i$ meets the following equation:

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}. \tag{39}$$

However, iGSE has the disadvantage that it ignores the changes of core loss under dc bias. Many studies have proved that the core loss will increase as the dc bias increases [25], [26]. In [27], a factor is proposed to estimate the effect of dc bias on the core loss. Referred to this idea, a factor $C_{\text{new}}$ is introduced and is defined as

$$C_{\text{new}} = \frac{P_{\text{core}}(B_{\text{ac}}, B_{\text{dc}})}{P_{\text{core}}(B_{\text{ac}}, B_{\text{dc}} = 0)} \tag{40}$$

where $B_{\text{ac}}$ is the ac flux density and $B_{\text{dc}}$ is the dc flux density.

In this article, the core material is 3C90, and the B–H loop method is used to measure the transformer core loss. The core loss measurement occurs at $B_{\text{ac}} = 50$ mT, 100 mT, 150 mT, and $B_{\text{dc}} = 0$ mT, 50 mT, 100 mT, 150 mT, 200 mT. Through the analysis, Fig. 19 shows the relationship of $C_{\text{new}}$ with the ac flux density $B_{\text{ac}}$ and the dc flux density $B_{\text{dc}}$.

With the increase of the dc bias, the core loss is increasing. From Fig. 19, the core loss is not highly increased when the dc bias is low.

Therefore, for the proposed IFB-5R converter with dc bias, the transformer core loss can be expressed as follows:

$$P_{\text{Tr\_Fe\_loss}} = C_{\text{new}} \cdot P_{\text{Tr\_Fe\_loss}}(B_{\text{ac}}, B_{\text{dc}} = 0). \tag{41}$$

For the proposed IFB-5R converter, $B_{\text{dc\_max}} = 72$ mT in 400 V input voltage, so the dc bias is very low. From Fig. 14, the transformer core loss in the IFB-5R converter is not greatly affected by the dc bias.

The transformer copper loss is caused by the current following through the resistance of the primary and secondary windings. Therefore, the transformer copper loss is given by

$$P_{\text{Tr\_Cu\_loss}} = I_{p\_\text{Tr}}^2 R_{p\_\text{Tr}} + I_{s\_\text{Tr}}^2 R_{s\_\text{Tr}} \tag{42}$$

where $I_{p\_\text{Tr}}$ and $I_{s\_\text{Tr}}$ are the rms current of the primary and secondary windings. Because the circulating current in the primary circuit is reduced. Therefore, the copper loss in the IFB-5R converter is also reduced.

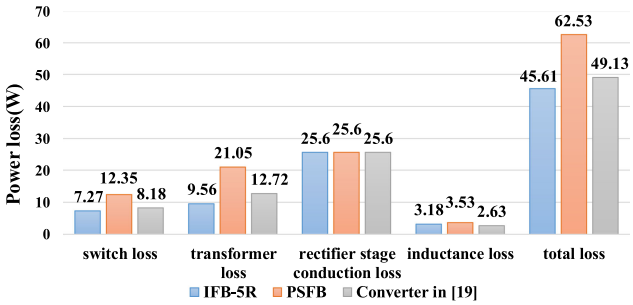


Fig. 20. Power loss of three converters when $V_{\rm in} = 400$ V in the rated load.

*3) Rectifier Stage Conduction Loss:* The rectifier stage conduction loss is mainly caused by the voltage drop of the diodes. Thus, the rectifier stage conduction loss is calculated by

$$P_{\rm DR\_con\_loss} = 2V_{\rm DR}I_o \tag{43}$$

where $V_{\rm DR}$ is the voltage drop of the rectifier stage diode and the voltage drop of all diodes in the rectifier stage are expressed the same.

As seen from (43), although one more diode is added to the proposed IFB-5R converter, the power loss of the rectifier stage is not increased.

*4) Filter Inductance Loss:* The filter inductance loss includes the inductance core loss and the inductance copper loss. Because the IFB-5R converter has a lower current ripple than the PSFB converter, a smaller core and smaller number of turns are selected. Therefore, the core loss and copper loss are lower than the PSFB converter. In the prototype, the output filter inductance core is selected as Kool M$\mu$ 77715.

*5) Loss Breakdown:* In 300 V input voltage and 250 V output voltage, the duty cycle is close to the maximum value, the PSFB converter, the converter in [19], and the proposed IFB-5R converter work in the low circulating loss. Therefore, the efficiency of the three converters is approximately the same. Under the condition of 400 V input and 250 V/4 A output, the duty cycle of the converter becomes small. The losses of the PSFB converter, the converter in [19], and the proposed IFB-5R converter are calculated. And the loss distribution diagram is shown in Fig. 20. As seen, the proposed IFB-5R converter can effectively reduce power loss and improve efficiency.

The volume of the heat sink can be evaluated according to the following equation:

$$R_{\rm th} = \frac{\Delta T}{Q}, R_{\rm th} = \frac{l}{\lambda \cdot S} \tag{44}$$

where $\Delta T$ is the temperature difference; $Q$ is the quantity of heat; $R_{\rm th}$ is the thermal resistance; $l$ is the depth of the heat sink; $S$ is the superficial area of the heat sink; and $\lambda$ is the heat conductivity coefficient. In the heat sink evaluation, the average depth of the heat sink is defined as 1 cm. The ambient temperature is 20 °C, and the temperature of the switches is 50 °C. Therefore, $\Delta T$ is 30 °C. the heat conductivity coefficient of aluminum is 237 W/m °C. The loss in the primary four switches is 7.27 W. According to (44), the average surface area of the heat sink for the primary switches is evaluated as $S = \frac{l \cdot Q}{\lambda \cdot \Delta T} = 0.102\ {\rm cm}^2$.

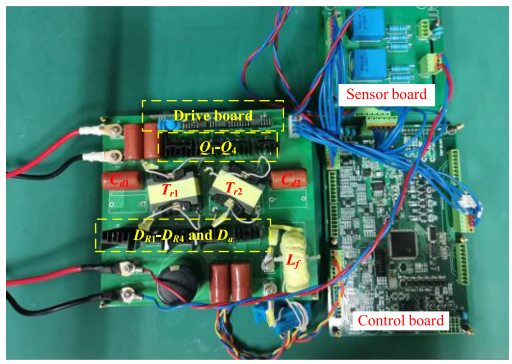


Fig. 21. Schematic diagram of the experimental topology.

TABLE I
DETAILED SPECIFICATIONS

| Components | Parameters | Value |
|---|---|---|
| Switching frequency | $f_s$ | 100 $k$Hz |
| Input voltage | $V_{in}$ | 300 V~400 V |
| Output voltage | $V_o$ | 250 V |
| Switches | $Q_1$- $Q_4$ | FDA24N50 |
| | $T_{r1}$, $T_{r2}$ | PQ40/40 |
| Transformers | $n$ | 0.94 |
| | $L_m$ | 1mH |
| | $L_k$ | 15.3$\mu$H |
| Diodes | $D_{R1}$-$D_{R4}$ | RHRP8120 |
| | $D_{Ra}$ | RHRP8120 |
| Output filter inductance | $L_f$ | 600$\mu$H (77715 @Magnetics) |

The loss in the secondary diodes is 25.6 W. In terms of the same method, the average surface area of the heat sink in the secondary diodes is evaluated as $S = \frac{l \cdot Q}{\lambda \cdot \Delta T} = 0.359\ {\rm cm}^2$. Therefore, the average surface area of the heat sink for the primary switches should be larger than 0.102 cm$^2$, and the average surface area of the heat sink for the secondary diodes should be larger than 0.359 cm$^2$.

## V. EXPERIMENTAL RESULTS

An experimental prototype with 300–400 V input and 250 V/4 A output is made to verify the performance of the proposed IFB-5R dc-dc converter. The asymmetrical PWM modulation signals are generated by the voltage and current dual closed-loop algorithm. The control algorithm is implemented in TMS320F28335. The main components and parameters of the proposed IFB-5R prototype are listed in Table I. Fig. 21 shows the experimental prototype.

The key voltage and current waveforms in the steady state are shown in Figs. 22 and 23. Fig. 22 shows the waveforms when the input voltage is 300 V and the load power is 300 and 1000 W. Fig. 23 shows the waveforms when the input voltage is 400 V and the load power is 300 and 1000 W. The dashed borders indicate that the circulating current on the primary side of the proposed IFB-5R converter is reduced. The key voltage and current waveforms are consistent with the ideal waveforms, and the circulating current is also reduced as expected.

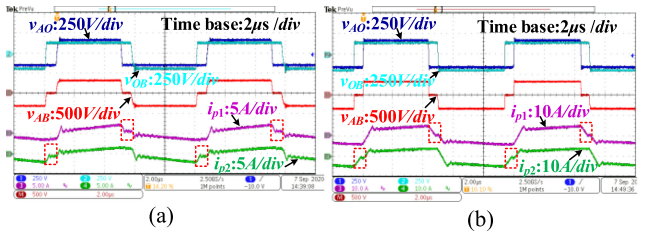


Fig. 22. Steady waveforms when $V_{\rm in}$=300 V. (a) $P$ = 300 W. (b) $P$ = 1000 W.

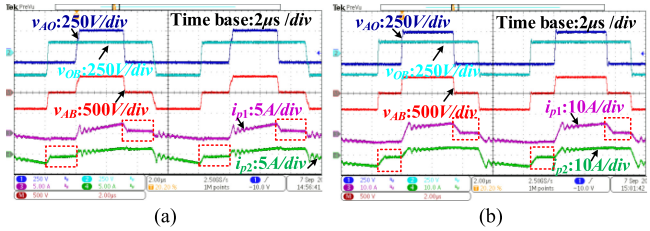


Fig. 23. Steady waveforms when $V_{\rm in}$=400 V. (a) $P$ = 300 W. (b) $P$ = 1000 W.

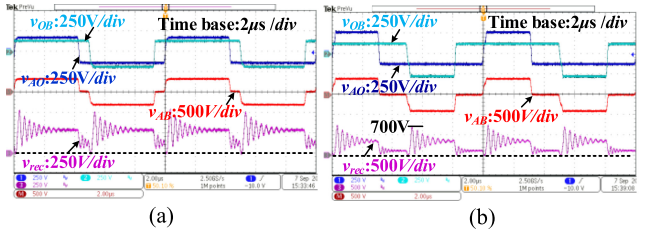


Fig. 24. Rectifier stage output. (a) $V_{\rm in}$=300 V. (b) $V_{\rm in}$=400 V.

The rectifier stage output with the input voltage of 300 and 400 V is shown in Fig. 24. As seen, during the freewheeling period, the rectifier stage output voltage is still larger than zero. This proves that the output filter inductance of the proposed IFB-5R converter can be reduced. In 400 V input voltage, the peak voltage of $v_{\rm rec}$ is approximately 700 V, which coincides with the simulation results in Fig. 15. The reverse voltage of the rectifier diodes is 1200 V, and it is reliable without the snubber circuit. The snubber causes more loss, so the snubber is not used in the prototype.

Fig. 25 shows the ZVS of $Q_1$ under different input and output conditions. When the input voltage is 300 and 400 V, and the output power is 300 and 1000 W, $Q_1$ can still realize the soft switching. In the other half of the switching cycle, $Q_3$ works the same modes as $Q_1$. Therefore, $Q_3$ can also achieve soft switching.

Fig. 26 shows the ZVS of $Q_2$ under the different input and output conditions. As seen, $Q_2$ can also achieve the ZVS. At the same time, it can be inferred that $Q_4$ can also realize soft switching. In Figs. 25 and 26, the converter can ZVS in the 300 W output power, which is the 30% rated load. It demonstrates the design of the leakage inductance in Section III-D.

Fig. 27 shows the dynamic experimental results with the load changes for the proposed IFB-5R converter. Fig. 27(a) shows the waveforms for the load changed from 300 to 1000 W, and Fig. 27(b) shows the waveforms for the load changed from 1000 to 300 W. The proposed IFB-5R converter has a good dynamic response.

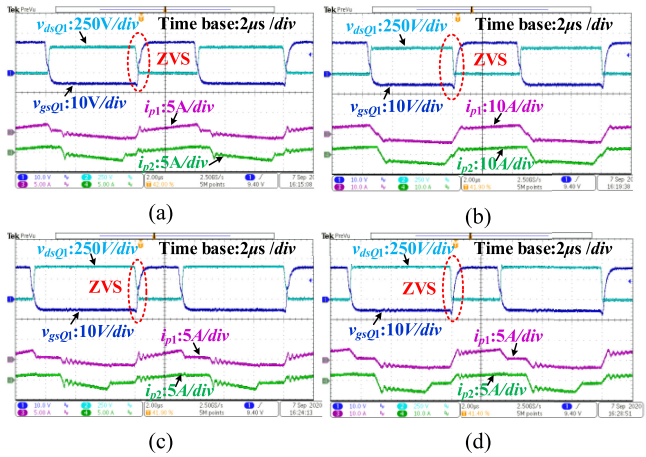


Fig. 25. ZVS for Q1. (a) $V_{\rm in}$ = 300 V, $P$ = 300 W. (b) $V_{\rm in}$ = 300 V, $P$ = 1000 W. (c) $V_{\rm in}$ = 400 V, $P$ = 300 W. (d) $V_{\rm in}$ = 400 V, $P$ = 1000 W.

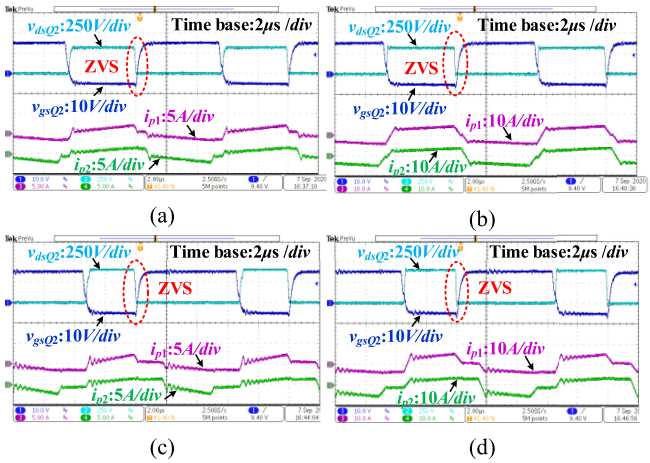


Fig. 26. ZVS for Q2. (a) $V_{\rm in}$ = 300 V, $P$=300 W. (b) $V_{\rm in}$ = 300 V, $P$ = 1000 W. (c) $V_{\rm in}$ = 400 V, $P$ = 300 W. (d) $V_{\rm in}$ = 400 V, $P$ = 1000 W.

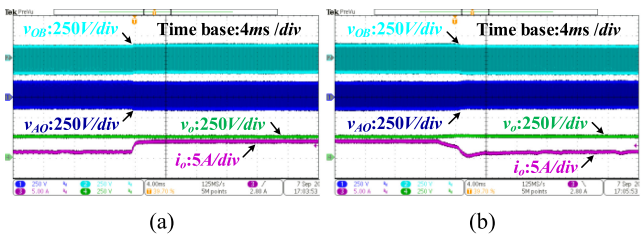


Fig. 27. Dynamic load shedding results. (a) From 300 to 1000 W. (b) From 1000 to 300 W.

Fig. 28 shows the dynamic response with the input voltage changed from 300 to 400 V. As seen in Figs. 22 and 23, the duty cycle is decreased with the increase of the input voltage. Therefore, the voltage of $v_{cd1}$ is increased, and the voltage of $v_{cd2}$ is decreased. During this interval, the output voltage is stable and constant.

Fig. 29 shows the soft start-up waveforms in 350 V input voltage. As seen in Fig. 29(a), before $t_1$, the voltages across

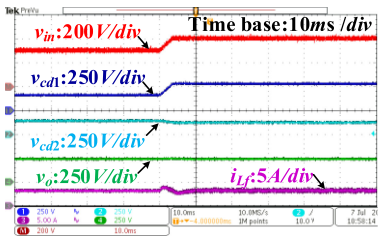


Fig. 28. Dynamic response with the input voltage change from 300 to 400 V.

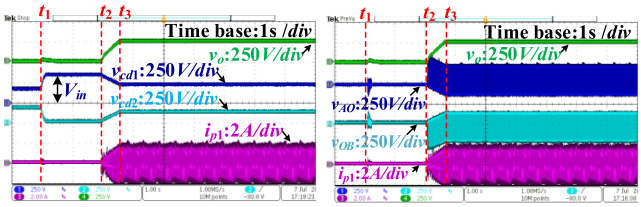


Fig. 29. Soft start-up waveforms in 350 V input voltage. (a) Output voltage and input voltages. (b) Output voltage and voltages across the primary windings of the transformers.

TABLE II
COMPONENTS OF PSFB CONVERTER AND CONVERTER IN [19]

| | PSFB converter | Converter in [19] |
|---|---|---|
| Switches | FDA24N50 | FDA24N50 |
| Transformer(s) | PQ50/50 | PQ40/40 2ea |
| Diodes | RHRP8120 | RHRP8120 |
| Output filter inductance | 730$\mu$H (77715 @Magnetics) | 430$\mu$H (77715 @Magnetics) |

$C_{d1}$ and $C_{d2}$ are equal to $V_{\text{in}}/2$. At $t_1$, the duty cycle of $Q_2$ and $Q_4$ starts to increase gradually to discharge $C_{d2}$, and $Q_1$ and $Q_3$ are still turned OFF. The voltage of $C_{d2}$ is discharged to zero, and the voltage of $C_{d1}$ is charged to $V_{in}$. At $t_2$, the duty cycle of $Q_2$ and $Q_4$ is equal to one. After $t_2$, the converter starts the soft start-up. The duty cycle of $Q_1$ and $Q_3$ are increased gradually from zero, while the duty cycle of $Q_2$ and $Q_4$ are decreased gradually from one. At $t_3$, the output voltage reaches the voltage reference, and the soft start-up is finished. After $t_3$, the converter work in the normal operation. Fig. 29(b) shows the voltages across the primary windings of the transformers. During the soft start-up, there is no large inrush current.

Table II gives the detailed components of the PSFB converter and the converter in [19]. Fig. 30 shows the efficiency of the IFB-5R converter, the PSFB converter, and the converter in [19]. Compared with the other two converters, the IFB-5R converter improves efficiency. Especially when the input voltage is 400 V, the efficiency of the IFB-5R converter is improved by about 1.7% compared to PSFB converter. It indicates the IFB-5R converter has good performance.

## VI. CONCLUSION

This article presents an improved full-bridge converter with a five-diode rectifier stage controlled by the asymmetric PWM method. Compared with the PSFB converter and the converter in [19], the IFB-5R converter improves the performance in the following aspects. All switches can achieve the ZVS. In the freewheeling period, the circulating current is reduced, and the conduction loss in the primary circuit is reduced. The two transformers share the load power equally so that the capacity and volume of each transformer can be optimized. Furthermore, the output filter inductance is reduced. With the above good performance, the efficiency of the IFB-5R converter is improved. A prototype with 300–400 V input and 250 V/4 A output is built to verify the effectiveness of the IFB-5R converter.

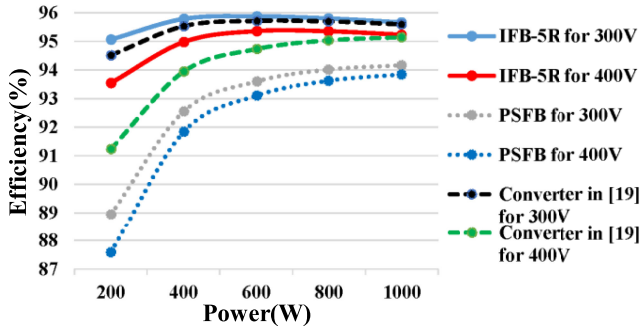


Fig. 30. Efficiency comparison of three converters.

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**Yunqiu Zhu** received the B.S. degree in electrical engineering in 2019 from the Beijing Institute of Technology, Beijing, China, where she is currently working toward the M.S. degree.

Her research interests include the topology and modeling of dc-dc converters.

**Zhiqiang Guo** (Member, IEEE) received the B.S. degree in automation from the Hebei University of Technology, Tianjin, China, in 2008, and the M.S. and Ph.D. degrees in electrical engineering from the Beijing Institute of Technology, Beijing, China, in 2010 and 2015, respectively.

He was a Postdoctoral Research Fellow with the Department of Electrical Engineering, Tsinghua University, Beijing, China, from 2015 to 2017. In 2017, he joined the Faculty of School of Automation, Beijing Institute of Technology, where he is an Assistant Professor. He has authored more than 40 papers and two books in the field of power electronics. His research interests include dc-dc converters, distributed generation, and microgrid applications.

**Qingbo Geng** was born in 1968. He received the B.S. degree in automation from the Harbin Institute of Technology, Harbin, China, in 1991, and the M.S. and Ph.D. degrees in control science and engineering from the Beijing Institute of Technology, Beijing, China, in 1994 and 2013, respectively.

He is currently an Associate Researcher with the School of Automation, Beijing Institute of Technology. His research interests include embedded system intelligent control and UAV control.