A Synchronous Auxiliary Resonant Commutated Pole Soft-Switching Inverter With Improved Load Adaptability

Wenkang Gong, *Graduate Student Member, IEEE*, Shangzhi Pan, *Senior Member, IEEE*, Wenqiang Lin, Yuan Shang, Jinwu Gong, *Member, IEEE*, Fei Liu, *Senior Member, IEEE*, and Xiaoming Zha, *Member, IEEE*

***Abstract*—To realize a soft-switching inverter with small volume and high efficiency, a synchronous auxiliary resonant commutated pole (SARCP) soft-switching inverter with improved load adaptability is proposed, which only contains two auxiliary inductors. In one switching cycle, all commutation processes can be synchronously assisted by an auxiliary inductor. Soft switching is achievable for all switches of the SARCP inverter. Compared with the auxiliary resonant commutated pole (ARCP) inverter, the SARCP inverter has improved load adaptability, especially in the light load current condition, which is beneficial to reduce the total power loss and the dc-link capacitance. The equivalent circuits of the SARCP inverter are given under different operation modes. The operation principle, soft-switching implementation conditions, parameter optimization design methods, and the characteristics of the SARCP inverter are analyzed. Finally, simulation and experimental results verify the effectiveness of the SARCP inverter.**

***Index Terms*—Auxiliary resonant commutated pole (ARCP), inverter, soft-switching, synchronous auxiliary resonant commutated pole (SARCP).**

I. Introduction

THERE is an enormous demand for better performance and higher efficiency of inverters in the development of unmanned aerial vehicle (UAV) technology [1]–[3]. The capacity of the power supply battery of the UAV is limited. Improving the efficiency of the UAV motor drive system and reducing the weight and volume of the converter can effectively increase the cruising range and load capacity of the UAV. For the UAV applications that are sensitive to the volume and weight of the converter, the traditional hard-switching inverter has severe power losses, which increases the volume of the heat dissipation system, resulting in lower efficiency and larger volume of the converter. There are also severe electromagnetic interference problems, which affect the reliability of the converter and peripheral circuits. Soft-switching technology can help relieve these problems [4]–[7].

The soft-switching inverter is divided into two catalogs: 1) the resonant dc-link (RDCL) inverter [8], [9] and 2) the auxiliary resonant commutated pole (ARCP) inverter [10]–[12]. The RDCL inverter improves the efficiency of the devices by reducing the switching loss [13], [14]. However, the resonance peak value of the dc-link voltage exceeds twice the power supply voltage, which increases the voltage stress of the main switches. And all the auxiliary components are in the main power channel, which makes them suffer a large conduction loss. McMurray and Doncker first proposed the ARCP inverter [15] in which all switches can realize soft switching. The ARCP inverter does not increase the original voltage and current stress of the main power device, which is more suitable for high power inversion applications. But it should be noted that the ARCP inverter contains three auxiliary commutation inductors and two large dc-link capacitors, thereby increasing the volume of the device dramatically.

For the ARCP inverters, fixed timing control keeps the turned-ON time of auxiliary switches fixed in each switching cycle when the load current changes [16]. Fixed timing control is simple and easy to be implemented, but it reduces the efficiency at lower output power. And the power loss of its auxiliary circuit is relatively high, which is not conducive to improving efficiency.

In [17] and [18], these inverters removed two large dc-link capacitors, but they included transformers or coupling inductors, which was ineffective to reduce the device volume. In [19] and [20], the variable timing control was proposed, adjusting the triggering time of auxiliary switches according to the load current. Although the variable timing control method is with lower power loss and better load adaptability, it requires separate detection circuits and peripheral logic control circuits, resulting in a complicated control system. In [21] and [22], the DARCP inverter was proposed. There were no two large dc-link capacitors, transformers, or coupled inductors. Within the commutation process, the power loss of the auxiliary circuit could also be reduced. However, in the auxiliary circuit of the DARCP inverter, there were a large number of passive components, leading to its control strategy being more complex and inefficient.

Putting forth effort on these problems, a synchronous auxiliary resonant commutated pole (SARCP) soft-switching inverter

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The authors are with the School of Electrical Engineering and Automation, Wuhan University, Wuhan 430072, China (e-mail: wenkang.gong@whu.edu.cn; shangzhi.pan@whu.edu.cn; linwq@whu.edu.cn; shang-yuan@foxmail.com; gongjinwu@whu.edu.cn; dyj_lf@163.com; xmzha@whu.edu.cn).

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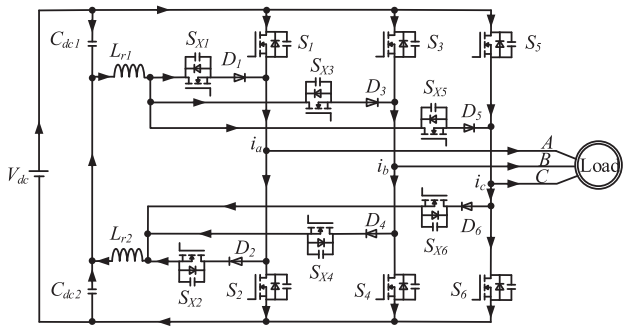

Fig. 1 SARCP soft-switching inverter.

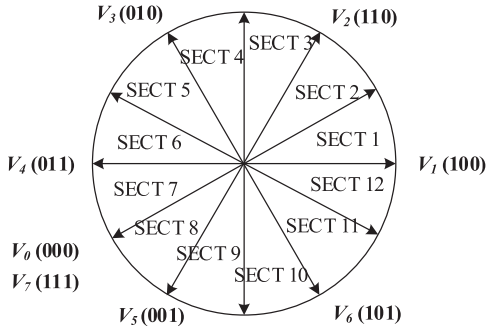

Fig. 2 Sections of inverter voltage space vector diagram switching region.

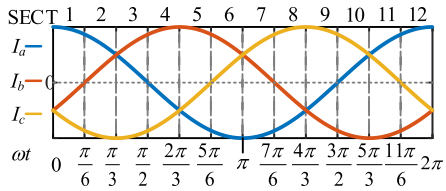

Fig. 3 Theoretical waveform of the SARCP inverter current.

with improved load adaptability is proposed in this article. The SARCP inverter only contains two inductors in the auxiliary circuit. In one switching cycle, the commutation processes of the two-phase main switches are synchronously assisted by an auxiliary inductor. Compared with the ARCP inverter, the SARCP inverter has a smaller dc-link capacitance. Furthermore, when fixed timing control is applied to the two inverters, the SARCP inverter has improved load adaptability, especially under the light load current condition, so the total power loss of the SARCP inverter is lower. In brief, the SARCP inverter can achieve a smaller volume and higher efficiency in contrast to the ARCP inverter.

In this article, the topology of the SARCP inverter is introduced briefly at first, then the operation principle and the parameter design procedure are described in detail. And the characteristics of the proposed inverter are analyzed minutely. Finally, the effectiveness of the SARCP inverter is verified by simulation and experimental results.

II. Circuit Topology and Operation Principle

A. Circuit Topology

An SARCP soft-switching inverter with improved load adaptability is proposed in this article. As shown in Fig. 1, the proposed topology consists of dc-link voltage source ($V_{\rm dc}$), the dc-link capacitors ($C_{\rm dc1} - C_{\rm dc2}$), the auxiliary switches ($S_{x1} - S_{x6}$), the auxiliary diodes ($D_1 - D_6$), the auxiliary commutation inductors ($L_{r1} - L_{r2}$), the main switches ($S_1 - S_6$) with parasitic diodes and parasitic capacitances, and the three-phase ac load (*Load*).

In the SARCP inverter, the auxiliary commutation inductor L_{r1} provides zero-voltage-switching (ZVS) turn-ON conditions for the three main upper switches (S_1, S_3, S_5). In one switching cycle, the commutation processes of all main upper switches are synchronously assisted by L_{r1}. Similarly, L_{r2} is responsible for synchronously assisting the commutation processes of the three main lower switches (S_2, S_4, and S_6).

B. Modulation Strategy

An SVPWM modulation strategy of the 12 sectors is applied to the SARCP inverter. Assuming the SARCP inverter works with a unity power factor, the corresponding voltage sector definition is shown in Fig. 2. In the normal SVPWM modulation strategy, the whole utility cycle can be divided into six voltage sectors [23]. According to the maximum absolute value of the phase current in the inverter, the six sectors are divided into 12 sectors. For example, in SECT 1, phase-A has the maximum absolute values of the phase current and phase voltage. And in SECT 2, phase-C has the maximum absolute values of the phase current and phase voltage [24], [25].

The theoretical waveform of the three-phase inverter current is shown in Fig. 3. In one switching cycle, there are only one zero vector and two nonzero vectors applied for modulation, and the switching state of the phase with the maximum current always remains unchanged.

In the main circuit, "1" means that the upper switch is turned ON and the lower switch is turned OFF. "0" means that the upper switch is turned OFF and the lower switch is turned ON. Taking phase-A as an example, when under positive load current condition, the switching process from "0" to "1" is the hard switching. And during the state from "1" to "0," the current in S_2 will first flow into its parasitic diode. Thus, the switching process from "1" to "0" is normal soft switching.

It is assumed that the SARCP inverter works with a unity power factor. To minimize the number of switching processes, in SECT 2, the switching sequence is "000-110-100-000." The main switches S_6 is always in conduction, so there are only four switching processes in one switching cycle. Align the two hard-switching processes to facilitate L_{r1} synchronously assisting the commutation processes of phase-A and phase-B. The switching sequence is shown in Fig. 4. L_{r2} is kept inactive.

Therefore, within a switching cycle, the SARCP inverter only needs one auxiliary commutation inductor to act once. By contrast, the ARCP inverter needs two auxiliary commutation inductors to act once each, which means that the auxiliary circuit of the SARCP inverter has fewer working times and lower total power loss.

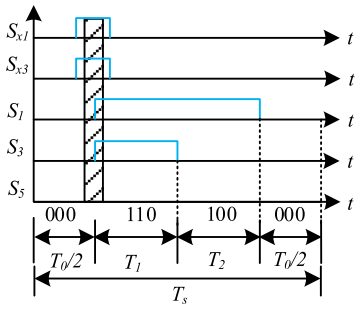

Fig. 4 Switching sequence in SECT 2.

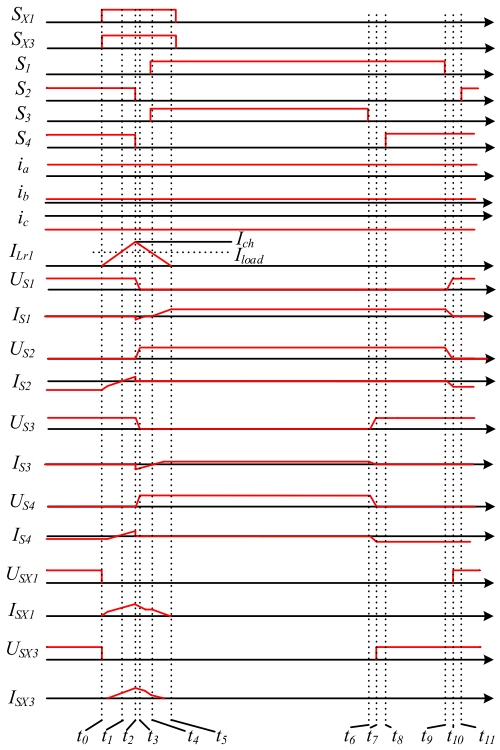

Fig. 5. Theoretical waveform of the commutation processes in SECT 2.

C. Operation Principle

In SECT 2, only the commutation process from "000" to "110" needs to be assisted. In order to facilitate the analysis, the following assumptions are employed.

1) In one switching cycle, the load inductor current ripple is small and it can be considered as a constant current source.
2) The values of the auxiliary commutation inductors (L_{r1} – L_{r2}) are equal. The values of the dc-link capacitors ($C_{\rm dc1}$ – $C_{\rm dc2}$) are equal.
3) In one switching cycle, the dc-link capacitances ($C_{\rm dc1}$ – $C_{\rm dc2}$) are so large that the midpoint voltage of the dc-link remains unchanged.
4) The referential positive directions of the physical quantities in the SARCP inverter are consistent with the arrow direction in Fig. 1.

The theoretical waveform of the commutation processes in SECT 2 is shown in Fig. 5. There are 12 operating modes of the SARCP inverter, and their equivalent circuits are shown in Fig. 6.

Mode 0 [$\sim t_0$]*:* Initial state. The switching state of the SARCP inverter is "000," and it operates in a steady state. The input dc voltage source $V_{\rm dc}$ supplies energy to the load via S_2, S_4, and S_6. S_2, S_4, and S_6 carry the load current i_a, i_b, and i_c, respectively. The auxiliary circuits are not activated.

Mode 1 [t_0, t_1]*:* At instant t_0, S_{x1} and S_{x3} are turned ON synchronously, which can achieve zero-current-switching (ZCS) turn-ON because they are connected in series with L_{r1}. In SECT 2 ($i_a \geq i_b$), when $i_a = i_b$, D_1 and D_3 conduct synchronously. $C_{\rm dc2}$ charges L_{r1}. And the current through L_{r1} is I_{Lr1} ($I_{Lr1} = I_{Sx1} + I_{Sx3}$). I_{Lr1} rises from zero at a linear rate of $V_{\rm dc}$ / $2L_{r1}$. And the load currents i_a and i_b are commutated to L_{r1} from S_2 and S_4. When the current through L_{r1} rises to $I_{\rm load}$ ($I_{\rm load} = i_a + i_b$), the negative currents through S_2 and S_4 fall to zero, and Mode 1 ends.

When $i_a > i_b$, due to the unequal midpoint voltages of the phase-A and phase-B, D_1 conducts ahead of D_3. Therefore, the inductor current I_{Lr1} first flows through S_{x1}. When D_3 conducts, I_{Lr1} flows through S_{x1} and S_{x3} at the same time. And the load currents i_a and i_b are commutated to L_{r1} from S_2 and S_4. Mode 1 ends when the negative currents through S_2 and S_4 both fall to zero. The theoretical waveform of Mode 1 is shown in Fig. 5.

Mode 2 [t_1, t_2]*:* At instant t_1, $C_{\rm dc2}$ continues charging L_{r1}. The current through L_{r1} keeps rising at a linear rate of $V_{\rm dc}$ / $2L_{r1}$. Both the positive current through S_{x1} and S_2 and the positive current through S_{x3} and S_4 rise linearly. I_{Lr1} reaches the threshold $I_{\rm ch}$ until time t_2, and mode 2 ends. The expression of threshold $I_{\rm ch}$ is

$$I_{\rm ch} = i_a + i_b + I_{\rm boost}. \tag{1}$$

$I_{\rm boost}$ is determined by the dead time T_d. The expression of $I_{\rm boost}$ is

$$I_{\rm boost} \geq T_d \frac{V_{\rm dc}}{2L_{r1}}. \tag{2}$$

In Mode 1 and Mode 2, L_{r1} is charged, and the expression of the total charging time of L_{r1} is

$$t_2 - t_0 = I_{\rm ch} * \frac{2L_{r1}}{V_{\rm dc}}. \tag{3}$$

Mode 3 [t_2, t_3]*:* At instant t_2, S_2 and S_4 are turned OFF synchronously, which can achieve pseudo-ZVS turn-OFF because they are connected in parallel with parasitic capacitances. I_{Lr1} discharges the parasitic capacitances of S_1 and S_3 and charges the parasitic capacitances of S_2 and S_4. At the same time, the voltages on S_1 and S_3 decrease, and the voltages on S_2 and S_4 increase. Till time t_3, the voltages on S_1 and S_3 decrease to zero, and the parasitic diodes of them start to conduct. Mode 3 ends. The operation time of this mode is

$$t_3 - t_2 = 4 * C_r \frac{V_{\rm dc}}{I_{\rm boost}}. \tag{4}$$

Since the main switch is MOSFET, and the value of parasitic capacitances is very small, the operation time of Mode 3 can be ignored. Therefore, the commutation processes of the SARCP inverter are not affected.

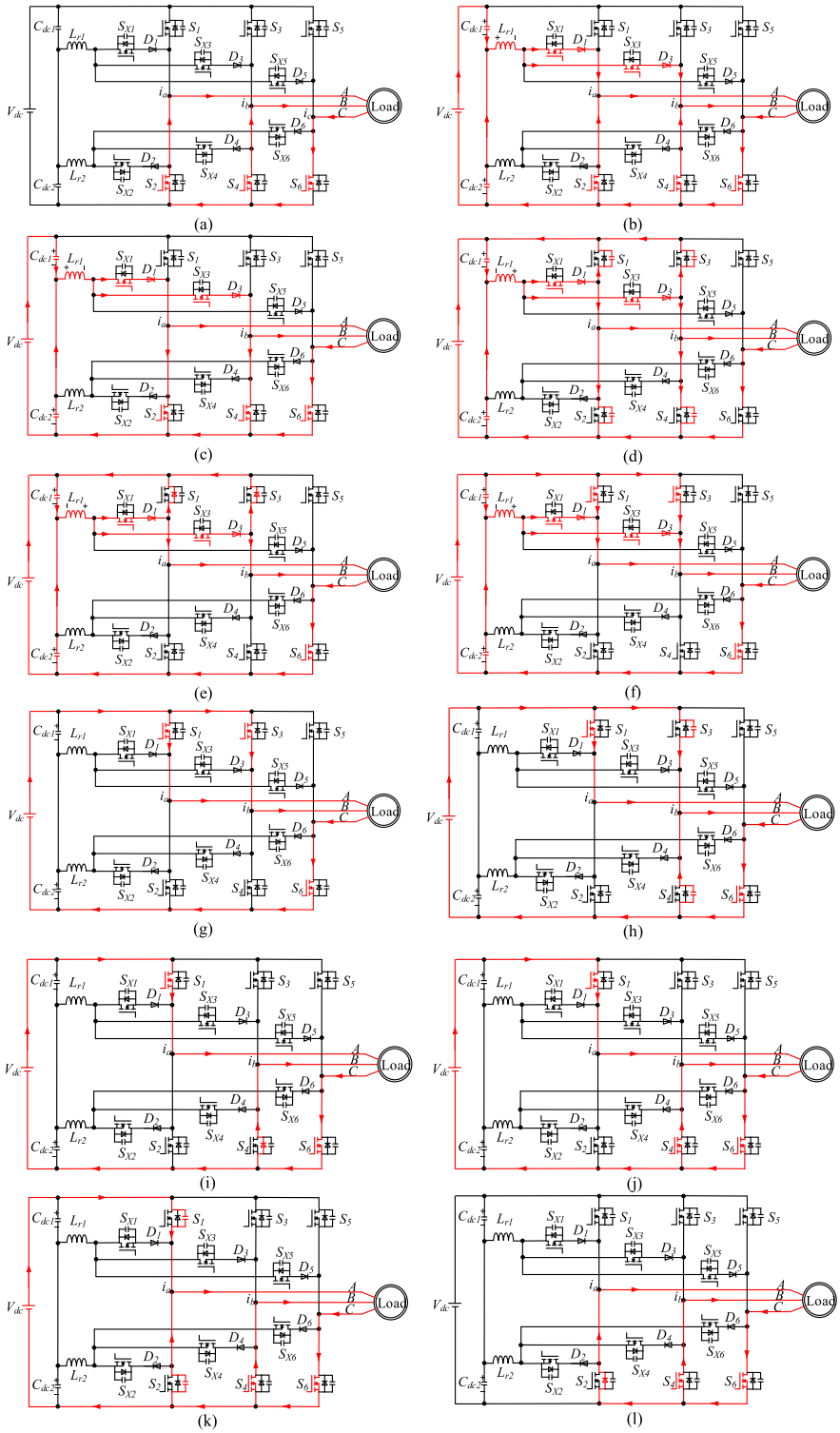

Fig. 6. Equivalent circuits of different operation modes. (a) Mode 0. (b) Mode 1. (c) Mode 2. (d) Mode 3. (e) Mode 4. (f) Mode 5. (g) Mode 6. (h) Mode 7. (i) Mode 8. (j) Mode 9. (k) Mode 10. (l) Mode 11.

Mode 4 [t_3, t_4]*:* At instant t_3, the parasitic diodes of S_1 and S_3 conduct. The boost current I_{boost} through L_{r1} circulates in the series circuits $L_{r1} - S_{x1} - D_1 - S_1 - C_{\text{dc1}}$ and $L_{r1} - S_{x3} - D_3 - S_3 - C_{\text{dc1}}$. S_1 and S_3 can be turned ON under the ZVS condition. L_{r1} charges C_{dc1}. The current through L_{r1} decreases at a linear rate of $V_{\text{dc}} / 2L_{r1}$.

In SECT 2, when $i_a = i_b$, the parasitic diodes of S_1 and S_3 keep ON until I_{Lr1} decreases to I_{load}. When $i_a > i_b$, the reduction of I_{Sx1} to i_a takes less time than the reduction of I_{Sx3} to i_b. Accordingly, when $I_{Sx1} = i_a$, the current through the parasitic diode of S_1 decreases to zero. And the parasitic diode of S_3 still keeps ON, leaving the voltages on S_1 and S_3 clamped at zero. The

boost current $I_{\rm boost}$ through L_{r1} circulates in the series circuit $L_{r1} - S_{x3} - D_3 - S_3 - C_{\rm dc1}$. The parasitic diode of S_3 keeps ON until I_{Lr1} decreases to $I_{\rm load}$. At instant t_4, $I_{Lr1} = I_{\rm load}$, and the parasitic diodes turn OFF. Mode 4 ends. The operation time of this mode is

$$t_4 - t_3 \le I_{\rm boost}\frac{2L_{r1}}{V_d}. \tag{5}$$

Mode 5 [t_4, t_5]*:* Before instant t_4, S_1 and S_3 are turned ON synchronously. The current through L_{r1} continues falling at a linear rate of $V_{\rm dc}/2L_{r1}$. The currents through S_1 and S_3 displace the load current through L_{r1}. At instant t_5, the current through L_{r1} falls to zero. S_{x1} and S_{x3} can be turned OFF under the ZCS condition. Mode 5 ends.

In Mode 4 and Mode 5, L_{r1} is discharged, and expression of the total discharging time is

$$t_5 - t_3 = (I_{\rm load} + I_{\rm boost})\frac{2L_{r1}}{V_{\rm dc}}. \tag{6}$$

Mode 6 [t_5, t_6]*:* The switching state of the SARCP inverter is "110," and the SARCP inverter operates in the steady state. The input dc voltage source $V_{\rm dc}$ supplies energy to the load via S_1, S_3, and S_6. And S_1, S_3, and S_6 carry the load current i_a, i_b, and i_c, respectively.

Mode 7 [t_6, t_7]*:* At instant t_6, S_3 is turned OFF. The phase current i_b charges the parasitic capacitance of S_3 and discharges the parasitic capacitance of S_4. Due to the existence of parasitic capacitance, S_3 can achieve pseudo-ZVS turn-OFF.

Mode 8 [t_7, t_8]*:* At instant t_7, the voltage on S_4 decreases to zero. The parasitic diode of S_4 conducts. S_4 can be turned ON under the ZVS condition. The auxiliary circuits are not activated.

Mode 9 [t_8, t_9]*:* At instant t_8, S_4 is turned ON under ZVS condition, and the circuit reaches the state "100."

Mode 10 [t_9, t_{10}]*:* At instant t_9, S_1 is turned OFF. The phase current i_a charges the parasitic capacitance of S_1 and discharges the parasitic capacitance of S_2. Due to the existence of parasitic capacitance, S_1 can achieve pseudo-ZVS turn-OFF.

Mode 11 [t_{10}, t_{11}]*:* At instant t_{10}, the voltage on S_2 decreases to zero. The parasitic diode of S_2 conducts. S_2 can be turned ON under the ZVS condition. The auxiliary circuits are not activated. After S_2 is turned ON, the commutation processes end. The circuit reaches the switching state "000" and returns to the initial steady-state Mode 0.

III. Parameter Design

A. Soft-Switching Condition Analysis

For the SARCP inverter, there are three types of soft-switching as follows.

1) The main switches realize ZVS turn-ON through the auxiliary circuit

When the switching state changes from "000" to "110," there are two conditions for S_1 and S_3 to achieve ZVS turn-ON.

First, in Mode 3, the energy of the parasitic capacitances of S_1 and S_3 can be released by I_{Lr1} through resonance, and then parasitic diodes of S_1 and S_3 conduct. Therefore, the dead time T_d should be longer than the duration of the resonance process

$$T_d > t_3 - t_2 = 4 * C_r\frac{V_{\rm dc}}{I_{\rm boost}}. \tag{7}$$

Second, in Mode 4, before the inductor current I_{Lr1} decreases to $I_{\rm load}$, the parasitic diodes of S_1 and S_3 keep ON, creating the ZVS condition for S_1 and S_3. Thus, the maximum of T_d is

$$T_d < I_{\rm boost}\frac{2L_{r1}}{V_{\rm dc}}. \tag{8}$$

Combining (7) with (8), the range of dead time T_d is

$$4 * C_r\frac{V_{\rm dc}}{I_{\rm boost}} < T_d < I_{\rm boost}\frac{2L_{r1}}{V_{\rm dc}}. \tag{9}$$

As the main switch, the value of parasitic capacitance C_r of the MOSFET is so small that the duration of the resonance process can be ignored. Therefore, the conditions for the main switches to realize ZVS turn-ON through the auxiliary circuit can be simplified as

$$T_d < I_{\rm boost}\frac{2L_{r1}}{V_{\rm dc}}. \tag{10}$$

2) The main switches realize normal soft-switching without the auxiliary circuit.

During the switching state from "110" to "100," the phase current i_b charges the parasitic capacitance of S_3 and discharges the parasitic capacitance of S_4. When the voltage on S_4 decreases to zero, the parasitic diode of S_4 conducts. The duration of the resonance process is

$$t_7 - t_6 = 2 * C_r\frac{V_{\rm dc}}{i_b}. \tag{11}$$

Since the value of i_b can be regarded as a constant during one switching cycle, the condition for the main switches to realize normal soft switching is: during the dead time T_d, the voltage on the parasitic capacitance of S_4 can be reduced to zero by i_b through resonance. The minimum value of i_b is

$$i_b > 2 * C_r\frac{V_{\rm dc}}{T_d}. \tag{12}$$

The C_r is very small, so S_4 can achieve ZVS turn-ON.

3) The auxiliary switches realize ZCS turn-ON and turn-OFF

Auxiliary switches S_{x1} and S_{x3} can achieve ZCS turn-ON and turn-OFF because they are connected in series with the auxiliary commutation inductor L_{r1}.

B. Design and Optimization of Parameters

The charging time of the L_r is T_c. The switching period is T_k. The switching frequency is f_k. The maximum value of the phase current (load current) is $I_{\rm max}$. During the process of parameter design, three important parameters T_d, T_c, and L_r need to be satisfied as follows.

1) The charging time T_c and the dead time T_d.

It is assumed that the duration of the switching process in the Datasheet of the main switch is $T_{\rm d\text{-}min}$. In terms of (9), the

design procedure expression of T_d and T_c is as follows:

$$T_{d-\min} < T_d < T_c - I_{\max}\frac{2L_{r1}}{V_{\rm dc}}. \tag{13}$$

2) The auxiliary commutation inductor L_r.

Choosing an appropriate value of L_r can minimize the total loss of the auxiliary circuit. Since all auxiliary switches are wide bandgap semiconductor devices and realize ZCS turn-ON and turn-OFF, their switching loss is negligible. The conduction loss is almost equal to the total loss of the auxiliary circuit, and it is approximately proportional to the square of the current rms value.

The current of the auxiliary circuit is generated by L_r. Assuming the current RMS value of the L_r is $I_{\rm Lr\cdot RMS}$, the expression of $I_{\rm Lr\cdot RMS}$ is

$$I_{\rm Lr\_RMS} = \sqrt{\frac{1}{2}}\cdot\sqrt{\frac{2T_{\rm C}}{T_k}}\cdot\frac{I_{\rm ch}}{\sqrt{3}} = \sqrt{\frac{T_{\rm C}}{3T_k}}\cdot I_{\rm ch}. \tag{14}$$

According to (1), (3), and (10), in order to ensure that the soft switching can be realized, T_c should be appropriately larger. So, the expression of T_c is

$$T_c = I_{\rm ch}\frac{2L_{r1}}{V_{\rm dc}} = \left(I_{\max} + \frac{V_{\rm dc}}{2L_{r1}}T_d\right)\cdot\frac{2L_{r1}}{V_{\rm dc}}\cdot 1.05. \tag{15}$$

Combining (14) with (15), the expression of $I_{\rm Lr\cdot RMS}$ is

$$I_{\rm Lr\_RMS} = \sqrt{\frac{2f_kL_{r1}}{3V_{\rm dc}}}\cdot\left(\left(I_{\max} + \frac{V_{\rm dc}}{2L_{r1}}T_d\right)\cdot 1.05\right)^{3/2}. \tag{16}$$

According to (13) and (16), an appropriate value of L_r needs to be selected to minimize the value of $I_{\rm Lr\cdot RMS}$.

3) Example of parameter design optimization.

In accordance with (16), an example is shown below to illustrate the parameter design and optimization processes of the SARCP inverter. The dc voltage $V_{\rm dc}$ is 50 V, and the switching frequency f_k is 20 k, and the output maximum load phase current $I_{\max}$ is 28 A. The feasible range of the dead time is $T_d \in$ (150 ns, 400 ns). In order to reduce the volume of the device, the range of L_r is $L_r \in$ (0.01 μH and 1 μH).

Fig. 7 shows the influence of the dead time T_d and the auxiliary inductor L_r on the rms value $I_{\rm Lr\cdot RMS}$ of the auxiliary inductor current. By choosing an appropriate value of L_r and T_d, $I_{\rm Lr\cdot RMS}$ can be minimized. On the basis of the actual engineering design, the L_r is selected as 0.22 μH, and T_d is selected as 190 ns. According to (15), the charging time T_c of the L_r is 0.45 μs, and the $I_{\rm Lr\cdot RMS}$ is 2.88 A.

IV. Characteristics of the Proposed Inverter

A. Load Adaptability Analysis

When the modulation strategy in Section II-B is applied to the SARCP inverter, in one switching cycle, it only needs one auxiliary commutation inductor to act once. However, the ARCP inverter needs two auxiliary commutation inductors to act once each. When the fixed time control method is applied to the auxiliary circuits, compared with the ARCP inverter, the SARCP inverter can have higher efficiency and improved load adaptability, especially under the light load current condition. In

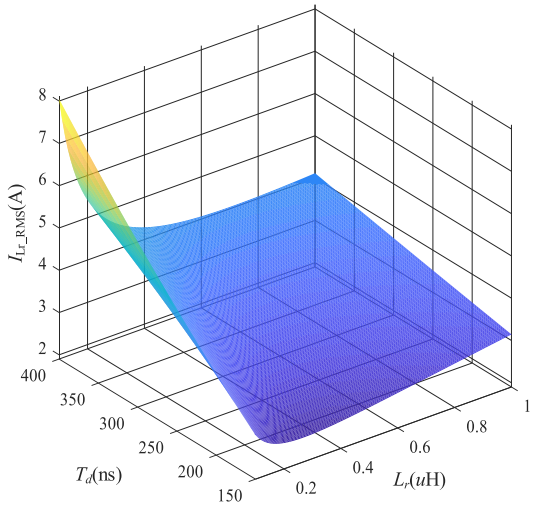

Fig. 7. RMS value $I_{\rm Lr\cdot RMS}$ of the auxiliary inductor current under different T_d and L_r.

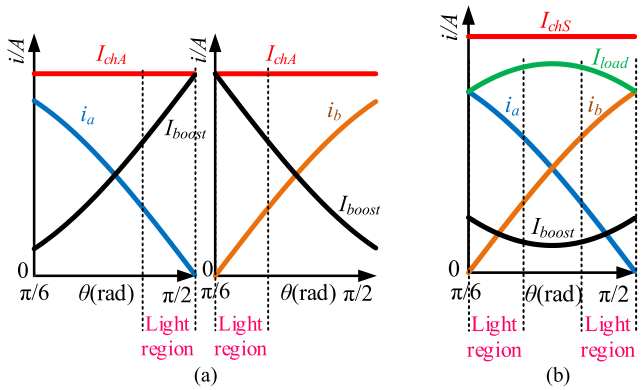

Fig. 8. Comparison of $I_{\rm boost}$ between the ARCP inverter and the SARCP inverter. (a) ARCP inverter. (b) SARCP inverter.

SECT 2, the light load current range is the light region shown in Fig. 8.

For the ARCP inverter and the SARCP inverter, as a condition for the main switches to realize ZVS turn-ON through the auxiliary circuit, the peak value $I_{\rm ch}$ of the inductor charging current must be large enough. $I_{\rm load}$ is the load current that needs to be assisted. $I_{\rm ch}$ is shown in (17), which is designed according to the maximum value of $I_{\rm load}$

$$I_{\rm ch} = I_{\rm load} + I_{\rm boost} \geq I_{\rm load} + T_d\frac{V_{\rm dc}}{2L_{r1}}. \tag{17}$$

The output maximum load phase current is $I_{\max}$, and the peak value of the inductor charging current is $I_{\rm chA}$. When the modulation strategy in Section II-B is applied to the ARCP inverter, $I_{\rm load}$ of the ARCP inverter is the phase current. In SECT 2, the maximum value of $I_{\rm load}$ is $\sqrt{3}I_{\max}/2$. $I_{\rm chA}$ is

$$I_{\rm chA} = \frac{\sqrt{3}}{2}I_{\max} + I_{\rm boost} \geq i_a + I_{\rm boost}. \tag{18}$$

In SECT 2, for the SARCP inverter, $I_{\rm load} = i_a + i_b$, so the maximum value of $I_{\rm load}$ is $I_{\max}$. The peak value of inductor charging current $I_{\rm chS}$ is

$$I_{\rm chS} = I_{\max} + I_{\rm boost} \geq i_a + i_b + I_{\rm boost}. \tag{19}$$

Combining (18) with (19), the comparison of boost current $I_{\rm boost}$ between the ARCP inverter and the SARCP inverter is shown in Fig. 8.

Compared with the ARCP inverter, the $I_{\rm boost}$ of the SARCP inverter is smaller and changes in a smaller range, especially in the light load current region. $I_{\rm boost}$ flows through the auxiliary circuit and the main circuit. The small $I_{\rm boost}$ is in favor of achieving lower conduction losses of the auxiliary circuit and the main circuit. Therefore, the SARCP inverter could have better load adaptability and lower conduction loss.

B. Value of the DC-Link Capacitance

It is assumed that both inverters have the same modulation strategy and operating conditions. The larger the dc-link capacitance is, the smaller the midpoint potential fluctuation is. The dc-link capacitance of the ARCP inverter and the SARCP inverter are C_A and C_S, respectively. In one switching cycle, the fluctuations of midpoint potential on the dc-link of the ARCP inverter and the SARCP inverter are ΔU_A and ΔU_S, respectively. And the energy of dc-link capacitors released by the two inverters is E_A and E_S, respectively. Combining (18) with (19), E_A and E_S are as follows:

$$E_A = \frac{1}{2}C_A\Delta U_A^2 = 2LI_{\rm chA}^2 = \frac{3}{2}L\left(I_{\max}+\frac{2}{\sqrt{3}}I_{\rm boost}\right)^2 \tag{20}$$

$$E_S = \frac{1}{2}C_S\Delta {U_S}^2 = L{I_{\rm chS}}^2 = L(I_{\max}+I_{\rm boost})^2. \tag{21}$$

When the fluctuations of midpoint potential on the dc-link of the two inverters are equal ($\Delta U_A^2 = \Delta {U_S}^2$), the value of the dc-link capacitors of the SARCP inverter is less than two-thirds of that of the ARCP inverter ($C_S < 2C_A/3$).

The comparison of the number of components of the two inverters is given in Table 1.

For inverters, the volume of the auxiliary inductor and dc-link capacitance is much larger than that of the diode. Therefore, compared with the ARCP inverter, the SARCP inverter is more conducive to reducing the device's volume.

C. Power Loss Analysis

Assuming that the ARCP inverter and the SARCP inverter are under the same circuit condition, the modulation strategy in Section II-B is applied to the two inverters. Since the power losses of the main circuits are approximately equal, the theoretical power losses of the auxiliary circuits are compared. In one switching cycle, the performance of the two inverters is compared from the following points.

1) The total power loss of the auxiliary commutation inductor.

The power loss of the auxiliary commutation inductor mainly includes iron loss and copper loss. In one switching cycle, the SARCP inverter only needs one auxiliary commutation inductor to act once. However, the ARCP inverter needs two auxiliary commutation inductors to act once each.

The iron loss of the inductor is estimated according to the Steinmetz equation ($P_v = kf_\alpha B_\beta$) [26], [27]. The iron losses of the auxiliary inductors in the two inverters are P_{vA} and P_{vS}, respectively. As a rule of thumb, the value of β is 2.4. Except for the peak values of currents of the auxiliary inductors, the working conditions of the two inverters are the same, so the relationship between P_{vA} and P_{vS} is as (22). The iron loss of the SARCP inverter is less than four-fifths of that of the ARCP inverter ($P_{vS} < 4P_{vA}$ /5)

$$\frac{P_{vS}}{P_{vA}} = \frac{{I_{\max}}^\beta}{2*\left(\frac{\sqrt{3}}{2}I_{\max}\right)^\beta} = \frac{1}{2}*\left(\frac{2}{\sqrt{3}}\right)^{2.4} < \frac{4}{5}. \tag{22}$$

In one switching cycle, the rms value of the current on the auxiliary commutation inductor in the ARCP inverter and the SARCP inverter are $I_{\rm Lr\_RMS\_A}$ and $I_{\rm Lr\_RMS\_S}$, respectively. And the copper losses of the auxiliary inductors in the two inverters are $P_{\rm cuA}$ and $P_{\rm cuS}$, respectively. Combining (14) and (15), with (18), $P_{\rm cuA}$ is

$$P_{\rm cuA} = 2I_{\rm Lr\_RMS\_A}^2\left(R_{\rm ac}+R_{\rm dc}\right) = \frac{8L_rf_k}{3V_{\rm dc}}I_{\rm chA}^3\left(R_{\rm ac}+R_{\rm dc}\right)$$
$$= \frac{\sqrt{3}L_rf_k}{V_{\rm dc}}(I_{\max}+\frac{2}{\sqrt{3}}I_{\rm boost})^3\cdot\left(R_{\rm ac}+R_{\rm dc}\right). \tag{23}$$

Combining (14) and (15) with (19), $P_{\rm cuS}$ is

$$P_{\rm cuS} = I_{\rm Lr\_RMS\_S}^2\left(R_{\rm ac}+R_{\rm dc}\right) = \frac{4L_rf_k}{3V_{\rm dc}}I_{\rm chS}^3\left(R_{\rm ac}+R_{\rm dc}\right)$$
$$= \frac{4L_rf_k}{3V_{\rm dc}}(I_{\max}+I_{\rm boost})^3\cdot\left(R_{\rm ac}+R_{\rm dc}\right). \tag{24}$$

Combining (23) with (24), it can be concluded that the copper loss of the SARCP inverter is less than four-fifths of that of the ARCP inverter ($P_{\rm cuS} < 4P_{\rm cuA}$ /5).

Thus, the total power loss of the auxiliary commutation inductor of the SARCP inverter is less than four-fifths of that of the ARCP inverter.

2) The total conduction loss of the auxiliary switching transistors.

The auxiliary switching transistors include the auxiliary switches and the auxiliary diodes. To facilitate the analysis, it is assumed that the conduction loss of the auxiliary diode is as (25). The forward voltage and the ON-resistance of the auxiliary diode are v_{d0} and r_d, respectively

$$P_{\rm d\_con} = v_{d0}I_{\alpha v} + r_dI_{\rm RMS}^2. \tag{25}$$

The ON-resistance of the auxiliary switch is r_s. It is assumed that the v_{d0}, r_d, and r_s of the ARCP inverter and the SARCP inverter are the same. For the ARCP inverter, the current average value of the L_r is $I_{\rm av\cdot A}$. In one switching cycle, combining (18) with (25), the total conduction loss of the auxiliary circuits of the ARCP inverter is $P_{\rm conA}$

$$P_{\rm cont} = 2\left(v_{\rm d0}I_{\rm av-A} + r_{\rm d}I_{\rm Lr\_RMS\_A}^2 + r_sI_{\rm Lr\_RMS\_A}^2\right)$$
$$= \frac{3v_{\rm d0}L_rf_k}{V_{\rm dc}}\left(I_{\max}+\frac{2}{\sqrt{3}}I_{\rm boost}\right)^2$$
$$+\frac{\sqrt{3}L_rf_k}{V_{\rm dc}}\left(I_{\max}+\frac{2}{\sqrt{3}}I_{\rm boost}\right)^3\left(r_{\rm d}+r_s\right). \tag{26}$$

TABLE I
NUMBER OF COMPONENTS OF TWO INVERTERS

	ARCP inverter	SARCP inverter
The main switch	6	6
The auxiliary switch	6	6
The auxiliary diode	0	6
The auxiliary inductor	3	2
The value of the dc-link capacitances	C_A	$< 0.67{*}C_A$

TABLE II
COMPARISON OF THEORETICAL POWER LOSS OF TWO INVERTERS

	ARCP inverter	SARCP inverter
Loss of auxiliary commutation inductor	1	<4/5
The conduction loss of auxiliary switch transistors	1	<4/5
Total loss of the auxiliary circuits	1	<4/5

For the SARCP inverter, the current average value of L_r is $I_{\mathrm{av\cdot S}}$, and the total conduction loss of the auxiliary circuits is P_{conS}. In SECT 2, the commutation processes of phase-A and phase-B are synchronously assisted by L_{r1}. In the auxiliary circuits, when the auxiliary current in one phase is approximately I_{chS} and the other phase is approximately 0, P_{conS} can be maximized. Combining (19) with (25), P_{conS} is

$$\begin{aligned} P_{\mathrm{conS}} &\le (v_{\mathrm{d0}} I_{\mathrm{av-S}} + r_{\mathrm{d}} I^2{}_{\mathrm{Lr\_RMS\_S}} + r_s I^2{}_{\mathrm{Lr\_RMS\_S}}) \\ &= \frac{2 v_{\mathrm{d0}} L_r f_k}{V_{dc}} (I_{\max} + I_{\mathrm{boost}})^2 \\ &\quad + \frac{4 L_r f_k}{3 V_{\mathrm{dc}}} (I_{\max} + I_{\mathrm{boost}})^3 (r_{\mathrm{d}} + r_s). \end{aligned} \tag{27}$$

Combining (26) with (27), it can be concluded that the total conduction loss of the auxiliary switching transistors of the SARCP inverter is less than four-fifths of that of the ARCP inverter ($P_{\mathrm{conS}} < 4P_{\mathrm{conA}}$ /5).

To compare the theoretical losses of the auxiliary circuits of the two inverters, the values of the power loss of the ARCP inverter are taken as reference "1." The values of the power losses of the SARCP inverter are shown in Table II.

In summary, the total power loss of the auxiliary circuit of the SARCP inverter is less than four-fifths of that of the ARCP inverter. Since the power losses of the main circuits of the two inverters are approximately equal, the SARCP inverter has a smaller total power loss.

V. SIMULATION AND EXPERIMENTAL RESULTS

To verify the above theoretical analysis, a simulation model in Simulink and a 1-kW prototype of the SARCP inverter are built. The output ac voltage frequency (f_{base}) is 250 Hz. And the parameters of the SARCP inverter are shown in Table III.

TABLE III
PARAMETERS OF THE SARCP INVERTER

Components	Parameters
DC-link voltage (V_{dc})	50 V
L_{r1} and L_{r2}	0.22μH
C_{dc1} and C_{dc2}	130μF
Switching frequency (f_k)	20 kHz
Dead time (T_d)	190 ns
The controller	STM32G431CBT6
The main switch ($S_1 \sim S_6$)	FDMT800150DC
The auxiliary switch ($S_{x1} \sim S_{x6}$)	EPC2033
The auxiliary diode ($D_1 \sim D_6$)	ES3C-13-F
Resistance-inductive load	R = 1Ω, L = 47μH, cosφ=0.99

A. Simulation Results

In one switching cycle, for the SARCP inverter, the commutation processes of the two-phase circuit are synchronously assisted by an auxiliary commutation inductor. In SECT 2, the commutation processes of the phase-A and phase-B circuits are synchronously assisted by L_{r1}. Phase-A circuit is under the heavy load current conditions, and the phase-B circuit is in the light load current conditions. The simulation waveform in Fig. 9 shows the commutation process of phase-A. The commutation waveform of phase-B is shown in Fig. 10.

Figs. 9(a) and 10(a) show the waveforms of S_2 and S_4 during turn-OFF transition, respectively. Due to the effects of parasitic capacitances, S_2 and S_4 are turned OFF under pseudo-ZVS conditions. Figs. 9(b) and 10(b) show the waveforms of S_1 and S_3 during turn-ON transition, respectively. It can be clearly seen that the gate drive signal is sent out after U_{S1} and U_{S3} decrease to zero. S_1 and S_3 are turned ON under ZVS conditions. Figs. 9(c) and 10(c) show the waveforms of S_{x1} and S_{x3} during turn-ON and turn-OFF transitions, respectively. Figs. 9(d) and 10(d) show the waveforms of D_1 and D_3 during turn-ON and turn-OFF transitions, respectively. The currents flowing through S_{x1}, D_1 and S_{x3}, D_3 are buffered by L_{r1}, so they can be turned ON and turned OFF under ZCS conditions.

B. Experimental Results

A 1-kW prototype of the SARCP inverter is built, and the size of the prototype is shown in Fig. 11.

The neutral voltage of dc-link capacitors V_m and the inverter output current waveforms are shown in Fig. 12. V_m fluctuates around V_{dc} / 2 but always remains stable.

In SECT 2, the commutation processes of phase-A and phase-B are synchronously assisted by L_{r1}. To illustrate that this commutation process is not affected by the values of i_a

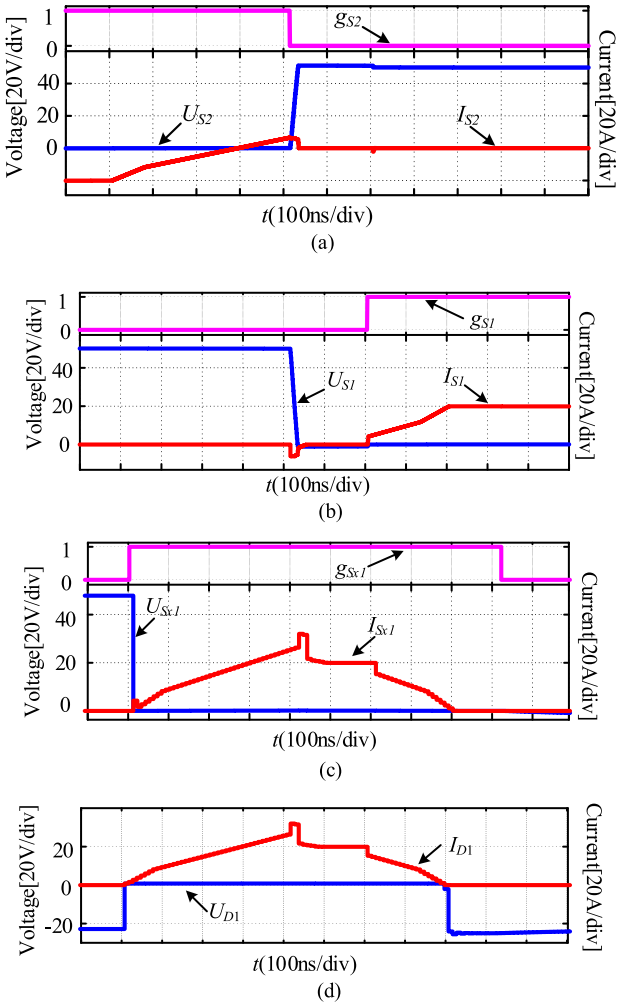

Fig. 9. Voltage and current simulation waveforms of phase A of the SARCP inverter. (a) S_2 turn-OFF. (b) S_2 turn-ON. (c) S_{x1} turn-ON and turn-OFF. (d) D_1 turn-ON and turn-OFF.

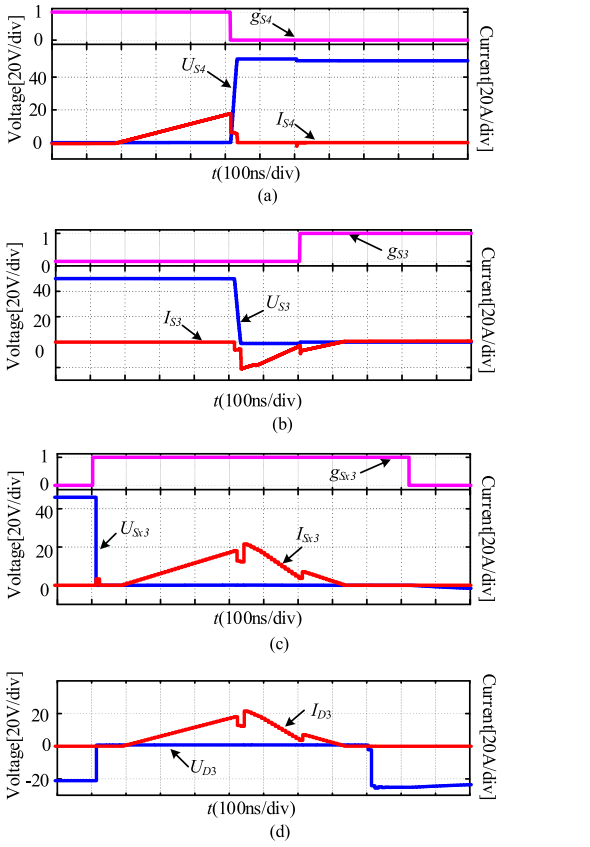

Fig. 10. Voltage and current simulation waveforms of phase B of the SARCP inverter. (a) S_4 turn-OFF. (b) S_3 turn-ON. (c) S_{x3} turn-ON and turn-OFF. (d) D_3 turn-ON and turn-OFF.

and i_b, the soft-switching waveforms for main switches under different load current conditions are given, respectively. When $i_a = 20$ A and $i_b = 1$ A, the waveforms of the synchronous turn-OFF processes of S_2 and S_4 are shown in Fig. 13, and the waveforms of the synchronous turn-ON processes of S_1 and S_3 are shown in Fig. 14. When $i_a = 11$ A and $i_b = 10$ A, the waveforms of the synchronous turn-ON processes of S_1 and S_3 are shown in Fig. 15.

As shown in Fig. 13, due to the parasitic capacitances, both S_2 and S_4 can achieve pseudo-ZVS turn-OFF. Figs. 14 and 15 show that the driving voltages of both S_1 and S_3 start to rise after U_{S1} and U_{S3} fall to zero, proving that S_1 and S_3 can be synchronously assisted by L_{r1} to achieve ZVS turn-ON.

Fig. 16 shows the energy conversion efficiency curve of the SARCP inverter and the hard-switching counterpart. When the output power is 1 kW, the efficiency of the SARCP inverter and the hard-switching counterpart is 99.1% and 98.3%, respectively.

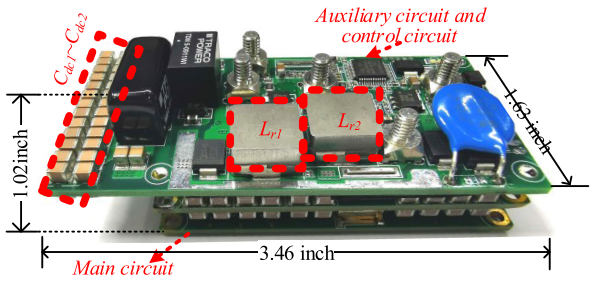

Fig. 11. 1-kW prototype of the SARCP inverter.

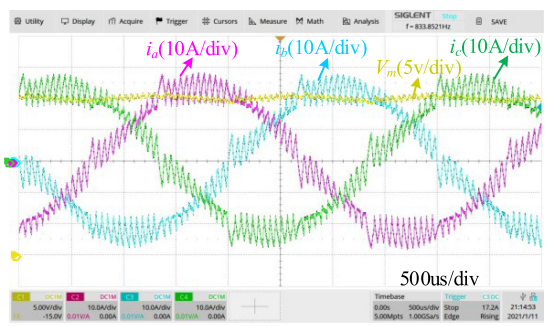

Fig. 12. Neutral voltage of DC-link capacitors and the inverter output current waveform.

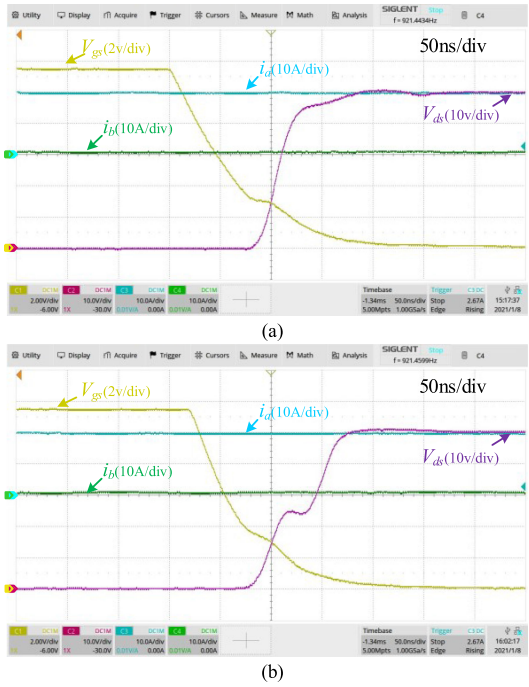

Fig. 13. Voltage and current waveforms of S_2 and S_4 turn-OFF processes ($i_a = 20$ A and $i_b = 1$ A). (a) S_2 turn-OFF. (b) S_4 turn-OFF.

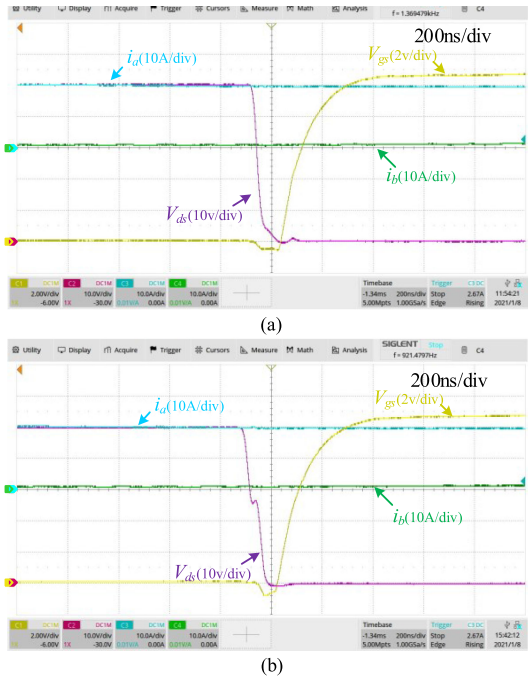

Fig. 14. Voltage and current waveforms of S_1 and S_3 turn-ON processes ($i_a = 20$ A and $i_b = 1$ A). (a) S_1 turn-ON. (b) S_3 turn-ON.

In summary, all main switches of the SARCP inverter can achieve ZVS turn-ON and pseudo-ZVS turn-OFF. And all auxiliary switches of the SARCP inverter can achieve ZCS turn-ON and turn-OFF. And the efficiency of the SARCP inverter is 0.8% higher than that of the hard-switch counterpart. The simulation and experiment results verify the effectiveness of the SARCP inverter.

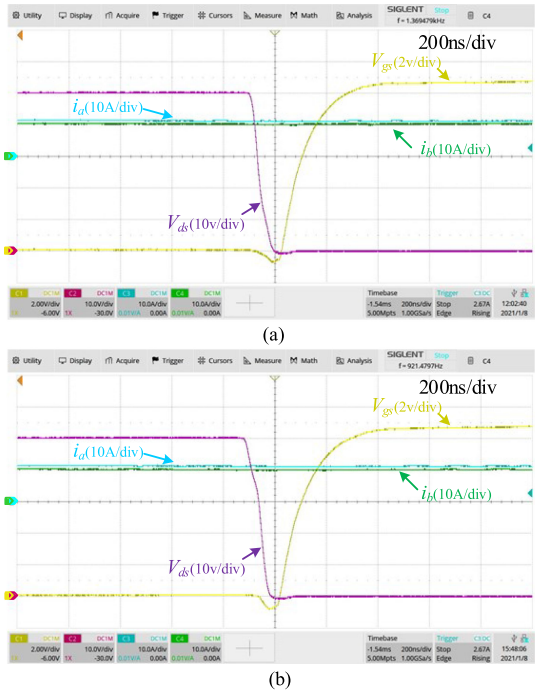

Fig. 15. Voltage and current waveforms of S_1 and S_3 turn-ON processes ($i_a = 11$ A and $i_b = 10$ A). (a) S_1 turn-ON. (b) S_3 turn-ON.

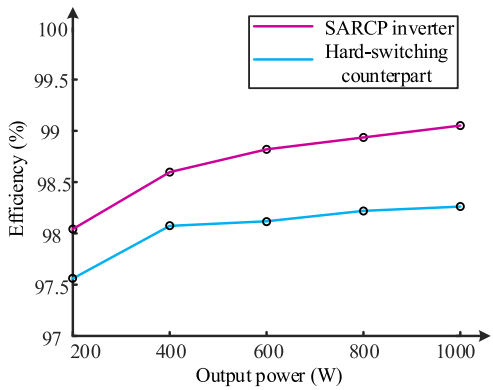

Fig. 16. Experimental efficiency curve.

VI. Conclusion

In order to overcome defects of the ARCP inverter, an SARCP soft-switching inverter with improved load adaptability is proposed. Theoretical analysis and experimental results draw the following conclusions.

1) All switches in the main circuit can achieve ZVS turn-ON and pseudo-ZVS turn-OFF. And all switches in the auxiliary circuit can achieve ZCS turn-ON and turn-OFF;
2) compared with the ARCP inverter, when fixed timing control is applied to the two inverters, the SARCP inverter has improved load adaptability, especially under the light load current condition;
3) compared with the ARCP inverter, the SARCP inverter has fewer auxiliary inductors, smaller dc-link capacitance, and lower total power loss, which is more effective to reduce the volume of the device and improve the efficiency; 4)

when the rated power of the inverter is 1 kW, the SARCP inverter can achieve an energy conversion efficiency of 99.1%. Under the same conditions, compared with the hard-switching inverter, the SARCP inverters can improve the energy conversion efficiency by 0.8%.

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Wenkang Gong (Graduate Student Member, IEEE) was born in Jingzhou, China, in 1997. He received the B.S. degree from Northeastern University, Shenyang, China, in 2019. He is currently working toward the M.S. degree in electrical engineering and automation with Wuhan University, Wuhan, China.

His research interests include soft-switching technology, and high-efficiency and high-power-density converters.

Shangzhi Pan (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1998 and 2001, respectively, and the Ph.D. degree from Queen's University, Kingston, ON, Canada, in 2008.

In 2018, he joined the College of Electrical Engineering, Wuhan University, Wuhan, China, where he is currently a Professor. He has also been an Adjunct Faculty with the Queen's Center of Energy and Power Electronics Applied Research Laboratory (ePOWER) since 2014. Previously, he was the VP of research and development with SPARQ Systems, a Queen's Spun-off photovoltaic microinverter company, in 2010. He was a Senior Research Engineer with Queen's University from 2008 to 2013. His research interests include digital control techniques for power converters, grid-connected inverters, voltage regulators for computing systems, power converters for renewable energy sources, and power converters for electric vehicles.

Wenqiang Lin was born in Quanzhou, China, in 1992. He received the B.S. degree from Fuzhou University, Fuzhou, China, in 2016. He is currently working toward the Ph.D. degree in electrical engineering with Wuhan University, Wuhan, China.

His research interests include soft-switching technology, and high-efficiency and high-power-density converters.

Yuan Shang was born in Shiyan, China, in 1995. He received the B.S. degree from the University of Electronic Science and Technology, Chengdu, China, in 2018. He is currently working toward the M.S. degree in electrical engineering and automation with Wuhan University, Wuhan, China.

His research interests include soft-switching technology, and high-efficiency and high-power-density converters.

Jinwu Gong (Member, IEEE) received the B.Eng. and Ph.D. degrees in electrical engineering from Wuhan University, Wuhan, China, in 2004 and 2012, respectively.

From 2017 to 2018, he was a Visiting Scholar with FEEC. He is currently an Associate Professor with Wuhan University. His current research interests include wide bandgap devices, design of high-efficiency and high-power-density power electronic converters, applications of power electronics technology in power systems, and key technologies of large-capacity power quality control equipment.

Fei Liu (Senior Member, IEEE) was born in Hanchuan, China, in 1977. He received the B.S., M.S., and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 2000, 2004, and 2008, respectively.

He has been a faculty member with Wuhan University since 2010 and is currently an Associate Professor with the School of Electrical Engineering, Wuhan University, Wuhan, China. His research interests include dc microgrid, cascaded multilevel converter, and interface of utility-scale photovoltaic conversion systems.

Xiaoming Zha (Member, IEEE) was born in Huaining, China, in 1967. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Wuhan University, Wuhan, China, in 1989, 1992, and 2001, respectively.

He was a Postdoctoral Fellow with the University of Alberta, Canada, from 2001 to 2003. He has been a faculty member with Wuhan University, since 1992, and became a Professor in 2003. He is currently the Deputy Dean with the School of Electrical Engineering, Wuhan University. His research interests include power electronic converter, the application of power electronics in smart grid and renewable energy generation, the analysis and control of microgrid, the analysis and control of power quality, and frequency control of high-voltage high-power electric motors.