A Single-Switch High Step-Up DC–DC Converter Based on Three-Winding Coupled Inductor and Pump Capacitor Unit

Jie Ding, Shiwei Zhao, *Member, IEEE*, Shuang Gao, and Huajie Yin

***Abstract*—In this article, a novel single-switch, high step-up dc–dc converter based on three-winding coupled inductor and voltage multiplier circuit (VMC) is proposed. And on this basis, pump capacitor unit (PCU) is integrated to achieve a very high voltage gain. The converter makes full use of the advantages of three-winding coupled inductor, skillfully combines it with the VMC, and integrates the PCU that can be used in superposition to further improve the voltage gain. The voltage stress of the switch is reduced by using a passive clamping circuit to recycle the leakage energy of the coupled inductor. The operating principle and steady-state analysis of the presented converter in continuous conduction mode are introduced in detail. Moreover, the comparative analysis shows that under the same conditions, the proposed converter has higher voltage gain and lower voltage stress than others. Several advantages include high voltage gain, low voltage stress, low turns ratio of coupled inductor, and high conversion efficiency, make the proposed converter very suitable for new energy generation applications, such as photovoltaic systems. Finally, the feasibility of the proposed converter and the correctness of theoretical analysis are verified by a 500-W prototype at 50 kHz switching frequency.**

***Index Terms*—Circuits and systems, low-power electronics, MOSFET circuits, power semiconductor switches, switched capacitor circuits, switched circuits, switched mode power supplies, switching converters.**

I. Introduction

With the intensification of global problems such as energy crisis, greenhouse effect and air pollution, new renewable, and environment-friendly energy sources have developed rapidly. Due to the characteristics of pollution-free, renewable and high reliability, photovoltaics and fuel cells have been widely used and studied in recent years [1], [2]. The output voltage of a typical photovoltaic module is 30–50 V and the power is about 200–500 W. In order to raise its voltage to the conventional dc bus voltage (360–400 V) to connect the grid, a dc–dc converter with a high voltage gain is needed. However, the conversion efficiency of the converter is closely related to the efficiency of the photovoltaic power generation system. Therefore, it is an urgent problem to study the high-voltage gain and high-efficiency dc–dc converter suitable for low and medium power applications [3].

Limited by parasitic parameters, voltage stress of semiconductor device, conversion efficiency, and other factors, it is difficult for basic Boost and Buck–Boost converters to achieve high voltage gain. Therefore, scholars at home and abroad have proposed a variety of solutions for the high step-up dc–dc converter in the new energy generation applications.

On the basis of the traditional Boost converter, the voltage conversion ratio of the converter can be improved by increasing the switched capacitor and switched inductor network units [4]–[6]. However, the higher the voltage gain is, the more switched capacitor/inductor network units need to be used, which not only reduces the efficiency and reliability of the converter but also increases the cost. Pan *et al.* [7]–[9] integrate switched capacitors in an interleaved converter. Although it can improve the voltage gain, the voltage transmission ratio is still limited, so it cannot meet the occasion of higher voltage gain conversion. Moreover, the switch and the inductor are twice that of the original. So, the power density is low, the cost is high, and the drive control is complicated. A second winding is added on the inductor to form a coupled inductor converter in [10] and [11]. However, when such converters realize high voltage gain conversion, the turns ratio of coupled inductor is too high, resulting in increased leakage inductor and excessive voltage stress of components. In order to solve this problem, Andrade *et al.* [12]–[17] and Wai and Duan [36] integrate the switched capacitor in the coupled inductor converter. Although the turns ratio of the coupled inductor can be reduced to a certain extent, when the voltage gain is further increased, it is inevitable that there will be more switched capacitors, resulting in a larger number of components. Which will reduce the power density, efficiency, and reliability of the converter. Choudhury [18] and Lee [19] apply the coupled inductor to the quadratic Boost converter to form a cascaded coupled inductor dc–dc converter. Although this kind of converters can achieve very high voltage gain under the condition of low turns ratio of coupled inductor, the voltage stress of the switch is relatively large, and the conduction loss

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The authors are with the School of Electrical Engineering, South China University of Technology, Guangzhou 510640, China (e-mail: 726991596@qq.com; epswzhao@scut.edu.cn; 1191996890@qq.com; epyin@scut.edu.cn).

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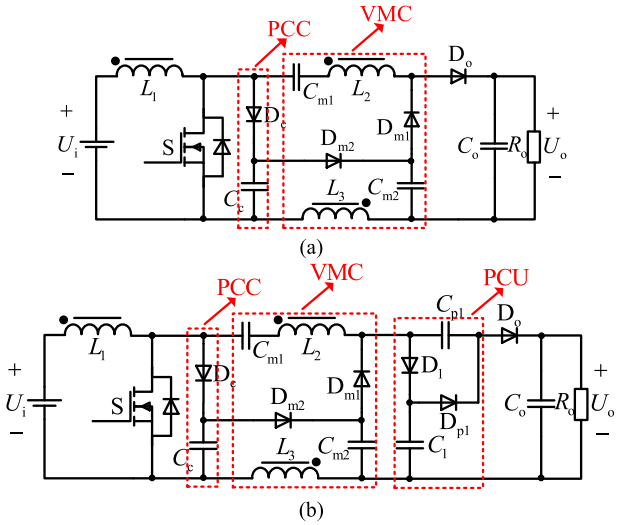

Fig. 1. Proposed converter topology.

of the diode in the front stage is very large, so the efficiency of the converter is low. High step-up converter with three-winding coupled inductor can achieve higher voltage gain with a certain number of components, so more and more researchers begin to study it recently [20]–[34].

This article presents a single-switch, high-voltage gain dc–dc converter based on three-winding coupled inductor and pump capacitor unit (PCU). Due to the integration of voltage multiplier circuit (VMC) and PCU, the voltage conversion ratio is very high, and the voltage stress of power devices is very low of the proposed converter. Therefore, the power devices with low voltage level and low conduction loss can be selected to improve the efficiency of the converter. The three-winding coupled inductor provides a static voltage gain, while the VMC and the PCU provide an additional voltage gain. Moreover, the application of three-winding coupled inductor cannot only adjust the voltage gain but also flexibly regulate the voltage stress of components. The superiority of the proposed converter and the feasibility of its application in photovoltaic power generation systems are demonstrated through comparative analysis with similar converter presented recently and experimental results.

II. Operation Principle and Steady-State Analysis of Proposed Converter

The presented topology is shown in Fig. 1(a) consists of passive clamping circuit (PCC: diode D_c, capacitor C_c), VMC (diodes D_{m1}, and D_{m2} capacitors C_{m1}, and C_{m2}), output circuit (diode D_o, capacitor C_o), main switch (S), and three-winding coupled inductor (L_1, L_2, and L_3). The circuit structure is shown in Fig. 1(b) integrates the PCU (diodes D_1, and D_{p1}, capacitor C_1, and C_{p1}) on the basis of Fig. 1(a). For convenience of analysis, as shown in Fig. 2, the coupled inductor model is regarded as an ideal transformer with turns ratio of $n_1/n_2/n_3$ and the magnetizing inductor L_m, in parallel, and then in series with the leakage inductor L_k, where L_k is the sum of the primary side leakage inductor and the secondary–tertiary side conversion to the primary side leakage inductor.

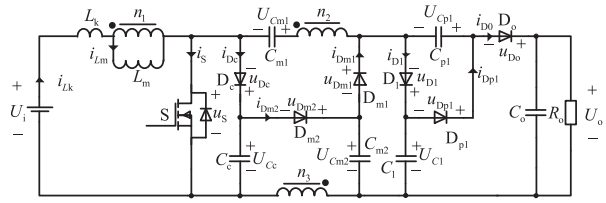

Fig. 2. Equivalent circuit of the converter topology proposed in Fig. 1(b).

To simplify the circuit analysis in proposed converter, some assumptions are presumed in the following.

1) All components are ideal, without considering parasitic parameters.
2) All capacitors are large enough that their voltage ripple can be ignored.
3) The turns ratio N_{21} of the coupled inductor is defined as $N_{21} = n_2: n_1$ and the turns ratio N_{31} is defined as $N_{31} = n_3: n_1$.

The converter has five modes in a switching cycle T_s, and the current flow path of each mode and the main operating waveforms in continuous conduction mode (CCM) are shown in Figs. 3 and 4, respectively. The main operating process is described as follows.

Mode I [t_0-t_1]: In this mode, the main switch S and diodes D_{m2}, D_1, and D_o are ON, and diodes D_c, D_{m1}, and D_{p1} are OFF. In this short process, the current of leakage inductor i_{Lk}, increases linearly, and the secondary-tertiary winding current of the coupled inductor decreases linearly. As shown in Fig. 3(a), the secondary and tertiary side winding is in series with capacitor C_{m1} to charge capacitor C_1 through diode D_1. It is also connected in series with capacitors C_{m1}, and C_{p1} to power the output capacitor C_o and load R_o. The capacitor C_c and tertiary side winding charge the capacitor C_{m2}. At time t_1, the current of leakage inductor rises to the same as the magnetizing current i_{Lm}, that is, when the secondary-tertiary side winding current decreases to zero, the diodes D_{m2}, D_o, and D_1 are turned OFF to enter mode II.

Mode II [t_1-t_2]: As shown in Fig. 3(b), the switch S, and diodes D_{m1}, and D_{p1} are turned ON, and diodes D_c, D_{m2}, D_1 and D_o are turned OFF. The currents of leakage inductor and magnetizing inductor increase linearly under the action of the input voltage, U_i. Meanwhile, the secondary, tertiary side winding and the capacitor C_{m2} start to charge capacitor C_{m1} through diode D_{m1}, and capacitor C_1 starts to charge capacitor C_{p1} through diode D_{p1}. The output capacitor C_o supplies power to the load solely. At time t_2, the switch S is turned OFF, and mode III is entered. By applying Kirchhoff voltage law on the circuit, the voltage of magnetizing inductor, u_{Lm-II}, and capacitors C_c, C_{m1}, C_{m2}, C_1, and C_{p1}, U_{Cc}, U_{Cm1}, U_{Cm2}, U_{C1}, and U_{Cp1}, satisfy the following relationship:

$$u_{Lm-\mathrm{II}} = U_i \tag{1}$$

$$U_{Cm1} = (N_{21} + N_{31})u_{Lm-\mathrm{II}} + U_{Cm2} \tag{2}$$

$$U_{Cp1} = U_{C1} - U_{Cm2}. \tag{3}$$

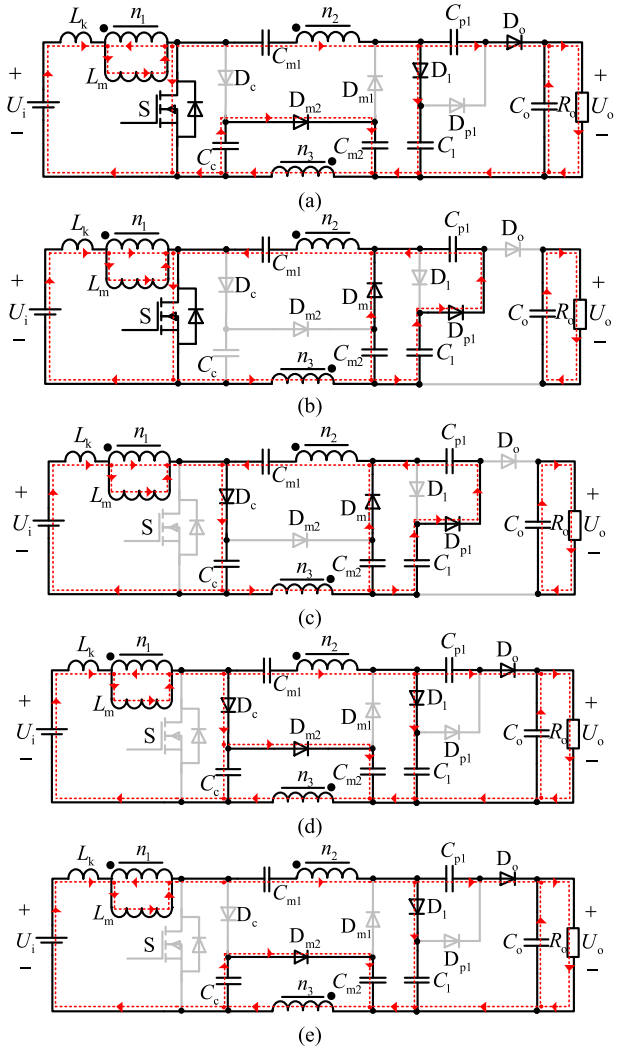

Fig. 3. Current flow path of presented converter in one period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

Mode III [t_2-t_3]: In this brief process, the switch S, and diodes D_{m2}, D_1, and D_o are OFF, and diodes D_c, D_{m1}, and D_{p1} are ON. According to Fig. 3(c), leakage inductor energy is absorbed by capacitor C_c through diode D_c. Due to the role of leakage inductor, the diodes D_{m1} and D_{p1} continue to conduct until t_3, when the current of leakage inductor drops to the same as the magnetizing current, that is the secondary–tertiary side winding current decreases to zero, the diodes D_{m1} and D_{p1} are turned OFF, and this mode ends to enter the mode IV.

Mode IV [t_3-t_4]: As shown in Fig. 3(d), the switch S, and diodes D_{m1} and D_{p1} are OFF, and diodes D_c, D_{m2}, D_1, and D_o are ON. At this point, the coupled inductor and capacitors C_{m1}, and C_{p1} in series to power the output capacitor C_o and load R_o. At time t_4, the switch S is turned ON to enter mode V. In this mode, the voltage of magnetizing inductor, $u_{Lm-\mathrm{IV}}$, capacitors C_1, C_{m2}, U_{C1}, U_{Cm2}, and the output voltage U_o are, respectively, as follows:

$$u_{Lm-\mathrm{VI}} = U_i - U_{Cc} \tag{4}$$

$$U_{C1} = U_{Cc} + U_{Cm1} - (N_{21} + N_{31})u_{Lm-\mathrm{VI}} \tag{5}$$

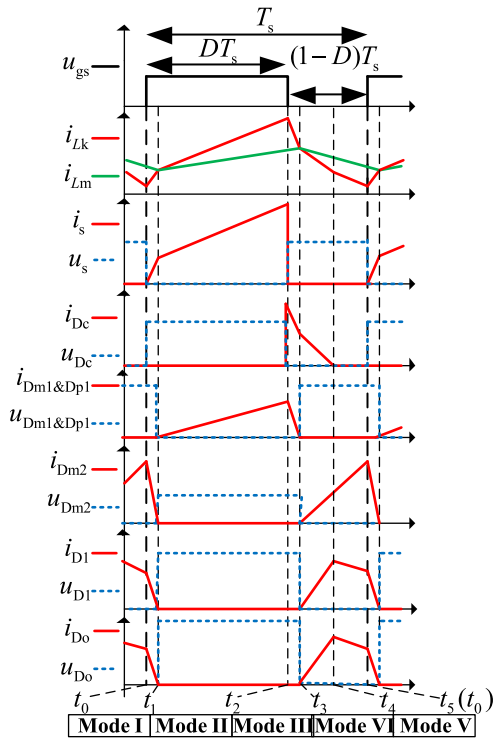

Fig. 4. Main waveforms of the proposed converter in CCM operation.

$$U_{Cm2} = U_{Cc} - N_{31}u_{Lm-\mathrm{VI}} \tag{6}$$

$$U_o = U_{C1} + U_{Cp1}. \tag{7}$$

Mode V [t_4-t_5]: As shown in Fig. 3(e), the switch S, and diodes D_{m1}, D_c, and D_{p1} are OFF, and diodes D_1, D_{m2}, and D_o are ON. In this mode, the clamp diode D_c naturally turns OFF and there is no reverse-recovery problem for D_c, the other current paths are the same as the previous mode. This interval ends when the switch S is turned ON at $t = t_5$, which is the beginning of the next switching period.

From the above-mentioned analysis, in the VMC, the tertiary winding L_3 of the coupled inductor which placed in the power supply loop for the output load is fully used to achieve high voltage gain. When the switch S is ON, the voltage of the secondary winding L_2, tertiary winding L_3, and capacitor C_{m2} is transferred to C_{m1}. When the switch S is OFF, the voltage of capacitor C_c and the third winding L_3 is transferred to capacitor C_{m2}. Meanwhile, the voltage of L_3 can also be transferred to the output capacitor C_o. The PCU can be used to further improve the voltage gain of the converter. During the switch-on period, the voltage of the already high voltage capacitor C_1 is transferred to C_{p1}. During the switch-OFF period, the voltage of capacitor C_{p1} is transferred to the output capacitor C_o. Therefore, these two combinations further improve the voltage gain of the proposed converter.

In order to simplify the steady-state analysis of the converter, the two transient processes I and III caused by leakage inductor are ignored, and only modes II, IV, and V are considered. According to the volt-second balance of the magnetizing inductor,

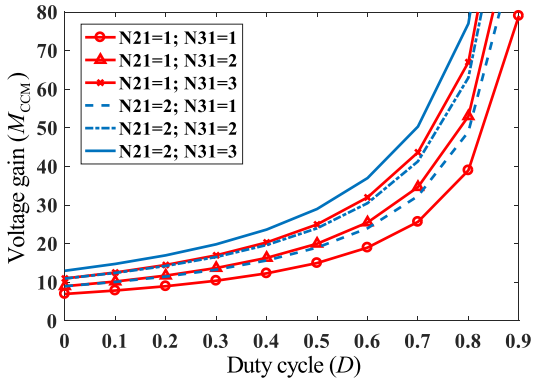

Fig. 5. Voltage gain curve with different turn ratio of coupled inductor.

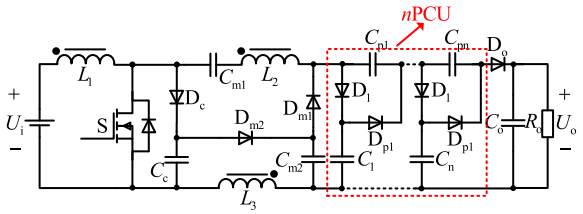

Fig. 6. High step-up dc–dc converter based on three-winding coupled inductor and *n*PCU.

it can be written as follows:

$$Du_{Lm-\mathrm{II}} + (1-D)u_{Lm-\mathrm{VI}} = 0 \tag{8}$$

where D is the duty cycle of the main switch S.

From (1)–(8), it can be obtained as follows:

$$U_{Cc} = U_\mathrm{i}/(1-D) \tag{9}$$

$$U_{C\mathrm{m1}} = [1 + N_{21}(1-D) + N_{31}]U_\mathrm{i}/(1-D) \tag{10}$$

$$U_{C\mathrm{m2}} = (1 + DN_{31})U_\mathrm{i}/(1-D) \tag{11}$$

$$U_{C1} = [2 + (N_{21} + N_{31} + N_{31}D)]U_\mathrm{i}/(1-D) \tag{12}$$

$$U_{C\mathrm{p1}} = (1 + N_{21} + N_{31})U_\mathrm{i}/(1-D) \tag{13}$$

$$M_\mathrm{CCM} = U_\mathrm{o}/U_\mathrm{i} = [3 + 2N_{21} + (2+D)N_{31}]/(1-D) \tag{14}$$

where M_CCM is the voltage gain of the converter operating in CCM.

The ideal voltage gain of the presented converter operating in CCM, M_CCM, changing with duty cycle of the switch under different turns ratio of the coupled inductor are shown in Fig. 5. It can be seen that a very high voltage gain can be obtained by adjusting the turns ratio of the coupled inductor without extremely large duty cycle of the switch. Moreover, when the converter is applied to distributed generation system, the turns ratio of the coupled inductor is not too high.

When the voltage gain needs to be further increased, the number of PCUs can be increased, as shown in Fig. 6. Similarly, the voltage gain of the converter with n PCUs can be expressed as follows:

$$M_\mathrm{CCM} = \frac{U_\mathrm{o}}{U_\mathrm{i}} = \frac{2 + n + (1+n)N_{21} + (1+n+D)N_{31}}{1-D}. \tag{15}$$

From (15), we can see that every time a PCU is added, the voltage gain increases by $(1+N_{21}+N_{31})/(1-D)$, and the voltage stress on the switching device will be further reduced. Of course, excessive number of PCUs will also bring some disadvantages, such as increasing the design cost and volume of the converter, which is not conducive to the miniaturization of the converter, etc., so it needs to be considered in many aspects in actual engineering applications.

III. Key Parameter Design of Proposed Converter

When selecting switches and diodes, it is necessary to calculate their voltage and current stresses, which are as follows.

A. Voltage Stress Analysis

According to the operating principle of the converter, the voltage stress of the components can be calculated as follows:

$$U_{\mathrm{S,\ Dc-stress}} = U_\mathrm{o}/[3 + 2N_{21} + (2+D)N_{31})] \tag{16}$$

$$U_{\mathrm{Dm1-stress}} = (1+N_{21}+N_{31})U_\mathrm{o}/[3+2N_{21}+(2+D)N_{31})] \tag{17}$$

$$U_{\mathrm{Dm2-stress}} = N_{31}U_\mathrm{o}/[3 + 2N_{21} + (2+D)N_{31})] \tag{18}$$

$$U_{\mathrm{D1,Dp1,Do-stress}} = \frac{(1 + N_{21} + N_{31})U_\mathrm{o}}{3 + 2N_{21} + (2+D)N_{31}} \tag{19}$$

where $U_{\mathrm{S,\ Dc\text{-}stress}}$ is the voltage stress of the switch S and diode $\mathrm{D_c}$; $U_{\mathrm{Dm1\text{-}stress}}$ and $U_{\mathrm{Dm2\text{-}stress}}$ are the voltage stresses of $\mathrm{D_{m1}}$, and $\mathrm{D_{m2}}$, respectively; $U_{\mathrm{D1,\ Dp1,\ Do\text{-}stress}}$ is the voltage stress of diodes $\mathrm{D_1}$, $\mathrm{D_{p1}}$, and $\mathrm{D_o}$.

B. Current Stress Analysis

Through the analysis of the converter in CCM, the ripple of magnetizing current can be written as follows:

$$\Delta I_{Lm} = DU_\mathrm{i}/(f_\mathrm{s}L_\mathrm{m}) \tag{20}$$

where f_s is the switching frequency of the converter.

The average value of magnetizing current can be written as follows:

$$I_{Lm} = I_\mathrm{i} = [3 + 2N_{21} + (2+D)N_{31}]I_\mathrm{o}/(1-D) \tag{21}$$

where I_i and I_o are the average values of input and output currents, respectively.

Hence, the peak value of magnetizing current can be expressed as follows:

$$i_{Lm-\mathrm{peak}} = \frac{[3 + 2N_{21} + (2+D)N_{31}]\,I_\mathrm{o}}{1-D} + \frac{DU_\mathrm{i}}{2f_\mathrm{s}L_\mathrm{m}}. \tag{22}$$

According to the charge conservation of capacitors, the average current of diodes $\mathrm{D_o}$, $\mathrm{D_c}$, $\mathrm{D_{m1}}$, $\mathrm{D_{m2}}$, $\mathrm{D_{p1}}$, and $\mathrm{D_1}$ is equal to the output current I_o, so the peak current of each diode and switch can be approximately expressed as follows:

$$\begin{aligned} i_{\mathrm{Do-peak}} &= i_{\mathrm{Dc-peak}} = i_{\mathrm{D1-peak}} \\ &= i_{\mathrm{Dm2-peak}} = 2I_\mathrm{o}/(1-D) \end{aligned} \tag{23}$$

$$i_{\mathrm{Dm1-peak}} = i_{\mathrm{Dp1-peak}} = 2I_\mathrm{o}/D \tag{24}$$

TABLE I
PERFORMANCE COMPARISON OF VARIOUS CIRCUIT TOPOLOGIES

Converters	Number of Components				Voltage gain	Voltage stress on main switch	Voltage stress on output diode	Max Efficien, %
	S	D	C	CL+L				
Fig. 1(a)	1	4	4	1^{3w}+0	$[2+N_{21}+N_{31}(1+D)]/(1-D)$	$U_o/[2+N_{21}+N_{31}(1+D)]$	$(1+N_{21}+N_{31})U_o/[2+N_{21}+N_{31}(1+D)]$	98.24 at 200W
Fig. 1(b)	1	6	6	1^{3w}+0	$[3+2N_{21}+N_{31}(2+D)]/(1-D)$	$U_o/[3+2N_{21}+N_{31}(2+D)]$	$(1+N_{21}+N_{31})U_o/[3+2N_{21}+N_{31}(2+D)]$	97.92 at 200W
[20]	2	6	6	1^{3w}+0	$(2+N_{21}+N_{31})/[2(1-D)]$	$U_o/(2+N_{21}+N_{31})$	$(N_{21}+N_{31})U_o/[2(2+N_{21}+N_{31})]$	97.82 at 250W
[21]	1	6	6	1^{3w}+0	$[3+2N_{21}+N_{31}(1+D)]/(1-D)$	$U_o/[3+2N_{21}+N_{31}(1+D)]$	$(1+N_{31})U_o/[3+2N_{21}+N_{31}(1+D)]$	94.70 at 107W
[22]	1	6	6	1^{3w}+0	$[2+N_{21}+N_{31}(2-D)]/(1-D)$	$U_o/[2+N_{21}+N_{31}(2-D)]$	$(1+N_{21})U_o/[2+N_{21}+N_{31}(2-D)]$	95.07 at 50W
[23]	2	5	5	1^{3w}+0	$[2+D+N_{31}(1+D)]/(1-D)$	$U_o/[2+D+N_{31}(1+D)]$	$(1+N_{31})U_o/[2+D+N_{31}(1+D)]$	95.31 at 175W
[24]	3	4	5	1^{3w}+0	$(2+N_{21}+N_{31})/[2(1-D)]$	$U_o/(2+N_{21}+N_{31})$	$(1+N_{21})U_o/(2+N_{21}+N_{31})$	95.62 at 60W
[25]	1	5	5	1^{3w}+0	$(3+2N_{21}+N_{31})/(1-D)$	$U_o/(3+2N_{21}+N_{31})$	$(1+N_{21}+N_{31})U_o/(3+2N_{21}+N_{31})$	96.20 at 180W
[26]	1	5	5	1^{3w}+0	$(3+N_{21}+N_{31})/(1-D)$	$U_o/(3+N_{21}+N_{31})$	$(1+N_{21}+N_{31})U_o/(3+N_{21}+N_{31})$	\\
[27]	1	5	5	1^{3w}+0	$(1+N_{21}+N_{31}D)/(1-D)$	$U_o/(1+N_{21}+N_{31}D)$	$N_{21}U_o/(1+N_{21}+N_{31}D)$	96.70 at 115W
[28]	2	4	5	1^{3w}+0	$(3+2N_{21}+N_{31})/(1-D)$	$U_o/(3+2N_{21}+N_{31})$	$(1+N_{21}+N_{31})U_o/(3+2N_{21}+N_{31})$	93.90 at 120W
[29]	2	4	4	1^{3w}+0	$(1+D+N_{31})/(1-D)$	$U_o/(1+D+N_{31})$	$N_{31}U_o/(1+D+N_{31})$	96.40 at 300W
[30]	2	4	3	1^{3w}+1	$(1+N_{31})/(1-D)$	$U_o/(1+N_{31})$	$N_{31}U_o/(1+N_{31})$	97.52 at 250W
[31]	1	4	4	1^{3w}+0	$[2-D+N_{21}(1-D)+N_{31})]/(1-D)$	$U_o/[2-D+N_{21}(1-D)+N_{31})]$	$N_{31}U_o/[2-D+N_{21}(1-D)+N_{31})]$	96.81 at 600W
[32]	1	4	4	1^{3w}+0	$(2N_{21}+N_{31}-1)/[(1-D)(N_{21}-1)]$	$(N_{21}-1)U_o/(2N_{21}+N_{31}-1)$	$N_{31}U_o/(2N_{21}+N_{31}-1)$	97.70 at 300W
[33]	1	4	4	1^{3w}+0	$(2+N_{21}+N_{31})/(1-D)$	$U_o/(2+N_{21}+N_{31})$	$(1+N_{21}+N_{31})U_o/(2+N_{21}+N_{31})$	98.00 at 100W
[34]	2	3	4	1^{3w}+0	$(2+N_{21}+N_{31})/(1-D)$	$U_o/(2+N_{21}+N_{31})$	$N_{31}U_o/(2+N_{21}+N_{31})$	95.20 at 110W
[12]	1	8	8	1^{2w}+0	$[4+N_{21}(2-D)-D]/(1-D)$	$U_o/[4+N_{21}(2-D)-D]$	$[N_{21}(2-D)-D]U_o/[4+N_{21}(2-D)-D]$	\\
[13]	1	6	6	1^{2w}+0	$[2+N_{21}(2-D)]/(1-D)$	$U_o/[2+N_{21}(2-D)]$	$N_{21}U_o/[2+N_{21}(2-D)]$	\\
[14&15]	1	6	6	1^{2w}+0	$[1+N_{21}(2+D)]/(1-D)$	$U_o/[1+N_{21}(2+D)]$	$N_{31}U_o/[1+N_{21}(2+D)]$	\\
[16&17]	2	4	5	1^{2w}+0	$(2+2N_{21})/(1-D)$	$U_o/(2+2N_{21})$	$U_o/2$	\\

S = Switch; D = Diode; C = Capacitor; CL = Coupled Inductor; L = Inductor; 3w = 3-winding; 2w = 2-winding.

$$i_{\mathrm{S-peak}} = i_{L\mathrm{m-peak}} + (i_{\mathrm{Dp1-peak}} + i_{\mathrm{Dm1-peak}})(1 + N_{21} + N_{31}). \tag{25}$$

C. Magnetizing Inductor Design

To ensure that the converter operates in CCM, the average magnetizing current $I_{L\mathrm{m}}$, must be greater than half of the magnetizing current ripple $\Delta I_{L\mathrm{m}}$. It can be known from (21) and (22) that the minimum value of magnetizing inductor is

$$L_{\mathrm{m}} \geq D(1-D)^2 R_{\mathrm{o}}/2f_s[(3+2N_{21}+(2+D)N_{31})]^2. \tag{26}$$

In this design example, $D = 0.62$ and $N_{21} = N_{31} = 7/18$ are selected based on (14). Therefore, when the switching frequency is 50 kHz and the output load $R_{\mathrm{o}} = 2000\ \Omega$, the magnetizing inductance L_{m} can be calculated as follows:

$$L_{\mathrm{m}} \geq 77.8\mu\mathrm{H}. \tag{27}$$

Finally, the value of the magnetizing inductance is selected as 80 μH.

D. Capacitors Design

In order to make the capacitor ripple within a certain range, the capacity of the capacitor should meet

$$C_{\mathrm{x}} \geq U_{\mathrm{o}}/(\Delta U_{C\mathrm{x}} R_{\mathrm{o}} f_s) \tag{28}$$

$$C_{\mathrm{o}} \geq DU_{\mathrm{o}}/(\Delta U_{C\mathrm{o}} R_{\mathrm{o}} f_s) \tag{29}$$

where $\Delta U_{C_{\mathrm{x}}}$ is the ripple of the capacitor, x = c, m1, m2, 1, p1, and $\Delta U_{C\mathrm{o}}$ is the ripple of the output capacitor C_{o}.

There is ESR in the actual capacitor. Considering ESR of the capacitor, the ripple of the capacitor will be further increased. Therefore, when choosing the capacitor, its capacity should be much larger than the theoretical value of (28) and (29).

IV. CONVERTER PERFORMANCE COMPARISON

To demonstrate the superiority of the proposed converter, some comparisons are discussed with other similar converters that recently presented in [12]–[17] and [20]–[34]. Table I presents a comparison of the main performance of the proposed converter with that of other converters with coupled inductor recently presented. It can be seen from Table I, with the same number of components, the voltage gain of the converters proposed in [13]–[15], [21], and [22] is much lower than that proposed in Fig. 1(b). In addition, it is worth noting that although the proposed converters in [12] and [20] with more components than the proposed converter in Fig. 1(b), their voltage gain is not as high as the presented topology in Fig. 1(b). The converters proposed in [16], [17], and [23]–[34], with fewer components than the presented converter in Fig. 1(b); however, their voltage gain is much lower than the proposed topology in Fig. 1(b). The maximum efficiency of all converters is given in Table I.

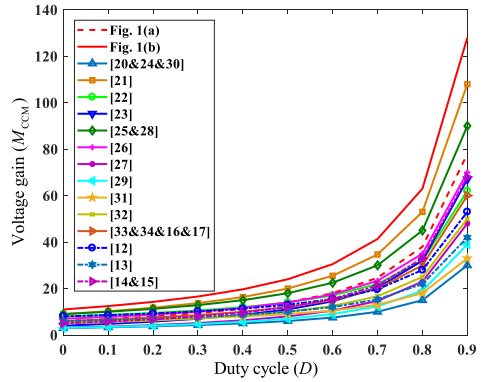

Fig. 7. Comparison of voltage gain with other similar converters.

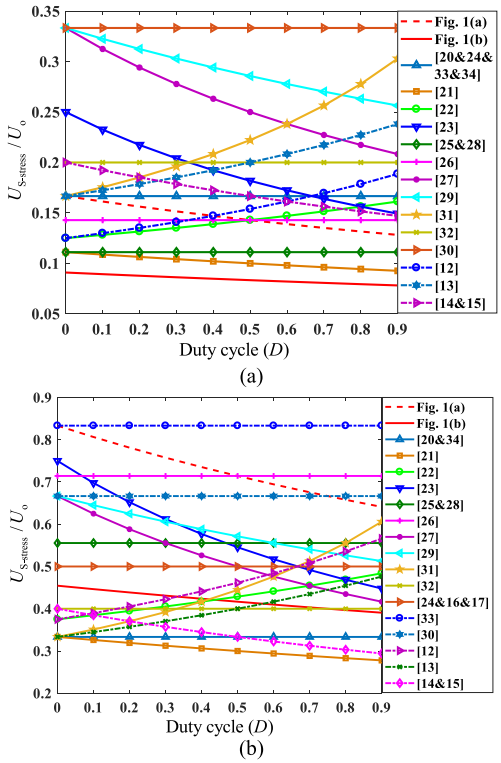

Fig. 8. Comparison of voltage stress with other similar converters. (a) Main switch. (b) Output diode.

As indicated in this table, the maximum efficiency of converters introduced in most papers is lower than the suggested converter. By having brief comparisons between the presented dc–dc converter and studied similar converters under the same condition, it can be concluded that the proposed dc–dc converter has higher voltage gain and higher conversion efficiency.

Fig. 7 shows the voltage gain curve of the proposed and other similar topologies with $N_{21} = N_{31} = 2$. It can be seen that the voltage gain of the proposed converter in Fig. 1(b) is greater than the converters presented in [12]–[17], and [20]–[34] for any values of duty cycle. According to Fig. 8(a), the main switch's voltage stress of the proposed converter in Fig. 1(b) is less than the other circuit structures for all ranges of duty cycle. In addition the voltage gain of the proposed converter shown in Fig. 1(a) is higher than the proposed converters proposed in [12]–[17], [20], [22]–[24], [26], [27], and [29]–[34], although the proposed converter in [12]–[17], [20], [22]–[24], [26], [27], [29], and [30] uses more components than the converter shown in Fig. 1(a), and the converter proposed in [31]–[34] has the same number of components as the converter shown in Fig. 1(a). It can be seen from Fig. 8(b) that the output diode voltage stress of the proposed converter in Fig. 1(b) is less than that of converters presented in [16], [17], [23]–[30], and [33] for all ranges of duty cycle. Although the voltage stress of the output diode of the converters presented in [12]–[15], [20]–[22], [31], [32], and [34] is lower than that of the converter proposed in Fig. 1(b) when the duty cycle is in a certain range or all ranges, they have much smaller voltage gain and much larger voltage stress of the main switch than the converter proposed in Fig. 1(b). From the above-mentioned comparative analysis, it can be seen that the two converters proposed in Fig. 1 can achieve higher voltage gain and lower voltage stress under the condition that the number of components is the same or even less. These advantages are due to the efficient integration with VMC and PCU in the proposed converter.

TABLE II
MAIN PARAMETERS OF THE CIRCUIT

Components	Parameters
Input voltage: U_i	30V
Output voltage: U_o	380V
Rated power: P_o	500W
Switching frequency: f_s	50kHz
Coupled inductor	EE-55 ferrite core
n_3: n_2: n_1	7: 7: 18
L_m	80μH
L_k	3uH
MOSFET S	IRFP4668Pbf/200V
Diodes D_c, D_{m1}, D_{m2}, D_1, D_{p1}, D_o	MUR1560/600V
Capacitor C_c	100uF/100V(Ceramic)
Capacitors C_{m1}, C_{m2}, C_1, C_{p1}	220μF/250V(Electrolytic)
Output Capacitor C_o	100μF/450V(Electrolytic)

V. EXPERIMENTAL RESULTS AND ANALYSIS

In order to verify the feasibility of the presented converter and correctness above-mentioned analysis, a 500-W prototype is built according to Fig. 1(b). The main parameters of the converter are given in Table II.

Fig. 9 shows the experimental waveforms measured under the conditions of $U_i = 30$ V, $U_o = 380$ V, and load $R_o = 500$ Ω, which is basically consistent with the theoretical analysis. When the duty cycle is about 0.62, the converter achieves a high voltage gain conversion from 30 to 380 V. Fig. 9(a) shows the switch driving voltage, leakage inductor, and secondary-tertiary side winding current waveforms. Fig. 9(b) is the voltage and current waveforms of the switch S and the diode D_c. It can be seen that the PCC effectively weakens the leakage voltage spike on the switch. The voltage stress of the switch S and the diode D_c is only about 80 V (Ignore voltage spikes caused by circuit parasitic parameters), which is consistent with the theoretical calculation.

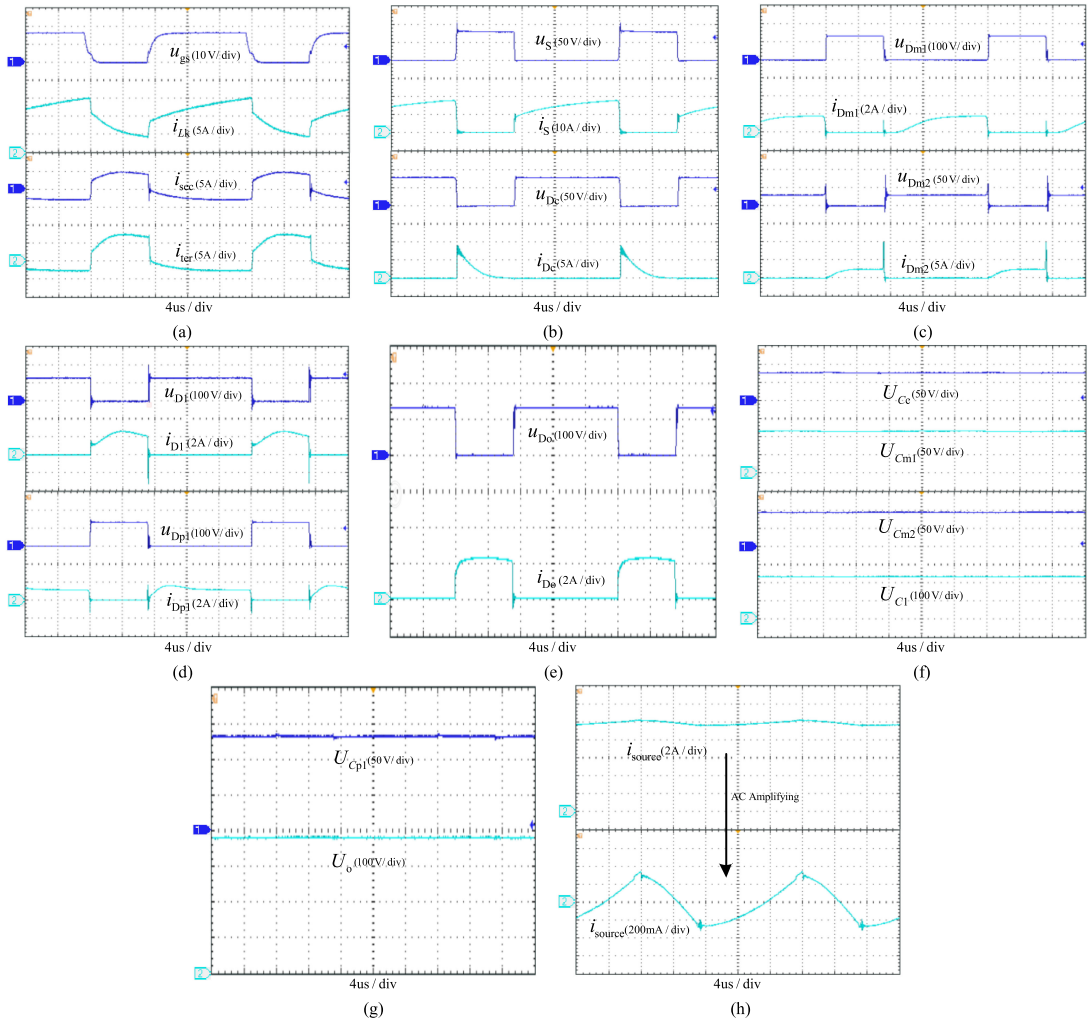

Fig. 9. Experimental waveforms. (a) Driving voltage of the switch $u_{\rm gs}$, leakage inductor current i_{Lk}, and secondary-tertiary side winding current $i_{\rm sec}$, $i_{\rm ter}$. (b) Voltage and current waveforms of the switch S and the diode D_c. (c) Voltage and current waveforms of the diodes D_{m1}, D_{m2}. (d) Voltage and current waveforms of the diodes D_1, D_{p1}. (e) Voltage and current waveforms of the diode D_o. (f) Voltage waveforms of the capacitors C_c, C_{m1}, C_{m2}, and C_1. (g) Voltage waveforms of the capacitors C_c, C_o. (h) Input current ripple.

Fig. 9(c)–(e) shows the voltage and current waveforms of diode D_{m1}, D_{m2}, D_1, D_{p1}, and D_o. It can be seen that the voltage stress (ignore voltage spikes caused by circuit parasitic parameters) of diodes D_{m1}, D_{m2}, D_1, D_{p1}, and D_o are about 132, 30, 122, 135, and 135 V, respectively, which is basically consistent with the theoretical calculation value and has the characteristics of low voltage stress. Fig. 9(f) and (g) shows the voltage waveforms of the capacitors, C_c, C_{m1}, C_{m2}, C_1, C_{p1}, and C_o, and their voltage are about 75, 115, 95, 230, 132, and 380 V, respectively, which are basically the same as the theoretical calculation values. Fig. 9(h) shows the input current ripple after adding 1000 μF of input filter capacitor. It can be seen that the peak-to-peak value of the ripple is about 600 mA and the ripple coefficient is about 6%.

Fig. 10 shows the dynamic response waveforms of the converter in open-loop conditions. It can be seen from Fig. 10(a), the voltage across the load R_0 is equal to zero before the start of switching. When the converter starts to work, it takes about 165 ms to reach a steady-state from starting. As shown in Fig. 10(b), the transition time from duty cycle 0.5 to 0.6 is about 20 ms, and

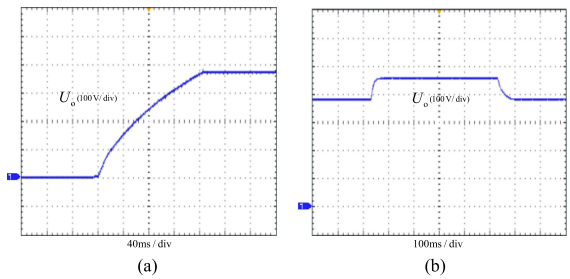

Fig. 10. Dynamic response of the converter. (a) At startup. (b) Duty cycle 0.5 to 0.6.

the transition time from duty cycle 0.6 to 0.5 is about 50 ms, so the proposed converter has better transient response.

Fig. 11 demonstrates the theoretical and measured voltage gain curve. It can be seen from Fig. 11 that when the duty cycle is small, the measured voltage gain is slightly smaller than the theoretical value. As the duty cycle increases, the measured voltage gain is almost the same as the theoretical value, and

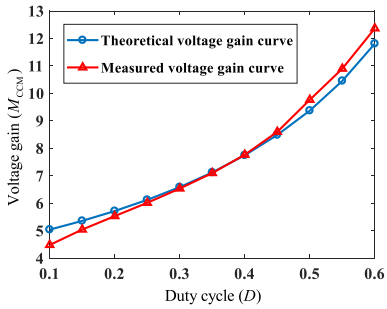

Fig. 11. Measured and theoretical voltage gain curve.

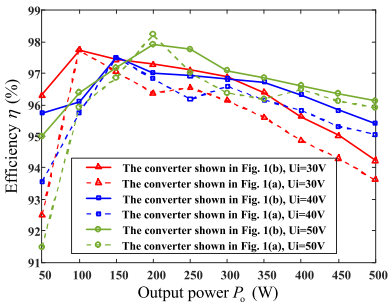

Fig. 12. Efficiency curve of the proposed converter.

finally, slightly higher than the theoretical value. The measured voltage gain curve is basically consistent with theoretical calculating value. The main reason for the difference between the actual measured value and the theoretically calculated value is the existence of L_k, and it can be concluded that the actual voltage gain of the converter is related to L_k, f_s, and R_0 [35]. But within the allowable error range, the correctness of the theoretical calculation is verified.

Fig. 12 is a comparison efficiency curve of the converter shown in Fig. 1. The main instruments used to measure efficiency are as follows: digital multimeter (VC890C+), programmable dc power supply (IT6521C). During the measurement process, always keep the input and output ports of the experimental prototype to measure the real-time data of voltage and current. In order to ensure the fairness of the comparison, the converter's turns ratio shown in Fig. 1(a) is set to 18:18:18, as far as possible to make it work with the same duty cycle. It can be seen that the maximum power points of the two converters shown in Fig. 1 at input voltages of 30, 40, and 50 V are 100, 150, and 200 W, respectively, and their efficiencies are 97.73% (97.73%), 97.50% (97.50%), and 97.92% (98.24%). At full load (500 W), the efficiency of the input voltage 30, 40, and 50 V is 94.23% (93.62%), 95.41 (95.07%), and 96.12% (95.91%), respectively, the converter shown in Fig. 1(b) from light load to full load, the efficiency is basically higher than the converter shown in Fig. 1(a). This is because the number of secondary-tertiary windings of the converter shown in Fig. 1(b) is small, and due to the limited volume of magnetic core skeleton, there are many secondary-tertiary windings of the converter shown in Fig. 1(a), which have to be reduced wire diameter. Also, the turns ratio of the converter shown in Fig. 1(a) is greater, the current converted

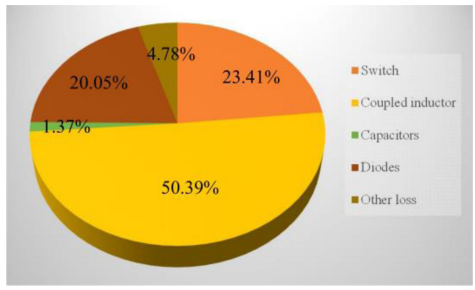

Fig. 13. Theoretical analysis of power loss distribution at rated power.

to the primary side is also greater, which undoubtedly further increases the copper loss of the coupled inductor.

The calculated loss distribution of the experimental prototype of the converter in Fig. 1(b) is shown in Fig. 13 when the input voltage is 30 V and at full load (500 W). It can be seen that the dominant losses occur in the switch and coupled inductor. The design of the coupled inductor can be optimized for mass production.

VI. Conclusion

This article presents a high step-up three-winding coupled inductor dc–dc converter integrated with VMC and PCU. In addition, PCUs can be integrated into N, which increases the flexibility of the converter and can increase or decrease the number of PCUs according to specific requirements. The biggest advantage of the proposed converter is that it can achieve high voltage gain conversion with a small turn ratio of the coupled inductor and an appropriate operating duty cycle. Therefore, the voltage stress of the components is low and the efficiency of the converter is high. The superiority of the presented converter is verified by comparison with the coupled inductor converter proposed in recent years. Theoretical analysis and experimental results show that the proposed converter has the characteristics of high voltage gain, low voltage stress, and high operating efficiency, so it is very suitable for new energy power generation systems, such as photovoltaic power generation.

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Jie Ding was born in Suizhou, China, in 1993. He received the B.Eng. degree from Yangtze University, Jingzhou, China, in 2017, and the M.Sc. degree from the South China University of Technology, Guangzhou, China, in 2020, all in electrical engineering.

His research interests mainly include power electronics converter topologies, high step-up dc–dc converters and their applications, such as dc microgrid and electric vehicles.

Shiwei Zhao (Member, IEEE) received the B.Sc. degree from the Central South University, Changsha, China, in 2000, the M.Sc. degree from the South China University of Technology, Guangzhou, China, in 2003, and the Ph.D. degree from The Hong Kong Polytechnic University, Hong Kong, in 2008.

He is currently an Associate Professor with the South China University of Technology. He mainly engaged in switched reluctance motor and its drive control, permanent magnet synchronous motor and its drive control, dc–dc inverter, and other alike.

Shuang Gao received the B.Sc. degree from the Hubei University of Technology, Wuhan, China, in 2018, and the M.Sc. degree from the South China University of Technology, Guangzhou, China, in 2021.

His research interests include power electronic converters, dc microgrids, and integration of renewable energy in microgrids.

Huajie Yin received the B.Sc. and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 1989 and 1994, respectively, all in electrical engineering.

He is currently a Professor with the South China University of Technology, Guangzhou, China. He mainly engaged in permanent magnet motor and its drive control, brushless dc motor and its drive control, and dual rotor permanent magnet wind power system.