A Push–Pull Series Connected Modular Multilevel Converter for HVdc Applications

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***Abstract*—This article introduces a push–pull series connected (PPSC) ac–dc converter intended for high-voltage direct current applications. The proposed topology requires fewer submodules compared to a standard modular multilevel converter (MMC) to withstand the same dc voltage. Each converter phase unit is connected to its corresponding phase on the ac side via a center-tapped single-phase transformer which also provides the galvanic isolation needed in most applications. The required arm inductance can be merged into the transformer leakage inductance avoiding the need for additional inductors. In this article, both the design and operation of the converter are discussed in detail. Furthermore, a comparison of the PPSC and MMC in terms of energy storage requirements and efficiency is presented. The converter concept and the control strategy proposed is validated by computer simulations using the piecewise linear electrical circuit simulation (PLECS) simulation package as well as through experiments on a small-scale, 300-V, 2-kW laboratory prototype.**

***Index Terms*—High-voltage direct current (HVdc), modular multilevel converter (MMC), push–pull converters.**

I. Introduction

HIGH-VOLTAGE direct current (HVdc) transmission is a well-established way of transmitting high power over long distances as an alternative to the use of flexible ac transmission systems (FACTS) [1]. The use of voltage source converters (VSCs) in HVdc applications has brought about benefits such as black start capability and independent control of active and reactive powers [2]. In recent years, multilevel converters have been used widely to exploit the benefits of the VSC-HVdc [3].

A modular structured converter, named the modular multilevel converter (MMC) [4], intended for use in HVdc applications was a significant breakthrough in ac–dc conversion [5]. Each phase consists of two arms that are constructed by the series connection of identical half-bridge cells and an arm inductor.

In recent years, researchers have been trying to investigate different arrangements in order to optimize the number of levels, the size and the number of the passive components, and the energy storage requirements of the MMC. Over the past few years, there have been a significant number of publications intended to address some of these issues [6]. Some hybrid topologies such as the alternate arm converter (AAC) [7] and the parallel hybrid modular multilevel converter (PH-MMC) [8] have been introduced in order to reduce the energy storage requirements and the converter losses. However, both of the hybrid topologies suffer from dc bus ripple which needs to be filtered. The ac and the dc sides are not completely decoupled in the PH-MMC, which makes the internal energy management difficult [9]. The AAC provides dc fault blocking capability since full bridge submodules (SMs) are used in its arms. Additional to the SMs, there are series connected director switches (DSs) in each arm which conduct alternately, normally with some degree of overlap. In the AAC, capacitor balancing becomes more complex when the converter is operated away from the "sweet-spot" [7]. The operating region of the AAC is increased in [10] by extending the zero current switching operation of the DSs through the transformer on-load tap changer. An arm phase-shift conducting modulation (PSCM) strategy, which allows half-bridge SMs to be used, is proposed in [11] to eliminate the sweet-spot limitation in the AAC. However, the dc fault ride through capability of the AAC is sacrificed and the bulky dc filters are still required in the PSCM-AAC. However, fewer SMs and devices, and smaller capacitors are required compared to a standard MMC with half-bridge SMs. An extended-overlap (EO) mode of AAC operation was introduced in [12] and [13] which frees the sweet-spot constraint by extending the overlap period to 60°. The EO-AAC retains the benefits of the AAC such as dc fault ride through capability, smaller capacitors, and lower energy storage requirement, without the need for bulky dc capacitor filters. However, the converter requires more switching devices compared to the traditional AAC and the hybrid arm MMC (with dc fault blocking capability), which increases the construction cost. Comprehensive comparisons between different versions of the AAC and the MMC in terms of cost, volume, efficiency, etc., can be found in [12], [14], and [15].

In high-voltage transmission applications, the number of power modules becomes very large, which, in turn, increases

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the cost and the complexity of the converter system. In order to reduce the number of SMs in the MMC, series connection of the converter phases on the dc side has been proposed in [16]. However, the converter in [16] requires twice the number of arm inductors that are used in an MMC. The series bridge converter (SBC) [17] is another hybrid series connected topology that decreases the number of SMs and the energy storage requirement of the converter. Like the PH-MMC, the SBC requires unfolding bridges for its operation, and decoupling of the ac and dc side controllers is not fully achieved. A control strategy for internal energy balance and experimental validation of the SBC is reported in [18]. The series chain-link converter [19] is another series connected MMC that aims to decrease the required SM count.

An MMC applying the push–pull transformer arrangement was first introduced in [20] for battery storage systems. The push–pull phases were connected in parallel to give low-voltage, high-current operation. Some other MMC topologies have since been proposed, applying three-winding transformers to eliminate the arm inductors, by merging the function of the arm inductors into the transformer leakage inductance [21]–[23]. In offshore systems, for example, the overall cost increases with the size of the platform [24]. Therefore, elimination of air core reactors, which require a large space, is an advantage considering grid connected offshore wind farms.

This article introduces a new push–pull series connected (PPSC) ac–dc converter intended for HVdc applications. The proposed converter combines both the push–pull transformer arrangement on the ac side per-phase and series connection of the phases on the dc side in contrast to the previously reported parallel arrangements. This makes the circuit attractive for high-voltage lower current applications. In this way, the proposed converter has the potential to reduce the number of the switching devices and the passive components whilst retaining the modularity of the MMC. The contributions of this article are as follows:

1) a detailed theoretical model of the proposed converter;
2) a comparison of the new topology with the state-of-the-art;
3) steady-state modeling to explain and illustrate the voltage and current wave-shaping in the new converter;
4) development of a suitable control strategy for the proposed three-phase converter;
5) experimental validation of the proposed approach in a small-scale laboratory prototype.

The rest of the article is organized as follows. Section II introduces the PPSC. The idealized voltage wave-shaping together with the current and voltage equations are discussed along with the conditions for power balance in each arm. A comparison between the PPSC and the MMC in terms of the number of SMs, capacitor sizing, energy management, and efficiency is carried out in Section III. Steady-state simulation results for the PPSC are also shown. In Section IV, a control strategy developed for the PPSC is described in detail. In Section V, the design of a small-scale laboratory prototype and its digital control system are described. Experimental results, which validate the converter operation and the control approach, are given. Finally, Section VI concludes this article.

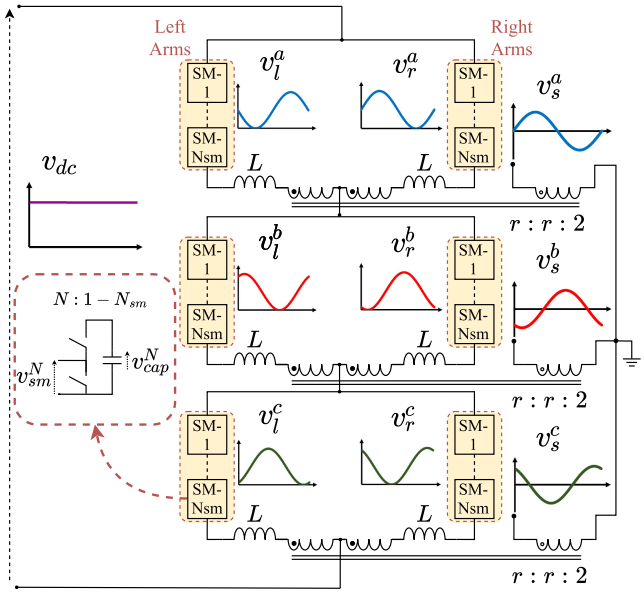


Fig. 1. Three-phase schematic of the PPSC together with the ideal voltage waveforms.

II. Push–Pull Series Connected Converter

The three-phase arrangement and the ideal voltage waveforms for the PPSC is shown in Fig. 1. The converter phases are series connected on the dc side and each converter phase is connected to the corresponding line input phase via a center-tapped single-phase transformer. As the arm inductances can be merged into the transformer leakage inductances in the PPSC, there is no need for separate arm inductors. While the MMC is known as transformer-less converter [25], transformers are generally required in practical HVdc applications to isolate the converter from the grid, to provide the desired voltage level for the converter, and to prevent zero sequence current flow into the converter [20], [26]–[28]. The transformers are also normally implemented using single-phase units for ease of installation and transportation [29]. Therefore, the requirement for single-phase transformers may not be a drawback for the PPSC. Moreover, the elimination of separate arm inductors may be a benefit, particularly in size and weight sensitive applications such as offshore platforms for wind farms [24]. Note that the inductors L in Fig. 1 represent the leakage inductances of the transformer.

A modular arm structure using cascaded half-bridges (SMs) with dc floating capacitors is used for voltage shaping in each arm. The left and the right arms together comprise one phase of the converter. Each arm is responsible for generating one-third of the dc voltage and half of the ac voltage. Ideally, the dc offset in each arm cancels on the ac side, whereas all the ac components cancel on the dc side. The voltages on the SM capacitors must be controlled for successful operation. There are three main requirements: maintaining the total stored energy in the converter at a reference value, balancing the energy storage between the arms, and maintaining each capacitor voltage close to a reference value [30].

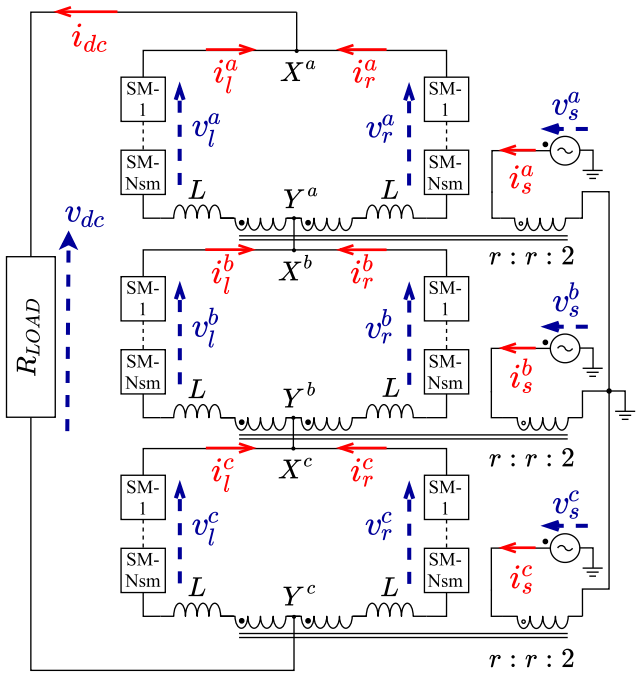


Fig. 2. Three-phase grid connected circuit model for PPSC.

An issue with the push–pull configuration is that differences in the dc component of the two arm currents flowing into the transformer windings can cause saturation. To prevent this, the difference between the dc components of the left and the right arm currents must be regulated to zero. A solution to ensure this is presented later in the article.

A. Current and Voltage Equations

The three-phase grid connected circuit representation for the PPSC used in both the simulation and the experimental prototype to validate converter operation is shown in Fig. 2. The voltage wave-shaping and the current equations in a converter phase employing push–pull operation are analyzed in detail in [20]. The same methods can be applied to the PPSC in the analysis of the current and voltage equations. For simplicity, the dc side is modeled with a resistive load R_{LOAD}. To keep the power balance in an HVdc transmission system, the converter station at one end controls the active power delivered, whilst the other is responsible for regulating the dc voltage [31]. Therefore, the resistive load here represents the station that fixes the power. This simplified linear load on the dc side is satisfactory to analyze the operation of the converter [32]. Three center-tapped single-phase transformers connect the converter arms to their corresponding phase voltages v_s^k $(k = a, b, c)$. The ratio between one-half of the secondary winding and the primary winding is defined as $r/2$.

Due to the series connection, the dc current i_{dc} flows through all converter phases. Additionally, the full ac phase current i_s^k, scaled by the turns-ratio, circulates within each converter phase. The left and right arm currents of each converter phase are referred to as i_l^k and i_r^k, respectively. To achieve the voltage handling capability and multilevel operation, the converter arms are structured as cascaded half-bridges (SMs). The total number of SMs in each arm is denoted as N_{sm} and v_{cap}^N represents the SM capacitor voltage C_{sm}^N of the Nth SM ($N : 1 - N_{\text{sm}}$). v_{sm}^N is the voltage contributed by the Nth SM (see Fig. 1). The left and right arm voltages $v_{l,r}^k$ are a summation of the SM voltages in the corresponding phase arm. Ignoring switching effects due to the multilevel operation, each arm can be represented as a variable voltage source. For simplicity in the analysis of the PPSC, the following is also assumed.

1) The converter is in the steady state.
2) There are no power losses in the system.
3) The ac grid is balanced.

With these assumptions, the arm voltages and currents will be identical for each phase. The ac grid voltage and current of kth phase ($k = 1$, 2, and 3 corresponding to the phases a, b, and c, respectively) are defined as

$$v_s^k = V_s \sin\left(\omega t - \frac{2(k-1)}{3}\pi\right) \tag{1}$$

$$i_s^k = I_s \sin\left(\omega t - \frac{2(k-1)}{3}\pi + \varphi\right). \tag{2}$$

We adopt the convention that time-varying components are denoted by lower case letters, and upper case letters denote constant values in this article.

Each converter phase produces one-third of the dc voltage assuming balanced phases, i.e., $V_{\text{dc}}^k = V_{\text{dc}}/3$ (between points X^k and Y^k). Neglecting the voltage drop across the arm inductors, the arm voltages are obtained from Fig. 2 as

$$v_l^k = \frac{V_{\text{dc}}}{3} - \frac{r v_s^k}{2} \tag{3}$$

$$v_r^k = \frac{V_{\text{dc}}}{3} + \frac{r v_s^k}{2}. \tag{4}$$

The modulation index m $(0 \le m \le 1)$, between the dc voltage and the amplitude of the ac voltage, can be defined as

$$m = \frac{3rV_s}{2V_{\text{dc}}} \tag{5}$$

which means that $m = 1$ corresponds to the maximum ac side voltage that can be generated with conventional modulation. In this way, the peak ac voltage is limited to one-third of the dc voltage to operate the PPSC in the linear modulation region. This is ensured by limiting the peak-to-peak ac voltage to one-half of the dc voltage in the MMC

$$m_{\text{MMC}} = \frac{2rV_s}{V_{\text{dc}}}. \tag{6}$$

The MMC is normally operated in this linear modulation region instead of overmodulation, which increases the harmonic components in the output voltage [33]. The ac voltage harmonics reduce the power quality of the system, which is not desirable especially in HVdc applications. However, unwanted factors may cause voltage fluctuations and eventually give rise to overmodulation of the converter. Therefore, a safety margin of $\pm 10\%$ for ac voltage fluctuations is generally considered in the modulation of an MMC [14]. Although the relationship between the ac

voltage amplitude and the dc voltage in the PPSC is different from the MMC, the modulation region constraint is the same as an MMC for HVdc applications. Similar to the MMC, the proposed converter may be operated in overmodulation mode. However, in this introductory article about the PPSC, only the linear modulation region is considered in the analyses to explain the operation of the converter.

Substituting (5) into (3) and (4), the arm voltages can be expressed as

$$v_l^k = \frac{V_{\rm dc}}{3}\left(1 - m\sin\left(\omega t - \frac{2(k-1)}{3}\pi\right)\right) \tag{7}$$

$$v_r^k = \frac{V_{\rm dc}}{3}\left(1 + m\sin\left(\omega t - \frac{2(k-1)}{3}\pi\right)\right). \tag{8}$$

Substituting (7) and (8) into (3) and (4) yields

$$V_s = \frac{2m}{3r}V_{\rm dc}\sin(\omega t - \frac{2(k-1)}{3}\pi). \tag{9}$$

The dc current flows through all the converter phases and splits equally into the arms. Since these currents enter the secondary windings with opposite signs, there is no dc flux induced in the transformer core.

The relationship between the ac grid current and the ac components of the arm currents $(i_l^k)_{\rm ac}$ and $(i_r^k)_{\rm ac}$ can be expressed as

$$i_s^k = \frac{r}{2}((i_l^k)_{\rm ac} - (i_r^k)_{\rm ac}). \tag{10}$$

Since the ac current must circulate within the mesh in each phase, the arm currents can be expressed as

$$i_l^k = \frac{i_{\rm dc}}{2} + \frac{i_s^k}{r} \tag{11}$$

$$i_r^k = \frac{i_{\rm dc}}{2} - \frac{i_s^k}{r}. \tag{12}$$

Hence, each converter chain-link must be rated for half of the dc current plus the full ac current. The rms value of the arm current is therefore

$$I_{\rm arm}^{\rm rms} = \sqrt{\left(\frac{I_{\rm dc}}{2}\right)^2 + \frac{\left(\frac{I_s}{r}\right)^2}{2}}. \tag{13}$$

Neglecting the switching ripple and the voltage across the arm inductors, the total voltage v_{XY}^k between points X^k and Y^k is found as

$$v_{XY}^k = \frac{v_l^k + v_r^k}{2}. \tag{14}$$

Substituting (3) and (4) into (14) yields

$$v_{XY}^k = \frac{V_{\rm dc}}{3}. \tag{15}$$

Hence, in the ideal situation, all the ac components of the arm voltages cancel out on the dc side, leaving the dc side voltage ripple free. As a result, there is no need for filtering on the dc side since the dc voltage and current are free from ac ripple.

B. Circulating Current Considerations

It is also important to consider the potential for circulating currents within each phase caused by ripple in the arm voltages. This is an effect that is very well known in the MMC circuit. A comprehensive study is provided in [34] and the ripple voltage analysis there can be applied to the PPSC since the arm structure is the same as an MMC. The insertion indices for the left and the right arms in the PPSC are defined as

$$n_{l,r}^k = \frac{1}{3}\left(1 \pm m\sin\left(\omega t - \frac{2(k-1)}{3}\pi\right)\right). \tag{16}$$

Assuming perfect capacitor voltage balancing, identical SMs, and an infinite switching frequency, the current through the capacitors in the SMs in Fig. 1 can be shown as a function of the insertion indices as given in (17). The capacitor voltages can be determined by integrating the capacitor currents (18)

$$(i_{\rm cap}^{l,r})_k = n_{l,r}^k i_{l,r}^k \tag{17}$$

$$(v_{\rm cap}^{l,r})_k = \frac{1}{C_{\rm sm}}\int n_{l,r}^k i_{l,r}^k dt. \tag{18}$$

Here, the arm currents in (11) and (12) are considered, where the dc current is pure dc and is equally shared between the arms, and the ac current consists only of the fundamental component. In this way, the effect of the fundamental component of the ac current and inserting/bypassing the SMs on the ripple in the arm voltages can be illustrated. The total arm voltages in the left and the right arms can be found by multiplying the capacitor voltages with the number of SMs and the insertion indices as

$$v_{l,r}^k = \frac{N_{\rm sm}}{C_{\rm sm}} n_{l,r}^k \int n_{l,r}^k i_{l,r}^k dt. \tag{19}$$

Performing the integrations and expanding (19), the total arm voltages are found as

$$\begin{aligned} v_{l,r}^k = \frac{1}{72C_{\rm sm}\omega}\Bigg(& \left(I_{\rm dc} - \frac{I_s}{r}m\cos(\varphi)\right)(4N_{\rm sm}\omega t \\ & + 4mN_{\rm sm}\omega t\sin(\omega t)) - 4\frac{I_s}{r}mN_{\rm sm}\sin(\varphi) \\ & \pm 4I_{\rm dc}mN_{\rm sm}\cos(\omega t) \pm 8\frac{I_s}{r}N_{\rm sm}\cos(\omega t + \varphi) \\ & \pm \frac{I_s}{r}m^2N_{\rm sm}\cos(\omega t + \varphi) - 2I_{\rm dc}m^2N_{\rm sm}\sin(2\omega t) \\ & + 6\frac{I_s}{r}mN_{\rm sm}\sin(2\omega t + \varphi) \\ & \pm \frac{I_s}{r}m^2N_{\rm sm}\cos(3\omega t + \varphi)\Bigg). \end{aligned} \tag{20}$$

Note that the first term in (20) must equate to zero when there is power balance in steady state. This is confirmed by substituting the power balance equation (23) derived in the next subsection. Similarly to the MMC, the odd harmonic components in the left and right arm voltages (upper and lower arm voltages in an MMC) in each phase have opposite signs, whereas the even harmonics are in phase. However, the effect of the ripple voltage on circulating current is quite different between the MMC and the PPSC circuits. In the MMC (within each phase), the arms

are in series and the ripple voltages add, taking into account the phase shift of each component. In combination with the other phases, these voltages create circulating currents between phases. Conversely, in the PPSC, the ripple voltages in each arm subtract in the loop formed in each phase. The dominant component in the arm voltage ripple is at twice supply frequency and it has the same phase shift in each arm; this causes the well-known twice supply frequency circulating current in the MMC [34]. Within the PPSC, these components cancel, assuming a symmetrical circuit, and there is no circulating current generated at twice supply frequency. The same is true of all even harmonics in the ripple voltage. Odd harmonic voltages in the ripple add in the PPSC and can create circulating currents, but their amplitude is very small compared to the second harmonic, and, in combination with the phase impedance, the current generated is very small. For example, with the parameters used here, the third harmonic circulating current component is typically 1% of the fundamental and other components are smaller. Consequently, it is not necessary to employ any techniques to mitigate ac circulating current in the PPSC phases. It is, however, necessary to mitigate against the possibility of a dc circulating current within each phase in the PPSC, which can be created by even quite small asymmetries. Fortunately, the solution to this is quite straightforward as discussed in Section IV-A.

C. Power Balance in Each Arm

In steady state, the mean power contributed by each arm must be zero. Considering the left and the right arms of each phase in the PPSC, the instantaneous power of the arms can be expressed as

$$p_{l,r}^{k} = v_{l,r}^{k} i_{l,r}^{k}. \tag{21}$$

Substituting (7), (8), (11), and (12) into (21) and averaging the result over a line period gives the average active power of the left and right arms in the kth phase as

$$\overline{p_{l,r}^{k}} = \underbrace{\frac{1}{2}\overline{\frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{3}}}_{P_{\mathrm{dc}}^{k}} - \underbrace{\frac{1}{2}\frac{V_s I_s \cos(\varphi)}{2}}_{P_{\mathrm{ac}}^{k}}. \tag{22}$$

Consequently, for steady-state power balance, (22) equates to zero and the dc current can be expressed in terms of the ac current as

$$I_{\mathrm{dc}} = \frac{m I_s \cos(\varphi)}{r}. \tag{23}$$

III. Comparison and Simulation Results

In this section, a comparison between the PPSC and the MMC in terms of the number of SMs, capacitor sizing, energy storage, and efficiency is carried out. Since the parameters, such as the capacitor value, total energy requirement, the voltage and current ratings of the switching devices, the total installed semiconductor power requirement, etc., has a direct impact on the size, weight, and cost of an MMC-HVdc [6], [35], the converters are compared by using these parameters. Results from a simulation study validating the steady-state analysis of the converter voltage and current waveforms are also included. Simulation of a full switching model of a typical MMC HVdc system with hundreds of SMs is difficult and time consuming [36]. Hence, the parameters from a scaled-down MMC HVdc system model described in [37], developed as an industrial demonstrator for a full-scale HVdc system, is used in the simulation of the PPSC and in the comparative evaluations. This industrial "small-scale" demonstrator specification has been used as the basis for evaluating different converter arrangements in a number of previous publications [14], [38], [39]. It has the benefit of being at a sufficient scale to give a meaningful comparison (i.e., enough levels) while having a manageable number of cells for a full switching simulation without special computing resources. In order to carry out comparisons between converters, the active power, dc side voltage, ac grid voltage, and nominal cell voltage $V_{\mathrm{cap}}^{\mathrm{nom}}$ ratings are chosen equal for both converters as shown in Table I. For simplicity, the line impedance is neglected in the capacitor sizing and the efficiency analysis for both converters.

TABLE I
Converter Specifications

		PPSC	MMC
Rated power	P	20MW	
Line-to-line rms voltage	V_{ac}	11kV	
dc voltage	V_{dc}	20kV	
Frequency	f	50Hz	
Nominal cell capacitor voltage	V_{cap}^{nom}	1.5kV	

A. Number of SMs in Each Arm

Assuming unity modulation index, according to (7) and (8), each converter arm must be capable of producing two-thirds of the dc voltage. Hence, the minimum number of SMs per arm for the PPSC is

$$N_{\mathrm{sm}}^{\mathrm{PPSC}} = \frac{2V_{\mathrm{dc}}}{3V_{\mathrm{cap}}^{\mathrm{nom}}}. \tag{24}$$

In a standard MMC each arm must be capable of producing full dc voltage. Therefore, the minimum number of SMs per arm for the MMC is

$$N_{\mathrm{sm}}^{\mathrm{MMC}} = \frac{V_{\mathrm{dc}}}{V_{\mathrm{cap}}^{\mathrm{nom}}}. \tag{25}$$

B. Energy Requirement and Capacitor Sizing

The minimum SM capacitor size for a given capacitor voltage ripple may be predicted by considering the total energy stored in each arm [36]. The minimum capacitor value in each SM is related to the maximum energy deviation over a fundamental period in each arm by [14]

$$C_{\mathrm{sm}}^{\mathrm{min}} = \frac{\Delta E_{\mathrm{arm}}}{2N_{\mathrm{sm}}(V_{\mathrm{cap}}^{\mathrm{nom}})^2 \Delta V} \tag{26}$$

where $C_{\mathrm{sm}}^{\mathrm{min}}$ is the minimum required capacitor value, ΔE_{arm} is the maximum energy deviation in each arm, and ΔV is the allowed voltage ripple factor for the capacitor voltages. A typical

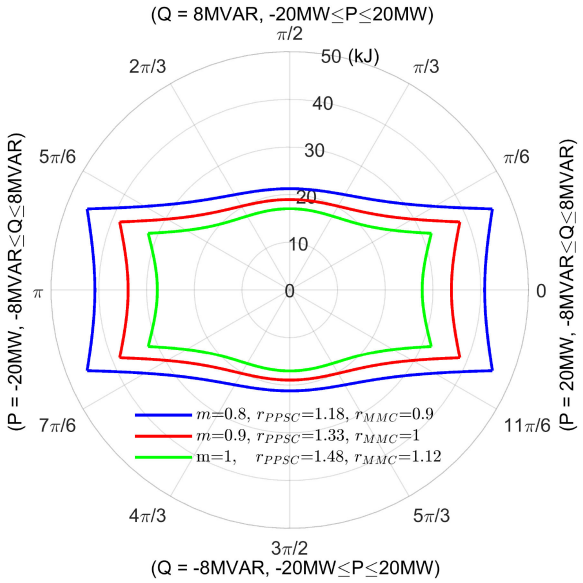


Fig. 3. Maximum peak-to-peak energy deviation for different operating points (kJ).

value of $\pm 10\%$ voltage ripple factor [40] is considered in this analysis.

Integrating the instantaneous power in (21) gives the instantaneous energy of the arm

$$e_{l,r}^{k} = \int p_{l,r}^{k} dt. \tag{27}$$

Substituting (9) and (23) into (27) gives the instantaneous energy deviation of each arm as

$$e_{l,r}^{k} = \frac{V_s I_s}{4m\omega} \cos(\varphi) \left(2 - m^2 + m^2 \cos(\omega t)\right) + \cos(-\omega t + \varphi) \left(2 + m \sin(\omega t)\right). \tag{28}$$

This result is identical to that obtained for the MMC in [41] when the MMC modulation index is defined as in (6). Note that for the same modulation index and ac and dc side voltages, the turns ratio (r) differs by a factor of 4/3 between the two converters.

In Fig. 3, the peak-to-peak energy deviation values over a cycle are plotted as a function of phase angle φ for different modulation index values, $m = 0.8$, 0.9, and 1. Here, φ varies between 0 and 2π for different operating points within the rated power ranges (± 20 MW and ± 8 MVAR).

The peak-to-peak energy deviation is decreased by increasing the modulation index value. For calculating the required capacitance, a modulation index of $m = 0.9$ is assumed since this will allow a typical value of $\pm 10\%$ ac voltage variation. At $m = 0.9$, the maximum peak-to-peak energy deviation (38.37 kJ) is reached when the converter works at full rated active and reactive power. Hence, this can be considered as the worst case when calculating the minimum capacitor value using (26). The total energy stored in the converter can be calculated from the total capacitor energies as

$$E_{\text{tot}} = \frac{6N_{\text{sm}}(V_{\text{cap}}^{\text{nom}})^2}{2} C_{\text{sm}}^{\text{min}}. \tag{29}$$

C. Semiconductor Losses

The expressions in the Appendix, which are derived from analytical methods described in [42] and [43], are used to estimate both the conduction and switching losses for the PPSC and the MMC.

In order to have a fair comparison between converters in terms of power losses, switching devices from the same manufacturer and the same device family were chosen for both converters. In this article, the Hitachi MBN1200F33F IGBT modules [44], which are rated at a nominal collector emitter voltage $(V_{cc}^{\text{nom}})_{1200}$ of 3300 V and a dc-collector current $(I_c^{\text{nom}})_{1200}$ of 1.2 kA, were used as switching devices in the MMC. It is worth noting that the aim of this article is not to find the most appropriate rated devices for the converters but to compare the loss behavior of the converters. The rms arm current in the PPSC is 1.5 times higher than the rms arm current in the MMC, as calculated from (13). Therefore, the Hitachi MBN1800F33F IGBT modules [45], which are rated at a nominal collector emitter voltage $(V_{cc}^{\text{nom}})_{1800}$ of 3300 V and a dc-collector current $(I_c^{\text{nom}})_{1800}$ of 1.8 kA, were used as switching devices in the PPSC. Note that the total installed semiconductor powers [46] of the converters are equal to

$$N_{\text{sm}}^{\text{MMC}}(V_{cc}^{\text{nom}})_{1200}(I_c^{\text{nom}})_{1200} = N_{\text{sm}}^{\text{PPSC}}(V_{cc}^{\text{nom}})_{1800}(I_c^{\text{nom}})_{1800}. \tag{30}$$

A level shifted carrier based modulation technique, called phase disposition (PD) pulsewidth modulation (PWM), with the sorting algorithm presented in [47] is used to generate the reference voltages in the converter arms. Many different modulation methods and capacitor balancing techniques have been introduced in the literature to further improve the performance of the MMC [6], [47], [48]. The same modulation and capacitor balancing methods used for the MMC can be applied to the PPSC. As is the case with the MMC, they have no effect on the basic sizing of the converter or the transformers. For a full-scale converter with a very large number of cells, it would also be possible to use the "nearest level" modulation technique [49]. Since the aim of this article is to validate the operation of the proposed converter and to illustrate a fair comparison with the MMC, we have only considered one approach, and, in line with previous work undertaking similar studies [12], [18], and [19], we have used a simple carrier-based method for the comparisons. Accordingly, the same carrier and sorting frequencies (both 1 kHz as in Table II) were considered in both converters for a fair comparison in terms of loss analysis.

The total power losses in the PPSC and the MMC as a percentage of rated power for different modulation index values ($m = 0.8$, 0.9, and 1) are illustrated in Fig. 4. The total losses are almost equal in both converters for a given modulation index. The overall loss decreases with the modulation index in both converters.

TABLE II
NUMERICAL COMPARISON

		PPSC	MMC
Nominal SM capacitor voltage	V_{cap}^{nom}	1.5kV	1.5kV
Modulation index	m	0.9	0.9
Transformer turn ratio	r	1.33	1
Number of SMs per arm	N_{sm}	9	14
Nominal SM capacitor value	C_{sm}^{nom}	9.47mF	6.32mF
Total energy requirement	E_{tot}	597.24kJ	597.24kJ
Energy per power	E_{tot}/S	29.8kJ/MVA	29.8kJ/MVA
Nominal dc Current	I_{dc}^{nom}	1kA	1kA
Arm Current (rms)	I_{arm}^{rms}	975A	650A
Number of Arm Inductors	N_{arm_ind}	-	6
Arm Inductance	L	2.85mH*	4.7mH
Phase Inductors	L_{ph}	3.22mH	3.22mH
Carrier frequency	f_{PWM}	1kHz	1kHz
Sorting frequency	f_{SORT}	1kHz	1kHz
Insulation voltage rating of secondary winding**	V_{ins}^{a}	19.31kV	8.98kV
	V_{ins}^{b}	12.64kV	
	V_{ins}^{c}	5.97kV	
Secondary side apparent power rating	S_{tr}^{k}	8.23MVA	6.66MVA

*This represents the equivalent leakage inductance as viewed from each secondary side of the transformer for the PPSC.
**For each secondary windings for the PPSC.

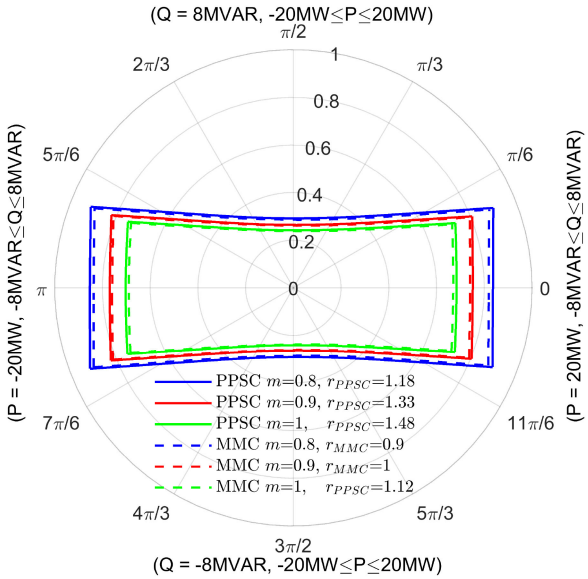


Fig. 4. Analytical results of total losses in the PPSC and the MMC as a percentage of the rated power.

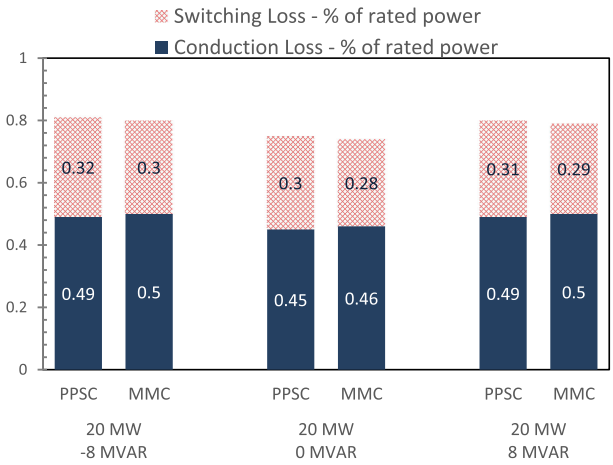


Fig. 5. Loss breakdown of the PPSC and the MMC as a percentage of the rated power when both converters work at rectification mode with different reactive power variations.

Fig. 5 shows the comparison between the PPSC and the MMC in terms of conduction and switching losses, as a percentage of the rated power. For simplicity, the results are illustrated only for rectification of the full rated active power with different reactive power variations and $m = 0.9$ ($r_{\text{PPSC}} = 1.33$ and $r_{\text{MMC}} = 1$). The loss breakdown is almost equal in both converters.

D. Numerical Comparison

A summary of the numerical comparison is shown in Table II. The number of SMs per arm in each converter is calculated by (24) and (25). The PPSC requires 33% less SMs than an MMC for the same nominal cell voltage and nominal modulation index. Since the PD PWM method is used in the comparisons, $(2N_{\text{sm}} + 1)$ voltage levels are generated at the output of the converters. Thus, a smaller number of voltage levels with larger voltage steps are generated at the output of the PPSC compared to a standard MMC for a given nominal dc and SM capacitor voltage. However, given the number of cells in a full-scale HVdc converter, the expected difference in waveform fidelity due to the reduction in number of levels will be minimal.

Although the rms arm current in the MMC is approximately 33% smaller than that of the PPSC, the loss breakdown and the overall efficiency of the converters are similar for a given modulation index (and corresponding transformer turns ratio). The PPSC uses less semiconductors of a higher current rating than the MMC, but the overall "installed semiconductor powers" of both converters are equal.

The transformers can be designed to provide enough leakage inductance in each arm path, eliminating the need for separate arm inductors in the PPSC. Considering offshore converter platforms, where the space is limited, this may be an advantage. Transformers with 18% reactance, as reported in [37], are considered in the simulations of both converters.

The SM capacitor value and the current rating of the IGBTs in the PPSC are 50% larger than the MMC case. Note that the voltage rating of the IGBTs are the same for both converters. Clearly, each SM for the PPSC would be approximately 50% larger than the MMC. However, the total SM volume would be about the same since the total energy storage and the installed semiconductor power requirements are the same for both converters. It is anticipated that the same total energy could be

distributed in a more compact way due to the smaller number of SMs in the PPSC.

Since the secondary windings of the transformer units in Fig. 1 are directly connected to the arm stacks, dc stress contributes to the insulation voltage and apparent power rating of the transformers in the PPSC. Note that this is not the case for the MMC. Moreover, the insulation voltage with respect to the ground of each secondary winding varies for each transformer unit in the PPSC due to the series connection of the phases on the dc side. In the case where the negative pole of the dc link is grounded as an example, the maximum insulation voltage for each secondary winding for three-phase PPSC and the MMC are calculated as in (31) and (32), respectively (see Table II). Recall that $k = 1$, 2, and 3 for the phases a, b, and c, respectively

$$V^k_{\text{ins,PPSC}} = \frac{r_{\text{PPSC}}\, V_s}{2} + \frac{(3-k)\, V_{\text{dc}}}{3} \tag{31}$$

$$V^k_{\text{ins,MMC}} = r_{\text{MMC}}\, V_s. \tag{32}$$

The single-phase transformers in the PPSC must be rated for the rms arm current since the arm currents are carried by the secondary windings of the transformers. The dc current does not contribute to the transformer apparent power rating in the MMC as the arm currents do not flow into the transformer windings. The rating of the primary winding is the same in both cases. The apparent power rating of the single-phase transformers (based on the secondary) are calculated as follows and illustrated in Table II:

$$S^k_{\text{tr,PPSC}} = r_{\text{PPSC}}\, V_s^{\text{rms}}\, I_{\text{arm}}^{\text{rms}} \tag{33}$$

$$S^k_{\text{tr,MMC}} = V_s^{\text{rms}}\, I_s^{\text{rms}}. \tag{34}$$

The numerical comparisons have shown that the overall footprint of the converter stacks would be about the same size. The overall converter footprint is increased by the six arm inductors in the MMC. The PPSC does not require physical arm inductors. However, due to the higher insulation requirements and the increased secondary winding apparent power, each transformer unit will be larger in the PPSC. In this numerical example, the total insulation voltage rating of the transformers used in the PPSC is 40% higher than the MMC case. Moreover, the overall apparent power rating of the transformers in the PPSC is 23% higher than the MMC.

E. Simulation Results

The specifications summarized in Tables I and II, for a small scale HVdc demonstrator [37], are used to validate the PPSC converter operation through simulation studies. A transformer turns ratio of $r_{\text{PPSC}} = 1.33$ which results in a modulation index of $m = 0.9$ is used in the simulation of the PPSC to allow a $\pm 10\%$ ac voltage variation margin. The arrangement shown in Fig. 2 is used in the simulations with the dc side modeled as a resistive load R_{LOAD} of 20 Ω in series with an inductance of 22 mH as suggested in [37].

Simulation results are initially obtained for 20-MW active power and zero reactive power exchanged with the grid. Fig. 6 illustrates the converter ac output voltages and the grid side ac currents.

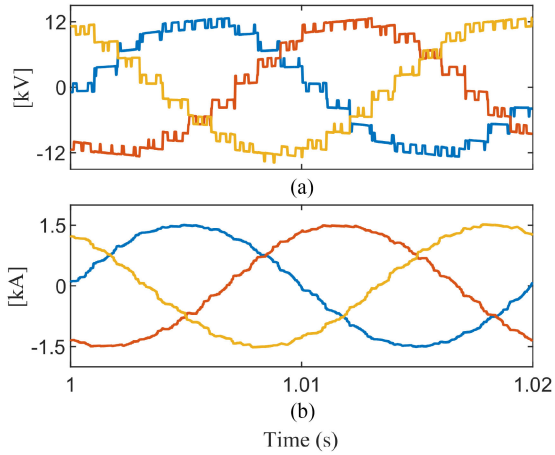


Fig. 6. Simulation plots of converter ac output voltage and ac grid current for PPSC, 20-MW rectification, and 0-MVAR reactive power exchange. (a) AC converter output voltage measured on the secondary side of the transformer. (b) AC current measured on the primary side of the transformer.

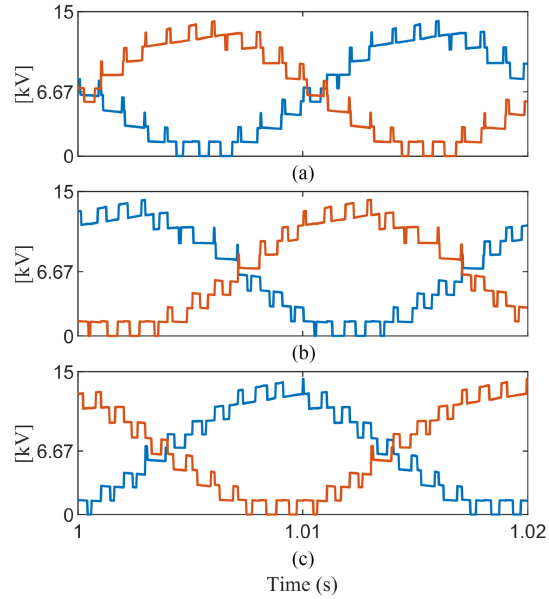


Fig. 7. Simulation plots of converter arm voltages of the PPSC, 20-MW rectification, and 0-MVAR reactive power exchange. (a) Phase a. (b) Phase b. (c) Phase c.

The arm voltages illustrated in Fig. 7 have components at supply frequency along with a dc offset and switching ripple resulting from the PWM operation. As expected, the dc offset is one-third of the total dc voltage (6.67 kV). Fig. 8 shows the arm currents. These have a mean value of ($I_{\text{dc}}/2 =$ 500 A) and, therefore, sum to the total dc current in each phase. The circulating currents and the fast Fourier transform (FFT) of the phase-a circulating current are illustrated in Fig. 9(a) and (b), respectively. The second harmonic current component is approximately zero as expected. The third harmonic component of the circulating current as calculated from (20) for the

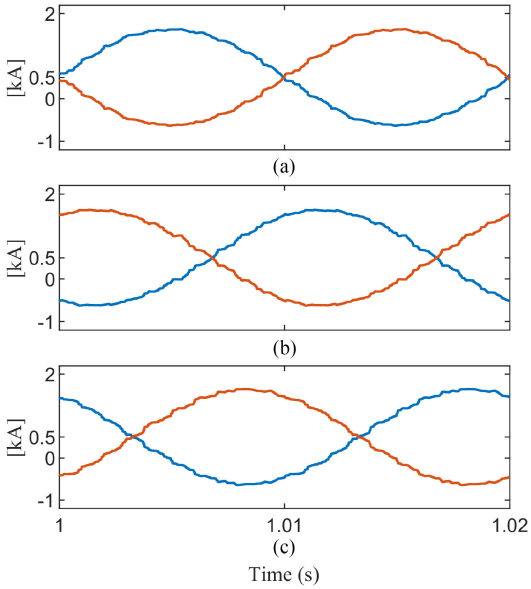


Fig. 8. Simulation plots of converter arm currents of the PPSC, 20-MW rectification, and 0-MVAR reactive power exchange. (a) Phase-*a*. (b) Phase-*b*. (c) Phase-*c*.

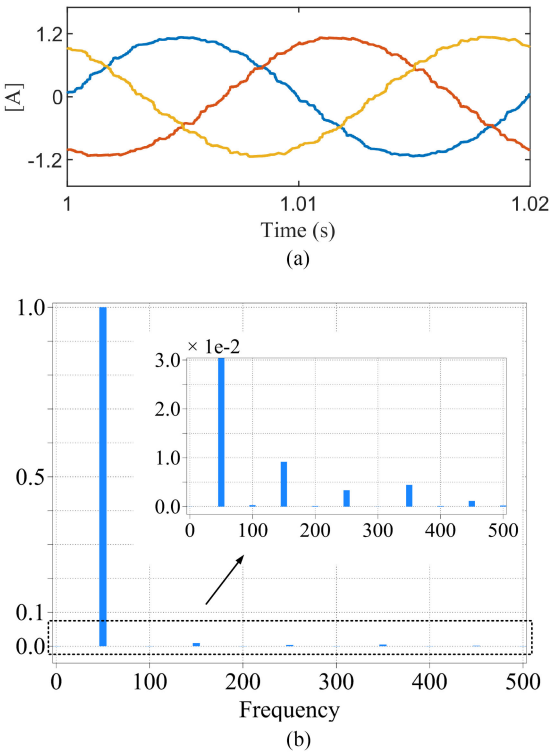


Fig. 9. Simulation plots of circulating currents of the PPSC, 20-MW rectification, and 0-MVAR reactive power exchange. (a) Circulating currents. (b) FFT of the circulating current in phase-*a* normalized to the fundamental component.

arm impedances given in Table II is approximately 1% of the fundamental component.

The dc voltage and dc current are shown in Fig. 10. While the voltage has switching components with a peak-to-peak magnitude of $3V_{\text{cap}}^{\text{nom}}$, the low frequency arm components cancel on the dc side, leaving the dc current free from low frequency ac ripple.

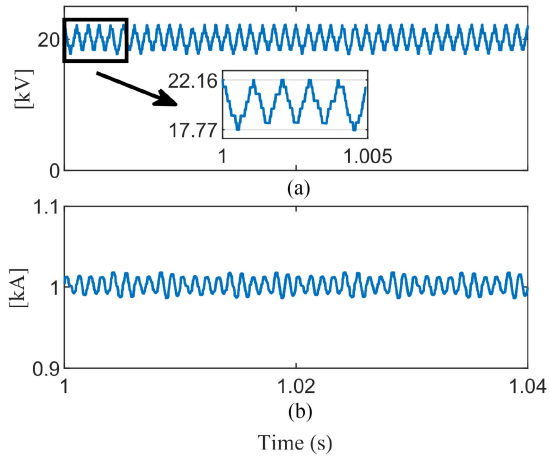


Fig. 10. Simulation plots of converter dc output voltage and dc load current for PPSC, 20-MW rectification, and 0-MVAR reactive power exchange. (a) DC converter output voltage. (b) DC load current.

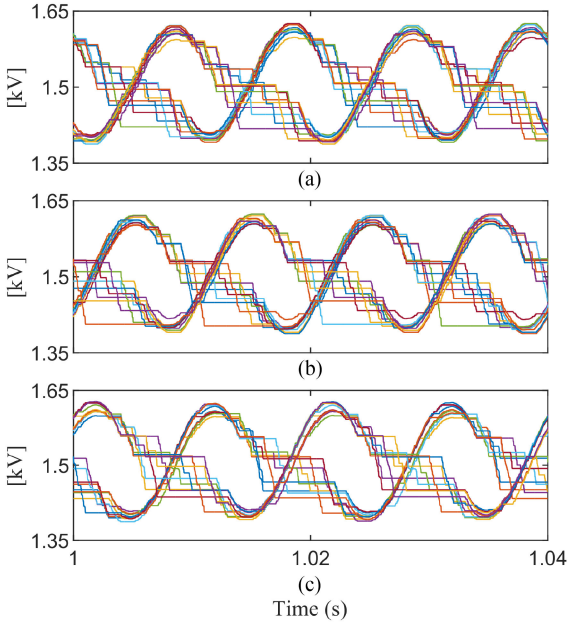


Fig. 11. Simulation plots of capacitor voltages for PPSC, 20-MW rectification, and 0-MVAR reactive power exchange. (a) Phase-*a*. (b) Phase-*b*. (c) Phase-*c*.

Fig. 11 shows the SM capacitor voltages which are well balanced with an average value equal to the reference of $V_{\text{cap}}^{\text{nom}} = 1.5$ kV. Similar to an MMC, the ripple is at the grid supply frequency and, in this case, is less than $\pm 10\%$, noting that $\pm 10\%$ is the design value for worst case ($P = 20$ MW, $Q = 8$ MVAR, and $m = 0.9$).

The transient response of the converter to a 10% ac voltage sag is illustrated in Fig. 12. Initially, the converter is operating at a modulation index of $m = 0.9$, rectifying 20-MW active power and exchanging 8-MVAR reactive power with the grid. At 1.08 s, a voltage sag of 10% is applied to all grid phases which suddenly changes the modulation index to approximately $m = 0.8$. The converter is able to adapt to the new modulation index and adjust the ac output voltage accordingly to continue

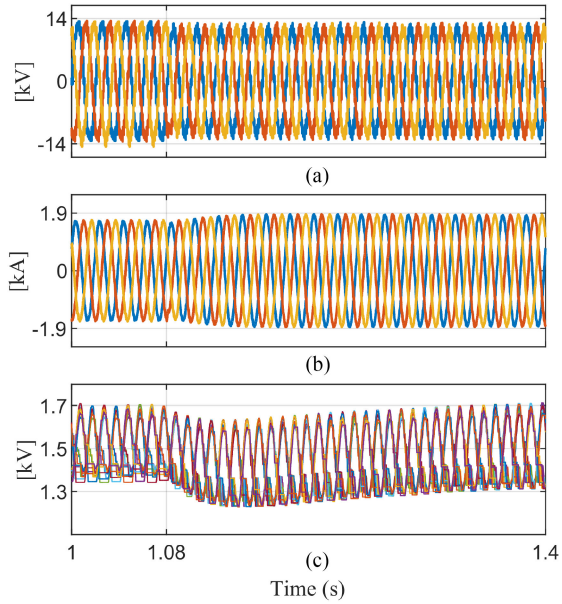


Fig. 12. Simulation plots for transient response of PPSC for a 10% ac voltage sag, 20-MW rectification, and 8-MVAR reactive power exchange. (a) AC converter output voltage measured on the secondary side of the transformer. (b) AC current measured on the primary side of the transformer. (c) Capacitor voltages of phase-a.

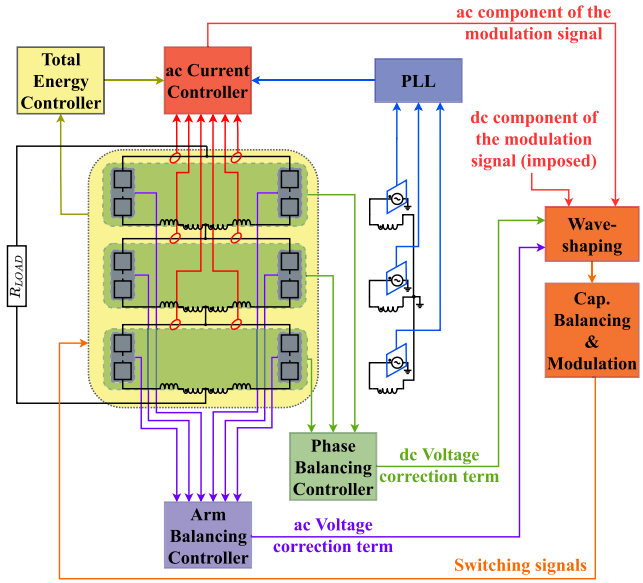


Fig. 13. General control philosophy for PPSC.

exchanging the required power with the grid. Accordingly, the ac current magnitude is increased to maintain the same power. The capacitor voltages are well balanced throughout the transient and their average value is controlled to the nominal value (1.5 kV). The capacitor voltage ripple increases since the modulation index is decreased and the current increases.

IV. Control Strategy for the PPSC

In this section, the control strategy used for validation of the PPSC operation is explained. Since the same arrangement (see Fig. 2) is used for the simulation and the experimental setup, the control strategy is developed for that arrangement.

Control of the PPSC is very similar in concept to that of the traditional MMC with similar objectives, namely: 1) the total energy stored in the converter must be maintained; 2) internal energy balance must be achieved within the converter [50]. In a standard MMC, internal energy balance is achieved by balancing the energy share among three parallel converter phases, controlling the power exchange between the two arms in each phase, and ensuring the SM capacitor balance within each arm through sorting [6]. A similar approach can be used for the PPSC, the main difference being the use of voltage components rather than circulating currents because of the parallel–series duality between the topologies. Phase balancing and arm balancing are achieved by modifying the circulating current references in the MMC [51]. In the PPSC, the same dc current flows in all phases, while the ac current circulates within them. Consequently, the ac and dc voltage components of each phase/arm are used to achieve phase and arm balancing. Additionally, the dc current difference between the left and right arms in each phase must be actively driven to zero to prevent transformer saturation. Many variations on the basic approach for control and modulation of the standard MMC have been presented in the literature. All of those can be applied to the PPSC with appropriate modification for the parallel/series duality. In this introductory article on the PPSC topology, the basic control strategy is utilized in order to prove the operation of the proposed converter.

The general control philosophy is illustrated in Fig. 13. In this case, the dc side voltage is set to a reference value by imposing the dc modulation term and the dc current is not controlled in closed loop. The dc side power is determined by the load connected. A total energy controller maintains the overall converter energy at the desired value by acting on the real power component of the ac side currents (via an ac current control loop) to maintain balance of the ac and dc side powers (neglecting losses) in steady state. The current loops are much faster than the energy controller and also allow the reactive power to be controlled independently. Furthermore, two controllers are needed. The first ensures energy balance between the three series connected phases by acting on the dc modulation signals to adjust the contribution of each phase to the total dc voltage. The second additional controller balances the active power between the left and the right arms by generating an ac voltage correction term for each phase, which is added to the corresponding ac modulation signal. The composite ac and dc modulation signals for each arm then form the inputs to the modulator. The individual controllers are discussed in more detail as follows.

A. AC Current Controller

Three independent single-phase ac current controllers [see Fig. 14(b)] are used employing a standard quadrature signal generator based phase locked loop (QSG-PLL) [52] to calculate the phase angle θ_s^k of each phase for synchronization. The ac current reference is then formed by summing the reference active

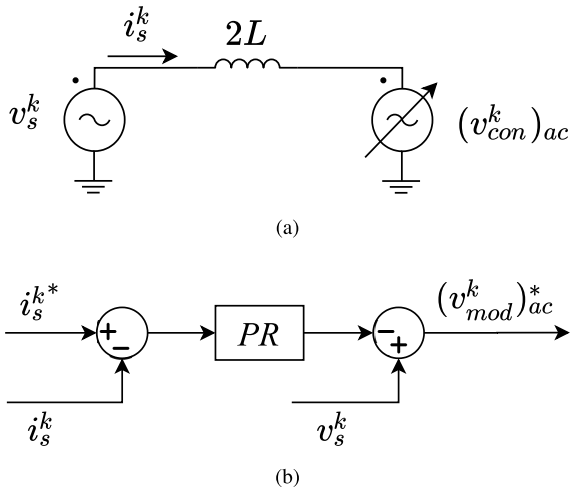


Fig. 14. Equivalent ac grid side and ac current controller for phases $k = a, b, c$. (a) AC side equivalent circuit for each phase. (b) Single-phase ac current controllers.

and reactive power components (35)

$$i_s^{k*} = I_{\text{act}}^* \sin(\theta_s^k) + I_{\text{react}}^* \cos(\theta_s^k). \tag{35}$$

As mentioned before, in the PPSC, the dc components of the two arm currents must be equal to avoid transformer saturation. To ensure this, the arm currents are sensed and the ac currents are calculated from the difference of the two arm currents as

$$i_s^k = \frac{i_l^k - i_r^k}{2}. \tag{36}$$

In this way, any difference between the dc components of the arm currents is detected and compensated for by the ac current controller generating a dc offset term in the arm voltage references. Asymmetry between two arms is expected to be small in a good design, and, therefore, the correction terms will be small. Since the ac current controller has higher bandwidth than any of the other controllers, it can be assumed that the dc voltage offsets generated by the ac current controller will not affect the slow energy balancing controllers.

Fig. 14(a) shows the ac equivalent circuit for each phase where $(v_{\text{con}}^k)_{\text{ac}}$ is the ac output voltage of each converter phase and is expressed as the difference between the left and the right arm voltages

$$(v_{\text{con}}^k)_{\text{ac}} = v_r^k - v_l^k. \tag{37}$$

The sum of the transformer leakage inductance referred to the secondary, i.e., $2L$ forms the equivalent inductance for the current control. A standard proportional resonant (PR) controller (reported in [53]) is used to track the ac current references. It is important to note that since the supply voltage is measured on the grid side of the transformer, the transformer is contained within the high bandwidth current loop. It is assumed that the magnetizing current is negligible and, therefore, that the primary current follows the scaled secondary current with negligible error. This is a good assumption for a grid transformer where the magnetizing current is typically less than 2% [20].

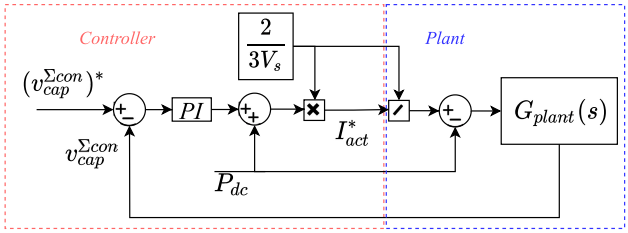


Fig. 15. Total energy controller.

B. Total Energy Controller

Assuming well-balanced capacitors and neglecting the capacitor voltage ripple, the relationship between the total capacitor voltage and the power for a given number of SMs can be approximated as

$$p = C_{\text{sm}}^{\text{nom}} V_{\text{cap}}^{\text{nom}} \frac{dv_{\text{cap}}^{\Sigma}}{dt}. \tag{38}$$

The plant for each energy controller therefore has the form

$$G_{\text{plant}}(s) = \frac{v_{\text{cap}}^{\Sigma}(s)}{p(s)} = \frac{1}{sC_{\text{sm}}^{\text{nom}} V_{\text{cap}}^{\text{nom}}}. \tag{39}$$

Fig. 15 shows the total energy controller block diagram. Global power balance is achieved by maintaining the total capacitor voltage summed over all SMs at a reference value, i.e., $(v_{\text{cap}}^{\Sigma\text{con}})^* = 6N_{\text{sm}}V_{\text{cap}}^{\text{nom}}$. A proportional–integral (PI) controller acts on the total voltage error and sets the active power part of the ac current reference after scaling. The control is augmented by feed-forward of the dc power value.

C. Phase Balancing Controller

Phase energy balancing is achieved by regulating the proportion of the total dc side power contributed by each phase by adjusting its contribution to the total dc voltage. This is directly analogous to the MMC case where the same objective is achieved by adjusting the contribution of each phase to the total dc current.

Three PI controllers are used for phase balancing to force the total SM capacitor voltages in each phase to track the reference value $(v_{\text{cap}}^{\Sigma\text{ph}})^* = 2N_{\text{sm}}V_{\text{cap}}^{\text{nom}}$ as shown in Fig. 16. Feed forward of the ac power divided by I_{dc}, together with the PI controller outputs, is used to derive a share factor x_{dc}^k of the total dc voltage for each phase. The reference dc modulation signal $(v_{\text{mod}}^k)_{\text{dc}}^*$ for each phase is then formed by multiplying its share factor by the total dc voltage reference $(V_{\text{mod}}^{\text{dc}})^*$. Note that $x_{\text{dc}}^{\Sigma\text{ph}} = 1$ so that the balancing action does not affect the total dc voltage.

D. Arm Balancing Controller

Under ideal operating conditions and with a perfectly symmetrical circuit, an arm balancing controller would not be needed according to (22). However, for example, since it is imperative to ensure equal dc currents in both arms, any difference in the dc voltage drop across each arm impedance will be reflected in a difference in the dc modulation terms as discussed in Section IV-A. This will unbalance the arm energies unless corrective action is taken. Other parameter differences between

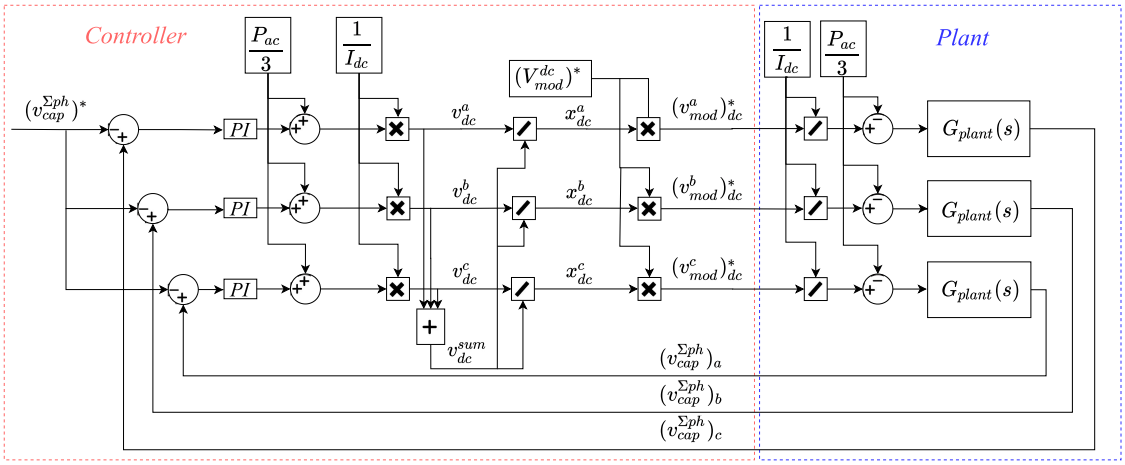


Fig. 16. Phase balancing controller.

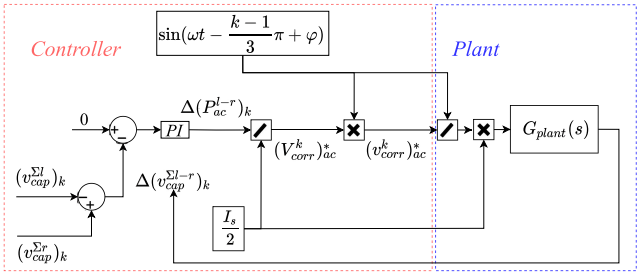


Fig. 17. Arm balancing controller.

the arms will also create imbalance. Recalling that an ac current circulates in each phase, it is possible to mitigate any imbalance created by parameter differences by adding a common mode ac voltage term to the modulation reference for both arms. This allows energy transfer between the two arms with no effect on the overall ac voltage generated at the grid side.

Fig. 17 illustrates the controller which implements arm balancing. A PI controller acts on the capacitor voltage difference between the arms, $\Delta(v_{\text{cap}}^{\Sigma l-r})_k$, and generates a mean ac power difference term $\Delta(P_{\text{ac}}^{l-r})_k$. Taking into account the ac phase current magnitude I_s, an ac voltage magnitude correction term $(V_{\text{corr}}^k)_{\text{ac}}^*$ is created. This, in turn, is used to generate ac voltage correction waveform $(v_{\text{corr}}^k)_{\text{ac}}^*$ in phase with the corresponding phase current. Note that whilst the common mode ac voltage correction term will appear on the dc voltage as ripple, it will be very small in any well-designed converter (noting that there will also be partial cancelation between the three phases).

Considering all the control actions, the final modulation signals for each arm are given by

$$(v_{\text{mod}}^k)_l^* = (v_{\text{mod}}^k)_{\text{dc}}^* - \frac{(v_{\text{mod}}^k)_{\text{ac}}^*}{2} + (v_{\text{corr}}^k)_{\text{ac}}^* \tag{40}$$

$$(v_{\text{mod}}^k)_r^* = (v_{\text{mod}}^k)_{\text{dc}}^* + \frac{(v_{\text{mod}}^k)_{\text{ac}}^*}{2} + (v_{\text{corr}}^k)_{\text{ac}}^*. \tag{41}$$

TABLE III
PPSC EXPERIMENTAL RIG SPECIFICATIONS

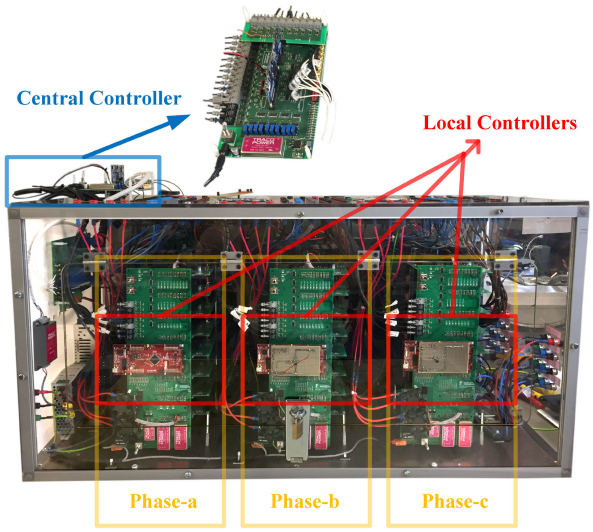
Rated power	P	1.5kW
Reactive Power	Q	±1kVAR
Line-to-line rms voltage	V_{ac}	190V
dc voltage	V_{dc}	300V
Frequency	f	50Hz
Transformer turn ratio	r	140/240
Transformer secondary leakage inductance	L	0.615mH
Transformer apparent power rating	S_k	2kVA
Nominal cell capacitor voltage	V_{cap}^{nom}	50V
Nominal SM capacitor value	C_{cap}^{nom}	3.9mF
dc load	R_{LOAD}	60Ω
Carrier frequency	f_{PWM}	8kHz
Sorting frequency	f_{SORT}	2kHz

V. PPSC EXPERIMENTAL RESULTS

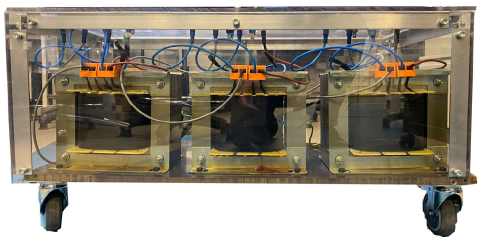
This section describes the experimental setup used for validating the proposed converter operation and explains the control strategy implementation. Experimental results for both steady-state and transient operation are presented.

A. Small-Scale Experimental Rig

Photographs of the small-scale converter prototype and the single-phase transformer units are shown in Fig. 18(a) and (b), respectively. In all the tests, the converter is operated in rectification mode using the basic arrangement shown in Fig. 2. A three-phase programmable power source (Chroma-61511) connected via three single-phase center-tapped transformers is used on the ac side with a resistive load on the dc side. The system parameters are given in Table III. Note that the transformer turns



(a)



(b)

Fig. 18. Photograph of the small-scale experimental setup. (a) Converter stacks and the controllers. (b) Single-phase transformer units.

TABLE IV
CONTROLLER PARAMETERS USED IN EXPERIMENT OF PPSC

	Bandwidth (Hz)	Phase margin
ac current controller	150	70°
PLL	3	50°
Total Energy controller	5	80°
Phase Balancing controller	3	80°
Arm Balancing controller	1	80°

ratio is represented by the ratio of the rms voltage ratings of the windings. Single-phase transformers with higher than the required power rating are used in the experiments due to their availability in the lab.

There are eight half-bridge SMs in each phase; four in each converter arm. Infineon IPB072N15N3 MOSFETs, rated at 150 V and 100 A are used for the switching devices. The SM capacitance value is greater than that required for ±10% voltage fluctuation (1.4 mF)—which would be a typical design value. This is due to limitations of the experimental rig which is a generic design used for testing other MMCs with higher specific energy. The design specifications for the control loops are given in Table IV.

B. Digital Control System

A central-local control structure using microcontroller units (MCUs) has been employed to implement the control strategies. A local MCU, using a Texas Instruments F28377S LaunchPad in each phase, sends the sum of the sensed SM capacitor voltages in each arm to the central controller (Texas Instruments F28379D). The central controller generates the reference voltages for each arm by using information from the local controllers. These reference voltages are then sent to the local control units. Switching signals for each SM are generated in the local controllers using a PD-PWM method described in [54] with capacitor voltage balancing algorithm explained in [47]. It should be noted that any modulation and capacitor voltage balancing method presented in literature for the standard MMC can be applied to the proposed converter.

C. Experimental Results

To experimentally validate the converter operation and its control, results for steady-state and transient operation are presented in this section. The data has been acquired via four oscilloscopes as well as via the central controller. The oscilloscopes that have been used are the following:

1) Tektronix TDS3014 with a bandwidth of 100 MHz and maximum sample rate of 1.25 GSa/s;
2) Tektronix MSO4034 with a bandwidth of 350 MHz and maximum sample rate of 2.5GSa/s;
3) Tektronix MSO4054 with a bandwidth of 500 MHz and maximum sample rate of 2.5GSa/s;
4) Agilent DSO-X 2004 A with a bandwidth of 70 MHz and maximum sample rate of 2GSa/s.

The data acquired via the central controller have a sampling frequency of 2 kHz, i.e., (PWM sampling frequency)/4.

1) Steady-State Experimental Results: The first study case considers steady-state operation. The power delivered to the dc load is 1.5 kW and the reactive power reference is set to zero. The converter ac output voltages, measured on the secondary side of the transformer, are shown in Fig. 19(a). As expected, the converter ac output voltage has nine levels. The ac grid currents in Fig. 19(b) are measured on the primary side of the transformer.

Figs. 20 and 21 illustrate the arm voltages and currents, respectively, of all the phases. As expected, the mean value of the arm voltage in each phase is approximately 100 V (one-third of the total dc output voltage). The sum of the arm currents in each phase is equal to the dc current (5 A). The circulating currents, which are calculated from (36), are illustrated in Fig. 22(a). Fig. 22(b) shows the FFT of the phase-*a* circulating current. As expected, the odd harmonics are dominant. Since the ac grid is not harmonic free and the components are not ideal in the practical system, the amplitudes are slightly higher than predicted. However, the dominant harmonic components are still only around 1.5% of the fundamental component and have a negligible effect.

Fig. 23 shows the dc voltage and current. The peak-to-peak value of the switching ripple in the dc voltage is approximately $3(V_{\text{cap}})_{\text{nom}}$. SM capacitor voltages in all three phases are shown in Fig. 24 illustrating that they are well balanced with a mean

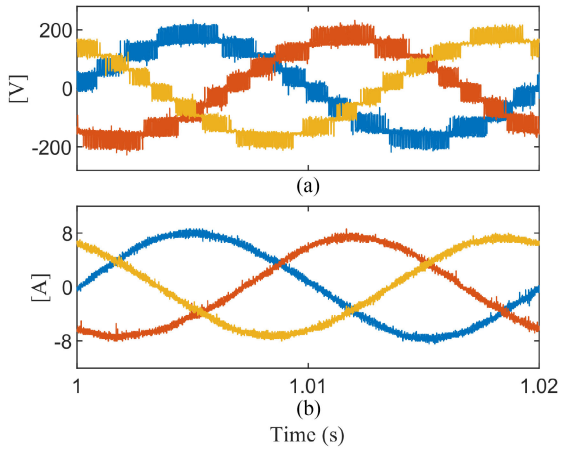


Fig. 19. Experimental plots of converter ac output voltage and ac grid current for PPSC, 1.5-kW rectification, and 0-kVAR reactive power exchange. (a) AC converter output voltages measured on the secondary side of the transformer (Tektronix MSO4034). (b) AC currents measured on the primary side of the transformer (Tektronix TDS3014).

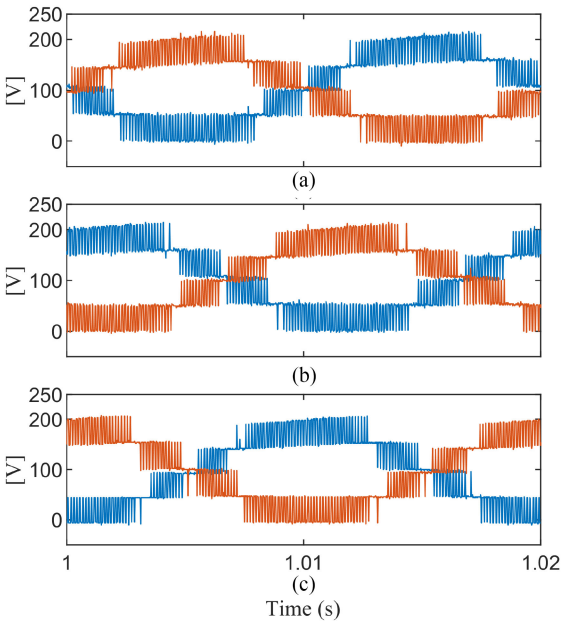


Fig. 20. Experimental plots of converter arm voltages of the PPSC, 1.5-kW rectification, and 0-kVAR reactive power exchange. (a) Phase-*a* (Tektronix MSO4054). (b) Phase-*b* (Tektronix MSO4054). (c) Phase-*c* (Agilent DSO-X 2004 A).

value equal to the reference of 50 V. As expected, the capacitor voltages have ripple at the grid supply frequency (50 Hz).

Operation of the converter for different reactive power requirements is also validated via experiments. Steady-state results when the converter exchanges inductive (1 kVAR) and capacitive (–1 kVAR) reactive power with the grid are illustrated in Figs. 25 and 26, respectively.

2) Transient Response of the AC Current Controller: In order to test the response of the ac current controller, a step change is applied to the reactive power component. The reactive power current reference is changed from 0 to 4 A at $t = 1.03$ with the initial conditions as given in Table III. This corresponds to a

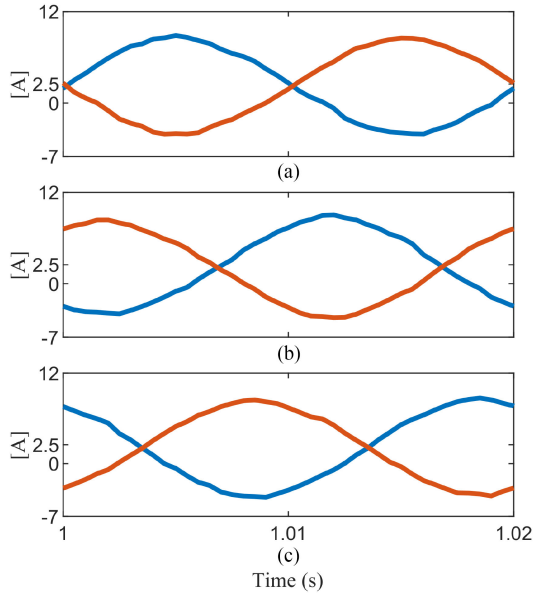


Fig. 21. Experimental plots of converter arm currents of the PPSC, 1.5-kW rectification, and 0-kVAR reactive power exchange (data acquired via the central controller for all the phases). (a) Phase-*a*. (b) Phase-*b*. (c) Phase-*c*.

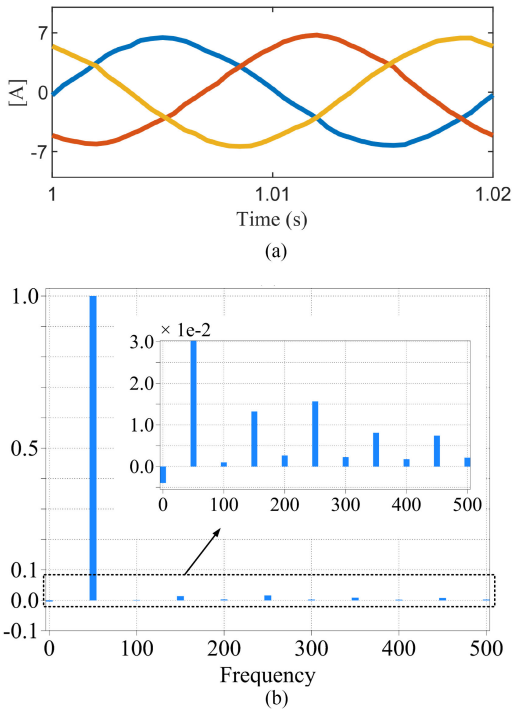


Fig. 22. Experimental plots of circulating currents of the PPSC, 1.5-kW rectification, and 0-kVAR reactive power exchange (data acquired via the central controller for all the phases). (a) Circulating currents. (b) FFT of the circulating current in phase-*a* normalized to the fundamental component.

step change in reactive power reference (from 0 to 1 kVAR) and, hence, the power factor (from 1 to 0.83). The transient response of the phase-*a* ac current controller is shown in Fig. 27. The current controller is able to retrack the sinusoidal ac current reference in approximately half a cycle.

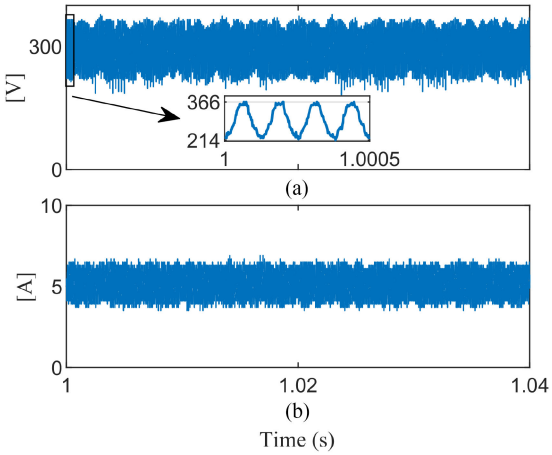


Fig. 23. Experimental plots of converter dc output voltage and dc load current for PPSC, 1.5-kW rectification, and 0-kVAR reactive power exchange. (a) DC converter output voltage (Tektronix MSO4034). (b) DC load current (Agilent DSO-X 2004 A).

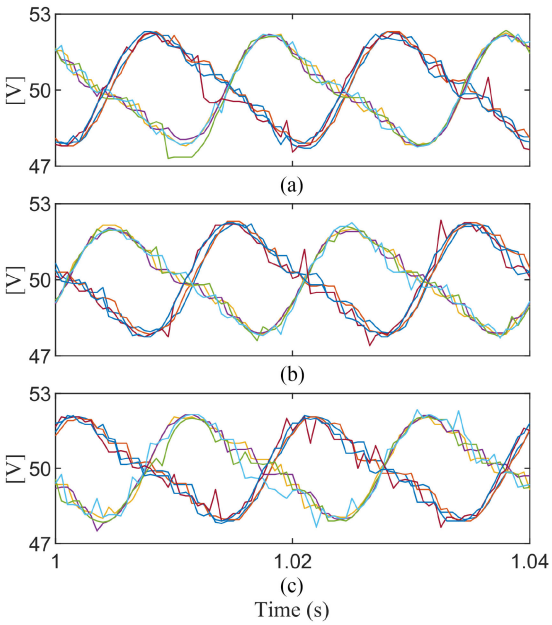


Fig. 24. Experimental plots of capacitor voltages for PPSC, 1.5-kW rectification, 0-kVAR reactive power exchange (data acquired via the central controller). (a) Phase-*a*. (b) Phase-*b*. (c) Phase-*c*.

3) Transient Response of the Total Energy Controller: The aim of this article case is to test the transient response of the total energy controller, which is responsible for keeping the total capacitor voltage of the converter at the desired reference value. Therefore, a step change in the total capacitor voltage reference $(v_{\text{cap}}^{\Sigma\text{con}})^*$ has been imposed to test its functionality. The reference value is changed from 1200 to 1272 V at $t = 1.1$ s as shown in Fig. 28. The controller restores the total energy balance of the converter within the designed settling time (0.4 s), as calculated from the specifications given in Table IV.

4) Transient Response of the Internal Energy Balancing Controllers: In order to verify the response of the internal energy balancing controller to disturbances, a dc load step has been

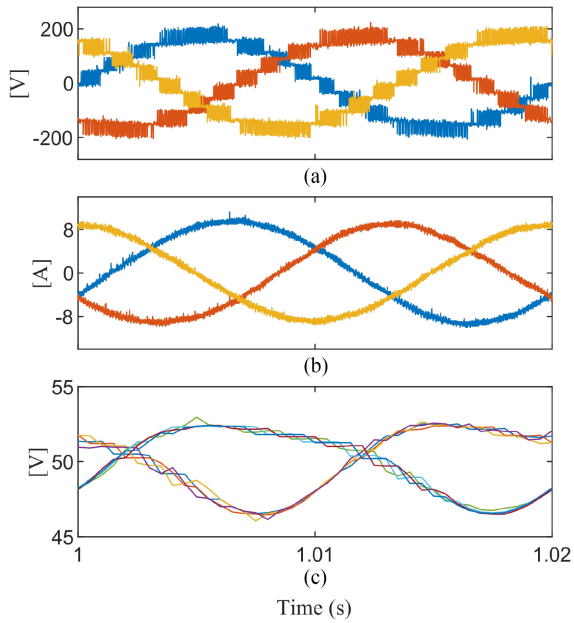


Fig. 25. Experimental plots for PPSC, 1.5-kW rectification, and 1-kVAR reactive power exchange (inductive). (a) AC converter output voltages measured on the secondary side of the transformer (Tektronix MSO4034). (b) AC currents measured on the primary side of the transformer (Tektronix TDS3014). (c) Capacitor voltages of phase-*a* (data acquired via the central controller).

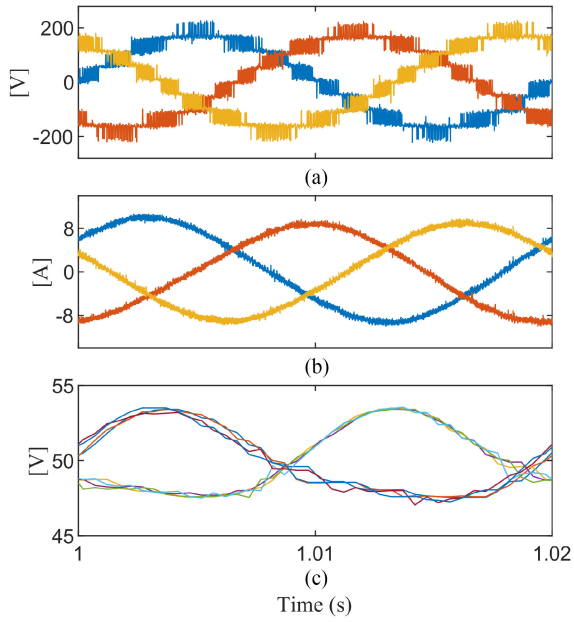


Fig. 26. Experimental plots for PPSC, 1.5-kW rectification, and –1-kVAR reactive power exchange (capacitive). (a) AC converter output voltages measured on the secondary side of the transformer (Tektronix MSO4034). (b) AC currents measured on the primary side of the transformer (Tektronix TDS3014). (c) Capacitor voltages of phase-*a* (data acquired via the central controller).

applied. The dc load is stepped up from 60 to 90 Ω at $t = 1.1$ s, which corresponds to a dc power change from 1.5 to 1 kW. The transient responses of the phase balancing and the arm balancing controllers are illustrated in Figs. 29 and 30, respectively. Fig. 29 illustrates the sharing factors of each phase for this transient. The phase balancing controllers are able to rebalance each phase

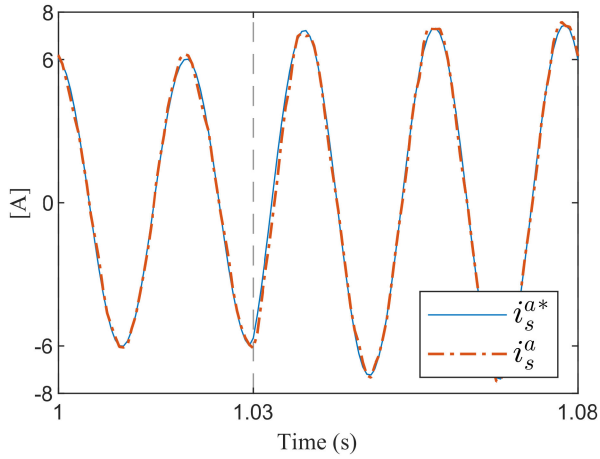


Fig. 27. Transient response of the ac current controller to a step change in the reactive part of the ac current (data acquired via the central controller).

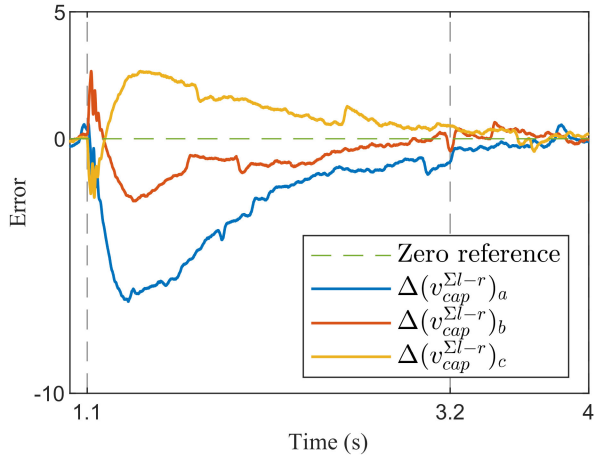


Fig. 30. Transient response of the arm balancing controller to a step change in the dc load (data acquired via the central controller).

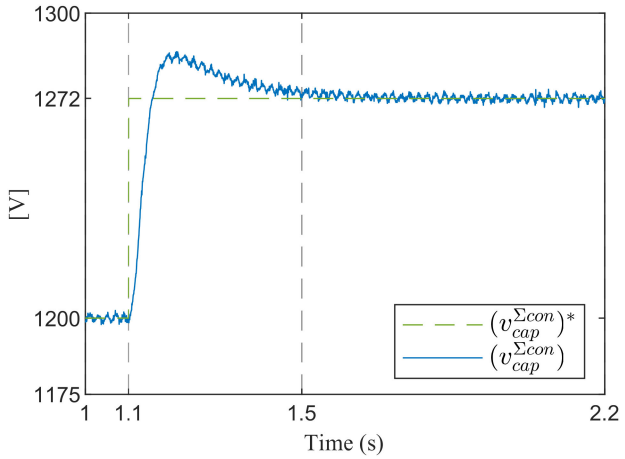


Fig. 28. Transient response of the total energy controller to a step change in the total capacitor voltage reference (data acquired via the central controller).

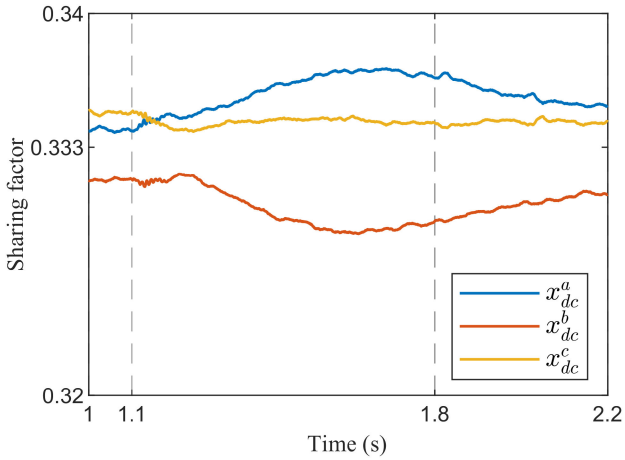


Fig. 29. Transient response of the phase balancing controller to a step change in the dc load (data acquired via the central controller).

with a settling time of 0.7 s as expected. The difference between the left and the right total capacitor voltages in each phase is recompensated to zero by the arm balancing controllers after the load change applied. The calculated settling time from the design parameters is approximately 2.1 s and matches well with the measured settling times shown in Fig. 30.

VI. Conclusion

This article has presented a new PPSC MMC. A detailed analysis of the operating principle has been presented and suitable control strategies for energy management have been derived. The proposed converter retains the benefits of the traditional MMC such as utilizing a modular arm structure and having ripple-free dc current. Series connection of the phases, rather than the MMC parallel connection, allows a reduction in the number of SMs (of a given voltage). The total energy storage requirement is the same as that for a traditional MMC, but it is distributed across fewer SMs. This may allow a more compact arrangement which will be attractive, for example, for offshore HVdc applications. The parallel/series duality of the PPSC with the MMC means that all of the research efforts on MMC control can be directly translated to the PPSC. In particular, like the MMC, the PPSC retains largely decoupled control of the ac and dc sides which is a feature lost in many other MMC variants. While the PPSC concept requires grid interface transformers to function (which the traditional MMC does not), transformers are mandatory in the majority of expected applications for other reasons and this is not seen as a disadvantage. Additionally, it is expected that the arm inductance can be provided by the transformers, and this may further decrease the overall converter footprint compared to a traditional MMC (which requires separate arm inductors). Steady-state experimental results obtained using a small-scale laboratory prototype have been presented to validate the operation of the converter. Experimental results obtained from transient tests have been presented to validate the energy management analysis and control design.

APPENDIX
LOSS ESTIMATIONS

Losses are calculated by using device datasheet parameters provided by the manufacturer and by considering the conduction states in the half-bridges. The methodology is well established [42], [43]. An identical approach is used for the MMC and the PPSC by substituting the appropriate arm voltages into (42) and (43) and device currents in (44) for each converter.

The number of half-bridge SMs that are ON in each arm at a given time can be approximated as follows:

$$n_{\text{on}} = \frac{v_{l,r}^{k}}{V_{\text{cap}}} \tag{42}$$

where $v_{l,r}^{k}$ is the instantaneous arm voltage. Hence, the number of half-bridge SMs that are OFF at every instant is

$$n_{\text{off}} = N_{\text{sm}} - n_{\text{on}}. \tag{43}$$

The instantaneous conduction losses for each arm can then be calculated by

$$p_{\text{cond}}^{\text{arm}} = \begin{cases} n_{\text{on}}\ P_{\text{IGBT}}(|i_{l,r}^{k}|) + \\ n_{\text{off}}\ P_{\text{diode}}(|i_{l,r}^{k}|), \quad \text{if } (i_{l,r}^{k} > 0) \\ n_{\text{on}}\ P_{\text{diode}}(|i_{l,r}^{k}|) + \\ n_{\text{off}}\ P_{\text{IGBT}}(|i_{l,r}^{k}|), \ \text{if } (i_{l,r}^{k} < 0). \end{cases} \tag{44}$$

Here, $P_{\text{IGBT}}(|i_{l,r}^{k}|)$ and $P_{\text{diode}}(|i_{l,r}^{k}|)$ represent the power loss characteristic curves of the IGBTs and diodes as a function of the current through them, which are obtained from the device datasheets. When the arm current is positive, an IGBT and a diode are conducting in the ON- and OFF-half-bridge SMs, respectively, and vice versa for the negative arm current. The instantaneous conduction power loss expression $p_{\text{cond}}^{\text{arm}}$ can then be averaged over a fundamental cycle to obtain the conduction losses for each arm.

The switching losses can be calculated considering the energy loss occurring during the commutation between the semiconductor devices due to the switching from one state to another. There are two types of commutations: 1) IGBT switches OFF and diode turns ON and 2) diode turns OFF and IGBT switches ON. Note that in the former, only the energy loss due to the IGBT switching OFF is considered and the energy loss due to the diode turn-ON is neglected.

The instantaneous switching power loss for each arm can be expressed as in (45), which can then be averaged over a fundamental period to obtain the switching losses in each arm

$$p_{\text{sw}} = f_{\text{sw}}\ n_{\text{on}} \left(\frac{E_{\text{on}}\ E_{\text{off}}\ E_{\text{rec}}\ |i_{l,r}^{k}|\ V_{\text{cap}}}{V_{\text{nom}}\ I_{\text{nom}}} \right). \tag{45}$$

Here, f_{sw} is the switching frequency. E_{on}, E_{off}, and E_{rec} are the energy loss values of turn-ON and turn-OFF of IGBT, and recovery loss of diode, respectively. The energy loss values for the devices are given in device datasheet for the device nominal current and voltage values (I_{nom} and V_{nom}). Therefore, the energy loss values in (45) are normalized by the *nominal semiconductor power* ($P_{\text{nom}} = V_{\text{nom}}\ I_{\text{nom}}$) of the devices.

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This article is dedicated to the memory of our fellow researcher, friend, and coauthor, Dr. Alessandro Costabeber. Alessandro was instrumental in the development of the topology and the research described in this article. He sadly died before the work could be completed.

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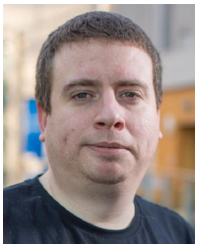

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