A Power Flow Tracing Method Based on Power Electronic Signaling for P2P Electricity Trading in DC Microgrids

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***Abstract*—This article proposes a novel power flow tracing method based on power electronic signaling for peer-to-peer (P2P) electricity trading in dc microgrids. It employs a superimposed low-frequency sinusoidal carrier to trace dc power flows according to the bus port impedance characteristics of power converters. In order to support fair and accurate P2P trading, source-to-load power signaling (S2LPS) and source-to-source power verification (S2SPV) methods are presented. Through S2LPS, the P2P dc power flow from a specific distributed source (DS) to a power load (PL) is determined by detecting the carrier's active power at the PLs bus port. The same carrier is used to check the actual output power of the DS by S2SPV. By implementing S2LPS and S2SPV, the power flows of the system are traced, recorded, and verified by each DS and PL. Accurate power flow tracing is achieved on the physical layer, providing reliable data for P2P electricity trading. The principles of the proposed method are deduced in detail. Furthermore, the modifications to the control loops of DSs and PLs are depicted for implementations in dc microgrids. Finally, a 2.5 kW experimental platform is built to validate the correctness and feasibility of the proposed method.**

***Index Terms*—Dc microgrids, peer-to-peer (P2P) trading, power electronic signaling, power flow tracing, superimposed carrier.**

I. Introduction

THE INCREASED penetration of renewable energy sources and energy storage sources poses significant challenges in system reliability and power management efficiency to traditional ac grid, and the dc microgrid could be a possible solution due to its improved efficiency, reduced complexity, and greater flexibility [1]–[3]. In dc microgrids, there are numerous prosumers that can both produce and consume power depending on different conditions and operation modes. Consequently, peer-to-peer (P2P) trading is a promising technique for dc microgrids as a next generation energy management method [4]–[10]. Through decentralized P2P structure, Prosumers can actively participate in the electricity market by acting as either sellers selling excess energy, or buyers purchasing electricity from other sellers. The ac grid can also reap significant benefits from the P2P structure, such as lower peak demand, lower investment costs, and reduced reserve requirements [4].

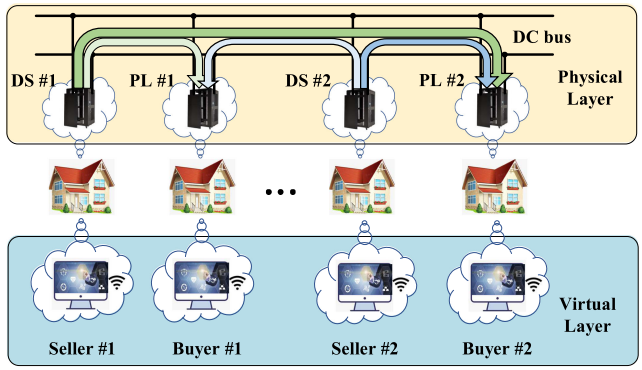

Fig. 1. Structure of P2P trading.

The P2P trading structure can be divided into two layers [5]: virtual layer and physical layer, as shown in Fig. 1. In the virtual layer, pricing mechanisms [6], [7] and information systems [7], [8] are implemented for financial and electricity transaction settlements. In the physical layer, traditional electrical networks are employed, and extra metering infrastructures are installed at bus ports of prosumers for input/output power measurements. Once the transaction between two prosumers is settled, the electrical network in the physical layer transfers power from the seller to the buyer in accordance with the virtual layer's instructions.

In P2P trading, most studies concentrate on the trading schemes [6]–[8] in the virtual layer, while physical layer only acts as a passive actuator [9], [10]. However, in practice, due to the absence of third-party arbitrators in the P2P scheme, disputes between seller, and buyer regarding the actual transmitted power may arise [5]. Furthermore, due to varying electricity storage statuses and power qualities of the sellers, and various demands of the buyers, distinguished electricity prices between

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each seller and each buyer are preferred in P2P trading scheme [11]–[13]. In this case, determining real-time P2P power flows contributes to a fair and reasonable pricing mechanism, and it could also facilitate the energy scheduling optimization in the virtual layer [14], [15]. Therefore, to ensure accurate and fair P2P transactions, it is necessary to trace the real-time P2P power flows from each seller to each buyer in the physical layer.

In the physical layer of dc microgrids, all prosumers are connected to a common dc bus via power electronics interface converters (PEICs), and the PEICs can be categorized into distributed sources (DSs) and power loads (PLs) according to the prosumer's character in P2P trading. The dc transferred power between DS and PL is mixed up in the bus, making it difficult for the PL (i.e., buyer) to distinguish the DS (i.e., seller) and the corresponding amount of received power. In this case, stamping power flows is a potential solution, and power electronic signaling (PES) is the most widely used power stamping method [16] in dc microgrids.

In the PES methods, PEICs are deployed to generate and control discernible signals for multiple information-oriented tasks [16]–[35]. PES methods can be further classified into three types: disturbance-based signaling, dc-bus signaling and PES digital communication method.

In the disturbance-based signaling method [17]–[24], small sinusoidal or impulse signals are superimposed by PEICs for monitoring, coordinating, and other purposes. In [17], in order to establish a logic channel among DSs in dc microgrids, sinusoidal signals of specific frequency are superimposed into the common bus by DSs. In [18], an adaptive droop controller based on a superimposed frequency is proposed, and the load sharing accuracy is improved without the use of an additional communication system. Similarly, the same superimposed frequency is used to achieve autonomous power management in [19]. In [20] and [21], positive feedback islanding detection methods with fast detection speed and high robustness are proposed and analyzed based on a power or current disturbance injection in the DSs control loop. In [22]–[24], the disturbance-based signaling method is employed for line impedance identification by injecting single impulse [22], [23] or sinusoidal signals with multiple frequencies [24] into the power electronics systems.

In the dc bus signaling method [25], [27], the dc bus voltage level is employed as an information carrier to set up communication links between difference source/storage PEICs. Each converter determines its operation mode according to the voltage level, realizing better power management, and system coordination.

PES digital communication method is a special kind of power line communication technique [29], [35]. Distinguished from the previous two types of methods, digital messages can be transmitted with the method. The digital data are modulated into the control loop [29], [31] or switching process [32], [35] of the PEIC transceiver, which causes voltage ripples on the dc bus. The PEIC receiver samples dc bus voltage ripples and decodes the data. Since no extra communication components are needed, the system structure can be simplified and the manufacturing cost can be reduced.

In conclusion, the traditional PES methods use power electronics circuits to generate recognizable signals, and the converter's operating messages are embedded in the power flows, resulting in benefits including simple implementation, high reliability, and low cost due to the absence of digital communication networks. However, these methods had no relevance to or application to P2P electricity trading. They are developed for system control purposes and the superimposed signals are only used to indicate system states. Furthermore, it is hard to build mathematical relationship between analogue/digital messages and power flows, making the messages incapable of representing quantitative power flow information. Thus, current PES methods cannot be directly used in power flow tracing.

This article proposes a novel PES method for P2P power flow tracing in residential dc microgrids to support fair and accurate P2P electricity trading. Inspired by current disturbance-based signaling methods, it employs superimposed low-frequency carriers to stamp dc power flows for physical layer tracing from the DS (i.e., seller) to the PL (i.e., buyer). In contrast to the traditional PES methods, the bus port impedances of power converters are controlled in the proposed method. Therefore, mathematical relationship between power flow and the carrier can be established, allowing the carrier to represent power flow information.

In the proposed method, a carrier with controlled active power is injected into the dc bus by each DS in rotation. Each PL measures the received active power at bus port to determine the source and corresponding amount of received dc power, which is termed as source-to-load power signaling (S2LPS) method in this article. In order to ensure the S2LPS data authenticity, the voltage amplitude of the carrier is used by other prosumers to check the actual dc output power of the DS, which is named as source-to-source power verification (S2SPV) method in this article. S2LPS measures the power flow between each DS and each PL, providing reliable physical layer data for P2P trading. The S2LPS and S2SPV data can be cross-checked, resolving trust issues between DSs and PLs.

The rest of this article is organized as follows. The origin of the proposed method is illustrated in Section II, and the principles of the proposed method, including S2LPS and S2SPV, are depicted in Section III. In Section IV, the implementations of the proposed method are provided. In Section V, a prototype platform is built to verify the feasibility of the proposed method. Finally, Section VI concludes this article.

The main contributions of this article are as follows.

1) For the first time, the P2P power flow tracing method based on a superimposed low-frequency carrier is proposed. The method successfully traces and monitors the power path from each seller to each buyer. The tracing results can be used to optimize the financial and energy scheduling model in the virtual layer.
2) A secondary verification mechanism is designed based on the superimposed carrier. The proposed mechanism allows the distributed ledger of P2P trading to be checked, which enhances system security.
3) The implementations of the proposed method are presented. The experimental results on a 2.5 kW experimental

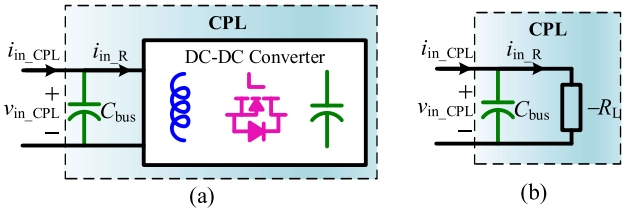

Fig. 2. (a) CPL's structure. (b) Equivalent circuit of a CPL at f_v.

platform validate the correctness and feasibility of the proposed method.

II. Origin of the Proposed Method

In a dc microgrid with a single DS and multiple PLs, the power sourcing from the DS to the PLs can be traced by measuring the dc current in each PL. However, when multiple DSs supply power concurrently, the power flows between DSs and PLs are mixed up in the dc bus and cannot be distinguished. In this case, in order to trace the power flows from a DS to PLs, it makes sense to stamp the power flow by superimposing a carrier with frequency f_v on dc voltage or current. Furthermore, according to circuitry basis, a DSs power distribution among PLs is determined by the dc bus port impedances of the PLs. If the PL's dc impedance is proportional to the impedance at carrier frequency f_v, then the dc power distribution can be derived based on the measured ac impedances.

Before proceeding, it is necessary to review the input impedance of a constant power load (CPL). As shown in Fig. 2(a), a CPL can be divided into two parts: input capacitor $C_{\rm bus}$ and the dc–dc converter paralleling with $C_{\rm bus}$. The input power of the CPL is

$$V_{\rm in\_CPL} I_{\rm in\_R} = P_{\rm dc\_in\_CPL} \tag{1}$$

where $V_{\rm in\_CPL}$ and $I_{\rm in\_R}$ are the converter's dc input voltage and current, respectively. Since $P_{\rm dc\_in\_CPL}$ is constant, it is deduced that

$$(V_{\rm in\_CPL} + \hat{v}_{\rm in\_CPL})(I_{\rm in\_R} + \hat{i}_{\rm in\_R}) = P_{\rm dc\_in\_CPL} \tag{2}$$

where $\hat{v}_{\rm in_CPL}$and $\hat{i}_{\rm in\_R}$ are the converter's input voltage and current disturbances at f_v, respectively. Derived in (1) and (2), it should be

$$\hat{v}_{\rm in\_CPL} I_{\rm in\_R} + V_{\rm in\_CPL} \hat{i}_{\rm in\_R} = 0. \tag{3}$$

Therefore, the converter's input impedance at f_v is

$$\frac{\hat{v}_{\rm in\_CPL}}{\hat{i}_{\rm in\_R}} = -\frac{V_{\rm in\_CPL}}{I_{\rm in\_R}} = -R_L \tag{4}$$

where $-R_{\rm L}$ is the dc closed-loop input impedance of the CPL.

Equation (4) indicates that the input impedances of the dc–dc converter are the same at f_v and dc. Thus, CPL can be simplified as an input capacitor $C_{\rm bus}$ paralleling with a negative resistor $-R_{\rm L}$ at f_v, as shown in Fig. 2(b). The resistor $-R_{\rm L}$ consumes active power, while $C_{\rm bus}$ absorbs reactive power. Due to this feature, the superimposed carrier can provide information about the impedance of CPLs. By analyzing the active power component of the superimposed carrier at bus port of each CPL, the P2P power flow can be determined.

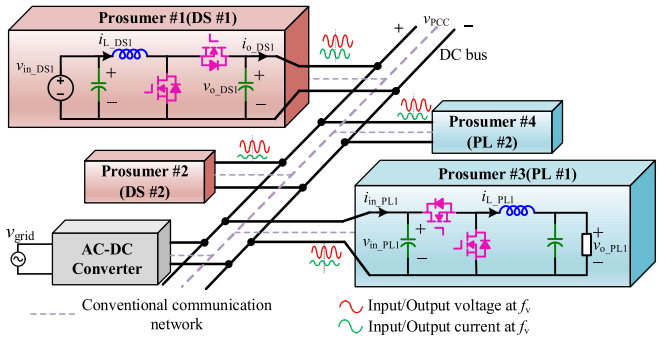

Fig. 3. Structure of the proposed system.

III. Principles of the Proposed Method

A. System Overview

The structure of the dc microgrid employing the proposed method is illustrated in Fig. 3. In the system, all sources and loads are connected to the dc bus via dedicated designed PEICs, which are bidirectional dc–dc converters in this article. When a prosumer acts as a DS (e.g., DS #1), it supplies power for other prosumers. When a prosumer acts as a PL (e.g., PL #1), it consumes power from dc bus.

It should be noted that the system is equipped with a conventional communication network, which enables the system to perform refined energy scheduling and P2P electricity trading in the virtual layer. By adapting the proposed method in the physical layer, the process of P2P trading can be verified. In order to provide a complete description of the method, the power flows of the system should be modeled.

Assume that the dc microgrid is in island mode, and the power flow between any two DS and PL remains constant throughout the power tracing period $T_{\rm p}$, implying that each PL operates as a CPL. In the model, the prosumers are divided into N DSs and M CPLs. The DSs are labeled as DS #i ($i = 1, 2, \ldots, N$), and the CPLs are labeled as CPL #j ($j = 1, 2, \ldots, M$) in turn. Thus, the system's power flows during $T_{\rm p}$ can be abstracted and written as

$$\boldsymbol{P}_{\rm sys} = \begin{pmatrix} P_{11} & \cdots & P_{1M} \\ \vdots & \ddots & \vdots \\ P_{N1} & \cdots & P_{NM} \end{pmatrix} \tag{5}$$

where P_{ij} denotes the dc transferred power from DS #i to CPL #j. By implementing S2LPS and S2SPV method, $\boldsymbol{P}_{\rm sys}$ is calculated and verified within $T_{\rm p}$. The construction process of $\boldsymbol{P}_{\rm sys}$ is depicted as follows.

As shown in Fig. 4, according to the number of DSs (N), $T_{\rm p}$ is divided into $3N$ slots, which are denoted as $T_{1a}, T_{1b}, T_{1c}, T_{2a}, T_{2b}, T_{2c}, \ldots, T_{Na}, T_{Nb}, T_{Nc}$ in order.

T_{ia} ($i = 1, 2, \ldots, N$) is the S2LPS slot for DS #i. In this period, a low-frequency sinusoidal carrier with specified active power is

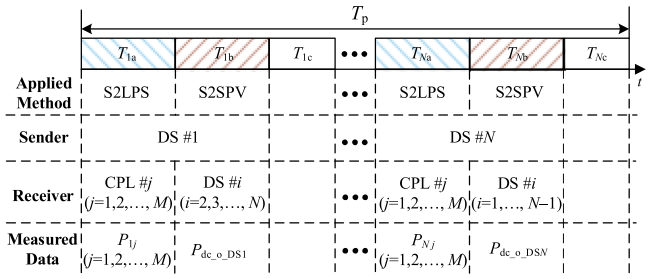

Fig. 4. Construction process of $\boldsymbol{P}_{\mathbf{sys}}$.

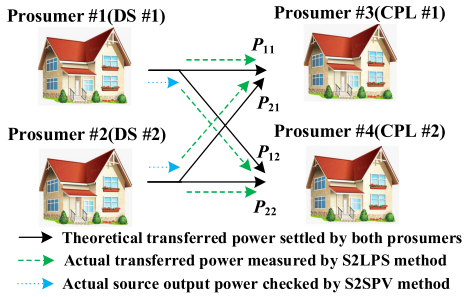

Fig. 5. Illustration example of the proposed system.

superimposed by DS #*i*. Based on the carrier, $P_{ij}(j = 1, 2, \ldots, M)$ is measured by CPL #*j*. The measured data are filled into $\boldsymbol{P}_{\mathbf{sys}}$ and compared with the transaction agreements settled in the virtual layer. Meanwhile, the data are broadcast to the rest prosumers via the conventional communication network.

T_{ib} ($i = 1, 2, \ldots, N$) is configured as S2SPV slot for DS #*i*. During T_{ib}, S2SPV method is employed, and the carrier with controlled active power is continually superimposed by DS #*i*. The voltage amplitude of the carrier is used by other DSs to estimate the output power of DS #*i* ($P_{\mathrm{dc\_o\_DS}i\_\mathrm{es}}$). Meanwhile, the actual dc output power of DS #*i* ($P_{\mathrm{dc\_o\_DS}i\_\mathrm{es}}$) is broadcast by DS #*i* to other DSs via the communication network. In every other DS, $P_{\mathrm{dc\_o\_DS}i}$ is compared with $P_{\mathrm{dc\_o\_DS}i\_\mathrm{es}}$ to ensure its authenticity.

T_{ic} ($i = 1, 2, \ldots, N$) is the idle slot arranged for the power transition process between T_{ib} and $T_{(i+1)a}$. During this period, the superimposed carrier is halted.

At the end of T_p, every P_{ij} in $\boldsymbol{P}_{\mathbf{sys}}$ is filled. Furthermore, $\boldsymbol{P}_{\mathbf{sys}}$ can be verified vertically by

$$P_{\mathrm{dc\_o\_DS}i\_\mathrm{es}} = \sum_{k=1}^{M} P_{ik}. \tag{6}$$

In order to enhance the data reliability, the input power of CPL #*i* in T_{ia} can be used to cross-check with data measured by S2LPS method, which is

$$P_{\mathrm{dc\_in\_CPL}j} = \sum_{k=1}^{N} P_{kj}. \tag{7}$$

With (7), $\boldsymbol{P}_{\mathbf{sys}}$ can be checked horizontally. After the aforementioned process, $\boldsymbol{P}_{\mathbf{sys}}$ is constructed and verified in each prosumer by S2LPS and S2SPV.

Fig. 5 depicts an example of a dc microgrid with two DSs and two CPLs applying the proposed method. It can be observed that the power flows between any two prosumers are monitored. The measured results $\boldsymbol{P}_{\mathbf{sys}}$ capture the real-time electricity transaction situation in the physical layer, which can be utilized to validate the distributed ledger in the virtual layer, ensuring the ledger's security and authenticity.

It should be noted that the frequency of the superimposed carrier f_v, must be chosen carefully to ensure the feasibility of the proposed method. In order to achieve high-precision control while minimizing hardware modification, f_v should be set lower than the control loop's cutoff frequency f_c. Since f_v is much lower

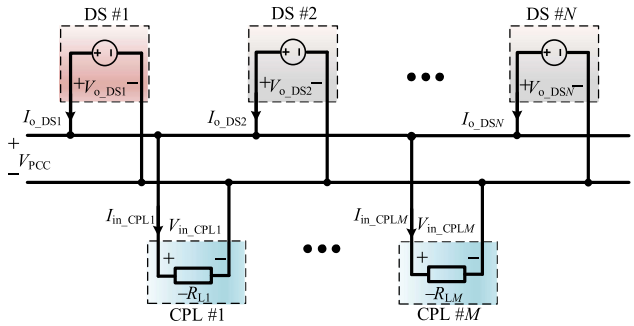

Fig. 6. DC equivalent circuit of the dc microgrid.

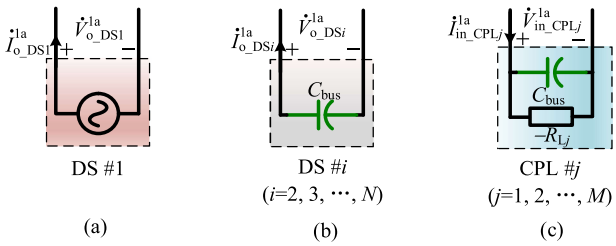

Fig. 7. Equivalent circuit at f_v of (a) DS #1, (b) DS #*i*, and (c) CPL #*j*.

than the switching frequency f_s, the impact of the switching ripple on the proposed method can be eliminated by signal filters, and it is ignored in this article.

The principles of S2LPS and S2SPV methods are put forward and analyzed in detail as follows.

B. Principle of S2LPS

Measuring the P2P power flow from a DS to a CPL is the foundation for constructing $\boldsymbol{P}_{\mathbf{sys}}$. This is accomplished through S2LPS method, which is based on a superimposed carrier with controlled active power. For instance, the dc transferred power from DS #1 to CPL #1, P_{11}, is measured by S2LPS as follows.

In residential dc microgrids, the line impedance is neglectable compared with the load impedance, so the dc equivalent circuit of the dc microgrid is shown in Fig. 6, where *N* DSs and *M* CPLs are all connected to the point of common coupling (PCC). CPL #*j* can be simplified as a negative resistor $-R_{\mathrm{L}j}$, which is the dc closed-loop input impedance of CPL #*j*.

As depicted in Fig. 7(a), during T_{1a}, a sinusoidal current $\dot{I}^{1a}_{o\_DS1}$ is superimposed by DS #1 into the dc bus, where superscript "1a" denotes the time slot T_{1a}, and subscript "DS1" denotes the converter. Suppose the angular frequency of $\dot{I}^{1a}_{o\_DS1}$ is

$$\omega_v = 2\pi f_v. \tag{8}$$

In order to build a relationship between dc power and ac active power at carrier's frequency, a linear correlation

$$P^{1a}_{ac\_o\_DS1} = -K_v P^{1a}_{dc\_o\_DS1} \tag{9}$$

is adopted in the S2LPS method, where $P^{1a}_{ac\_o\_DS1}$ and $P^{1a}_{dc\_o\_DS1}$ denotes DS #1's ac active power at f_v and dc output power in T_{1a}, respectively, and K_v is the predefined S2LPS gain. Equation (9) is the key to S2LPS method.

At f_v, the output active power of DS #1 is

$$P^{1a}_{ac\_o\_DS1} = |\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}| \times |\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}| \cos\theta_{DS1}. \tag{10}$$

Thus, the amplitude of $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}$ should be controlled by DS #1 as

$$|\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}| = \frac{-K_v P^{1a}_{dc\_o\_DS1}}{|\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}| \cos\theta_{DS1}} \tag{11}$$

where $\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}$ is the output voltage of DS #1 at f_v, and θ_{DS1} is the angle formed by $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}$ and $\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}$.

Since the line impedance is ignored, it can be found that

$$\begin{cases} \dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DS}\boldsymbol{i}} = \dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{PCC}}, i = 1, 2, 3, \ldots, N \\ \dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{in\_CPL}\boldsymbol{j}} = \dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{PCC}}, j = 1, 2, 3, \ldots, M \end{cases} \tag{12}$$

where $\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DS}\boldsymbol{i}}$ and $\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{in\_CPL}\boldsymbol{j}}$ are DS #i's output voltage and CPL #j's input voltage at f_v in T_{1a}, respectively. Thus, at f_v, the output active power of DS #1 and input active power of CPL #j are

$$\begin{cases} P^{1a}_{ac\_o\_DS1} = |\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{PCC}}| \times |\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}| \cos\theta_{DS1} \\ P^{1a}_{ac\_in\_CPL}{}_j = |\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{PCC}}| \times |\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{in\_CPL}\boldsymbol{j}}| \cos\theta_{CPL}{}_j \end{cases} \tag{13}$$

respectively, where $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{in\_CPL}\boldsymbol{j}}$ is CPL #j's input current at f_v, and $\theta_{CPL}{}_j$ denotes the angle formed by $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{in\_CPL}\boldsymbol{j}}$ and $\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{PCC}}$.

At f_v, assume that no active power is generated by other DSs, so the equivalent circuit of DS #i(i = 2,3,…,N) can be simplified to only one capacitor C_{bus}, as shown in Fig. 7(b). Besides, CPL #j can be simplified as C_{bus} paralleling with $-R_{Lj}$, as illustrated in Fig. 7(c). Based on Fig. 8(a) and (b), it can be deduced that

$$\begin{cases} |\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}| \cos\theta_{DS1} = \sum_{j=1}^{M} |\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{in\_CPL}\boldsymbol{j}}| \cos\theta_{CPL}{}_j \\ |\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{in\_CPL}\boldsymbol{j}}| \cos\theta_{CPL}{}_j = -\frac{|\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{in\_CPL}\boldsymbol{j}}|}{R_{Lj}}. \end{cases} \tag{14}$$

According to (12)–(14), it can be deduced that

$$\frac{P^{1a}_{ac\_in\_CPL1}}{P^{1a}_{ac\_o\_DS1}} = \frac{|\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{PCC}}|^2/R_{L1}}{\sum_{j=1}^{M} |\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{PCC}}|^2/R_{Lj}} = \frac{P_{11}}{\sum_{j=1}^{M} P_{1j}} = \frac{P_{11}}{P^{1a}_{dc\_o\_DS1}}. \tag{15}$$

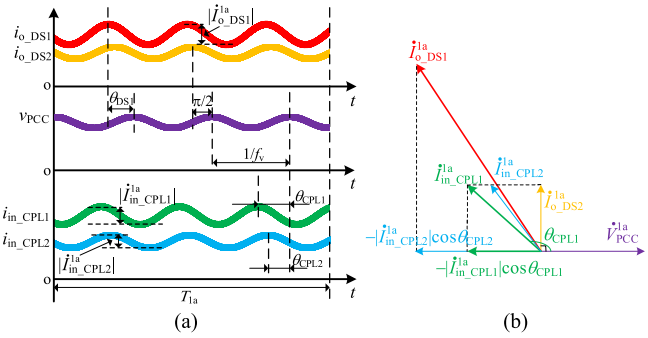

Fig. 8. (a) System waveforms applying S2LPS. (b) Corresponding vector diagram.

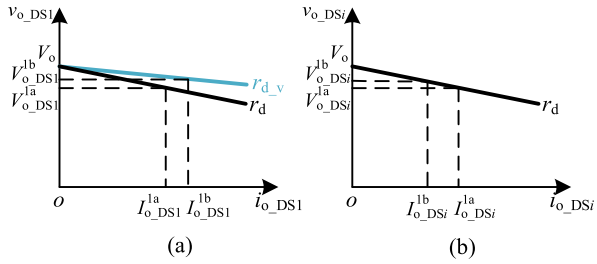

Fig. 9. Droop characteristics of (a) DS #1 and (b) DS #i(i=2,3,…,N).

Equation (15) indicates that the carrier's active power and a DSs dc output power distribution among CPLs are the same. By substituting (9) into (15), it can be derived as

$$P^{1a}_{ac\_in\_CPL1} = -K_v P_{11}. \tag{16}$$

Therefore, P_{11} can be determined by measuring the active power of the carrier at bus port of CPL #1.

The preceding derivations demonstrate that the P2P power flow from a specific DS to a CPL can be measured by S2LPS. However, it should be noted that the derivations are founded on three premises. First, the control loop of DS #1 should be modified so that $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}$ can be generated precisely as (11). Second, no active power at f_v should be generated by other DSs. Third, each PL should function as a CPL at f_v. The specifics of the implementations to ensure the three premises will be addressed in Section IV.

C. Principle of S2SPV

With S2LPS, the construction of $\boldsymbol{P}_{\mathbf{sys}}$ can be completed and its horizontal dimension data can be checked according to (7). However, in a P2P trading system, trust issues might occur between a DS and a PL due to the disagreements about the actual transferred power. To build a more convincible $\boldsymbol{P}_{\mathbf{sys}}$, the data authenticity of $\boldsymbol{P}_{\mathbf{sys}}$ should be checked in the vertical dimension as well, and it can be accomplished by S2SPV method in this article.

With S2SPV method, a DSs actual output power is checked by other DSs using the superimposed carrier. For example, the verification process of DS #1's actual output power $P_{dc\_o\_DS1}$, which is carried out in T_{1a} and T_{1b}, is depicted as follows.

As shown in Fig. 9, suppose the droop characteristic of DS #1 in T_{1a} is

$$V_{o\_DS1}^{1a}=V_o - r_d I_{o\_DS1}^{1a} \tag{17}$$

where V_o is the reference output voltage at zero load, r_d is DS #1's droop coefficient in T_{1a}, $V_{o\_DS1}^{1a}$ and $I_{o\_DS1}^{1a}$ are DS #1's dc output voltage and current in steady state of T_{1a}, respectively.

At the end of T_{1a}, the droop coefficient of DS #1 is changed to a new value r_{d_v} , while the droop coefficients of DS #*i* (i = 2,3,…,*N*) remain the same. InY DS #*i* (i = 1,2,3,…,*N*), the dc output power variation $\Delta P_{dc\_o\_DSi}$ caused by the change of droop coefficient is

$$\Delta P_{dc\_o\_DSi}=P_{dc\_o\_DSi}^{1b} - P_{dc\_o\_DSi}^{1a}. \tag{18}$$

$\Delta P_{dc\_o\_DSi}$ is broadcast to the rest prosumers via conventional communication networks. Since the total consumed power of CPLs are constant, the actual power variation of DS #1 can be calculated by every other DS #*i*($i = 2,3,\ldots,N$) as

$$\Delta P_{dc\_o\_DS1}= -\sum_{i=2}^{N}\Delta P_{dc\_o\_DSi}. \tag{19}$$

Thus, it can be written as

$$\frac{P_{dc\_o\_DS1}^{1b}}{P_{dc\_o\_DS1}^{1a}}=1-\frac{\sum_{i=2}^{N}\Delta P_{dc\_o\_DSi}}{P_{dc\_o\_DS1}^{1a}}. \tag{20}$$

During T_{1b}, the superimposed carrier is still generated and controlled by DS #1 in the same way as in T_{1a}, which is

$$|\dot{\boldsymbol{I}}_{\mathbf{o\_DS1}}^{\mathbf{1b}}|=\frac{-K_v P_{dc\_o\_DS1}^{1b}}{|\dot{\boldsymbol{V}}_{\mathbf{o\_DS1}}^{\mathbf{1b}}|\cos\theta_{DS1}}. \tag{21}$$

Besides, the system equivalent circuit at f_v in T_{1b} is the same as that in T_{1a}. Thus, it can be derived that

$$\frac{|\dot{\boldsymbol{V}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}|}{|\dot{\boldsymbol{I}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}|}=\frac{|\dot{\boldsymbol{V}}_{\mathbf{o\_DS1}}^{\mathbf{1b}}|}{|\dot{\boldsymbol{I}}_{\mathbf{o\_DS1}}^{\mathbf{1b}}|}=|Z_{load}| \tag{22}$$

$$|Z_{load}|=\frac{1}{-(\sum_{j=1}^{M}1/R_{Lj})+\mathrm{j}(N+M-1)\omega_v C_{bus}} \tag{23}$$

where Z_{load} is the load impedance of DS #1. By substituting (22) into (11), it can be derived as

$$\frac{P_{dc\_o\_DS1}^{1b}}{P_{dc\_o\_DS1}^{1a}}=\left(\frac{|\dot{\boldsymbol{V}}_{\mathbf{o\_DS1}}^{\mathbf{1b}}|}{|\dot{\boldsymbol{V}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}|}\right)^2. \tag{24}$$

Since the line impedance is ignored, it can be found that

$$\dot{\boldsymbol{V}}_{\mathbf{o\_DS}i}^{\mathbf{1b}}=\dot{\boldsymbol{V}}_{\mathbf{PCC}}^{\mathbf{1b}}, i=1,2,\ldots,N. \tag{25}$$

According to (19), (20), (24), and (25), the output power of DS #1 can be estimated by every other DS #*i*($\mathrm{i} = 2,3,\ldots,N$) as

$$P_{dc\_o\_DS1\_es}^{1a}=\frac{\sum_{i=2}^{N}\Delta P_{dc\_o\_DSi}}{1-\left(|\dot{\boldsymbol{V}}_{\mathbf{o\_DS}i}^{\mathbf{1b}}|/|\dot{\boldsymbol{V}}_{\mathbf{o\_DS}i}^{\mathbf{1a}}|\right)^2}. \tag{26}$$

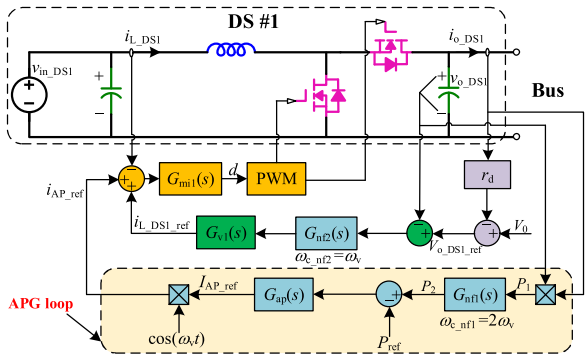

Fig. 10. Modified control diagram of DS #1.

$P_{dc\_o\_DS1\_es}^{1a}$ is compared with $P_{dc\_o\_DS1}^{1a}$, and the verification process for $P_{dc\_o\_DS1}^{1a}$ is completed. The results are also distributed to other prosumers via the conventional communication network.

The above-mentioned derivations demonstrate the verification process for DS #1's output power. Through S2SPV, the data authenticity from each DS is guaranteed by other prosumers in the system. Besides, these data can be cross-checked with data measured by S2LPS, solving trust issues between DSs and PLs.

IV. Implementation of the Proposed Method

This section aims to clarify the modification schemes for implementation of the proposed method. All changes are made in power control loops, making it simple to embed in the PEICs microcontrollers.

According to the analysis in Section III, control loop modifications should be implemented during T_{ia} and T_{ib}. For instance, the modifications in T_{1a} are depicted as follows.

A. Modification for DS #1

Conventionally, the control scheme of a bidirectional DS in dc microgrids consists of three loops, which are the droop control loop with droop coefficient r_d, the output voltage loop with a proportional-integral type compensator $G_{v1}(s)$, and the inductor current loop with a proportional–integral type compensator $G_{i1}(s)$.

As mentioned in Section III-B, $\dot{\boldsymbol{I}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}$ contains the output power information of DS #1. To precisely generate $\dot{\boldsymbol{I}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}$ as (11), an active power generation (APG) loop is added to the control scheme, as shown in Fig. 10. At f_v, DS #1's output current and voltage can be expressed as

$$\begin{cases}\dot{\boldsymbol{I}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}=|\dot{\boldsymbol{I}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}|\cos(2\pi f_v t)\\ \dot{\boldsymbol{V}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}=|\dot{\boldsymbol{V}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}|\cos(2\pi f_v t+\theta_{DS1})\end{cases} \tag{27}$$

respectively. Thus, P_1 can be derived as

$$P_1=\frac{1}{2}|\dot{\boldsymbol{V}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}|\times|\dot{\boldsymbol{I}}_{\mathbf{o\_DS1}}^{\mathbf{1a}}|[\cos\theta_{DS1}+\cos(4\pi f_v t+\theta_{DS1})]. \tag{28}$$

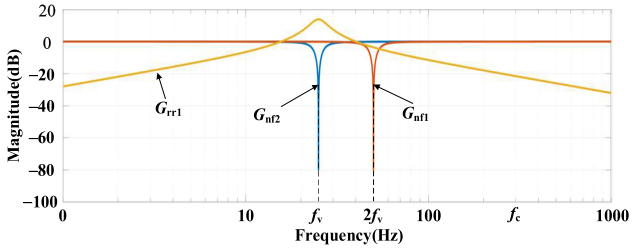

Fig. 11. Gain-frequency diagram of G_{nf1}, G_{nf2}, and G_{rr1}.

To extract the dc component, P_1 is passed through a notch filter

$$G_{nf1}(s)=\frac{(s/\omega_{c\_nf1})^2+2\varepsilon_{1\_nf1}\cdot s/\omega_{c\_nf1}+1}{(s/\omega_{c\_nf1})^2+2\varepsilon_{2\_nf1}\cdot s/\omega_{c\_nf1}+1} \tag{29}$$

where $\omega_{c\_nf2}=2\omega_v$ is the center frequency of the notch, and ε_{1_nf2} and ε_{2_nf2} are two coefficients related to the notch depth and the bandwidth. The gain-frequency diagram of $G_{nf1}(s)$ is illustrated in Fig. 11. So, P_2 can be expressed as

$$P_2=\frac{1}{2}|\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}|\times|\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}|\cos\theta_{DS1}=\frac{1}{2}P^{1a}_{ac\_o\_DS1}. \tag{30}$$

P_{ref} is the active power reference, which is

$$P_{ref}=-\frac{1}{2}K_vP^{1a}_{dc\_o\_DS1}. \tag{31}$$

To obtain the amplitude reference I_{AP_ref}, the deviation between P_2 and P_{ref} is compensated by a PI controller $G_{ap}(s)$ with low bandwidth. With I_{AP_ref}, the output of APG loop

$$i_{AP\_ref}(t)=I_{AP\_ref}\cos(\omega_v t) \tag{32}$$

is superimposed into the inductor current loop.

In steady state, i_{AP_ref} is a sinusoidal signal, so a proportional–integral–resonant type controller

$$G_{mi1}(s)=K_{p\_mi1}+\frac{K_{i\_mi1}}{s}+\frac{2K_{r\_mi1}\omega_{c\_mi1}s}{s^2+2\omega_{c\_mi1}s+\omega_v^2} \tag{33}$$

is adopted in the inductor current loop to achieve errorless control, where K_{p_mi1}, K_{i_mi1}, and K_{r_mi1} are the proportional, integral, and resonant coefficients of $G_{mi1}(s)$, respectively, and ω_{c_mi1} determines the bandwidth of $G_{mi1}(s)$.

The APG loop introduces components of f_v into DS #1's output voltage and current. To keep the dc droop characteristic unaffected, a notch filter

$$G_{nf2}(s)=\frac{(s/\omega_{c\_nf2})^2+2\varepsilon_{1\_nf2}\cdot s/\omega_{c\_nf2}+1}{(s/\omega_{c\_nf2})^2+2\varepsilon_{2\_nf2}\cdot s/\omega_{c\_nf2}+1} \tag{34}$$

is applied in the voltage compensation loop, where $\omega_{c\_nf2}=\omega_v$ is the center frequency, and ε_{1_nf2} and ε_{2_nf2} are two coefficients. The gain-frequency diagram of $G_{nf2}(s)$ is shown in Fig. 11.

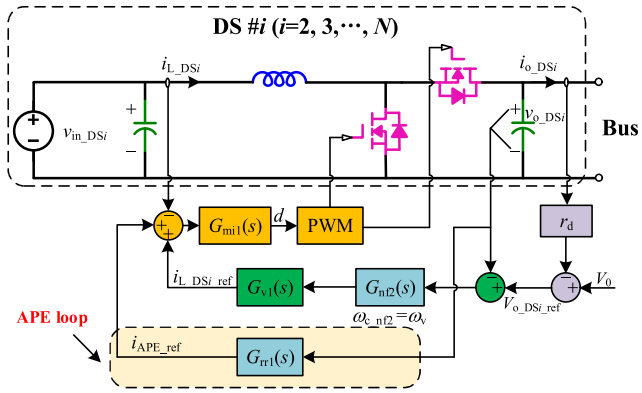

Fig. 12. Modified control diagram of DS #*i* (*i*=2,3, …,*N*).

B. Modification for Other DSs

The DS #*i*'s (i = 2, 3, …, N) inductor current and output voltage are

$$\begin{cases} i^{1a}_{L\_DSi}(t)=I^{1a}_{L\_DSi}+|\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{L\_DSi}}|\cos(2\pi f_v t+\varphi_{DSi}) \\ v^{1a}_{o\_DSi}(t)=V^{1a}_{o\_DSi}+|\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DSi}}|\cos(2\pi f_v t+\theta_{DS1}) \end{cases} \tag{35}$$

in steady state, respectively, where $\boldsymbol{I}^{\mathbf{1a}}_{\mathbf{L\_DSi}}$ and $\boldsymbol{V}^{\mathbf{1a}}_{\mathbf{o\_DSi}}$ are the DC inductor current and output voltage of DS #*i*, respectively, and φ_{DSi} denotes the angle formed by $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{L\_DSi}}$ and $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}$ in T_{1a}. The power loss on DS #*i* is insignificant compared with the output power, so DS #*i*'s output and input active power are equal, which as (37)

$$v^{1a}_{o\_DSi}(t)i^{1a}_{o\_DSi}(t)\cos\theta_{DSi}=v^{1a}_{in\_DSi}(t)i^{1a}_{L\_DSi}(t) \tag{36}$$

$$\frac{i^{1a}_{o\_DSi}(t)\cos\theta_{DSi}}{v^{1a}_{in\_DSi}(t)}=\frac{i^{1a}_{L\_DSi}(t)}{v^{1a}_{o\_DSi}(t)} \tag{37}$$

where $v^{1a}_{in\_DSi}(t)$ is the DS #*i*'s input voltage in T_{1a}.

When DS #1 is sending $\dot{I}^{1a}_{o\_DS1}$, the active power generated by every other DS #*i* should be zero, implying that $i_{o\_DSi}(t)\cos\theta_{DSi}$ should be constant. Since $v_{in\_DSi}(t)$ is constant, it should be satisfied that

$$\begin{cases} \frac{I^{1a}_{L\_DSi}}{V^{1a}_{o\_DSi}}=\frac{|\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{L\_DSi}}|}{|\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DSi}}|} \\ \varphi_{DSi}=\theta_{DS1}. \end{cases} \tag{38}$$

According to (38), an active power elimination (APE) loop is added paralleling with the original output voltage loop, as illustrated in Fig. 12. A resonator

$$G_{rr1}(s)=\frac{\lambda_1 s/\omega_{c\_rr1}}{(s/\omega_{c\_rr1})^2+\lambda_2 s/\omega_{c\_rr1}+1} \tag{39}$$

is employed to precisely control $\dot{\boldsymbol{I}}_{\mathbf{L\_DSi}}$, where $\omega_{c\_rr1}=\omega_v$ is the center frequency, and λ_1 and λ_2 are two coefficients that satisfy

$$G_{rr1}(\omega_v)=\frac{\lambda_1}{\lambda_2}=\frac{I^{1a}_{L\_DSi}|\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{o\_DSi}}|}{V^{1a}_{o\_DSi}}. \tag{40}$$

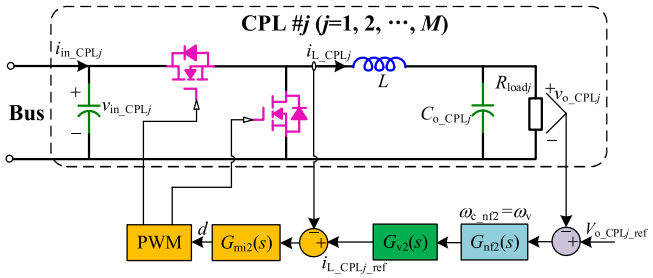

Fig. 13. Modified control diagram of CPL #*j* (*j*=1,2,…,*M*).

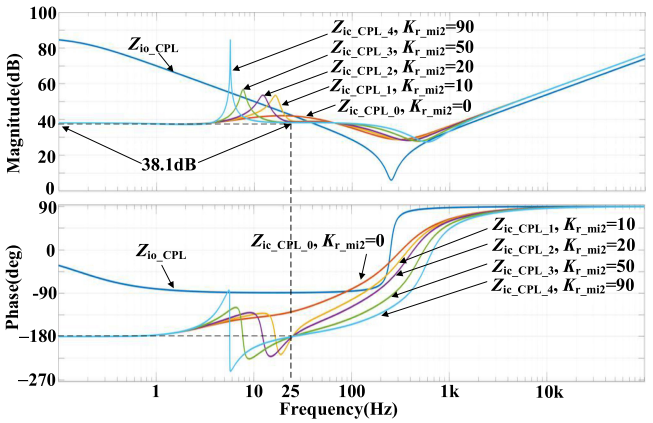

Fig. 14. Bode diagram of a CPL's input impedances with different $K_{\mathrm{r\_mi2}}$.

Besides, the phase delay of $G_{\mathrm{rr1}}(s)$ at f_{v} is zero, as illustrated in Fig. 11. Thus, (38) can be satisfied with the introduced $G_{\mathrm{rr1}}(s)$.

The variables $I^{1a}_{\mathrm{L\_DS}i}$, $V^{1a}_{\mathrm{o\_DS}i}$, and $|\dot{V}^{1a}_{\mathrm{o\_DS}i}|$ can be sampled by the DS #*i*'s microcontroller. Based on (40), λ_1/λ_2 can be online calculated and regulated by the microcontroller. $G_{\mathrm{rr1}}(s)$ eliminates the dc component of $v^{1a}_{\mathrm{o\_DS}i}(t)$ and amplifies the component at f_{v} with a gain of λ_1/λ_2. $i_{\mathrm{APE\_ref}}$ and $i_{\mathrm{L\_DS}i\_\mathrm{ref}}$ are added together to form the reference of $i_{\mathrm{L\_DS}i}$, as shown in Fig. 12. To achieve error-free tracking of the reference, the current loop controller is modified to $G_{\mathrm{mi1}}(s)$ with a resonant link, and $G_{\mathrm{nf2}}(s)$ is used to maintain the dc control characteristic.

C. Modification for CPLs

Conventionally, the control scheme of a bidirectional PL in dc microgrids consists of two loops: the output voltage loop and the inductor current loop, as depicted in Fig. 13.

At f_{v}, the PL should function as a CPL, which means the closed control loop gain should be sufficient. Thus, the inductor current compensator is modified to

$$G_{\mathrm{mi2}}(s)=K_{\mathrm{p\_mi2}}+\frac{K_{\mathrm{i\_mi2}}}{s}+\frac{2K_{\mathrm{r\_mi2}}\omega_{\mathrm{c\_mi2}}s}{s^2+2\omega_{\mathrm{c\_mi2}}s+\omega_{\mathrm{v}}^2} \quad (41)$$

where $K_{\mathrm{p\_mi2}}$, $K_{\mathrm{i\_mi2,}}$ and $K_{\mathrm{r\_mi2}}$ are the proportional, integral, and resonant coefficients of $G_{\mathrm{mi2}}(s)$, respectively, and $\omega_{\mathrm{c\_mi2}}$ determines the bandwidth of $\mathrm{G_{mi2}(s)}$. $G_{\mathrm{nf2}}(s)$ is also used in the voltage compensation loop to maintain the droop characteristic.

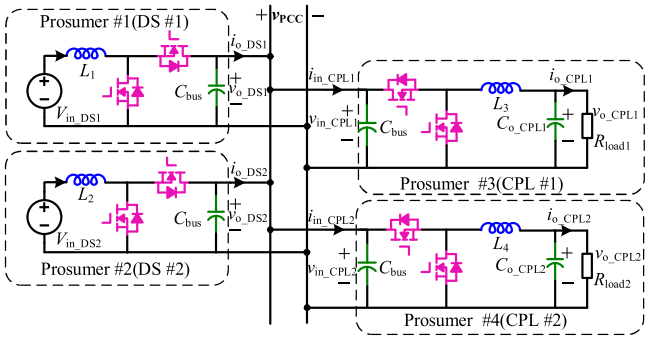

Fig. 15. Structure of the experimental platform.

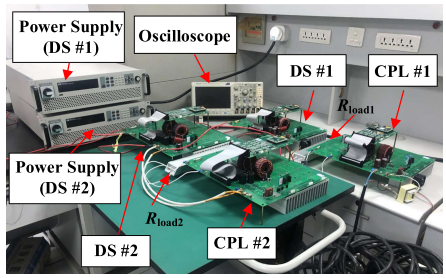

Fig. 16. Photograph of the experimental platform.

TABLE I
PARAMETERS OF DC MICROGRID SYSTEM

Description	Symbol	Value
Input voltage of DS #1, DS #2	$V_{\mathrm{in\ DS1}}$, $V_{\mathrm{in\ DS2}}$	120-200V
Bus voltage reference without load	V_{o}	375V
Output voltage of CPL #1, CPL #2	$V_{\mathrm{o\ CPL1}}$, $V_{\mathrm{o\ CPL2}}$	150-200V
Switching frequency	f_{s}	50kHz
Bus capacitance of PEIC #1~ #4	C_{bus}	100μF
Output capacitance of CPL #1, CPL #2	$C_{\mathrm{o\_CPL1}}$, $C_{\mathrm{o\_CPL2}}$	300μF
Inductance	L_1, L_2, L_3, L_4	2mH

By implementing the CPL modification scheme, Fig. 14 shows the bode diagram of a CPLs input impedances with V_{PCC} = 400V, $V_{\mathrm{o\_CPL}}$ = 200V, R_{load} = 20 Ω, L = 2 mH, $C_{\mathrm{o\_CPL}}$ = 200 μF, and $\omega_{\mathrm{v}} = 2\pi\times25$. The current and voltage control loop bandwidths are all set above 300 Hz. In Fig. 14, $Z_{\mathrm{io\_CPL}}$ is the open-loop input impedance and $Z_{\mathrm{ic\_CPL0}}$-$Z_{\mathrm{ic\_CPL4}}$ are the closed-loop input impedances with different $K_{\mathrm{r\_mi2}}$. It can be observed that with a sufficient $K_{\mathrm{r\_mi2}}$ ($K_{\mathrm{r\_mi2}}$ = 90), the input impedance appears to be a negative resistor at 25 Hz, and the magnitude gain at 25 Hz is 38.1 dB (80 Ω), which is the same as the dc input impedance. Therefore, the correctness of the CPL modification scheme is proved.

V. EXPERIMENTAL RESULTS

The correctness of the proposed power tracing method has been experimentally validated on a 2.5 kW dc microgrid platform. The structure and photo of the platform are shown in Fig. 15 and Fig. 16, respectively, and the platform parameters are provided in Table I. In the experimental system, prosumers #1 and #2 act as DSs, while prosumers #3 and #4 act as CPLs. TMS320F28377 from Texas Instruments is used in

TABLE II
CONTROL PARAMETERS

Description	Symbol	Value
Superimposed frequency	f_v	25Hz
S2LPS gain	K_v	0.0002
Length of T_p	T_p	40s
Length of T_{ia}, T_{ib}, T_{ic}	T_{ia}, T_{ib}, T_{ic}	4s, 8s, 8s
Droop coefficients	r_d, $r_{d\ v}$	1V/A, 0.95V/A
Coefficients of $G_{nf1}(s)$	ω_{c_nf1}, ε_{1_nf1}, ε_{2_nf1}	100π,5×10^{-1}, 5×10^{-4}
Coefficients of $G_{nf2}(s)$	ω_{c_nf2}, ε_{1_nf2}, ε_{2_nf2}	50π,5×10^{-1}, 5×10^{-4}
Coefficients of $G_{ap}(s)$	K_{p_ap}, K_{i_ap}	0.1, 100
Coefficients of $G_{mi1}(s)$	$K_{p\ mi1}$, $K_{i\ mi1}$, $K_{r\ mi1}$	0.3, 40, 8
Coefficients of $G_{mi2}(s)$	$K_{p\ mi2}$, $K_{i\ mi2}$, $K_{r\ mi2}$	0.3, 40, 90
Coefficients of $G_{v1}(s)$, $G_{v2}(s)$	$K_{p\ v1}$, $K_{i\ v1}$, $K_{p\ v2}$, $K_{i\ v2}$	0.6, 10, 0.5, 10

each converter to implement the proposed method, and MOSFET C3M0065090D from CREE is selected as the switches for bidirectional converters. The experimental control parameters are listed in Table II.

Based on the platform, two experiments are carried out. In Experiment I, the fundamentals of S2LPS are checked, while in Experiment II, an application example is provided, in which S2LPS and S2SPV are both applied.

A. Experiment I: S2LPS Test

This experiment aims to check the correctness of S2LPS principle. In this test, in order to determine the actual P_{11} and P_{12}, DS #2 is disconnected from the dc bus, and DS #1 supplies power for both CPLs. When DS #1 is sending out $I^{1a}_{o\_DS1}$, the operational waveforms of DS #1, CPL #1, and CPL #2 are demonstrated in Fig. 17(a)–(c), respectively.

In Fig. 17(a), $\tilde{v}_{o\_DS1}$ and $\tilde{i}_{o\_DS1}$ are the ac components of v_{o_DS1} and i_{o_DS1}, respectively. In order to offer a more explicit view, they are passed through band pass filters (BPFs) with a center frequency of 25 Hz to obtain $\tilde{v}_{o\_DS1\_fil}$ and $\tilde{i}_{o\_DS1\_fil}$, respectively. The dc output voltage V_{o_DS1} is 373.1 V and the dc output current I_{o_DS1} is 4.16 A. Thus, the actual dc output power $P_{dc\_o\_DS1}$ is 1552 W, and the theoretical active power at 25 Hz should be -0.3104 W based on (9). Calculated by $\tilde{v}_{o\_DS1\_fil}$ and $\tilde{i}_{o\_DS1\_fil}$, the output active power of DS #1 at 25 Hz is -0.3088 W. The error between theoretical and experimental results is less than 1%, which verifies the effectiveness of the APG loop.

In Fig. 17(b), $\tilde{v}_{in\_CPL1}$ and $\tilde{i}_{in\_CPL1}$ are the ac components of v_{in_CPL1} and i_{in_CPL1}, respectively. They are passed through the same BPFs to obtain $\tilde{v}_{in\_CPL1\_fil}$ and $\tilde{i}_{in\_CPL1\_fil}$, respectively. Due to the control loop modifications for CPL, no component of 25 Hz exists in v_{o_CPL1} and i_{o_CPL1}.

For CPL #1, the actual dc input power $P^{1a}_{dc\_in\_CPL1}$ is calculated as 1026 W. Calculated by $\tilde{v}_{in\_CPL1\_fil}$ and $\tilde{i}_{in\_CPL1\_fil}$, the input active power $P^{1a}_{ac\_in\_CPL1}$ is -0.2028 W at 25 Hz. According to (16), P_{11}, which is the P2P transferred power from DS #1 to CPL #1, is estimated as 1014 W by S2LPS. The error between estimated and actual results is 1.2%.

For CPL #2, similarly, the actual dc input power $P^{1a}_{dc\_in\_CPL2}$ is calculated as 522.8 W, while the estimated P_{12} is 515.0 W according to a measured active power $P^{1a}_{ac\_in\_CPL2}$ of -0.1030 W.

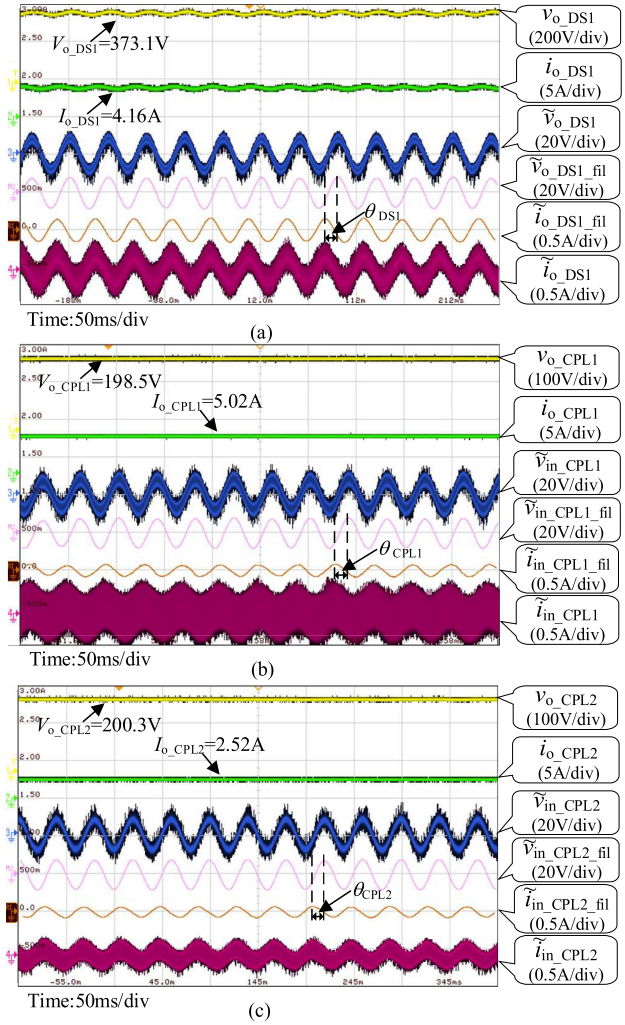

Fig. 17. Operational waveforms of (a) DS #1, (b) CPL #1, and (c) CPL #2.

TABLE III
CALCULATION RESULTS OF EXPERIMENT I

Variables	Estimated value	Actual value	Error
P_{11}	1014	1026	1.2%
P_{12}	515.0	522.8	1.5%

The estimated error is 1.5%, which verifies the correctness of S2LPS.

The calculation results of Experiment I is summarized in Table III. The estimated errors come from several factors. First, parasitic parameters are not considered in the derivation of S2LPS method. Second, the noninfinite control loop gain results in nonideal control characteristic. Third, the rounding and quantization errors in the computation process reduce the accuracy of the experimental results.

B. Experiment II: System Test

In this experiment, the system employing the proposed power flow tracing method is tested, and the correctness of S2SPV is checked. Based on S2LPS and S2SPV, the power flow matrix $\boldsymbol{P}_{\mathbf{sys}}$ is established.

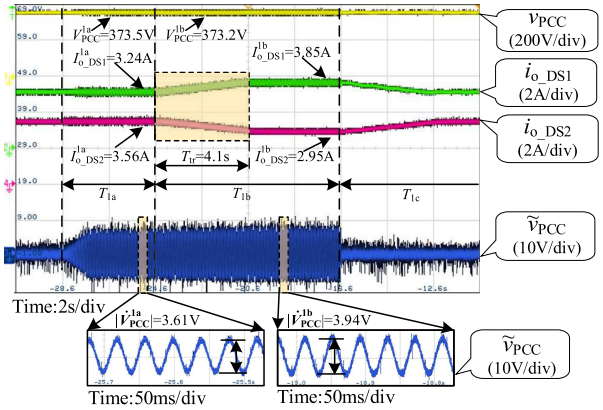

Fig. 18. System operational waveforms in T_{1a}, T_{1b}, and T_{1c}.

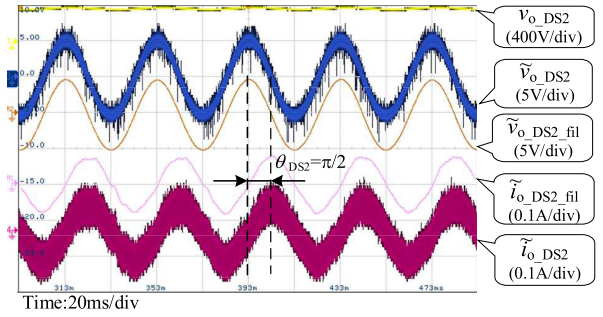

Fig. 19. Enlarged waveforms of DS #2's output voltage and current in T_{1a}.

In this test, DS #1 and DS #2 supply power for the dc bus. CPL #1 and CPL #2 consume around 1 kW and 1.5 kW of constant power, respectively. The power flow tracing and verification processes for DS #1 are illustrated as follows.

As shown in Fig. 18, at the beginning of T_{1a}, S2LPS method is applied and the APG loop in DS #1 is activated to generate $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS1}}$. To eliminate DS #2s influence to the S2LPS process, the APE loop in DS #2 begins to operate. It can be observed from Fig. 19 that $\boldsymbol{V}^{\mathbf{1a}}_{\mathbf{o\_DS2}}$ lags $\dot{\boldsymbol{I}}^{\mathbf{1a}}_{\mathbf{o\_DS2}}$ about $\pi/2$, confirming the correctness of the modification method in Section IV-B. Therefore, in the equivalent circuit at 25 Hz, DS #2 can be simplified as $C_{\rm bus}$.

In steady state of T_{1a}, the CPLs determine the transferred power from DS #1 by calculating the input active power at 25 Hz. As shown in Fig. 20(a) and (b), the input active power of CPL #1 and #2 are measured as –0.0976 W and –0.1445 W, respectively. According to (16), P_{11} and P_{12} can be calculated by S2LPS as 488.2 W and 722.3 W, respectively.

At the beginning of T_{1b}, DS #1 changes its droop coefficient from $r_{\rm d}$ = 1V/A to $r_{\rm d\_v}$ = 0.95V/A. Thus, DS #1's output current gradually increases and DS #2's output current gradually decreases, as illustrated in Fig. 18. The length of the transition process is $T_{\rm tr}$ = 4.1 s. According to the measured $V_{\rm PCC}$, $I_{\rm o\_DS1}$ and $I_{\rm o\_DS2}$, the dc output power variation $\Delta P_{\rm dc\_o\_DS2}$ is −227.8 W.

At the end of T_{1b}, DS #1 changes its droop coefficient to original value $r_{\rm d}$, and the APG and APE loops are deactivated.

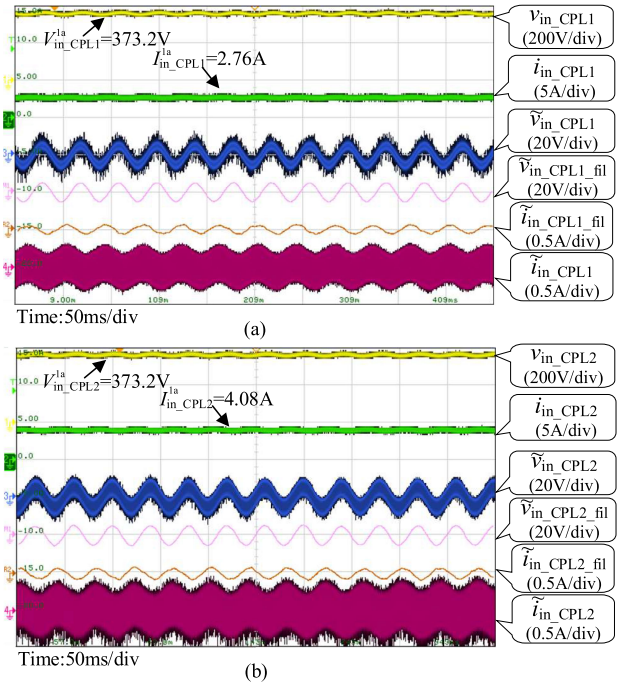

Fig. 20. Operational waveforms of (a) CPL #1, and (b) CPL #2 in T_{1a}.

TABLE IV
VERIFICATION RESULTS OF EXPERIMENT II

Variables	Estimated value	Actual value	Error
$P^{1a}_{\rm dc\_o\_DS1}$	1192	1210	1.5%
$P^{1a}_{\rm dc\_o\_DS2}$	1298	1330	2.4%
$P^{1a}_{\rm dc\_in\_CPL1}$	1021	1030	0.9%
$P^{1a}_{\rm dc\_in\_CPL2}$	1506	1523	1.1%

The length of T_{1c} is set to 8 s to guarantee the completion of power transition process caused by droop coefficient variation.

Zoom in on $\tilde{v}_{PCC}$, it can be measured that $|\dot{\boldsymbol{V}}^{\mathbf{1a}}_{\mathbf{PCC}}|$ = 3.61 V, and $|\dot{\boldsymbol{V}}^{\mathbf{1b}}_{\mathbf{PCC}}|$ = 3.94V. According to (26), it can be estimated that $P^{\rm 1a}_{\rm dc\_o\_DS1\_es}$= 1192W, while the actual output power of DS #1 in T_{1a} is $P^{\rm 1a}_{\rm dc\_o\_DS1}$= 1210W. The estimated error is 1.5%, which verifies the correctness of S2SPV principle.

So far, P_{11} and P_{12} have been measured and filled into $\boldsymbol{P}_{\mathbf{sys}}$. Similarly, P_{21} and P_{22} are measured in T_{2a}, and the power flow matrix $\boldsymbol{P}_{\mathbf{sys}}$ is filled in as

$$\mathbf{P}_{\rm sys}=\begin{pmatrix}488.2 & 722.3\\ 532.5 & 783.9\end{pmatrix}.$$

In T_{2b}, the correctness of $P^{\rm 1a}_{\rm dc\_o\_DS2}$ can be checked by S2SPV. Besides, $\boldsymbol{P}_{\mathbf{sys}}$ can be double-checked according to (6) and (7). The verification results of Experiment II are summarized in Table IV. The estimated errors are all less than 2.5%.

In this experiment, the construction of $\boldsymbol{P}_{\mathbf{sys}}$ takes 40 s, which is because T_{ia}, $T_{ib,}$ and T_{ic} are designed long enough to ensure the stabilization of the control loop outputs. It should be noted that T_{ia}, $T_{ib,}$ and T_{ic} can be significantly reduced through dedicated control parameter designs.

C. Power Loss Analysis

The proposed method introduces low-frequency voltage and current disturbances to the system, resulting in additional power losses. Take DS #1 as an example, the additional power losses $\Delta P_{\text{addi\_DS1}}$ are analyzed as follows.

Suppose the output voltage $v_{\text{o\_DS1}}$ and inductor current i_{L1} of DS1 are

$$\begin{cases} v_{\text{o\_DS1}} = V_{\text{o\_DS1}} + A\cos(\omega_v t) \\ i_{\text{L1}} = I_{\text{L1}} + B\cos(\omega_v t + \psi_1) \end{cases} \tag{42}$$

where A and B are the peak values of $v_{\text{o\_DS1}}$ and i_{L1} at ω_{v}, respectively. In general, the converter's total power losses P_{loss} are

$$P_{\text{loss}} = P_{\text{MOS}} + P_{\text{L}} + P_{\text{C}} \tag{43}$$

where P_{MOS}, $P_{\text{L,}}$ and P_{C} denote for the power loss on the switches, inductors, and output capacitors, respectively.

P_{MOS} consists of conduction loss P_{cond} and switching loss P_{sw} [36]. The conduction loss P_{cond} is calculated by

$$\begin{cases} P_{\text{cond}} = I_{\text{rms}}^2 R_{\text{DS\_on}} \\ I_{\text{rms}} = \sqrt{I_{\text{L1}}^2 + I_{\text{rms\_}\omega\text{v}}^2 + \frac{I_{\text{ripple}}^2}{12}} \\ I_{\text{ripple}} = \frac{D(V_{\text{o\_DS1}} - V_{\text{i\_DS1}})}{L_1 f_{\text{s}}} \end{cases} \tag{44}$$

where I_{L1}, $I_{\text{rms\_}\omega\text{v,}}$ and I_{ripple} represent the i_{L1}'s dc value, i_{L1}'s rms value at ω_{v}, and i_{L1}'s peak-to-peak value of the switching ripple, respectively. $R_{\text{DS\_on}}$ is the conduction resistance of the MOSFET, and D is the duty cycle of S_1. Since S_2 is soft-switching, the switching loss P_{sw} is

$$P_{\text{sw}} = P_{\text{vi}} + P_{\text{dead\_time}} + P_{\text{rr}} + P_{C_{\text{oss}}} \tag{45}$$

where P_{vi} denotes the power loss on S_1 caused by the overlap of voltage and current, $P_{\text{dead\_time}}$ is the antiparalleled diode conduction loss of S_2 during dead time, P_{rr} is the diode reverse recovery loss, and $P_{C\text{oss}}$ is the output capacitor loss of S_1 and S_2. Each of them can be further calculated by

$$\begin{cases} P_{\text{vi}} = \frac{f_{\text{s}}(t_{\text{r}}+t_{\text{f}})}{2} \int_0^1 v_{\text{o\_DS1}}(t) i_{\text{L1}}(t) dt \\ P_{\text{dead\_time}} = 2V_{\text{f}} f_{\text{s}} t_{\text{dead\_time}} \int_{00}^1 i_{\text{L1}}(t) dt \\ P_{\text{rr}} = V_{\text{f}} Q_{\text{rr}} f_{\text{s}} \\ P_{C_{\text{oss}}} = C_{\text{oss}} f_{\text{s}} \int_0^1 v_{\text{o\_DS1}}^2(t) dt \end{cases} \tag{46}$$

where t_{r} and t_{f} are the rise and fall time of the MOSFET, respectively, V_{f} is the forward conduction voltage drop of the diode, $t_{\text{dead-time}}$ is the duration of dead time, Q_{rr} is the diode reverse recovery charge, and C_{oss} is the MOSFET's output capacitance.

The inductor loss P_{L} consists of the core loss and the conduction loss. Since L_1 works in continuous-current mode, the core loss is ignored. So, the inductor loss is calculated as

$$P_{\text{L}} = I_{\text{C}}^2 R_{\text{esr\_L}} \tag{47}$$

where R_{esL} is the parasitic resistance of L_1, and I_{C} is the rms current on the capacitor.

The capacitor loss P_{C} is

$$P_{\text{C}} = I_{\text{C}}^2 R_{\text{esr\_C}} \tag{48}$$

where I_{C} is the rms current on C_{bus}, and $R_{\text{esr\_C}}$ is the parasitic resistance of C_{bus}.

The additional power losses $\Delta P_{\text{addi\_DS1}}$ are

$$\Delta P_{\text{addi\_DS1}} = \Delta P_{\text{cond}} + \Delta P_{\text{vi}} + \Delta P_{C_{\text{oss}}} + \Delta P_{\text{L}} + \Delta P_{\text{C}}.$$

For DS #1, it is calculated that $P_{\text{sw}} = 9.42$ W, $P_{\text{MOS}} = 12.11$ W, $P_{\text{L}} = 4.32$ W, and $P_{\text{C}} = 0.02$ W, according to (42)–(48). Thus, the total power losses $P_{\text{loss\_DS1}}$ are 16.46 W, while $\Delta P_{\text{addi\_DS1}}$ is calculated as 11.1 mW, which is 0.07% of $P_{\text{loss\_DS1}}$. Therefore, the additional power losses introduced by the proposed method can be ignored.

VI. Conclusion

This article proposes a power flow tracing control method for fair and accurate P2P trading in dc microgrids. The proposed method, which consists of S2LPS and S2SPV, is established on a superimposed low-frequency carrier. S2LPS measures the power flow between each DS and each CPL, providing reliable physical layer data for P2P trading. S2SPV checks the actual output power of DSs, so the data authenticity from each DS can be guaranteed by other prosumers in the system. The S2LPS and S2SPV data are cross-checked, resolving trust issues between DSs and PLs. The correctness and feasibility of the proposed method are validated on a 2.5 kW dc microgrid platform, and the errors between estimated and actual data are all less than 2.5%.

The proposed method obtains advantages of PES technique, including simple implementation, high reliability, and low cost. With the proposed method, advanced and dedicated transaction mechanisms considering the P2P power transmission status could be implemented in P2P trading scheme, ensuring the fairness and accuracy of P2P trading. The proposed method is also applicable in meshed dc microgrids and may inspire other researches in the area of P2P trading.

However, there are still some considerable issues that merit further research. First, power fluctuations caused by load variations are common in practice. Since the proposed method is established on the premise that each load is viewed as a CPL, the measuring period T_{p} should be much shorter than the intervals between two power fluctuation events. Consequently, the bandwidth of the proposed method should be further increased. Second, the impacts of the line impedance are not neglectable in large-scale dc microgrids. In this case, traditional line impedance measuring methods [22], [24] can be employed and the corresponding correction items can be provided to compensate the measuring errors and guarantee the fairness of P2P trading [37]. Third, for future commercial products applications, the accuracy of the proposed method should be improved with advanced metering instruments and dedicated control parameter designs.

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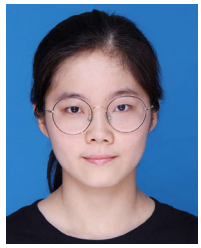

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